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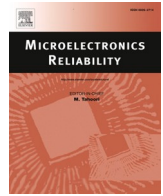
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# Aging investigation of the latest standard dual power modules using improved interconnect technologies by power cycling test

Yi Zhang<sup>a,c,\*</sup>, Rui Wu<sup>b</sup>, Francesco Iannuzzo<sup>a</sup>, Huai Wang<sup>a</sup>

<sup>a</sup> AAU Energy, Aalborg University, Aalborg, Denmark

<sup>b</sup> Vestas Wind Systems A/S, Aarhus, Denmark

<sup>c</sup> Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne

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## ABSTRACT

The latest standard “New Dual” power module has been developed for both silicon and silicon-carbide devices to meet the increasing demands in high reliability and high temperature power electronic applications. Due to the new package is just starting to release on the market, the reliability performance has not been fully studied. This paper investigates the power cycling capabilities of a 1.7 kV/1.8 kA IGBT power module based on the new package. Both the electrical and thermal performances have been studied before and after the power cycling. Neither the chips nor bond wires have noticeable degradation after 1.2 million cycles with  $\Delta T_j = 100$  K and  $T_{jmax} = 150$  °C. Nevertheless, the end-of-life criterion of an increased conduction voltage ( $V_{ce}$ ) in the test environment has been reached at about 600 k cycles. The further scanning acoustic microscopy test unveils that the fatigue site shifts from the conventional near-to-die interconnect (e.g., bond wire lift-offs) to the direct bond copper (DBC) substrate and baseplate layers. Considering the new package has more than ten times cycle life than the traditional power module, it expects the thermo-mechanical fatigue is not the life-limiting mechanism with further improved interconnect technologies. Meanwhile, as the previous bottlenecks (e.g., bond wires) are addressed, some new fatigue mechanisms, e.g., delamination of the DBC, become visible in this new package.

## 1. Introduction

High power applications in renewable energy, locomotive tractions, and other industrial applications demand high-reliability, high-temperature, scalable, and compact power modules. To meet these demands continuously, the power module packaging has undergone significant upgrades over the past three decades (see Fig. 1). In around 2015, multiple major power semiconductor suppliers have a joint effort to develop a new generation power module, which is aimed to solve the limitations of conventional standard power modules and include future opportunities such as new semiconductor materials and improved interconnect technologies. The concept prototype is released subsequently with a dimension of 100 mm × 140 mm as shown in Fig. 2 as well. The new packaging features advantages such as low-inductive, high-current, symmetrical design, etc. [1–3].

At present, several suppliers have released their power modules based on the new packaging, such as Infineon XHP [4], Mitsubishi LV100/HV100 [5], ABB LinPak [6], Hitachi nHPD2 [7], and other similar products [8]. The photos of the market available products are

included in Fig. 1. As the identical packaging has varied names in the market, the following part of this paper names it as “New Dual” power modules for simplification because two equivalent switches within this packaging as shown in Fig. 2.

In the previous standard power modules, aluminum bond wires and soft solders [9] are the typical materials to achieve packaging interconnections, which are often regarded as the major failure mechanisms [10]. To improve the reliability performance, some suppliers have applied state-of-the-art interconnect technologies to the New Dual power modules, such as copper bond wires, silver sintering [11,12], etc. In literature, these improved interconnect technologies alone and their integration based on conventional packaging layouts have shown a significant reliability improvement [13]. However, to the best of our knowledge, the reliability performance of integrating the improved interconnect technologies into the newly released New Dual power module is still an open question. To verify the reliability performance of the whole integration of the New Dual, an investigation of testing and failure mechanisms analysis is necessary.

In this paper, we investigate the power cycling capabilities of a 1.7

\* Corresponding author at: AAU Energy, Aalborg University, Aalborg, Denmark.  
E-mail address: [yiz@energy.aau.dk](mailto:yiz@energy.aau.dk) (Y. Zhang).

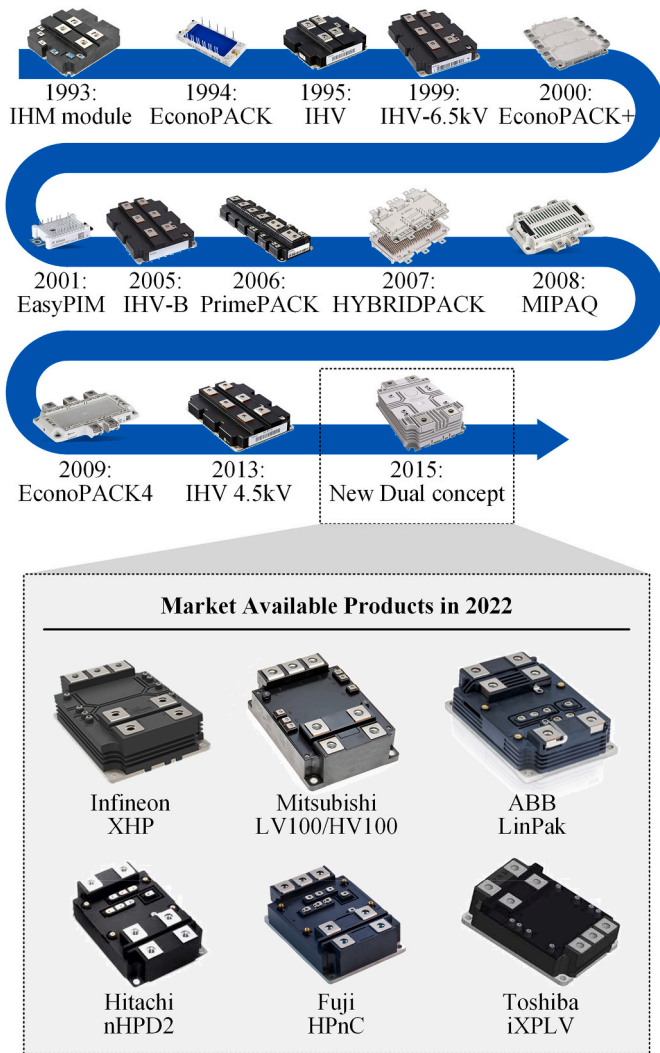


Fig. 1. Development of different power module packaging and the latest standard New Dual power modules.

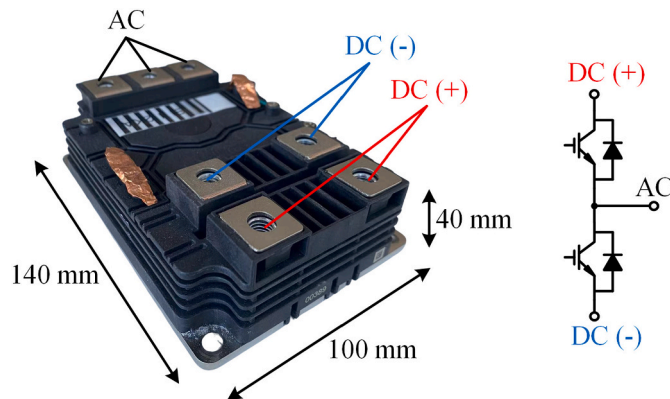


Fig. 2. The dimension and the equivalent circuit of the New Dual power module.

kV/1.8 kA New Dual IGBT power module. The testing procedure compares the electrical and thermal performances before and after around 1.2 million power cycles. The failure mechanisms of the New Dual have been investigated by a series of non-destructive methods, such as structure functions and scanning acoustic microscopy (SAM). The

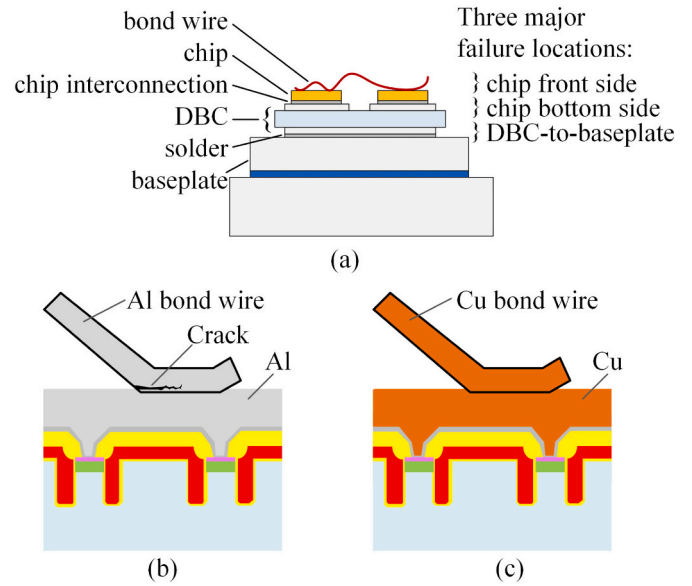


Fig. 3. (a) Typical power module structures and the three major failure locations, (b) aluminum-based chip front side in conventional power modules, and (c) copper-based technology in the tested New Dual power module.

testing and analyzed results serve to uncover the capabilities and potential limitations of the new standard power module.

## 2. Conventional power modules vs. the tested New Dual

### 2.1. Major failure mechanisms of conventional power modules

The major failure mechanisms of the conventional package technologies are related to three locations [14] as shown in Fig. 3(a): 1) Chip front side: aluminum (Al) is a standard material used on the chip front side, such as bond wires and chip metallization (see Fig. 3(b)). The typical lifetime limiting failure mechanism is bond wire lift-off [15]. Ref. [16] has uncovered that the failure mechanism is the propagation of cracks inside the Al wire bond itself, as illustrated in Fig. 3(b). In other words, the lifetime limit is not caused by the bonding process but by the material properties of Al. 2) Chip bottom side: the chip interconnection layer joins the die to the direct bond copper (DBC) layer which is also a common failure mode. The degradation is driven by the mismatch of the different expansion coefficients of the chip and the DBC. The degradation of the chip solder leads to an increased thermal resistance, which in return accelerates the bond wire lift-off [17]. 3) DBC to baseplate connection: the thermal management of some applications still benefits from the use of baseplates. The interconnect between DBC and baseplate has often found cracks, where the failure mechanism is similar to the aforementioned chip interconnection degradation.

### 2.2. The tested New Dual sample with improved interconnect technologies

To meet the demands of high reliability and temperature stability, some suppliers have applied several novel packaging technologies to the New Dual power modules with targeting to solve the aforementioned three bottlenecks, which are summarized as

- Copper (Cu) metallization on the chip: a thick Cu metallization has been applied on the studied New Dual IGBT module, which improves the capabilities of handling the short circuit. Additionally, Cu-metallization is the enabler for Cu-wire bonding.
- Cu bond wires: Cu has five times the higher yield strength and about 1.6 times higher melting temperature than Al [17]. The New Dual

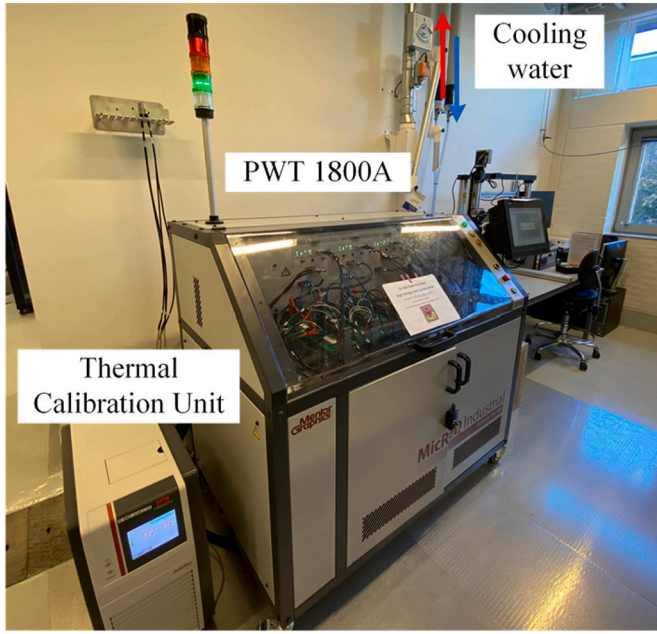
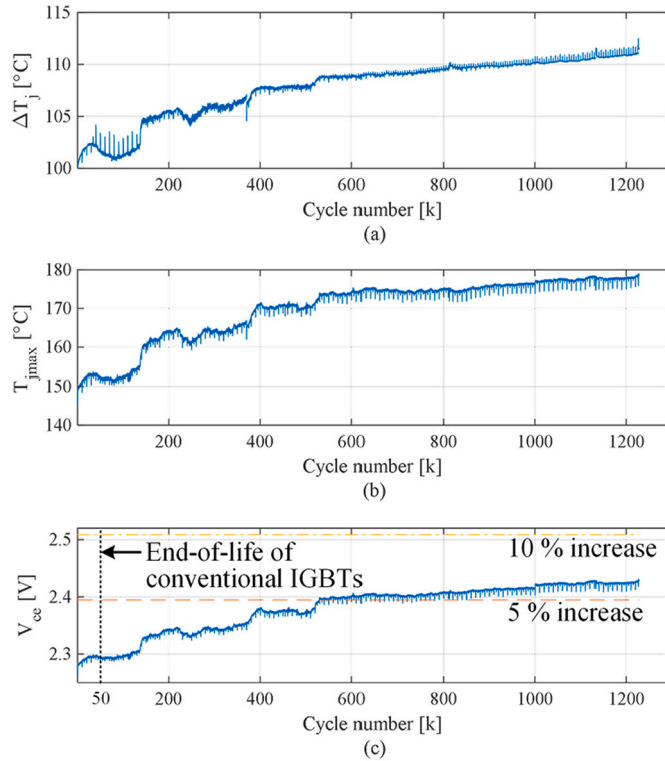


Fig. 4. Power cycling platform.

Fig. 5. Power cycling results: (a) temperature swings  $\Delta T_j$ , (b) maximum junction temperature  $T_{jmax}$ , and (c) conduction voltage drop  $V_{ce(on)}$ .

replaces the conventional Al to Cu as a more robust material, which improves its capabilities against thermo-mechanical stresses.

- Silver sintering connections: the sintering of small Ag particles forms a monometallic bond between die and substrate. The developed compact and porous Ag joint has a melting temperature of 962 °C [18].

It should be mentioned that the investigation of this paper is limited

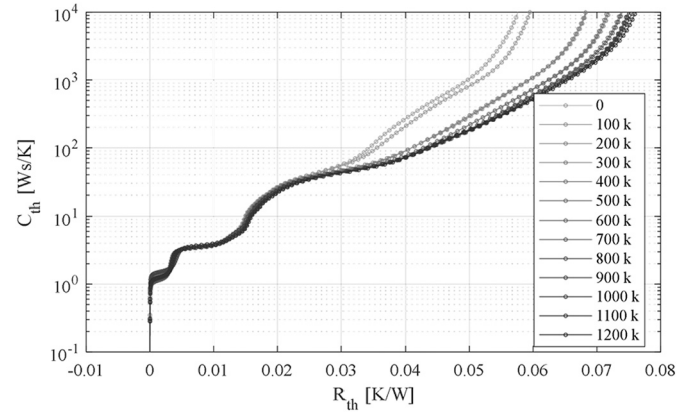


Fig. 6. Structure functions along with the power cycling.

the scope to one sample only. Although the tested New Dual sample has applied the mentioned novel interconnection technologies, other New Dual power modules with identical dimensions but from different suppliers may use completely different materials or technologies.

### 3. Power cycling of a New Dual power module

The tested New Dual power modules have improved interconnect technologies compared to their conventional counterparts. However, although the literature has many discussions on each specific interconnect technology (e.g., Cu bond wires, silver sintering, etc.), the state-of-the-art has very limited results regarding the reliability performance of the entire integration of the novel power module. Thus, this work investigates the power cycling capabilities of a 1.7 kV/1.8 kA New Dual power module. The testing procedures contain characterizations of electrical and thermal performances before and after around 1.2 million power cycles. Meanwhile, the analysis of the failure mechanisms has also been included.

#### 3.1. Testing system

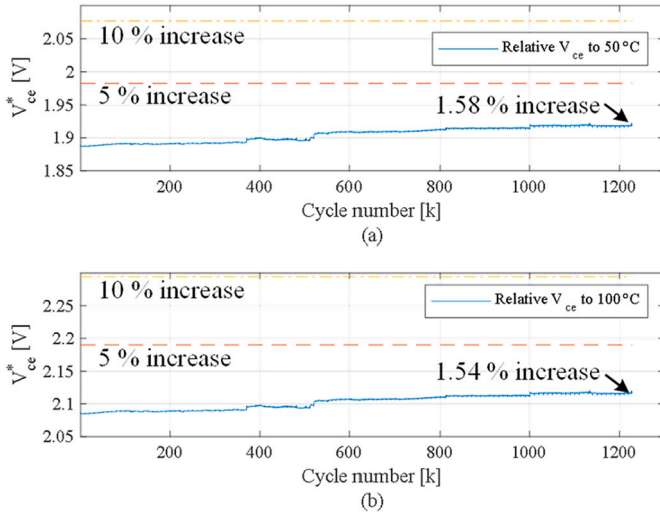
As shown in Fig. 4, Siemens MicReD PWT 1800A is used to do power cycling in this work. The testing condition is set as  $\Delta T_j = 100$  K and  $T_{jmax} = 150$  °C with  $t_{on} = t_{off} = 1.5$  s. The testing strategy is constant current with 1325 A. The gate voltage is 12 V to generate more heat inside the device.

#### 3.2. Power cycling results

The DUT has been cycled >1.2 million cycles under the constant heating current, as shown in Fig. 5. The temperature swing  $\Delta T_j$  starts with 100 K and the maximum temperature  $T_{jmax}$  initiates around 150 °C. After that, both temperatures increase with the cycle numbers. Finally,  $\Delta T_j$  has reached 110 K, and  $T_{jmax}$  has increased to around 175 °C after 1.2 million cycles. The low-frequency temperature fluctuations within the process are partially caused by the testing environment. Meanwhile, a routine checking procedure (i.e., thermal impedances and gate states) causes the high-frequency temperature ripples in both  $\Delta T_j$  and  $T_{jmax}$ .

After 1.2 million cycles,  $V_{ce(on)}$  has increased about 0.15 V which amounts to 7 % of  $V_{ce(on)}$  increase. Considering a 5 %  $V_{ce(on)}$  increase as the end-of-life (EOL) criterion in AQG324 [19], the cycle life of the tested New Dual power module is around 600 k. It is worthwhile to mention that the previous generation has a cycle life of 50 k only under the identical testing stress [20]. The cycle life of the tested New Dual thus has at least ten times longer cycle life. However, the  $V_{ce(on)}$  of the conventional power modules increases exponentially when  $V_{ce(on)}$  reaches the 5 % criterion. Whereas the New Dual is operated well after reaching the criterion. Moreover, even after the 5 % voltage increase, an





**Fig. 7.** Relative  $V_{ce(on)}$  to (a) 50 °C and (b) 100 °C to decouple the temperature effect of the measured voltage.

additional 600 k cycle life has been operated again without observing an exponential  $V_{ce(on)}$  increase. These phenomena let us doubt whether the tested device is failed after reaching the standard criterion of 5 %  $V_{ce(on)}$  increase.

### 3.3. Structure functions along with the power cycling

Structure function is provided in the standard JEDEC JESD51-14 [21] to identify the thermal impedance from the junction to the ambient. The obtained structure functions along with the power cycling are shown in Fig. 6. The  $C_{th}$ - $R_{th}$  curves have minor changes before  $R_{th} < 0.02$  K/W although 1.2 million cycles have been conducted. Meanwhile, the curves separate around  $R_{th} > 0.03$  K/W where the thermal resistance change is mainly caused by the thermal interface material (TIM). In this case, we use the thermal paste as TIM. In particular, the curves are right-shifted significantly from 100 k to 200 k cycles. The distinct thermal resistance increase occurs during this period, which causes the temperature step around 100 k to 200 k as shown in Fig. 5(a) and (b). It should be mentioned that the TIM degradation induces both temperature and  $V_{ce(on)}$  jumps, but which do not represent the degradation of the New Dual module.

### 3.4. Relative $V_{ce(on)}$ increase to reference temperatures

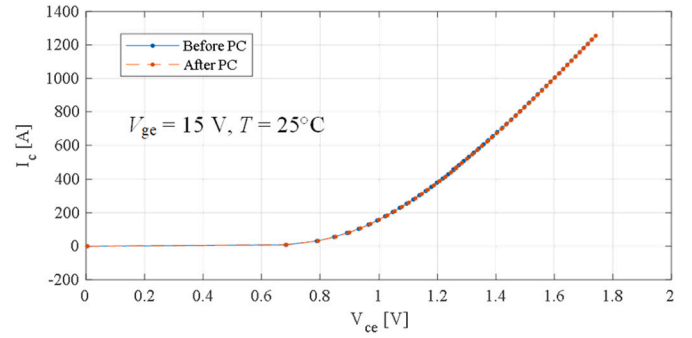
$V_{ce(on)}$  increase is related to both temperature and degradation. Accordingly, the temperature fluctuations of the test environment and/or TIM degradations would cause the  $V_{ce(on)}$  increase as well. Thus, the determination of EOL by the direct measurement of  $V_{ce(on)}$  is doubtful. Especially, the New Dual power module operates stably for an additional double cycle life after reaching the criterion of 5 %  $V_{ce(on)}$  increase.

To decouple the measurement of  $V_{ce(on)}$  from the effects of the testing environment (e.g., ambient temperature, the health status of the TIM, etc.), a relative  $V_{ce(on)}$  is proposed in this paper, which is defined as

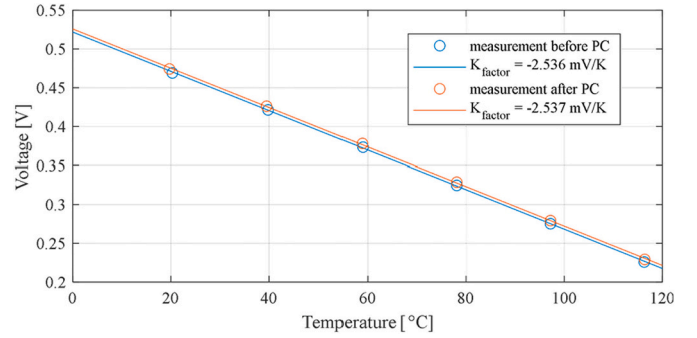
$$V_{ce(on)}^*(T_{ref}, I) = V_{ce(on)} - \alpha(I) \cdot (T_{jm} - T_{ref}) \quad (1)$$

where  $T_{ref}$  is the reference temperature,  $T_{jm}$  is the maximum junction temperature, and  $\alpha$  is a coefficient related to temperature under a specific current  $I$ . In this case, the current is constant with  $I = 1325$  A in the power cycling. The coefficient  $\alpha$  is thus correlated with the temperature only, which is 3.957 mV/K based on the measurement of the I-V curves under various temperatures.

According to the measured  $V_{ce(on)}$  and  $T_{jm}$  in Fig. 5(b) and (c), the corresponding relative  $V_{ce(on)}$  based on two reference temperatures is



**Fig. 8.** Output characteristics before and after the power cycling.



**Fig. 9.** K factor @ 100 mA calibration before and after the power cycling.

obtained as shown in Fig. 7. By decoupling the effects of the temperature, the relative  $V_{ce(on)}$  increases are minor after 1.2 million cycles. The first case has only a 1.58 % relative voltage increase under  $T_{ref} = 50$  °C and a 1.54 % increase for  $T_{ref} = 100$  °C. Both cases are far from the 5 % voltage increase, which is a possible reason that the New Dual operates stably for a long term even when it reaches the standard EOL of 5 %  $V_{ce(on)}$  increase. In other words, the New Dual power module has a much longer cycle life than 600 k which is defined by the standard EOL criterion.

## 4. Electrical and thermal performances comparison before and after the power cycling

### 4.1. Electrical performances

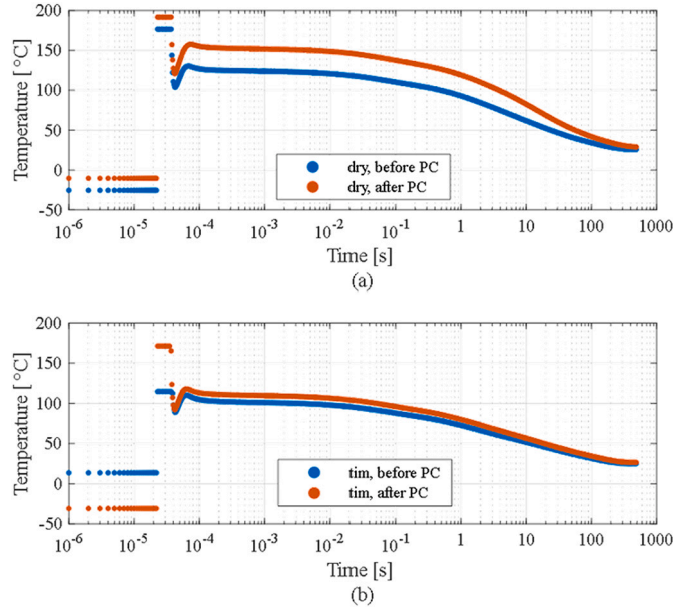
Output characteristics can reveal the health status of the IGBT chips and bond wires. The New Dual power module is measured with a B1506A curve tracer in this test. The characteristics are measured at the auxiliary terminals of the module – both before and after the power cycling.

The measured IGBT output characteristics at room temperature (25 °C) are shown in Fig. 8. The solid line is the characteristic before the power cycling, while the dashed line is the status after the power cycling. The two lines do not have an obvious difference between them. It reveals that the chip itself or bond wires have no obvious degradation.

### 4.2. Comparison of the K factor

The standard electric test method [22] is a widely applied method to determine the junction temperature of semiconductor dies. It utilizes a temperature-sensitive parameter (TSP) to sense the change of junction temperatures. The relationship between the TSP voltage and the junction temperature is determined by a calibrated K factor.

This paper selects the  $V_{ce}$  under 100 mA sensing current as the K factor to measure the junction temperature. The calibrated K factor



**Fig. 10.** Cooling curves before and after the power cycling: (a) dry - without thermal grease, and (b) tim - with thermal grease.

**Table 1**

Comparison of the  $R_{thja}$  before and after the power cycling.

TIM	Power cycling	Heating current	Power loss	$\Delta T_j$ (K)	$R_{thja}$ (K/kW)
w/o	Before	600 A	916 W	100	109
w/o	After	600 A	943 W	130	138
w/	Before	600 A	896 W	76	84
w/	After	600 A	906 W	89	98

before and after the power cycling is shown in Fig. 9, in which the K factor is  $-2.536$  mV/K before PC while the K factor is  $-2.537$  mV/K after PC, respectively. The 1.2 million power cycles do not change the K factor of the DUT significantly, which means that the estimated junction in Fig. 5(a) and (b) based on the K factor is trustable. Moreover, the unchanged K factor also reveals that the IGBT chips have no obvious degradation once again.

#### 4.3. Comparison of the $R_{thja}$

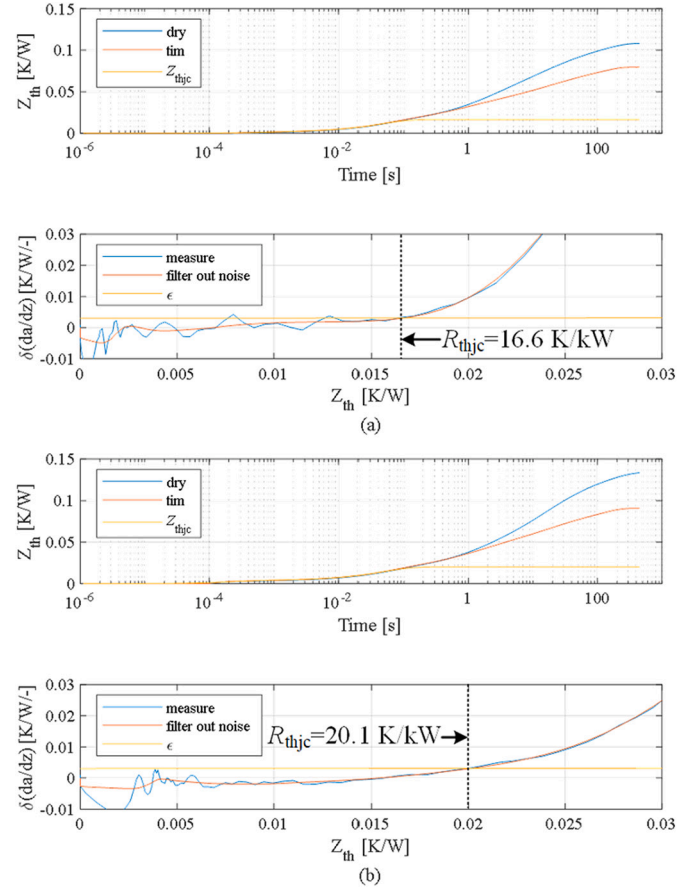
The last section shows the relative  $V_{ce(on)}^*$  has a minor increase of  $<5$  %. Thus, the second EOL criterion of the thermal impedance increase should be carefully studied.

The cooling curves of the New Dual power module are recorded as shown in Fig. 10. Without applying TIM (i.e., labeled as dry), the maximum temperature has increased by  $30$  °C from  $125$  °C before the power cycling, as shown in Fig. 10(a). This temperature change is caused by the different contact thermal resistance and/or package degradations. Meanwhile, the cooling curves with TIM are shown in Fig. 10(b). The maximum temperature has also increased by around  $13$  °C after the power cycling.

The corresponding power losses and temperature rises are listed in Table 1. The estimated  $R_{thja}$  is also summarized. All the measurements are repeated twice under the same conditions to reduce the impact of random effects. After the power cycling test,  $R_{thja}$  has increased by  $29$  K/kW (without TIM) and  $14$  K/kW (with TIM). However, the quantification of the package degradation requires further study.

#### 4.4. Comparison of the $R_{thjc}$

The aforementioned  $R_{thja}$  comparison does not quantify the New



**Fig. 11.** Determination of the  $R_{thjc}$ : (a) before and (b) after the power cycling.

**Table 2**

Comparison of the  $R_{thjc}$  before and after the power cycling.

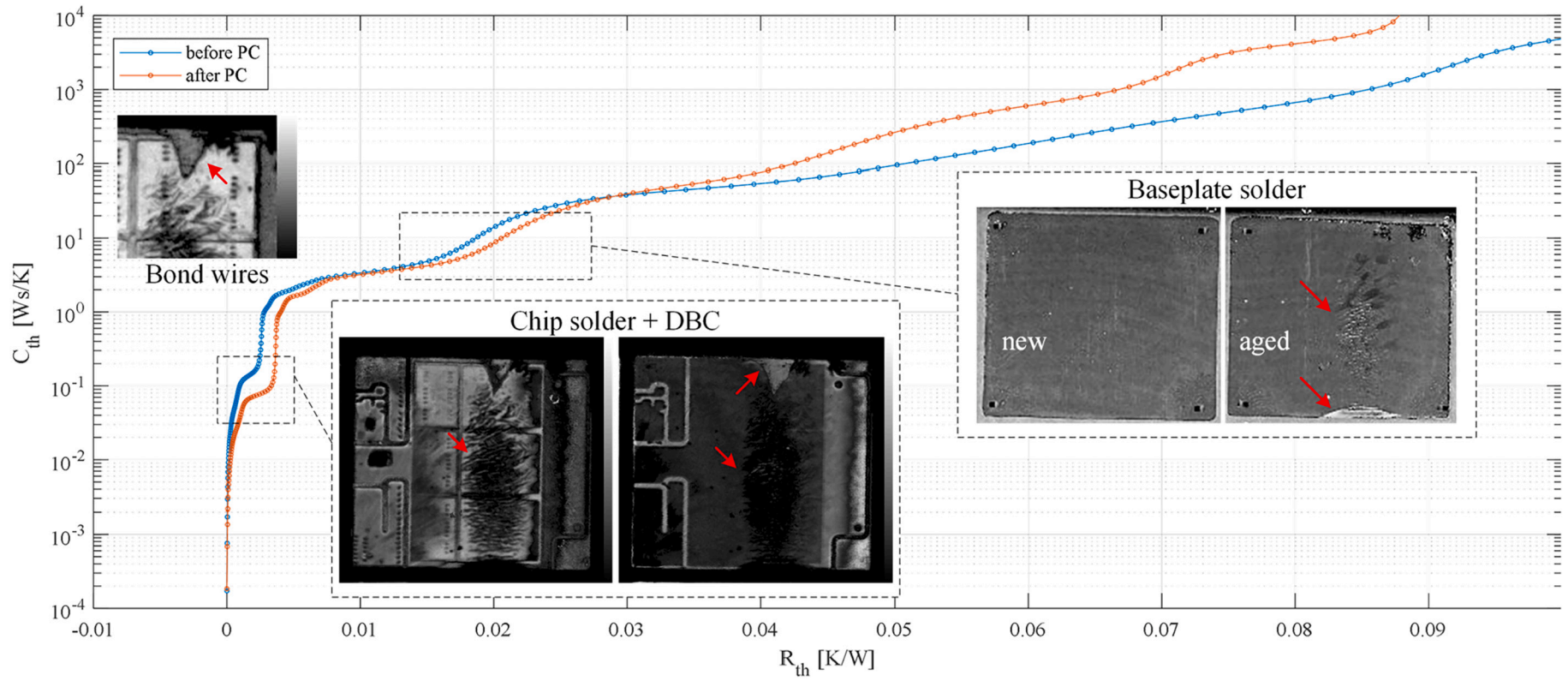
Before	$R_{thjc}$ [K/kW]	After	$R_{thjc}$ [K/kW]
Test#1	16.4	Test#1	21
Test#2	17	Test#2	21
Test#3	16	Test#3	21
Test#4	16.6	Test#4	20.1
Test#5	17	Test#5	21
Average	16.6	Average	20.8

Dual package degradation directly. In order to determine the  $R_{thjc}$ , a standard method based on dual interface measurements is utilized here [21]. As shown in Fig. 11, the  $Z_{thja}$  curves are measured under two different interface conditions (dry and tim). The separation point of the two curves helps us to determine the  $R_{thjc}$ . Meanwhile, a  $\delta(da/dz)$  curve is defined in the standard [21] to justify the separation point quantitatively, which is also shown in Fig. 11.

The obtained  $R_{thjc}$  is shown in Fig. 11. Each measurement has been repeated five times (listed in Table 2) to avoid possible random effects during the measurement. The  $R_{thjc}$  of the tested New Dual is  $16.6$  k/KW on average before the power cycling test. After 1.2 million cycles, the  $R_{thjc}$  increases to  $20.8$  k/KW on average. Approximately 25 %  $R_{thjc}$  increase along with the power cycling has reached one of the EOL criteria of a 20 %  $R_{thjc}$  increase [19]. Therefore, the power cycling test has introduced significant degradation on the New Dual power module from the perspective of the thermal resistance increase.

#### 4.5. Non-destructively measure New Dual package

The aforementioned analysis has uncovered that the tested New Dual



**Fig. 12.** Structure functions before and after the power cycling and corresponding scanning acoustic microscopy results (red arrows show the damages in the New Dual package).



power module has packaging fatigue, which causes the increase of the measured  $R_{thjc}$ . However, the failure mechanisms of the  $R_{thjc}$  increase are still not clear. Thus, a dedicated structure function analysis has been conducted once again. The SAM is also utilized here to identify the failure mechanism non-destructively.

As shown in Fig. 12, two structure functions are measured before and after the power cycling. Compared to the curve before the power cycling, the curve of the aged device is right-shifted. Specifically, the thermal resistance around the chip interconnection layer has increased while the corresponding thermal capacitance is decreasing slightly. In general, the increasing voids within the joint layer could cause this phenomenon [23]. Meanwhile, the structure functions have revealed the increased thermal resistance around the baseplate joint area.

The corresponding SAM results are also provided in Fig. 12. First, the bonding joints are clear to see on the front side of the chip, implying that the bond wires are in a good condition. Second, many scratches have been observed under the cycled IGBT chips, which result from delamination in one of the lower layers. It should be noted that a triangle area has been observed at the edge of the DBC after the power cycling. A possible failure mechanism is the delamination of the Cu-metallization from the ceramic substrate. Finally, the baseplate solder has delamination at the edge and the central area becomes thinner.

Thus, the above-measured results of the New Dual power module have revealed that the new package with improved interconnect technologies has more than ten times longer cycle life compared to the conventional power module based on Al [16]. The bond wire lift-off is not necessarily the lifetime limiting factor for the New Dual power module based on Cu interconnections. However, the solder/joint layer delamination is still a limiting factor including the chip bottom side and the DBC-to-baseplate connection. Moreover, it should be noted that the delamination of the Cu from the DBC ceramic has been identified as an additional failure mechanism in the New Dual power module, which is not often relevant for the conventional power modules. As the previous bottlenecks (e.g., bond wires) are addressed, some new fatigue mechanisms like delamination of the DBC become visible in this new package.

## 5. Conclusions

The latest standard New Dual 100 mm × 140 mm power module with low-inductive, high-current, high-temperature, and improved interconnect-technology designs. Although multiple manufacturers have provided their products based on the new package, the state-of-the-art has limited results regarding its reliability performances. This paper has investigated the power cycling capability of a 1.7 kV/1.8 kA New Dual power module. More than 1.2 million cycles have been conducted under the testing conditions of  $\Delta T_j = 100$  K,  $T_{jmax} = 150$  °C, and  $t_{on} = t_{off} = 1.5$  s. The conclusions can be drawn as follows.

- 1) The New Dual power module with improved interconnect technologies has more than ten times longer cycle life compared to the conventional power module-based aluminum.
- 2) The New Dual power module reaches a 5 %  $V_{ce(on)}$  increase at 600 k cycles. However, the  $V_{ce(on)}$  does not increase exponentially after the 5 %  $V_{ce(on)}$  increase. The New Dual sample even has operated stably for an additional 600 k cycles. The conventional EOL based on direct measurement of  $V_{ce(on)}$  is questionable.
- 3) A relative  $V_{ce(on)}^*$  is proposed in this paper to decouple the effects of the temperature. Based on the derived indicator,  $V_{ce(on)}^*$  has around 1.6 % increase after 1.2 million cycles.
- 4) The comparison of the electrical performance before and after PC testing reveals that both the IGBT chips and bond wires have no obvious degradation.
- 5) Both thermal impedance analysis and SAM measurements have indicated that the Cu-based bond wires have no noticeable degradation or lift-off after 1.2 million cycles.

- 6) The major fatigue effects due to load cycling are package degradation, including delamination of chip interconnection, baseplate solders, and DBC metallization.
- 7) The thermo-mechanical related cycling capability has been significantly improved in the New Dual power module. The major failure site has a trend to shift from the near-to-die interconnects (e.g., bond wire lift-offs) towards the DBC and baseplate. In particular, with improved interconnect technologies in the new package, some new bottlenecks are emerging, e.g., the delamination of the DBC.

## CRedit authorship contribution statement

**Zhang Yi:** Conceptualization, Methodology, Validation, Investigation, Writing-Original draft. **Wu Rui:** Validation, Investigation, Writing-Review & editing. **Iannuzzo Francesco:** Writing-Review & editing, Supervision. **Wang Huai:** Writing-Review & editing, Supervision.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data availability

The authors do not have permission to share data.

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## References

- [1] S. Hartmann, D. Trüssel, et al., Novel low inductive phase-leg IGBT module eases paralleling, *Power Electron. Eur.* 4 (2015) 15–18.
- [2] G. Borghoff, Implementation of low inductive strip line concept for symmetric switching in a new high power module, in: *PCIM Europe*, 2013, pp. 185–191.
- [3] S. Kicin, Ultra-fast switching 3 . 3kV SiC high-power module, in: *PCIM Europe*, 2020, pp. 150–157.
- [4] W. Brekel, W. Rusche, XHPTM 2 – the low-inductive, multi-package housing for the next generation of high-power applications, in: *PCIM Europe*, 2020, pp. 222–228.
- [5] T. Radke, N. Lakshmanan, The next generation of high power IGBT modules, *Bode's Power Syst.* (2019).
- [6] R. Schnell, S. Hartmann, LinPak , a new low inductive phase-leg IGBT module with easy paralleling for high power density converter designs Module scalability and record current density, in: *PCIM Europe*, 2015, pp. 224–231.
- [7] D. Kawase, H. Power, High voltage module with low internal inductance for next chip generation - next High Power Density Dual (nHPD2), in: *PCIM Europe*, 2015, pp. 217–223.
- [8] K. Yoshida, H. Ichikawa, S. Chen, T. Takaku, Y. Kobayashi, 7th generation high reliability HPnC module for traction applications, in: *PCIM Europe*, 2020, pp. 770–775.
- [9] A. Wintrich, N. Ulrich, T. Werner, T. Reimann, Application Manual Power Semiconductors, *Semikron Int.GmbH*, Nuremberg, Germany, 2015.
- [10] Y. Zhang, H. Wang, et al., Impact of lifetime model selections on the reliability prediction of IGBT modules in modular multilevel converters, in: *In Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 4202–4207.
- [11] J. Dai, J. Li, et al., Comparative thermal and structural characterization of sintered nano-silver and high-lead solder die attachments during power cycling, *IEEE Trans. Device Mater. Reliab.* 18 (2) (2018) 256–265.
- [12] Y. Sato, New solderless structure power module for high reliability, in: *PCIM Europe*, 2020, pp. 377–382.
- [13] T. Methfessel, H. Jähme, et al., End-of-life mechanism due to cyclic thermomechanical loading of power modules with. XT joining technology comparison of wear-out mechanisms standard power modules, in: *In Proc. 11th Int. Conf. Integrated Power Electronics Systems (CIPS)*, 2020, pp. 1–5.
- [14] A. Ciliox, New module generation for higher lifetime, in: *PCIM 2010*, 2010, pp. 238–243.
- [15] M. Ciappa, Selected failure mechanisms of modern power modules, *Microelectron. Reliab.* 42 (4–5) (2002) 653–667.

- [16] K.B. Pedersen, IGBT Module Reliability Physics-of-failure Based Characterization and Modelling, Aalborg University, 2014.
- [17] K. Guth, New assembly and interconnects beyond sintering methods, in: PCIM Europe, 2010.
- [18] K. Guth, End-of-life investigation on the .XT interconnect technology, in: PCIM Europe, 2015, pp. 72–79.
- [19] ECPE, ECPE Guideline AQG 324 Qualification of Power Modules for Use in Power Electronics Converter Units in Motor Vehicles, ECPE, 2019.
- [20] H. Ludwig, AN2010-02 Technical Information: IGBT Modules Use of Power Cycling Curves for IGBT4, 2010.
- [21] JEDEC, JESD51-14: Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-case of Semiconductor Devices With Heat Flow Through a Single Path, 2010.
- [22] EIA, JEDEC, EIA/JESD51-1: Integrated Circuits Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device), December. 1995.
- [23] M. Du, Q. Guo, et al., An improved cauer model of IGBT module: inclusive void fraction in solder layer, IEEE Trans. Compon. Packag. Manuf. Technol. 10 (8) (2020) 1401–1410.