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Sliding mode control for pulsed load power supply converters in DC shipboard microgrids

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ABSTRACT

Pulsed power load (PPL) is a special load type in shipboard microgrids (SMGs), which consists of the generation module, energy storage system, and various types of loads. Having a reliable power supply to shipboard loads is a challenge as the SMG operates in islanded mode in most cases. Particularly, the PPLs require high transient power transfer with fast dynamics and strong robustness. Conventional solution to supply for the PPL is based on proportional-integral (PI) control, which can be used by linearizing the system around the equilibrium operation point. However, for a pulsed power supply (PPS) system, the load demand drastically changes in a short time, usually in millisecond level, making the operating point changes when the pulsed power is triggered or terminated. To supply the PPL with fast dynamics and robustness, an improved PPS control method is presented in this paper. By adopting a nonlinear sliding mode control (SMC) method, fast voltage regulation and robust pulse power tracking can be achieved. In the PPS, the PPL power demand is divided into two terms: one is the average power that is supplied by the SMG and the other is the fast pulsed power that is supplied by the storage capacitor. The size and cost of the storage capacitor are reduced as it is intentionally driven to a deep discharge. The PPS system configuration and coordination principle, SMC controllers, and sizing of passive elements in the PPS are analyzed in detail. The effectiveness of the presented PPS is verified by simulation results.

1. Introduction

Naval ships have been equipped with different advanced weapon facilities, such as electromagnetic launch system (EMALS), radar system, and rail guns [1]. These loads share common features exhibiting pulsed operation and requiring large electrical energy within a short period and with periodical repetition, and thus they are categorized as pulsed power loads (PPLs) [2–4]. The load profile of the PPL can be described by characteristics of a peak power, pulse duration, and pulse repetition frequency (PRF), which denotes the reciprocal of the interval between two sequential pulses. The PPL waveforms vary according the different PLL types. For example, the pulse duration and PRF of marine radars are determined by the distance at which the target is located. The parameters of several typical PPLs in maritime applications are shown in Table 1 [5–7]. Such load presents specific requirements on the shipboard power system, which is also known as shipboard microgrid (SMG), since the system generation capacity is often smaller than the peak power of a PPL out of economy considerations. Take India's aircraft carrier INS Vikrant as an example, the rated power of diesel alternators is of 24 MW, which is much higher than the average power of EMALS, 6.35MVA, while the required transient power is up to 100 MW [8].

These PPLs bring challenges to the system by moving the system far away from the stationary operating point [9]. When the PPL operates, large voltage sags may occur in the bus voltage. Note that in some cases, the transient power of PPL may even exceed the generation capacity of SMG, which will be a threat to the system stability. Besides, in terms of dynamic response, the high power ramp rate of PPL, which requires up to hundreds of megawatts per second, can hardly be satisfied by diesel generators which can only provide tens of megawatts per minute in conventional ships [10–13]. Therefore, diesel generators have limited capability to track the load demand of PPL, and other power sources with faster dynamics are required. Thus, an energy storage system (ESS) is necessary to compensate for the power unbalance between the PPL

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Nomenclature

$p_p(t)$	Pulsed power
ΔE_p	Incremental energy in one pulse cycle
D_p	Pulse duty cycle
T_p	Pulse period
P_p	Peak power of PPL
I_p	Peak current of PPL
L_j	Inductance of j^{th} converter
C_j	Capacitance of j^{th} converter
v_{inj}	Input voltage of j^{th} converter
R	Load resistance
C	Filter capacitance
e_v	Voltage error
u_j	Control law of j^{th} converter
s_j	Sliding surface of j^{th} converter
λ_0, λ_1, λ_2	Control parameters in sliding surface
C_s	Storage capacitor
v_o*	Rated PPL voltage
v_o	PPL voltage
i_o	PPL current
i_{oj}	Load current provided by j^{th} converter
i_{Lj}*	Current reference of j^{th} converter
ΔE_{Cs}	Energy of C_s
v_{Cs_h}	Voltage of C_s before discharging
v_{Cs_l}	Voltage of C_s after discharging
$\bar{v}_{Cs}$	Average voltage of C_s
I_{L2_d}	Current of L_2 when C_s discharges
i_{oj}	Output current of j^{th} converter
i_{Lj_min}	Minimum current of j^{th} inductor current
i_{Lj_max}	Maximum current of j^{th} inductor current
i_C	Current of filter capacitor
$\bar{i}_{Lj}$	Average current of j^{th} inductor current
f_{sw}	Switching frequency
α_j	Percentage of i_{oj} in ripple current
t_r	Raising time of pulsed power of PPL
PPL	Pulsed power load
SMG	Shipboard microgrid
PPS	Pulsed power supply
SMC	Sliding mode control
EMALS	Electromagnetic launch system
PRF	Pulse repetition frequency
UC	Ultra-capacitor
MPC	Model predictive control
DVC	Direct voltage control

Table 1
Typical PPL parameters.

PPL type	Peak power	Pulse duration	PRF
EMALS	$10^1 \sim 10^2$ MW	10^0 s	10^{-1} Hz
Rail gun	10^3 MW	10^0 ms	$10^0 \sim 10^2$ Hz
Pulsed radar	10^1 kW	$10^{-2} \sim 10^0$ μs	10^4 Hz

and generators.

Different energy storage techniques that potentially suit SMGs are reviewed in [14]. Among these, batteries, ultra-capacitors (UCs), and flywheels are the most studied and adopted types due to their relatively mature techniques and good performances. Batteries have high energy density but limited power density, while UCs and flywheels can discharge fast, but the energy storage capacity is limited [15]. Thus, hybrid ESS consisting of batteries combined with UCs, or flywheels, are popular in maritime applications [16].

To manage the coordination of power sources and ESS and allow the PPLs operate properly in SMGs, the requirements on the PPS are summarized: 1) the power absorbed from the main system should be constant to allow the integration of PPLs into the generator-powered SMGs and avoid propagating the negative impact of PPLs to the shipboard network [17,18]; 2) the load voltage drop when PPL is activated should be as small as possible to ensure proper load operation [19].

Research on PPS is taken from the aspects of system configuration, converter topology, and control strategy to meet the PPL demands. From the aspect of system configuration, a straightforward way to supply for the PPL is directly connecting the energy storage device to the PPL in parallel [20–23]. In this configuration, the discharge of the ESS follows the characteristics of the ESS itself, and the main control challenge lies in how to charge the ESS fast. However, since the ESS is directly connected to the load terminal, the ESS capacity must match the peak load demand, which is not cost effective enough. Another configuration consists of multiple-stage energy storage to form the pulsed power generation with large voltage or current ratio between the input and output [17,24]. This configuration has the problem of large component size, which may not fit for maritime applications that require compact design. Besides, the configuration of using active controlled ESS provides a solution that meets the requirement in both PPS and power density [18]. In this configuration, the ESS capacity can be modified according to the operation principle as the ESS is integrated to the PPS through an interface converter, therefore potentially reducing the system size and cost. With these benefits, this paper presents a fixed-frequency Sliding mode control (SMC) in a cascade scheme for the half-bridge bidirectional DC-DC converter that adopts the configuration of active controlled ESS for the PPS.

Besides the circuit part, several control strategies in PPS are presented in literature. In [25], a hysteresis current control is presented to compensate the current tracking in an active ESS, and the PPL voltage ripple can be reduced. However, PPL in different peak power is not considered, while this condition is common in practice and may cause stability issues. Nonlinear control methods are also used due to the simple implementation and fast speed, which are preferred in the PPS application. Among them, model predictive control (MPC) and SMC are investigated for PPLs in literature [26,27]. The MPC predicts the system states every sampling period and calculate the switching states through the cost function [28]. Though MPC can integrate multivariable and optimize the operation, the heavy calculation burden and dependency on model accuracy are the barriers in PPS applications. In contrast, besides a fast dynamic response, SMC has the merits of simplicity and robustness in face of model uncertainties and strong perturbations [27,29]. Due to the periodical pulsed signals of PPLs, the system equilibrium point is unfixed, and the system variables vary in a periodic alternating manner [28]. SMC, as a variable structure control method, is suitable for large-signal applications, of which PPL is a typical one. Therefore, SMC could naturally fulfill the demand of robust control in the PPS.

The implementation of SMC in bidirectional DC/DC converters is studied in several applications [30]. The control structure with PI controller in the outer voltage loop and SMC controller in the inner current loop is commonly used [31]. This structure has faster response than general dual PI cascade controller. However, the chattering phenomenon caused by SMC may result in variable switching frequency [32]. Several methods have been proposed to mitigate this issue, e.g., fuzzy control method [33], which eliminates the perturbation by adjusting the fuzzy switching gain [34]. Direct voltage control based on SMC can also be implemented in bidirectional DC/DC converters, and

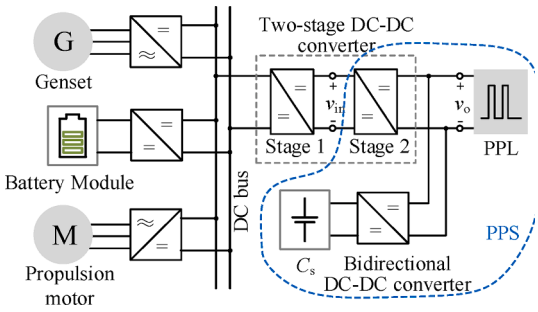

Fig. 1. DC shipboard microgrid with the a pulsed power load.

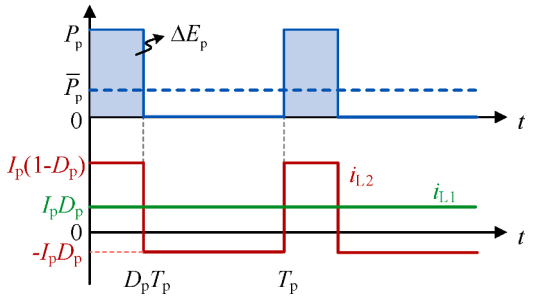

Fig. 2. PPL profile and ideal waveforms of power suppliers.

the controller could ensure fast transient response and robustness under load variation [35].

This paper takes a practical radar application as a study case to design and control a PPS, which consists of two interfaced buck converters to a DC SMG and an active controlled storage capacitor to provide the pulsed power. Based on feedback linearization theory, the sliding surfaces of a SMC in a direct voltage control (DVC) and current control for the buck converters in the PPS are designed, respectively. The feedback linearized SMCs can enforce the system voltage and current to track a desired dynamics on each converter in big signal, which makes the control more robust to PPLs. The main contributions of this paper are: 1) To develop a coordinated control method to prevent the negative impact of PPL propagating to the DC SMG. 2) To ensure fast and robust pulsed power supply to the PPL with reduced ESS capacity.

This paper is organized as follows. In section II, the system configuration, control principle and modeling of the PPS are discussed. Section III presents the sliding mode controller for the two converters in the PPS. Sizing of passive elements in the PPS is presented in section IV. Section V illustrates the simulation results that demonstrate the operation of PPS with the SMC. Finally, conclusions are drawn in section VI.

2. System configuration and control principle

This section presents the circuit configuration and dynamic model of the PPS in a 1 kV DC hybrid-electric ship. The DC SMG consists of generation sets, battery ESSs, and various types of shipboard loads. The generators and battery ESSs are parallel connected to the DC bus. Shipboard loads include the electric propulsion system, ship service loads, PPL and other dedicated high power loads. The diagram of a DC SMG is presented in Fig. 1, in which the specialized PPS is illustrated.

2.1. Circuit configuration

As shown in Fig. 1, there are two power suppliers for the PPL. One is the main system of the DC SMG, which provides power to the PPL through a SMG-side two-stage converter to step down from 1 kV to 200 V, and then from 200 V to 24 V. The other is the active storage capacitor C_s, which is connected to the PPL through a bidirectional DC-DC converter. Due to the high peak power associated to a PPL, low equivalent series resistance (ESR) storage capacitor is desired and placed as close to the PPL as practical [19]. Compared with conventional solution that using supercapacitor directly parallel connected to the PPL, the configuration adopted in this paper reduces the capacitance by using a small storage capacitor with a relative high voltage ripple, therefore reducing the cost [18].

Table 2
Parameters of the pulsed power load.

Parameters	Value
Rated PPL voltage v_o^*	24 V
Peak power P_p	4 kW
Pulse duty cycle D_p	20%
Pulse period T_p	5 ms

As the PPL connects to the SMG through a two-stage DC-DC converter, it is assumed that stage 1 provides a stable voltage v_{in} as the input of stage 2. In this paper, the buck converters are used as the interfaces between power sources and the PPL.

Fig. 2 illustrates the PPL profile and ideal waveforms of inductor currents. In practice, the pulse rise time and fall time, which are less than 100 μs, are much shorter than the pulse duration. Therefore, the load profile, denoted as $p_p(t)$, is ideally modelled as:

$$\begin{cases} \Delta E_p = \int_0^{D_pT_p} p_p(t)dt = P_pD_pT_p \\ p_p(0) = p_p(t_p) = 0 \end{cases} \tag{1}$$

where ΔE_p is the incremental energy in one pulse cycle, D_p is the duty cycle of the pulses, T_p is the pulse period, and P_p is the peak power [27].

The two power suppliers coordinate properly to meet the PPL demand in short response time and high peak power. The design is not optimized for efficiency if the PPS is designed only for the known peak-power demand, and the SMG generation power is larger than it needs to be [28]. Therefore, power averaging is used to make the PPS more cost effective and achieve high power density. Also, according to the requirements on PPS that the power absorbed from the main system should be constant to avoid propagating the negative impact of PPL to the SMG, the SMG side converter is designed to provide the average power of the PPL, as the green line shows in Fig. 2. While the storage capacitor C_s is designed to supply the extra current demanded by the PPL, and to sink current from the first buck converter by recharging the storage capacitor when the pulse is deactivated from D_pT_p to T_p in one pulse cycle, as the red line shows in Fig. 2.

In this paper, a case of pulsed load with the parameters shown in Table 2 is considered.

2.2. Dynamic model of the pulsed power supply system

As seen in Fig. 2, the PPS is formed by two buck converters: one reduces from a high voltage level v_{in} to a low voltage v_o, and another converter connected in parallel with the first buck converter regulating the current flow between the storage capacitor C_s and the PPL.

The buck converters can be modeled by the following bilinear models:

$$L_j\frac{di_{L_j}}{dt} = v_{in_j}\cdot u_j - v_o \tag{2}$$

$$C_j\frac{dv_o}{dt} = i_{L_j} - \frac{v_o}{R} \tag{3}$$

where L_j and C_j are the converters' inductor and capacitor, i_{Lj} is the inductor current, v_{inj} and v_o are the input and output voltages, R is the load resistance, u_j is the control input, and $j = 1, 2$. In the PPS configuration studied in this paper, the filter capacitor C equals to the capacitance of C_1 and C_2 in parallel.

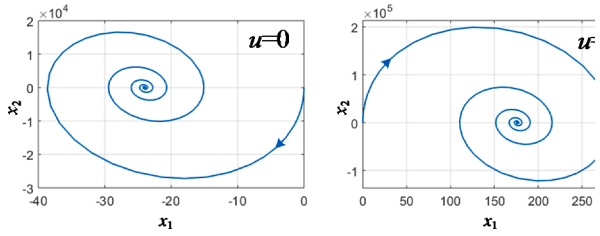

Fig. 3. State variable trajectories when $u = 0$ and 1.

3. Improved control scheme for PPL

In this section, the implementation of SMC in both SMG-side and active capacitor converters in the PPS are presented in detail. Both converters are going to be controlled by their corresponding SMC surfaces. According to the coordination strategy, these two converters are designed with direct voltage control (DVC) and current control, respectively, to meet the control objectives.

3.1. SMG-side converter control

The SMG-side buck converter is responsible for regulating the load voltage with small voltage fluctuation and fast dynamics. Therefore, the DVC is preferred, rather than the conventional dual-loop control in which the bandwidth of the outer voltage control loop is lower than then the inner current control loop [26]. Here, it is assumed that the perturbation induced in the output voltage of the stage 1 converter is small.

The control objective of stage 2 converter is to regulate the output voltage v_o to track the reference v_o^* of 24 V. Thus, define the error variables $x_1 = e_v = v_o - v_o^*$ and $x_2 = \dot{x}_1 = \dot{v}_o$ to regulate v_o. The derivative of x_2 can be deduced from (3) as

$$\dot{x}_2 = -\frac{1}{RC}x_2 - \frac{1}{LC}x_1 + \frac{v_{in}\cdot u - v_o^*}{LC} \tag{4}$$

The trajectories of the state variables in the phase plane when $u = 0$ and 1 are shown in Fig. 3 with the PPS parameters calculated in section IV and $v_{in} = 200$ V. Starting from the point ($x_1 = 0, x_2 = 0$), the trajectory is convergent to an equilibrium point at ($x_1 = -24, x_2 = 0$) and ($x_1 = 176, x_2 = 0$) when $u = 0$ and 1, respectively. Thus, it is reasonable to use the linear combination of x_1 and x_2 as the sliding surface for DVC in the SMG-side converter.

By feedback linearizing the converter, a given dynamics can be ensured [36]. In a SMC, the dynamic order is determined by the relative degrees of the systems. The relative degree r is the number of times that the system output should be differentiated until the input u appears in the expression. The relative degree gives information about to which degree the control directly regulates the output of the system.

By choosing the converter output voltage as the system output to be regulated, it is found that the relative degree is $r = 2$ for the SMG-side converter. Then, by defining the errors of the output voltage as $e_v = v_o - v_o^*$, a second-order dynamics can be imposed by identifying the derivative of the sliding surface with the following error functions:

$$\frac{ds_1}{dt} = \frac{d^2e_v}{dt^2} + \lambda_1\cdot\frac{de_v}{dt} + \lambda_0\cdot e_v = 0 \tag{5}$$

where s_1 is the sliding surface, λ_0 and λ_1 are the coefficients of the second-order dynamics imposed by the SMC. The error dynamics is exponentially stable if the coefficients λ_0 and λ_1 are chosen such that the Laplace s-polynomials

$$s_1^2 + \lambda_1\cdot s_1 + \lambda_0 = 0 \tag{6}$$

has all the poles in the left-hand of the Laplace plane [37]. By considering that the reference v_o^* is constant, so $\dot{v}_o^* = 0$ and $\ddot{v}_o^* = 0$, and integrating (5), lead to the following surface:

$$s_1 = \frac{dv_o}{dt} + \lambda_1\cdot v_o + \lambda_0\cdot\int\left(v_o - v_o^*\right)\cdot dt \tag{7}$$

This surface is a particular proportional plus integral and derivative (PID)-like surface that was previously reported in [30] for a resonant buck converter for tracking a constant voltage reference, in which the derivative gain has been set to 1, and λ_1 and λ_0 correspond to the proportional and integral gains, respectively. It is worth noting that in order to meet the requirements of high power rising rate and stable DC voltage for pulse load power supply, the surface in (7) is different from the existing linear surface to achieve fast dynamic response and robustness. The detailed design method is as follows.

To analyse the dynamic properties of the SMC defined in (6), the integral term is included as an extra state-space variable named as x_3, so the states for a single-stage buck converter are defined as

$$\begin{aligned} x_1 &= e_v = v_o - v_o^* \\ x_2 &= \dot{x}_1 = \frac{1}{C}\left(i_L - \frac{v_o}{R}\right) \\ x_3 &= \int x_1 dt = \int (v_o - v_o^*)dt \end{aligned} \tag{8}$$

Then the following state-space model, using (2) and (3), can be defined:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}u + \boldsymbol{D} \tag{9}$$

where,

$$\boldsymbol{A} = \begin{bmatrix} 0 & 1 & 0 \\ -\frac{1}{L_1C} & \frac{1}{RC} & 0 \\ 1 & 0 & 0 \end{bmatrix} \boldsymbol{B} = \begin{bmatrix} 0 \\ \frac{v_{in}}{L_1C} \\ 0 \end{bmatrix} \boldsymbol{D} = \begin{bmatrix} 0 \\ \frac{-v_o^*}{L_1C} \\ 0 \end{bmatrix} \boldsymbol{x} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}$$

The sliding surface of (7), for the buck converter, can be rewritten as

$$s_1 = \lambda_1 x_1 + 1\cdot x_2 + \lambda_0 x_3 = \boldsymbol{J}^T\boldsymbol{x} \tag{10}$$

where, $\boldsymbol{J}^T = [\lambda_1 \quad 1 \quad \lambda_0]$. The sliding controller takes a control action that drives the trajectory of the state variables towards the sliding surface, at the point $s_1 = 0$, hitting the surface regardless of the starting point. Once the states being close to the surface, the sliding controller should handle the control action and keep the trajectory of $\boldsymbol{x}$ within a small vicinity of the sliding surface, converging the states to the desired equilibrium point. To perform that, the existence condition should be meet [36,38,39], which ensures that the trajectories of × are always directed towards $s_1 = 0$, which is done using the Lyapunov's direct m2ethod $V(s_1) = \frac{1}{2}s_1^2$ [36,38,39], so that its derivative $\dot{V}(s_1) = s_1\dot{s}_1$ should be negative. Then, using (9), the derivative of (10) can be found as

$$\dot{s}_1 = \boldsymbol{J}^T\boldsymbol{A}\boldsymbol{x} + \boldsymbol{J}^T\boldsymbol{B}u + \boldsymbol{J}^T\boldsymbol{D} \tag{11}$$

The switching control law, (u_1=0, 1), can be chosen to ensure $\dot{V}(s_1) = s_1\dot{s}_1 < 0$. Therefore, for $s_1 < 0$, its derivative should be positive, and for $s_1 > 0$, the derivate is negative. This desired behavior can be accomplished by choosing the following control law:

$$u_1 = \frac{1}{2}[1 - sign(s_1)] = \begin{cases} 1, & s_1 < 0 \\ 0, & s_1 > 0 \end{cases} \tag{12}$$

In practice, to avoid complex calculation in signum, the control law can be realized via a comparison function by comparing the sliding surface with 0. When the surface is above 0, assign negative values to s_1; when the surface is below 0, assign positive values to s_1. By using (9), the derivative in (11) can be expressed in scalar representation as:

$$\dot{s}_1 = \lambda_0\left(v_o - v_o^*\right) + \frac{1}{C}\left(\lambda_1 - \frac{1}{RC}\right)\left(i_L - \frac{v_o}{R}\right) + \frac{v_{in}}{L_1C}u - \frac{v_o}{L_1C} \tag{13}$$

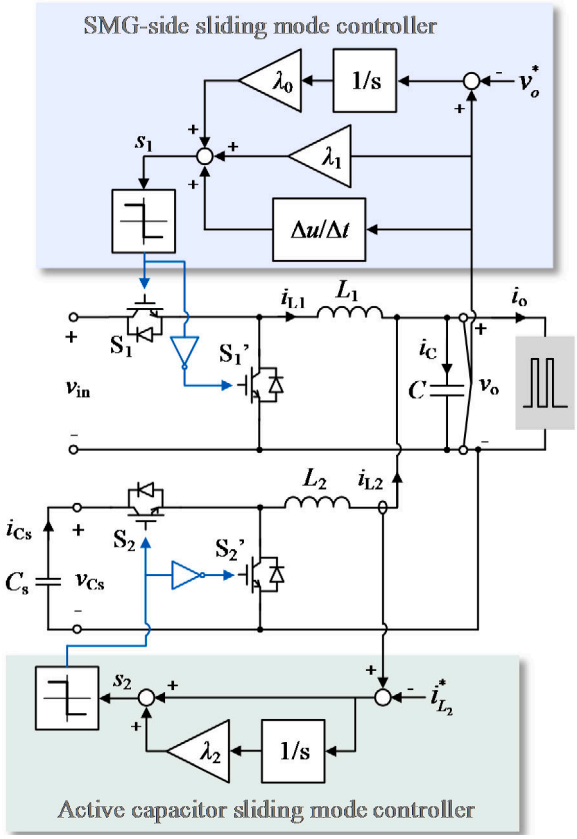

Fig. 4. Control diagram of the pulsed power supply system.

The design conditions of the sliding coefficients can be deduced considering the boundaries of the equivalent control, which is the continuous averaged value of the control has and known as u_{eq1}. The equivalent control can be obtained by averaging the buck converter model of (9) and by setting (13) to zero [36,38,39], as

$$u_{eq1} = \frac{\overline{v}_o}{v_{in}} + \lambda_0 \frac{L_1 C}{v_{in}} \left(\overline{v}_o - v_o^*\right) - \frac{L_1}{v_{in}} \left(\lambda_1 - \frac{1}{RC}\right) \left(\overline{i}_L - \frac{\overline{v}_o}{R}\right) \tag{14}$$

in which, $\overline{v}_o$ and $\overline{i}_L$ are the average values of v_o and i_L, respectively. The equivalent control is restricted to be inside the switching values, i.e., $0 < u_{eq1} < 1$. Therefore, the control parameters are limited by

$$\begin{aligned} 0 < \lambda_0 &< \frac{v_{in}}{L_1 C v_o^*} \\ 0 < \lambda_1 &< \frac{1}{RC} + \frac{R\left(v_{in} - v_o^*\right)}{v_o^*} \end{aligned} \tag{15}$$

By using the averaged dynamics of (9), the open loop dynamics of the buck converter can be described as

$$\frac{d^2\overline{v}_o}{dt^2} + \frac{1}{RC}\cdot\frac{d\overline{v}_o}{dt} + \frac{1}{L_1 C}\cdot\overline{v}_o = \frac{v_{in}}{L_1 C}\cdot u_{eq1} \tag{16}$$

with which, under the sliding surface ($s = 0$, $\dot{s} = 0$), the close loop dynamics is linearized

$$\frac{d^2\overline{v}_o}{dt^2} + \lambda_1 \cdot \frac{d\overline{v}_o}{dt} + \lambda_0 \cdot \overline{v}_o = \lambda_0 \cdot v_o^* \tag{17}$$

Comparing (17) with a standard form of a second-order system, i.e.,

$$\frac{d^2\overline{v}_o}{dt^2} + 2\xi\omega_n \cdot \frac{d\overline{v}_o}{dt} + \omega_n^2 \cdot \overline{v}_o = \omega_n^2 \cdot v_o^* \tag{18}$$

where ω_n and ξ are the undamped natural frequency and the damping ratio, respectively. Then, by identifying $\lambda_0 = \omega_n^2$ and $\lambda_1 = 2\xi\omega_n$, the system can be designed to behave as a linear second-order system, which could be under-damped for $0 < \xi < 1$, critically-damped for $\xi = 1$, or over-damped for $\xi > 1$.

The controller diagram of DVC using sliding mode controller in SMG-side buck converter is shown in Fig. 4.

3.2. Active capacitor controller

For the active capacitor converter, the control objective is to output the pulsed current with fast dynamic response. Therefore, the relative degree for the inductor current i_{L2} is $r = 1$, since this variable appears explicitly in (2). Then, defining the current tracking error $e_i = i_{L_2} - i_{L_2}^*$, a first-order dynamic can be imposed by the following identification:

$$\frac{ds_2}{dt} = \frac{de_i}{dt} + \lambda_2 \cdot e_i = 0 \tag{19}$$

where s_2 is the sliding surface, and λ_2 is the coefficient of the first-order imposed dynamic, which is stable if λ_2 is positive. Accordingly, the following sliding surface can be derived:

$$s_2 = e_i + \lambda_2 \cdot \int e_i \cdot dt \tag{20}$$

Similarly, the control law is derived by requiring $s_2 \dot{s}_2 < 0$. The control law for the active capacitor converter is defined as

$$u_2 = \frac{1}{2}\left[1 - sign(s_2)\right] = \begin{cases} 1, & s_2 < 0 \\ 0, & s_2 > 0 \end{cases} \tag{21}$$

Similar to the sign selection of s_1 in (12), the sign of s_2 in (21) can be obtained by using the comparison function. The time derivative of (20) is

$$\dot{s}_2 = \frac{1}{L_2}\left(v_{cs} \cdot u_2 - v_o\right) + \lambda_2 \left(i_{L2} - i_{L2}^*\right) \tag{22}$$

Letting $\dot{s}_2 = 0$ and the equivalent control using averaged dynamics is deduced as

$$u_{eq2} = \lambda_2 \left(i_{L2}^* - i_{L2}\right) + \frac{\overline{v}_o}{v_{cs}} \tag{23}$$

Considering the control boundary, $0 < u_{eq2} < 1$, the control parameter can be limited to:

$$0 < \lambda_2 < \frac{1}{L_2} \cdot \frac{v_{cs} - v_o^*}{i_{L2}^*} \tag{24}$$

The controller diagram in the active capacitor can be found in Fig. 4.

Since the capacitor C_s is aimed to supply the pulsed power to compensate the unbalance between PPL and the SMG-side converter, therefore, the current reference is calculated by:

$$i_{L_2}^* = \frac{p_{ppl}(t)}{v_0} - i_{L_1} = \frac{p_{ppl}(t) - D_p P_{ppl}}{v_0} \tag{25}$$

When the PPL is activated, the energy capacitor discharges and $i_{L_2}^*$ is positive. While during the interval between two pulses, the surplus power from SMG is charged into C_s, and i_{L2} is negative.

4. Sizing of inductor and capacitors of the PPS system

In this section, the design of storage capacitor C_s, inductors L_1, L_2, and output filter capacitor C are discussed.

4.1. Design of the storage capacitor

The capacitor C_s is desired to provide the pulsed component of the pulsed load. In one pulse cycle, neglecting the power losses in the switches, the energy of the C_s discharges is defined as

$$\Delta E_{C_s} = \int_0^{D_p T_p} v_o i_{L_2} dt \tag{26}$$

During $[0, D_pT_p]$, i_{L_2} is designed to be a positive constant discharging the current $I_{L_2\_d}$, which is $I_{L_2\_d} = (1 - D_p)I_p$. Also, ΔE_{C_s} can be calculated as

$$\Delta E_{C_s} = \frac{1}{2} C_s \left(v_{C_s\_h}^2 - v_{C_s\_l}^2 \right) \tag{27}$$

in which, v_{Cs_h} is the voltage from which C_s discharges in each pulse cycle, and v_{Cs_l} is the voltage that C_s reaches after being discharged in each pulse cycle. Note that v_{Cs_l} should be higher than the output voltage to ensure that the buck converter works properly. Combining (26) and (27), and substitute I_{L2_d} into I_{L2} during the pulsed power being activated, it can be derived that

$$C_s = \frac{(1 - D_p) P_p D_p T_p}{\Delta v_{C_s} \cdot \bar{v}_{C_s}} \tag{28}$$

in which, $\Delta v_{C_s} = v_{C_s\_h} - v_{C_s\_l}$ and $\bar{v}_{C_s} = (v_{C_s\_h} + v_{C_s\_l})/2$ are the voltage ripple and average voltage of C_s. From (28), to support a pulsed load with certain rated voltage, duty cycle and period, the capacitance of C_s can be reduced by increasing its average voltage and voltage ripple tolerance, and by reducing the pulsed current i_{L2_d}.

Taking the PPL parameters in Table 2 into (28), and assuming the allowed minimum voltage of C_s is 60% of the rated voltage, we have C_s = 4.3mF.

It should be noted that in practical applications, depending on the PPL types and the operation conditions, the duty cycle of a certain PPL may not be constant. Therefore, the capacitance of C_s can be larger than calculated to set redundancy.

4.2. Design of the SMG-side inductor

The SMG-side converter is designed to transfer the average power of the PPL. When the PPL is activated, the pulsed component of load power is provided by the C_s through the active capacitor converter. While when the PPL is deactivated, the surplus power from the SMG is charged into the C_s. Therefore, the PPL current consists of two parts, calculated as:

$$i_o = i_{L_1} + i_{L_2} - i_C = i_{o1} + i_{o2} \tag{29}$$

in which, i_{o1} and i_{o2} are the parts provided by the two buck converters, respectively. According to the coordination principle of the converters, the current in L_1 is calculated by

$$i_{o1} = D_p \cdot \frac{P_p}{v_o} \tag{30}$$

According to the relation between the inductor current and voltage, the inductor current i_{L1} increases by slope v_{L1}/L_1. The current increased during the switch conducting period t_{ON} and decreased during the switch turn-off period t_{OFF} are calculated by

$$|i_{L_1\_min} - i_{L_1\_max}| = \frac{v_{L_1\_ON}}{L_1} \cdot t_{ON} = \frac{v_{in} - v_o - v_{S1}}{L_1} \cdot \frac{D}{f_{sw}} \tag{31}$$

$$i_{L_1\_max} - i_{L_1\_min} = \frac{v_o + v_{S1'}}{L_1} \cdot \frac{1 - D}{f_{sw}} \tag{32}$$

where D and f_{sw} are the duty cycle and the switching frequency of S_1.

In steady state, the output current i_{o1} is the same as the average of inductor current, which can be written as

$$i_{o1} = \bar{i}_{L_1} = \frac{1}{2}(i_{L_1\_max} + i_{L_1\_min}) \tag{33}$$

In one switching period, the increase and decrease of the inductor current should be equal. Neglecting v_{S1}, then it can be derived that

$$i_{L_1\_max} = i_{o1} + \underbrace{\frac{v_o(v_{in} - v_o)}{2 v_{in} L_1 f_{sw}}}_{ripple\ \ current} \tag{34}$$

The second term in (34) is the amplitude of the ripple current in L_1. Therefore, according to the allowed ripple current, α(*100%) of i_{o1}, the inductance of L_1 can be calculated as follows:

$$L_1 = \frac{v_o(v_{in} - v_o)}{2 v_{in} \alpha i_{o1} f_{sw}} \tag{35}$$

Letting v_o = 24 V, v_{in} = 200 V, α = 20%, i_{o1} = 33.3A, f_{sw} = 100 kHz into (35), the inductance L_1 is calculated to be 15.8μH.

4.3. Design of the active capacitor side inductor

Since the active capacitor converter is aimed to provide the pulsed power to the PPL, it is desired to have a fast dynamic. Thus, the inductor L_2 which limits the increasing slope of the current is preferred to be small. On the other hand, the inductance should be designed to operate the converter in continuous conduction mode. Furthermore, considering the high power rating, the current ripple needs to be limited to reduce the conduction losses of the power switches. Thus, a tradeoff has to be made in designing the inductor L_2.

Similar with the derivation process for L_1, the inductance of L_2 can be calculated by (35) as well, while v_{in} should be replaced by the storage capacitor voltage v_{Cs}, and i_{o1} is replaced by i_{o2}.

$$i_{o2} = (1 - D_p) \cdot \frac{P_p}{v_o} \tag{36}$$

Letting v_{Cs} = 48 V, i_{o2}=133.3A. Thus, we can have L_2 = 2.1μH.

4.4. Design of the filter capacitor

Since the increasing slope of the inductor current is limited by the inductor value, the rising edge of the pulsed current has to be provided by the output capacitor C, and this results in the capacitor voltage drop. Similarly, at the falling edge of the pulsed load current, the surplus current is charged to C, causing capacitor voltage increase. Therefore, selecting the capacitance of C should meet the voltage tolerance of the pulsed load.

For either buck converter, in one switching cycle, during $[0, D/f_{sw}]$ and $[D/f_{sw}, 1/f_{sw}]$, meaning the switch S_j is ON and OFF, respectively, the inductor current i_{L_j} increases and decreases by:

$$\frac{di_{L_j\uparrow}}{dt} = \frac{1}{L_j}(v_{in_j} - v_o) \tag{37}$$

$$\frac{di_{L_j\downarrow}}{dt} = \left| \frac{1}{L_j}(-v_o) \right| = \frac{1}{L_j} v_o \tag{38}$$

At steady state, the inductor current i_{L_j} increases and decreases equally. However, at the raising edge of the pulsed current, since the capacitor C discharges, the capacitor voltage v_o decreases and results to be lower than its value at steady state. Therefore, the absolute value of $di_{Lj\uparrow}/dt$ becomes larger than that of $di_{Lj\downarrow}/dt$. Besides, the duty cycle is regulated to increase and raise the voltage by the controller, further making $\Delta i_{L_j\uparrow} = \frac{1}{L_j}\int_0^{D/f_{sw}} \left(v_{in_j} - v_o \right) dt > \Delta di_{L_j\downarrow} = \frac{1}{L_j}\int_{D/f_{sw}}^{1/f_{sw}} v_o dt$. With this effect, i_{L_j} increases when the PPL is activated, and the inductor current raising slope is limited by the inductance.

Similarly, at the falling edge of the pulsed current, the pulsed load current decreases, and a surplus current is charged into the capacitor C, increasing the capacitor voltage v_o. Thus, $\Delta i_{L_j\uparrow} < \Delta di_{L_j\downarrow}$, and i_{L_j} decreases when pulsed load is deactivated.

During the pulsed current raising edge, which is assumed to take the time of t_r, the inductor current increases and decreases are expressed as

Table 3
Control parameters of SMC and PI controllers.

SMC controller	SMG-side	$\lambda_0 = 1130^2$, $\lambda_1 = 1.8 \times 10^4$.
	Active capacitor	$\lambda_2 = 1.2 \times 10^5$.
PI controller	SMG-side	Voltage loop: kpv = 75, kiv = 10^5. Current loop: kpi = 3, kii = 20. LPF: $f_{c1} = 100$ kHz.
	Active capacitor	Current loop: kpi = 0.08, kii = 50. LPF: $f_{c2} = 100$ kHz.

follows respectively:

$$\Delta I_{L_j\uparrow} = \Delta i_{L_j\uparrow} \cdot \frac{t_r f_{sw}}{D} \tag{39}$$

$$\Delta I_{L_j\downarrow} = \Delta i_{L_j\downarrow} \cdot \frac{t_r f_{sw}}{1-D} \tag{40}$$

The difference between $\Delta I_{L_j\uparrow}$ and $\Delta I_{L_j\downarrow}$ is the change in the inductance current i_{L_j}, being equal to the pulsed current component provided by C_s, as expressed by

$$I_p = \sum_{j=1,2} \left(\Delta I_{L_j\uparrow} - \Delta I_{L_j\downarrow}\right) = t_r \left(\frac{v_{in} - \overline{v}_o}{L_1} + \frac{\overline{v}_{C_s} - \overline{v}_o}{L_2}\right) \tag{41}$$

For the SMG side converter, the input voltage v_{in} is constant, and ignoring the voltage change in C_s during the short period, (41) can be further expressed as

$$I_p = t_r \left[\frac{v_{in}}{L_1} + \frac{\overline{v}_{C_s}}{L_2} - \frac{(L_1 + L_2)\left(v_o^* - \frac{1}{2}\Delta v_o\right)}{L_1 L_2}\right] \tag{42}$$

Therefore, t_r can be calculated by

$$t_r = \frac{I_p L_1 L_2}{L_1 \overline{v}_{C_s} + L_2 v_{in} - (L_1 + L_2)\left(v_o^* - \frac{1}{2}\Delta v_o\right)} \tag{43}$$

During [0, t_r], C discharges with the capacitor current of

$$i_C = -I_p + \frac{I_p}{t_r} \cdot t \tag{44}$$

Therefore, the voltage drop on the pulsed load during one pulse cycle can be calculated by

$$\Delta v_o = \frac{I_p}{2C} t_r \tag{45}$$

Then, the capacitance of C is derived as

$$C = \frac{I_p^2 L_1 L_2}{2\Delta v_o \left[L_1 \overline{v}_{C_s} + L_2 v_{in} - (L_1 + L_2)\left(v_o^* - \frac{1}{2}\Delta v_o\right)\right]} \tag{46}$$

Taking the PPL parameters as well as L_1 and L_2 calculated in last subsections into (46), and letting the allowed voltage drop Δv_o be 3% of the reference voltage, the capacitor is selected as $C = 1.64$mF.

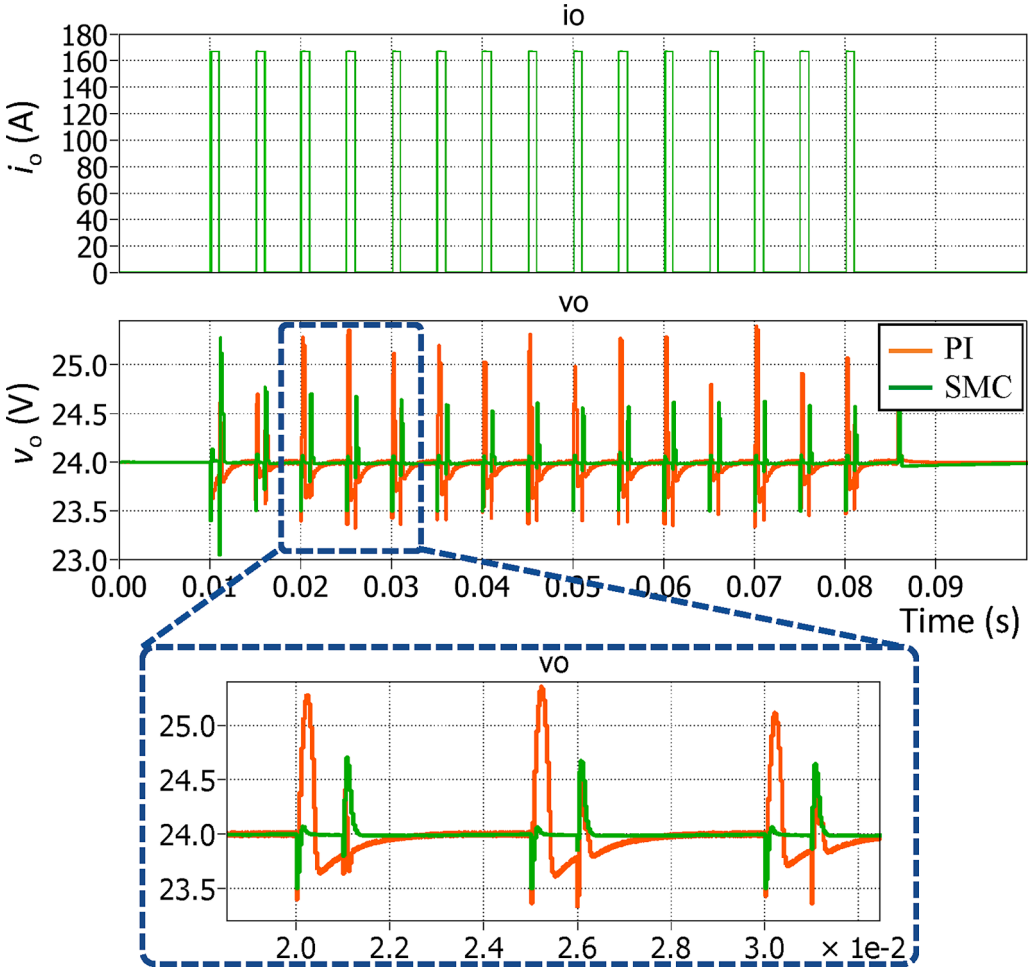

Fig. 5. Waveforms of the load current i_o and load voltage v_o in normal condition.

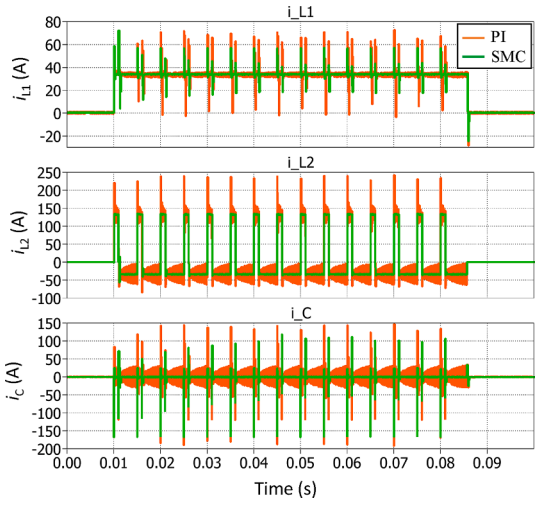

Fig. 6. Current waveforms of i_{L1}, i_{L2}, and i_C in normal condition.

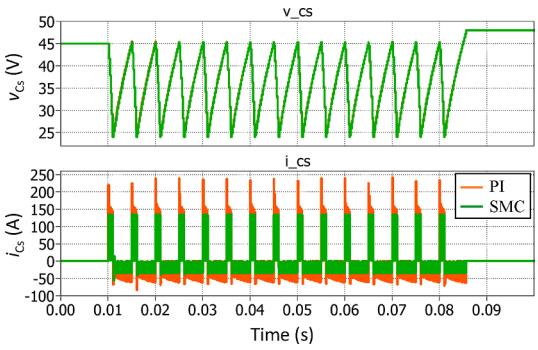

Fig. 7. Current and voltage of the storage capacitor in normal condition.

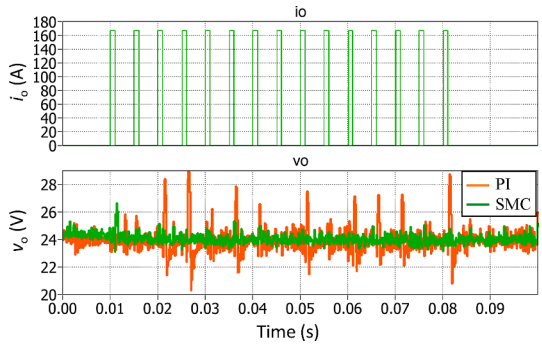

Fig. 8. Waveforms of load current i_o and load voltage v_o with sample noises.

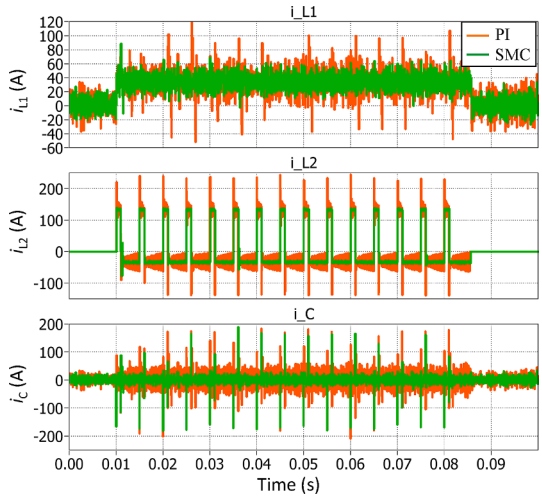

Fig. 9. Current waveforms of i_{L1}, i_{L2}, and i_C with sample noises.

5. Simulations

In this section, Matlab simulations are carried out to verify the feasibility of the presented PPS and control strategies. The circuit parameters in the PPS are as calculated in section IV, and the parameters for the 4 kW PPL are shown in Table 2. To verify the effectiveness, comparisons of the presented method and the conventional PI control method are demonstrated.

The control parameters of two methods are shown in Table 3. In the conventional PI control scheme, the SMG-side converter adopts a dual-loop controller, and the active capacitor is controlled by a current loop. The parameters of the PI controllers are tuned to achieve as fast dynamics as possible. The switching frequency is 100 kHz.

5.1. Dynamic response

The waveforms of load current i_o and load voltage v_o are shown in Fig. 5. The PPL is triggered at t = 0.01 s, and it lasts for 15 pulse cycles. As can be seen, both SMC and PI control schemes can provide good voltage regulation performance. However, in comparison, when the pulses are triggered and terminated, the transient state under SMC lasts for less than 0.4 ms, while it takes over 1 ms with the conventional PI controller. Furthermore, the voltage fluctuation under SMC is ± 0.7 V, smaller than that under PI with ± 1.2 V.

Fig. 6 shows the inductance current i_{L1}, i_{L2}, and filter capacitor current i_C in normal condition, representing the current flow from the DC SMG, the storage capacitor current and the filter capacitor current. Current sharing between the SMG-side converter and the active capacitor follows the desired principle, in which i_{L1} keeps constantly 34A, and i_{L2} is 133A when the pulsed power is activated and –34A charged to the storage capacitor when the pulsed power demand is terminated. It can be seen that the current ripple and fluctuation in i_{L1} under the SMC is around 0.5A, smaller than that under the PI controller, which is around 1.5A. The control performance difference is more significant in i_{L2} and i_C. The current ripple in i_{L2} under SMC is less than 2A, while it is up to 30A in PI control. As for the current ripple in i_C, it is 2A in SMC and 35A in PI controller. As i_{L2} is designed to provide the pulse component in the load current, the operating point in the active capacitor converter changes when the pulse is activated and deactivated in each pulse cycle. The amplitude of the current fluctuation in i_{L2} increases at every pulse in case of using PI control, while the current overshoot and ripple are kept small when using SMC.

The storage capacitor voltage and current are shown in Fig. 7. The storage capacitor discharges when the pulses are activated and charges when the pulses are inactivated. In each pulse cycle, the voltage v_{Cs} can be charged to the initial value, which is 45 V in this simulation case, and the large depth of discharge makes the capacitor fully utilized, allowing a smaller capacitor size with lower cost. As the storage capacitor current associate with i_{L2}, the current ripple and overshoot under the PI control are larger than that under SMC. The dynamic response is also improved in the presented PPS using the SMC.

5.2. Robustness to measurement noises

Taking the sample noises into consideration, which is inevitable in practice, comparison from the aspect of robustness against disturbances is taken for the presented SMC and conventional PI control. The amplitude of the disturbances is set to 1% of the rated value of each

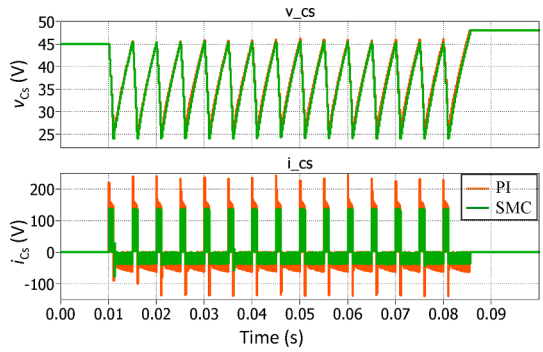

Fig. 10. Current and voltage of the storage capacitor with sample noises.

sample parameter.

Fig. 8 shows the load voltage in presence of noises in voltage and current measurements. With the measurement noise, the voltage fluctuates in the range of 23.2 V to 26.6 V when using the SMC controllers, while being 20.3 V to 28.9 V when using the PI controllers. This demonstrates that the presented PPS control scheme based on the SMC has better robustness to measurement noises than the conventional method based on the PI control.

The inductance currents i_{L1}, i_{L2}, and filter capacitor current i_C in presence of measurement noises are shown in Fig. 9. The current ripple of i_{L1} under the SMC is less than 35A, smaller than that under the PI control, which is up to 53A. The comparison of current ripple in i_{L2} between two controllers are significant that SMC has much better performance in current tracking against measurement noise. In i_C, the current ripple under SMC is approximately 40A, while it is 100A under PI controller. The simulation results verify the merit of the presented work using the SMC in terms of robustness to disturbances.

Fig. 10 shows the storage capacitor voltage and current in presence of sample noises. The maximum charging and discharging current under the PI control are −138A and 240A, respectively, with large overshoots, while under SMC there is tiny overshoots in the capacitor current, and the charging and discharging current are −36.5A and 136A, respectively. It shows that the impact of the measurement noise on the capacitor current is less significant when the PPS uses SMC rather than the PI control.

5.3. Robustness to PPS parameters

The robustness to PPS parameters is tested by changing L_1, L_2, and C, respectively. Here, the output voltage v_o is compared to show the differences in voltage control between the presented SMC and the conventional PI controllers. Change L_1 with 0.2 and 3 times of the calculated

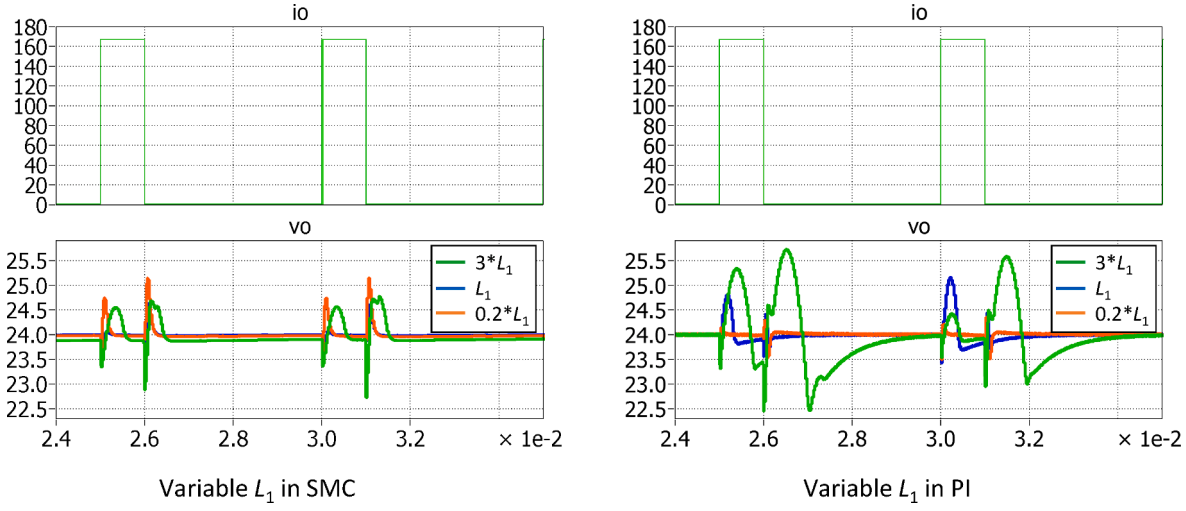

Fig. 11. Comparisons of SMC and PI controllers in different L_1.

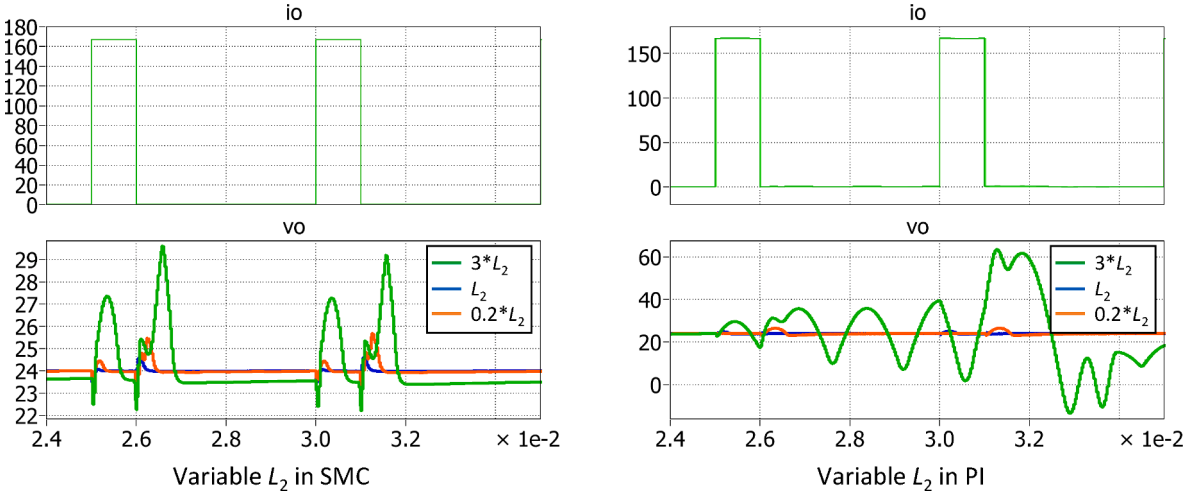

Fig. 12. Comparisons of SMC and PI controllers in different L_2.

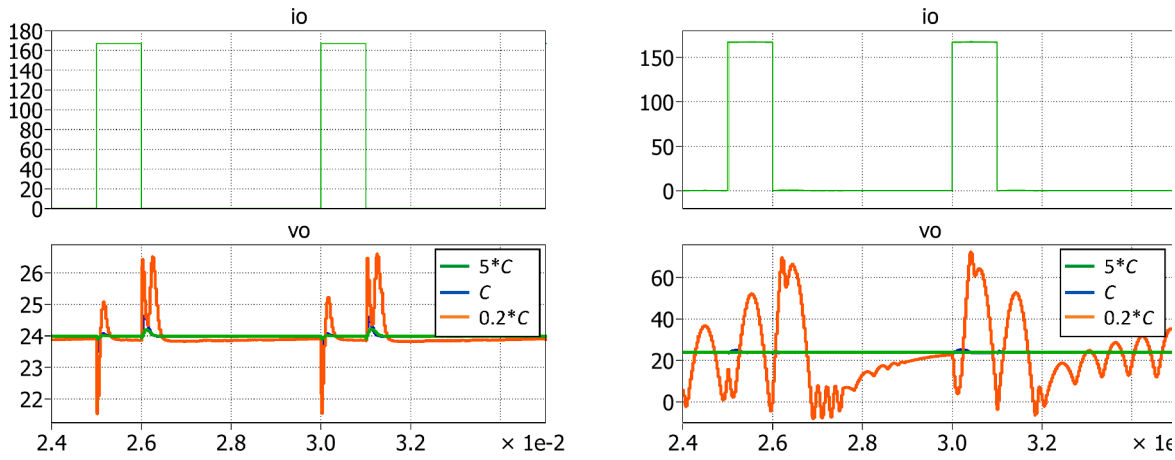

Fig. 13. Comparisons of SMC and PI controllers in different C.

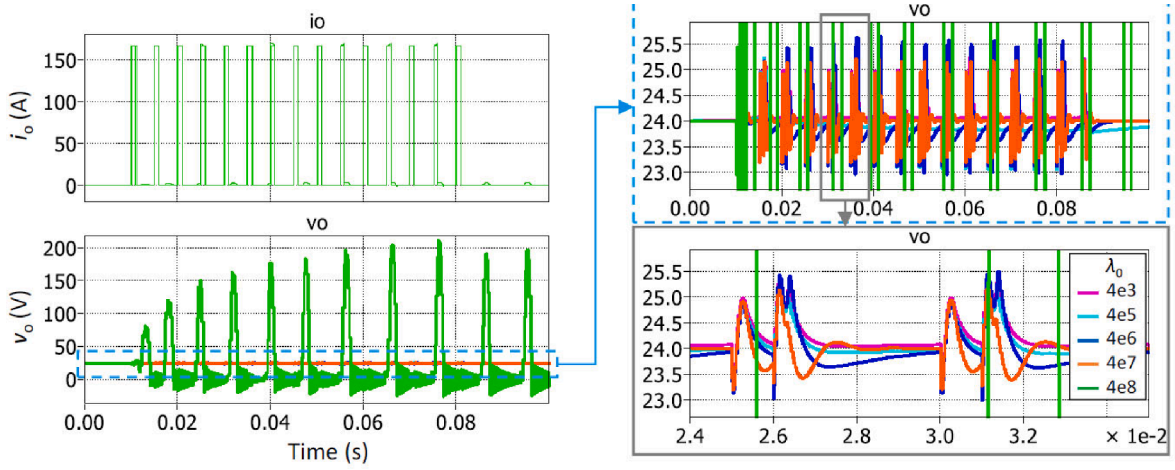

Fig. 14. Verification of λ_0, with fixed λ_1 and λ_2.

rated value, and keep L_2 and C constant, the comparison results are shown in Fig. 11. The voltage fluctuation is insignificant, less than $\pm$ 1.5 V, in these three L_1 values under SMC. In contrast, the PI controller is sensitive to L_1 value, that not only the voltage dynamic response gets worse, but also the voltage fluctuation increases when L_1 increases.

Change L_2 with 0.2 and 3 times of the calculated rated value, and keep L_1 and C constant, the comparison results are shown in Fig. 12. The output voltage has 5 V fluctuation under SMC when L_2 triples, while the system is out of control at the same scenario if using PI controller. Thus, the SMC is more robust against L_2 than the PI controller. Also, note that the voltage range in the case of changing L_2 is larger than that changing L_1, showing the PPS is sensitive to L_2.

Keep L_1 and L_2 constant, and change C from 0.2 to 5 times of the calculated value. The comparison results between SMC and PI controllers are shown in Fig. 13. When the C increases, the output voltage fluctuation is better mitigated intrinsically in both control methods.

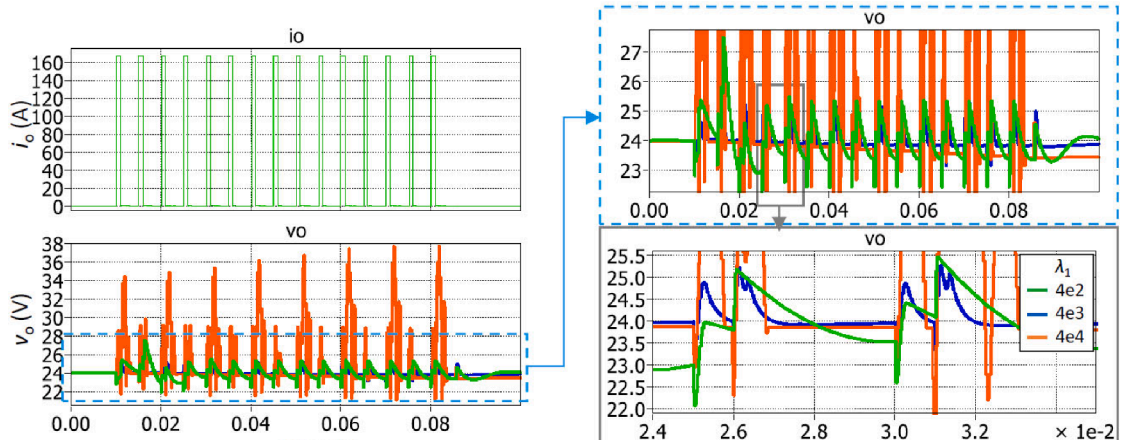

Fig. 15. Verification of λ_1, with fixed λ_0 and λ_2.

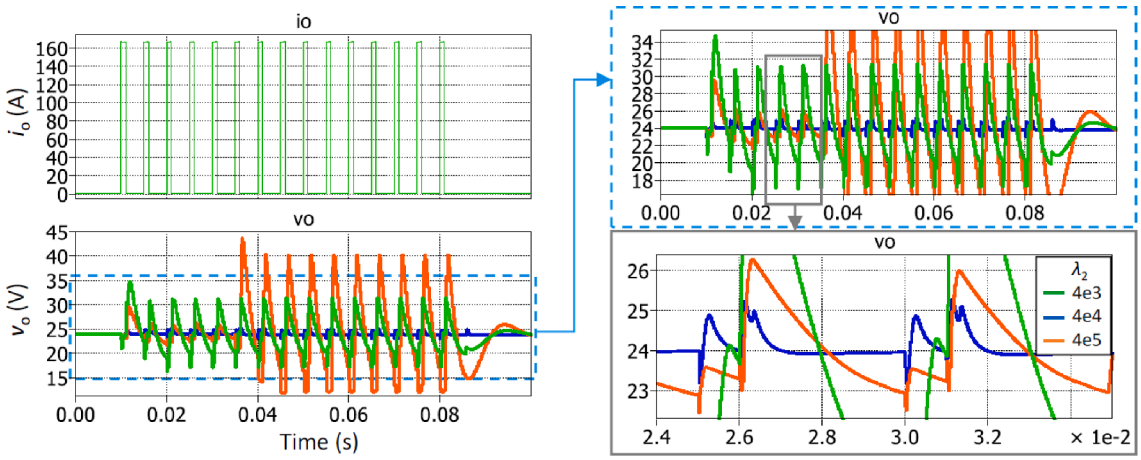

Fig. 16. Verification of λ_2, with fixed λ_0 and λ_1.

However, when reducing C, the output voltage can still be under control in the range of 21.4 V to 26.6 V in the case of using SMC, while with PI controller, the system suffers considerable oscillation. Thus, it can be concluded the SMC is more robust than PI controller for the PPS.

5.4. *Verification of control parameters*

To verify the control parameters of λ_0, λ_1 and λ_2 in the presented SMC, different values of the three sliding coefficients are tested in this section. According to the calculation in section 3, and substitute the circuit parameters given in section 4, the ranges of the sliding coefficients are obtained: $0 < \lambda_0$ less than 3.2×10^8, $0 < \lambda_1$ less than 4.2×10^3, and $0 < \lambda_2$ less than 6.7×10^4. In the following, three conditions in which each parameter is out of the range are simulated.

- Verification of λ_0.

Change λ_0 throughout the allowed range, and keep λ_1 and λ_2 within the calculated range. Here, λ_0 is set from 4×10^3 to 4×10^8, and $\lambda_1 = 4 \times 10^3$, $\lambda_2 = 4 \times 10^4$. The simulation results indicate that when λ_0 is smaller than the threshold, the voltage can be well controlled, and larger λ_0 leads to faster dynamics, as shown in Fig. 14.

- Verification of λ_1.

Change λ_1 throughout the allowed range, and keep λ_0 and λ_2 within the calculated range. Here, λ_1 is set from 4×10^2 to 4×10^4, and $\lambda_0 = 2 \times 10^5$, $\lambda_2 = 4 \times 10^4$. The simulation results are shown in Fig. 15, indicating that when λ_1 is smaller than the threshold, the voltage can be controlled with acceptable tolerance. Similar with the trend of λ_0, larger λ_1 leads to faster dynamics.

- Verification of λ_2.

Change λ_2 throughout the allowed range, and keep λ_0 and λ_1 within the calculated range. Here, λ_2 is set from 4×10^3 to 4×10^5, and $\lambda_0 = 2 \times 10^5$, $\lambda_1 = 4 \times 10^3$. The simulation results are shown in Fig. 16. It can be found when λ_2 is close to the threshold, the output voltage has good control performance with the tolerance less than 1 V, and when λ_2 exceeds the calculated range, the voltage becomes unstable. Note that when λ_2 decreases to 4000, the voltage ripple in v_o is up to 7.4 V.

6. Conclusions

In this paper, the control of a PPS with fast dynamic response and robustness is presented in detail. The PPS consists of two converters, one of which is the interface to the SMG and the other connects to a small storage capacitor. The storage capacitor is designed to provide the pulsed power, and the SMG provides the average power to the PPL. By using SMC in both buck converters in the PPS to regulate the output voltage and the pulsed current respectively, the demand of the PPL is well met. The sizing of the passive components in the PPS according to the control principle is discussed in detail. The effectiveness of the designed system parameters and the presented controllers are verified in the simulations of a PPS for a 4 kW PPL using Matlab/Simulink. Comparisons with the conventional control method for the PPS are taken, and the results show that the presented PPS in this paper can provide a good voltage regulation for PPLs with faster response and better robustness to disturbances and system parameters.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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