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A Symmetric Switched-Capacitor Based Basic Inverter Unit for Grid-Connected PV Systems

Hossein Khoun Jahan, Mitra Sarhangzadeh, Jaber Fallah Ardashir, and Frede Blaabjerg

Abstract- In this paper a new inverter unit is proposed. It is a compact switched-capacitor-based inverter, which is combined of four switches, two diodes and four capacitors. Since this inverter unit is a mid-point-clamped inverter, it can mitigate the capacitive leakage current in many applications. One of the main applications of the proposed inverter is in grid-tied photovoltaic (PV) systems, where the common-mode current brings many challenges. Other than the mentioned feature, the proposed inverter includes the following advantages: i) spontaneous balancing of the voltage across the capacitors without needing any control system or auxiliary circuits, ii) capability of full reactive power transfer, iii) low voltage stress on the capacitors compared to common three-level inverter topologies (NPC, T-type-NPC, FC and etc.), and iv) symmetric switching sequence, which causes a continuous input current. The feasibility and versatility of the proposed inverter unit is validated by experimental tests, which are conducted by using a lab-scale prototype.

Key Words- switched-capacitor, transformer-less inverter, self-balancing, leakage current, grid-tied PV system.

I. INTRODUCTION

Due to energy shortage and environment pollution, using renewable energy resources instead of conventional fossil-energy-based power plants is inevitable. Renewable energies resources are mostly reliant on power electronic converter to meet the requirements of power networks and customers. Whereas the infrastructures of power systems are based on ac voltage, and most of the renewable energy resources produces dc voltage, inverters play an important role in modern power systems. It goes without saying that among the renewable energy resources PV and wind systems are the most promising energy resources. PV-based electric sources mostly use dc-dc converter, dc-ac inverter or a combination of the two mentioned converters. The converters in PV systems are required to meet some special standards. The most important issues in this field are efficiency and the parasitic capacitor that appear between the PV panels and ground, which brings troublesome leakage current [1-2]. In order to reduce the volume and cost of grid-connected PV systems many attempt to eliminate bulky low-frequency transformer [3-5]. Other than reducing the cost, bulkiness and weight, eliminating transformers reduces the power losses and improves the efficiency. However, by removing

transformer in PV systems the galvanic isolation will disappear and causes some new challenges. As mentioned above, the capacitive leakage current is one of the main problems which might reduce power quality, cause safety problems and increase power losses.

Several strategies have been proposed to address inverter problems and improve the performance of these devices. The strategies can be categorized in three branches as i) advanced controlling methods [6-7] ii) improved switching strategies [8-9] and iii) topological solutions [10-12]. Inverters in different applications have special requirements where these devices in PV applications are required to limit capacitive leakage current, which arises from parasitic capacitances of PV modules. Additionally, they have to be of high efficiency and reliability. So far, many PV inverters have been introduced to fulfill the mentioned requirements. In order to reduce the cost and volume of the whole PV system the attempt is to use transformerless inverters. To address the problems in grid-tied PV systems three classes of topological solutions can be considered for PV inverters. The first solution is to decouple the dc-side from ac-side during zero voltage state. The H5 and HERIC PV inverters are the example of inverters that employ the mentioned solution that is the core idea of references [13-14]. The second solution is to use common-ground inverters. These types of inverters try to eliminate the leakage current by connecting the negative pole of the PV module to the ground of the grid. Although these inverters have successfully caused zero leakage current, they suffer from non-symmetric usage and non-equal power loss of the utilized components. Several common-ground PV inverters are introduced in [15-17]. The topological solution for grid-tied transformerless PV inverters are to use neutral point clamped inverters like Neutral point clamped (NPC) and T-type-NPC [18-20]. These inverters are used in many industrial applications. However, they have a symmetric structure and many other advantages, while the buck characteristic is counted as their main drawback.

To cover the challenge, this work is conducted to put forth a new three-level transformerless PV inverter. The

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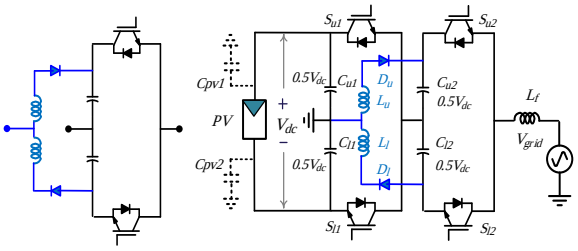
proposed inverter is a neutral-point-clamped inverter that uses four switches and two diodes. Two small inductors are also used to provide zero current switching condition for the diodes. The proposed inverter has a symmetric structure and it features leakage current limiting capability. Unlike the conventional NPC and T-type-NPC, this inverter has unity voltage gain and lower voltage stresses over the components. The proposed inverter can be configured as a three-phase inverter as well.

This work will be continued as follows; in the next section the configuration of the proposed inverter will be defined. Section III will deal with the component design of the proposed inverter. The three-phase configuration of the proposed inverter will be briefly explained in section IV. In section V, a detailed comparison will be provided where the proposed inverter will be compared with the well-known transformerless PV inverters. In section VI, by using a simulation model, the performances of the proposed inverter in a grid-tied PV system will be investigated. In order to prove the feasibility of the proposed inverter, it is tested experimentally using a lab-scale prototype. Experimental results are discussed in section VII. Finally, the overall work will be concluded in the last section.

II. CONFIGURATION OF THE PROPOSED INVERTER

The basic unit and overall configuration of the proposed inverter are exhibited in Figs.1 (a) and (b) respectively. As it is seen in Fig. 1(a) the basic unit is a half-bridge equipped with two diodes and small inductors. These diodes are served to charge the capacitors in appropriate switching instances. As seen in Fig.1(b), the overall configuration of the proposed inverter is a mid-point clamped inverter that can easily mitigate the common-mode voltage and develop a symmetric three-level ac voltage. The switching method and components status in different switching patterns are defined in Table I.



(a) (b)

Fig. 1. Proposed PV inverter, (a) basic unit, and (b) overall configuration.

TABLE I. OPERATION STATES OF THE INVERTER

Level	Switches states	Diodes states	Capacitors states	V_{out}
	S_{u1},S_{l1} ,S_{u2},S_{l2}	D_u,D_l	C_{u2}, C_{l2}	
1	1010	01	*D,C*	$1V_{dc}$
0	0110	10	*C,N*	$0V_{dc}$
0	1001	01	*N,C*	$0V_{dc}$
-1	0101	10	*C,D*	$-1V_{dc}$

The current paths for the positive, zero and negative voltage levels are, respectively, depicted in Fig. 2(a), (b) & (c) and (d).

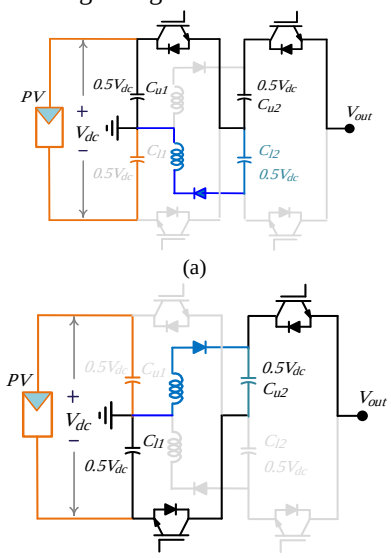
The operation principle can be defined as follows:

Positive voltage level: As seen in Fig. 2(a), to develop the positive voltage level the upper switches (S_{u1} and S_{u2}) are turned on. Under this condition C_{l2} is connected in parallel with C_{ul} so it is charged to $0.5V_{dc}$ through S_{u1}, D_{l2} and C_{u1}, simultaneously.

Zero voltage level: As it is seen in Figs. 2(b) and (c), there are two switching patterns to realize the zero voltage level. In the first switching pattern that is shown in Fig. 2(b), S_{l1} and S_{u2} are turned on. Under this condition C_{11} is paralleled with C_{u2} and it stays in the charging mode. In the second switching pattern, which is depicted in Fig. 2(c), S_{u1} and S_{l2} are turned on and put C_{l2} in the charging state. Since the zero voltage level is realized in each PWM switching cycle, and considering that during the two mentioned switching patterns two different capacitors are charged, it will be possible to reduce the voltage ripple across C_{u2} and C_{l2} as much as possible. Reduction in voltage ripple across the mentioned capacitors leads to a reduction in charging current of the capacitors. Considering that the main problem of switched-capacitor based converters is the inrush current of utilized capacitors, this problem is attenuated in the proposed inverter.

Negative voltage level: as shown in Fig. 2(d), in order to develop the negative voltage level, the lower switches (S_{l1} and S_{l2}) are turned on. Under this condition C_{u2} is put in the charging mode and it is charged to 0.5Vdc, spontaneously, through D_u and S_{l1}.

It is obvious that the neutral balancing of capacitors and continuous input current are preserved with the switching sequences according to Fig. 2.



(a)

(b)

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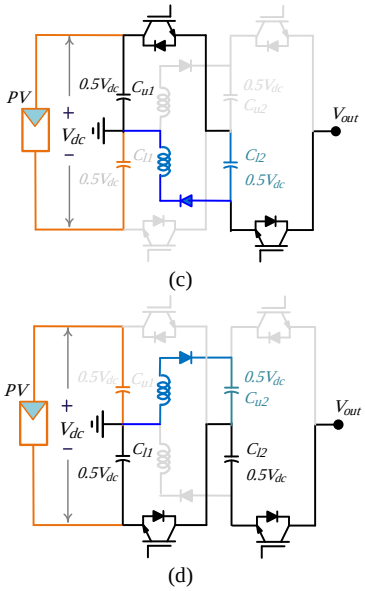

Fig. 2. Current path of (a) positive voltage level, (b) & (c) zero voltage level, and (d) negative voltage level.

III. COMPONENT SIZING

A. Voltage ripple and components sizing

The proposed inverter uses two splitting capacitors at the input cell and two switched-capacitors at the basic cell. The voltage across each of the input capacitor is calculated as

$$V_{Cu1} = V_{Cl1} = \frac{V_{dc}}{2} + \Delta v_{cin} \tag{1}$$

Where V_{Cu1}, V_{Cl1}, are the voltage stresses of the input capacitors and V_{dc} is the input voltage. Δv_{cin} is voltage ripple across the mentioned capacitors which is calculated as

$$C\frac{dv_{cin}}{dt} = \frac{mI_m}{2}(1-\cos 2\omega t) \tag{2}$$

$$\Delta v_{cin} = \frac{mI_m}{4Cf} \tag{3}$$

Where m, I_m, f, and $C(C=C_{u1}=C_{l1})$ are modulation index, the peak value of the output current, grid frequency and capacitances of the input capacitors.

As the switched-capacitors in the basic cell are in parallel with the input capacitors, in some proper switching instances, the voltage across these capacitors are the same as that across the input capacitors.

Referring to Figs. 2(a) and (d), it is understood that C_{u2} and C_{l2} are discharged when the positive and negative voltage levels are realized accordingly. Since in any switching period there are two switching strategies to develop the zero voltage level, we can put the desired capacitor in the charging mode during the zero voltage state. Thus the longest discharging duration of C_{u2} and C_{l2} is shorter than one switching cycle. Having this fact in mind, the maximum voltage ripple across C_{u2} and C_{2l} is given as

$$\Delta V_{Cu2(l2)} = \frac{mI_m}{2C_{u2(l2)}f_{sw}} \tag{4}$$

Where f_{sw} is the switching frequency.

B. Charging inductors to prevent power loss

Paralleling capacitors with different initial charge, as it is the case in switched-capacitor cell will cause energy loss. The following equation define the way the energy loss takes place in the switched-capacitor shown in Fig. 3.

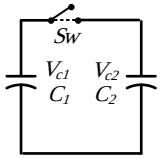

Fig. 3. Hard charging of capacitors

The energy before paralleling the capacitors is the summation of the energy stored in each capacitor as

$$U_0 = \frac{1}{2}C_1V_{c1}^2 + \frac{1}{2}C_2V_{c2}^2 \tag{5}$$

The voltage across the capacitors after paralleling the capacitors is given as

$$V_{C_t} = \frac{C_1V_{c1} + C_2V_{c2}}{C_1 + C_2} \tag{6}$$

The energy after paralleling the capacitors is given as

$$U_{1h} = \frac{1}{2}(C_1 + C_2)\left(\frac{C_1V_{c1} + C_2V_{c2}}{C_1 + C_2}\right)^2 = \frac{1}{2}\frac{(C_1V_{c1} + C_2V_{c2})^2}{C_1 + C_2} \tag{7}$$

In the case C1=C2=C, the aforementioned equations can be simplified as

$$U_0 = \frac{1}{2}C\left(V_{c1}^2 + V_{c2}^2\right) \tag{8}$$

$$V_{C_t} = \frac{V_{c1} + V_{c2}}{2} \tag{9}$$

$$U_{1h} = \frac{1}{2}CV_{Ct}^2 = \frac{C}{4}(V_{c1} + V_{c2})^2 \tag{10}$$

The energy loss after paralleling the capacitors is given as

$$\Delta U = U_0 - U_{1h} = \frac{1}{2}C(V_{c1} - V_{c2})^2 \tag{11}$$

As it is understood from (11) the hard charging of the capacitors increase energy loss. For the sake of avoiding energy losses, the capacitors can be charged through a small inductor as shown in Fig. 4, and described by (12) to (17).

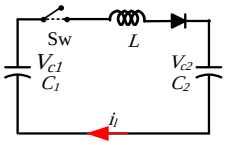

Fig. 4. Soft charging of capacitors.

After turning on the switch the current equation is obtained as

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$$L\frac{di_l}{dt} = V_{c1} - V_{c2} = \Delta v \tag{12}$$

$$i_l = \frac{\Delta v}{l\omega_r}\sin\omega_r t \tag{13}$$

Where $\omega_r = \sqrt{\frac{2}{LC}}$

Assuming an initial condition of $V_{c1}(0)=V+\Delta v$ and $V_{c2}(0)=V$, the voltage equation after turning on the switch is obtained as

$$V_{c1}(T_s) = V + \Delta v - \frac{1}{C}\int_0^{T_s} i_l(t)dt = V \tag{14}$$

$$V_{c2}(T_s) = V + \frac{1}{C}\int_0^{T_s} i_l(t)dt = V + \Delta v \tag{15}$$

The total energy stored in the capacitors before turning on the switch is given as

$$U_0 = \frac{1}{2}C\left((V_{c1}(0))^2 + (V_{c2}(0))^2\right) = \frac{1}{2}C\left((V+\Delta v)^2 + V^2\right)$$
$$U_0 = CV^2 + CV\Delta v + \frac{1}{2}C\Delta v^2 \tag{16}$$

The total energy after turning on the switch is given as

$$U_{1s} = \frac{1}{2}C\left((V_{c1}(T_s))^2 + (V_{c2}(T_s))^2\right) = \frac{1}{2}C\left(V^2 + (V+\Delta v)^2\right)$$
$$U_{1s} = CV^2 + CV\Delta v + \frac{1}{2}C\Delta v^2 \tag{17}$$

$$\Delta U = U_0 - U_{1s} = 0 \tag{18}$$

As it is implied from (16), (17) and (18) the energy stored in the capacitors before and after switching action is the same and no energy is lost. As the capacitors are charged in each switching cycle, hard charging of the capacitor will lead to a significant power loss. Using small inductor in the charging path will avoid the mentioned power loss.

The inductor L_u and L_l in the proposed inverter are used to limit the inrush current of the capacitors and limit the power loss that arises from inrush current of capacitors. The size of these small inductors are calculated by considering the fact that the charging process of the capacitors should last during a switching interval. Therefore, the inductor size is calculated as

$$L_{u(l)} = \frac{1}{C_{u2(l2)}(2\pi f_{sw})^2} \tag{19}$$

The switches and diodes in the proposed inverter should withstand the input dc voltage.

The charging current of the switched-capacitors is given as

$$L_{u(l)}\frac{di_{u(l)}}{dt} + (r_d + r_{sw} + 2ESR)i_{u(l)} = \Delta V_c + V_{ow} + V_{od} \tag{20}$$

Where r_d, r_{sw}, ESR, ΔV_c, V_{ow}, and V_{od} are resistance of diode, on-state resistance of switch, equal series resistance of a capacitor, on-state voltage of switch, and on-state voltage of switch and on-state voltage of charging diode.

According to Eq. (20), the charging current is limited by the charging inductor and parasitic resistance of the components. What is more, the charging inductors can provide zero current switching condition for diodes and smooth the charging current which reduces the EMI. Fig. 5 shows the current and voltage curves of the diodes. To explain the charging process of the capacitors the charging mode in positive and zero voltage levels are represented. Referring to Fig. 5(a), It is seen that voltage across L_l is V_{cu1}-V_{cl2}=ΔV, and voltage across L_u is zero, hence I_{dl} (current of diode D_l) begins to increase as seen in Fig. 5(c). As seen in Fig. 5(b), at the end of switching cycle when the zero voltage level mode is switched, the voltage across L_1 becomes -(V_{cl1}+V_{cl2}). When the voltage is reversed across L_1 the current start to decrease abruptly during t_s interval. As the current reaches to zero, the diode ceases to conduct. This is the case for L_u and diode D_u in the next switching period. Thus, the turn on and off of the diodes take palace under zero current condition. It is to be noted that, for simplicity, the parasitic resistance of the components is ignored in this analysis.

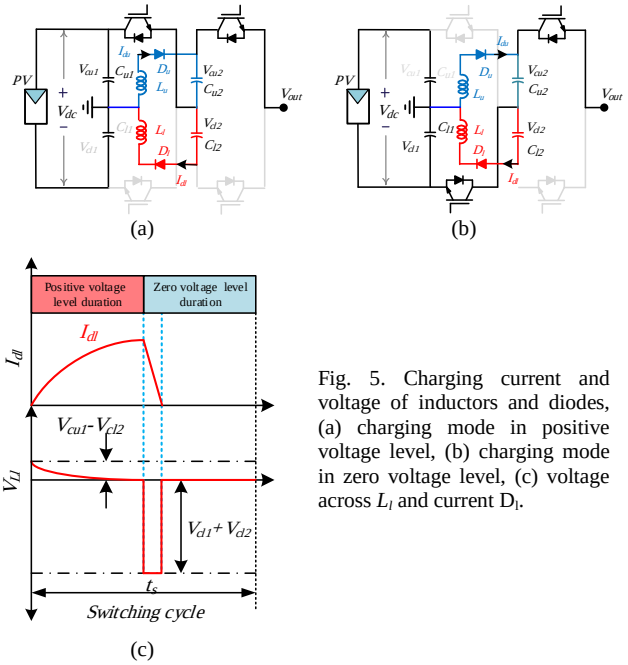

Fig. 5. Charging current and voltage of inductors and diodes, (a) charging mode in positive voltage level, (b) charging mode in zero voltage level, (c) voltage across L_l and current D_l.

The switches S_{u1} and S_{l1} have to withstand the load current plus the charging current, however S_{u2} and S_{l2} only tolerate the load current.

IV. THREE-PHASE CONFIGURATION

The three-phase inverters are one of the most important components in industry. The common three-phase inverter is synthesized with three traditional half-bridge inverters which develops a two-level voltage in each phase. In order to

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enhance the quality of the converted voltage and develop a three-level phase voltage, NPC, T-type NPC and flying-capacitor inverters were introduced. Although the mentioned inverter topologies can develop a three-level voltage, they have a buck characteristics and cannot effectively use the input dc voltage.

The three-phase configuration of the proposed inverter can cover many challenges in three-phase applications. As an advantage, the three-phase configuration can create three-level voltage with peak value equal to the input voltage. The three-phase configuration of the proposed inverter is exhibited in Fig. 6.

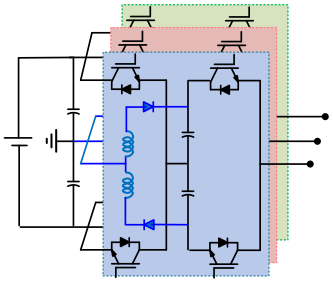

Fig. 6. Three-phase configuration of the proposed inverter.

V. BENCHMARKING WITH THE PRIOR-ART PV INVERTER

In this part the proposed inverter is compared with the well-known H5 [11], HERIC [12], Virtual-dc-bus [13], NPC [14], T-type NPC [15], and Flying-Capacitor [16] three-level inverters, from different point of views. All the mentioned inverters are employed in grid-tied PV applications and depicted in Fig.7. To do so, different features of the mentioned inverters along with the proposed inverter are indicated in Table II. As it is seen in this table the H5, and Virtual-dc-bus require five switches, HERIC uses six switches, the other inverters including the proposed one need four active switches. The NPC and the proposed inverter need two extra diodes, however, as the diodes in the proposed inverter are turned on and off in zero current condition, they experience no switching losses. As it is evident, the proposed and Flying-capacitor inverter use, respectively, two and one extra capacitor with respect to the other inverters. As an advantage, the voltage of the capacitors in the proposed topology are spontaneously balanced, which is not the case in the Flying-capacitor inverter as it needs auxiliary circuit and complicated switching methods to balance the voltage of the flying capacitor. Although to proposed inverter needs two inductors in charging path, these inductors are very small and would not add extra weight and cost to the inverter.

As it can be seen from the above paragraph, compared to some of the considered inverters, the proposed inverter uses some extra devices to approach a three-level voltage. This demerit can be ignored when considering the advantage that the voltage gain of the proposed inverter is unity and this important parameter in the NPC, T-type-NPC and Flying-capacitor inverters is half. Furthermore, the switches in the H5, HERIC, NPC, Flying-capacitor and the proposed inverter withstand the peak value of the output voltage (Vp), however, the voltage stress of the unidirectional switches in the T-type-NPC inverter is two times of the peak value of the output voltage (2Vp). Although the proposed inverter needs four capacitors, the voltage across the capacitors is 0.5Vp, as seen in Table II. The voltage stress of the capacitors in NPC, T-type-NPC, and Flying-capacitor is Vp. Hence, the capacitors in the proposed topology are small and cheap.

Other important feature is the possibility to be configured as a three-phase inverter. In this regards, the NPC, T-type-NPC, Flying-capacitor and the proposed inverters can be used as a three-phase converter by connecting three inverter units to a single input dc source. Nevertheless, this is not the case for the H5, HERIC, and Virtual-dc-bus inverters.

In the case of the common-mode voltage, the H5, and HERIC have a constant common-mode voltage equal to the input voltage. As the negative pole of input dc source is connected to the ground of the ac side in the Virtual-dc-bus inverter, this inverter develops zero common-mode voltage. The common-mode voltage in the other inverters including the proposed one varies with the ac-side voltage frequency and has a direct relation with the output current and an inverse relation to the input capacitors and ac-side frequency. Since the ac-side frequency is low compared to the switching frequency, the mentioned common-mode voltage would lead to an insignificant leakage current in grid-tied applications of the proposed inverter.

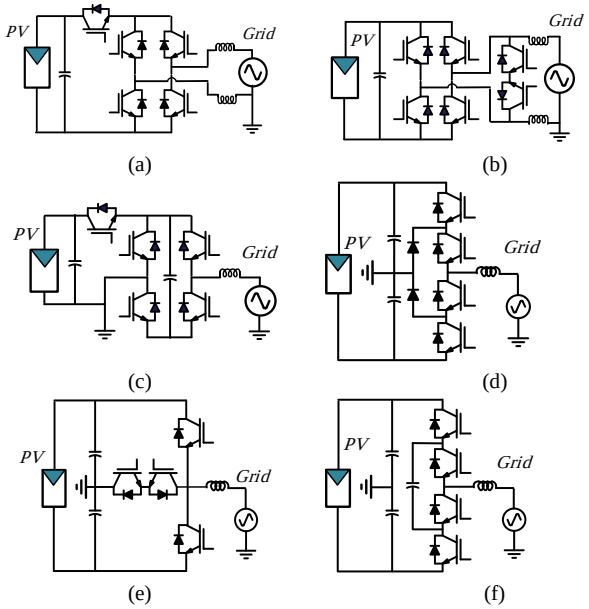

Fig. 7. Three-level inverter topologies in PV applications, (a) H5 [13], (b) HERIC [14], (c) Virtual-dc-bus [16], (d) NPC [19], (e) T-type-NPC [20], and (f) Flying-capacitor [18].

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Efficiency is one of the most important parameters in converters. In order to compare the efficiency of the considered inverters, it is assumed that the inverters are all constructed with IXFT50N50P3 switch and VS-249NQ150Pbf diode. The equal series resistance of the capacitors, the switching frequency, line frequency and the peak value of the output voltage are assumed 70 mΩ, 24 kHz, 50 Hz, and 320 V, respectively. The efficiency of the compared inverters is shown in Fig. 8.

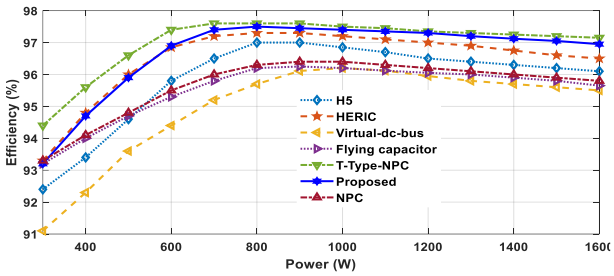

Fig. 8. Efficiency of the considered inverters.

Moreover, there are some other topologies that are based on switched-capacitor concept [11], [12], and [21]. As mentioned earlier, since the capacitors in the switched-capacitor cell are exposed to a hard charge, they experience energy loss as stated in (11). Other than energy loss, the inrush current appeared in these type of converters could increase the components' failure rate and bring about EMI. For instance, a sensor less cascaded half-bridge multilevel inverter, which is proposed in [21], would cause a significant energy loss when transferring the energy from the input source to several cascaded half-bridges cells. Using inductors to smoothly charge the capacitors can prevent the mentioned energy loss. However, using inductor would slow down the charging process and adversely affect the converter dynamic performance. This can be the main drawback of the switched-capacitor based multilevel inverter in [21]. Since the proposed inverter and the inverters mentioned in Table II are voltage source inverter they could not limit the fault current.

The other solution to address the problems in grid-tied PV system is using two-stage converters. In these kinds of converters, a dc-dc converter is used to track the maximum power point and conditioning the dc-link voltage. To this end a Z-source, quasi-Z-source, boost and dual-boost dc-dc converter are connected to a front-end inverter [22], [23] and [24]. Although these types of converters meet several requirements of grid-tied PV system such as limiting the fault current, they have a complex structure, more passive elements, and require a complicated control strategy. A new two-stage converter is suggested in [25]. This inverter uses two boosting inductors and two diodes to form a dc-dc stage. In order to reduce the number of switches, two switches of the utilized H-bridge are used to fix the dc-voltage link and develop ac voltage simultaneously. Even though this inverter succeeded to reduce a switch and it can effectively limit fault currents, it has caused the controlling process to be very complicated and limited the duty ratio of the booting factor.

In comparison to the proposed inverter, the switched-capacitor based inverter experience higher energy loss and suffer from EMI and inrush current due to not using the charging inductors. Also compared to two-stage converters, the proposed inverter has a very simple structure and controlling strategy. Especially compare to the topology suggested in [25], the proposed inverter uses very smaller inductor and the switches with lower switching stress.

TABLE II.
COMPARISON OF THE CONSIDERED COMMON THREE-LEVEL TOPOLOGIES

Topology / Parameters	H5 [13]	HERIC [14]	Virtual -dc-bus [16]	Flying-capacitor [18]	NPC [19]	T-type-NPC [20]	Proposed inverter
Number of switches	5	6	5	4	4	4	4
Number of diodes	-	-	-	0	2	-	2
Number of capacitors	1	1	2	3	2	2	4
Total voltage stress of the switches (×*Vp*)	4.5	5	5	4	4	6	4
Highest voltage stress of capacitors (×*Vp*)	1	1	1	1	1	1	0.5
Voltage gain	1	1	1	0.5	0.5	0.5	1
Three-phase possibility	No	No	No	Yes	Yes	Yes	Yes
Common-mode-voltage	V_{dc}	V_{dc}	0	$\frac{I_m \cos(\omega t)}{2C\omega}$	$\frac{I_m \cos(\omega t)}{2C\omega}$	$\frac{I_m \cos(\omega t)}{2C\omega}$	$\frac{I_m \cos(\omega t)}{2C\omega}$

VI. PERFORMANCE IN GRID-TIED PV SYSTEMS

In order to assess the performance of the proposed inverter in PV system, it is used as an interface inverter to deliver the power produced by a PV array to the grid. To do so, Proportional-Integral (PI) controllers are used like shown in Fig. 9. The characteristics of the considered system are listed in Table III. In this system, the observe and perturb maximum power point tracking algorithm is used to generate active power reference, the reactive power reference is assumed zero.

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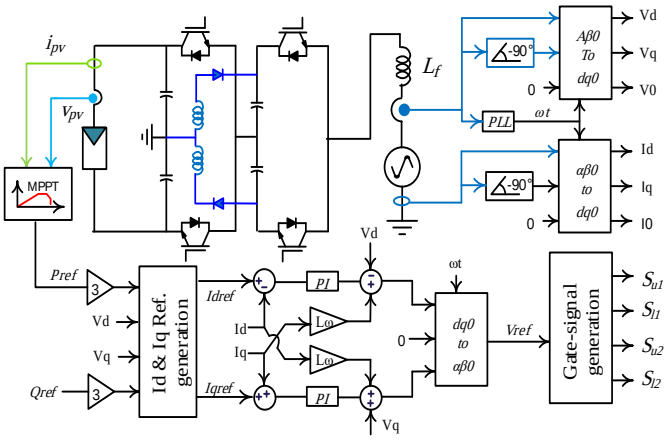

Fig. 9. Control schematics of the grid-connected PV system.

TABLE III.
CHARACTERISTICS OF THE SIMULATION MODEL

Parameters		*Values*
Terminal voltage of PV unit (V_{dc})		*425 V*
Base voltage (Peak)		*320 V*
Grid Voltage (peak)		*320 V*
Grid Frequency (f)		*50 Hz*
Grid-side filter (L_l)		*3.18 mH*
Charging Inductors (L_u , L_l)		*4 μH*
Base Apparent Power (single-phase)		*3 kVA*
Base Apparent Power (three-phase)		*14.4 kVA*
C_{u1}, C_{l1} ,C_{u2}, C_{l2}		*2200 μF*
Cpv (parasitic capacitance of PV), C_f		*800 nF, 4.6 μF*
Switching Frequency	*Su_1, S_{l1}*	*24 kHz*
	Su_2, S_{l2}	*50 Hz*
Kp, Ki (PI coefficients) (dc-link controller)		*15, 65*
Kp, Ki (PI coefficients) (grid-side controller)		*0.15, 6.6*

In order to investigate the performance of the proposed topology under different loading conditions, various irradiations are taken into account. Possible active power values for the assumed irradiations are exhibited in Fig. 10.

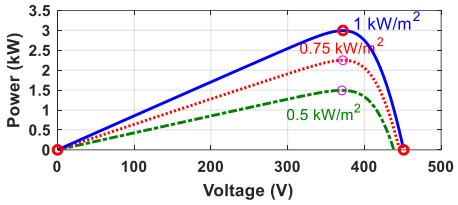

Fig. 10. Irradiances and related active power curves.

The injected power to the grid along with the irradiance are shown in Fig. 11. As seen in these figure, and referring to Fig. 10, it is evident that the injected power to the grid is according to the produced power of the PV module at the maximum power point and related irradiance.

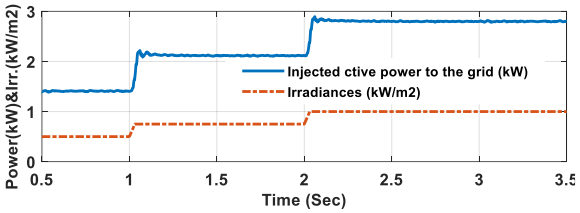

Fig. 11. Injected power to the grid under different irradiances.

Under the assumed conditions the voltages across the capacitors are shown in Fig. 12. As seen in this figure the voltage across the capacitors are half of the output voltage which can reduce the size and cost of the capacitors. Furthermore, as seen in these figures, the voltage ripple across switched-capacitors (C_{u2}, and C_{l2}) is insignificant because these capacitors reside in the charging mode in every switching cycle and experience a short discharging duration.

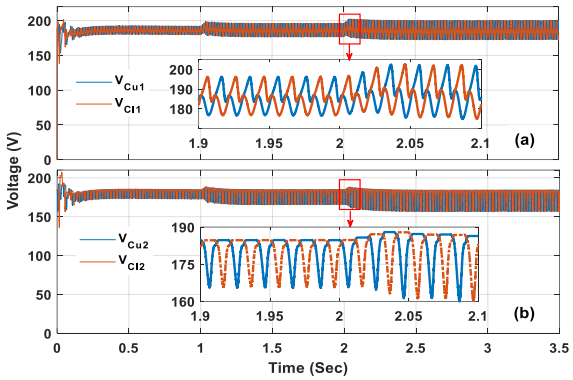

Fig. 12. Capacitor voltages (a) across C_{u1}, C_{l1}, and (b) across C_{u2}, C_{l2}.

The reference, mean and instantaneous values of the voltage of the dc link (voltage at the output terminals of the PV module), are exhibited in Fig. 13. As seen in this figure, the voltage across the output terminals of the PV module is perfectly set to the reference value which is dictated by the MPPT system.

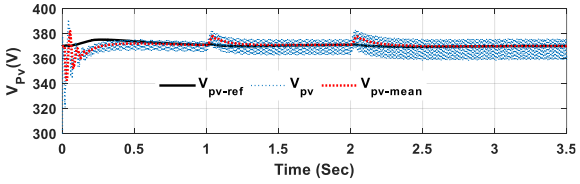

Fig. 13. Reference, mean and instantanious values of DC link voltage, under 25 C^o with different irradiances.

As mentioned earlier one of the most troublesome phenomenon in grid-tied PV system is the capacitive leakage current which appears due to the parasitic capacitor of the PV panels. The leakage current in the

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studied system is depicted in Fig. 14. As seen, the RMS value of the leakage current is lower than 1 mA, which is far below the value issued by VDE-AR-N-4105 standard. Thus, it is proved that the proposed inverter has deservedly mitigated the leakage current.

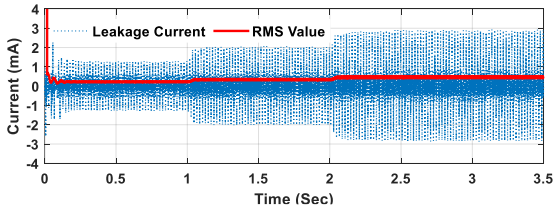

Fig.14. Leakage current from the parasitic capacitors of PV module.

Moreover, the output voltage of the inverter and that of the grid is exhibited in Fig. 15. This figure shows the three-level voltage that is developed through the proposed inverter.

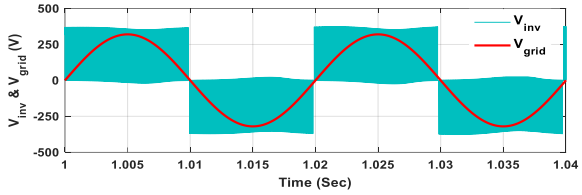

Fig. 15. Output voltage of inverter and grid-voltage.

The performance of the proposed inverter under harsh variation of the input voltage (which can happen under different temperature condition) is considered. by considering different temperatures which necessitates different voltage values on the output terminals of the PV module to track maximum power point, the performance of the proposed inverter is assessed. the maximum power point vs output voltage of the PV module for the assumed irradiance and temperatures is depicted in Fig. 16.

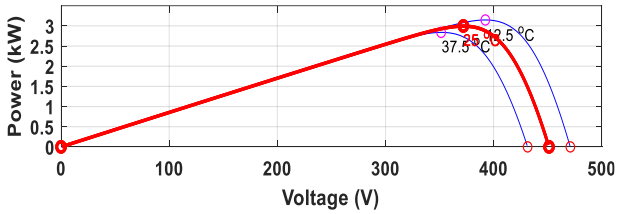

Fig. 16. Maximum power point under irradiance of 1000 W/m^2, and temperature of [12.5 25 37.5 25] ºC.

The voltage at the output terminal of PV module (input of the inverter) is shown in Fig.17, and the produced power, input current and the injected current are all exhibited in Fig.18. as seen in these figures, the MPPT system has succeeded to track the maximum power point by varying the terminal voltage of PV module. the input power with a continuous input current has been properly injected to the grid.

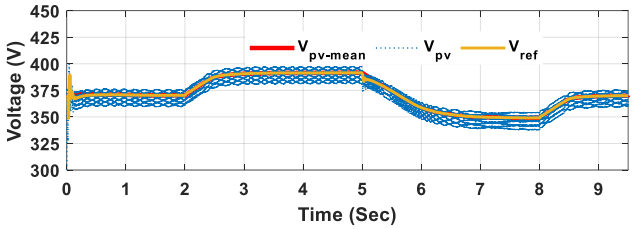

Fig. 17. Reference, mean and instantanious values of DC link voltage, under irradianc of 1000 W/m^2 and tempratures of [12.5 25 37.5 25] Cº.

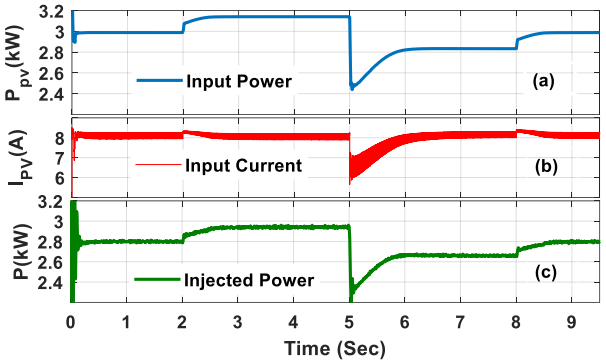

Fig. 18. Powers under dierrent temprature, (a) produced power by PV module, (b) input current, and (c) injected power to the grid.

VII. Experimental Results

In order to prove the feasibility of the proposed inverter, a lab-scale prototype was constructed and tested under different loading conditions. The prototype is shown in Fig. 19 and the utilized components are listed in table IV.

TABLE IV. COMPONENT CHARACTERISTICS.

Components	Type
Switches	IRFP450
Opto-coupler	TLP250
Microprocessor	DSP-F28335
Capacitors	3300 µF
Diodes	FFPF20UP40S
Output Filter	8 mH+20 µF

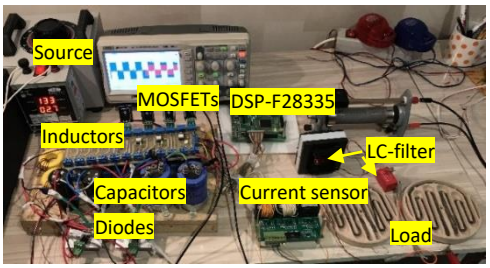

Fig. 19. Lab-scale prototype of the proposed inverter.

The three-level output voltage and its FFT analysis under no-load condition is shown are Fig. 20. As it is seen in this figure, the harmonics around the switching frequencies are dominant. As it is observable the magnitude of harmonics around the 25 kHz, 50 kHz,

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and 75 kHz (dominant harmonics) are 30 V, 15 V, and 10 V, respectively. With these values the THD of the output voltage is calculated to 15.5%.

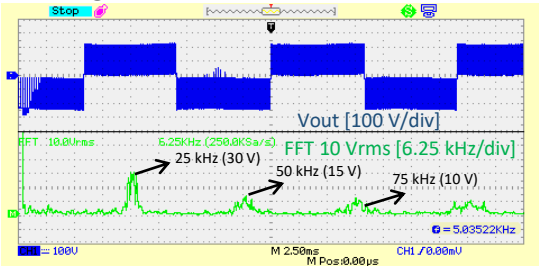


Fig. 20. Output voltage and its FFT analysis under no-load condition.

Further, the output voltage and load current under an inductive-resistive load of 30 Ω +15 mH is shown in Fig. 21.

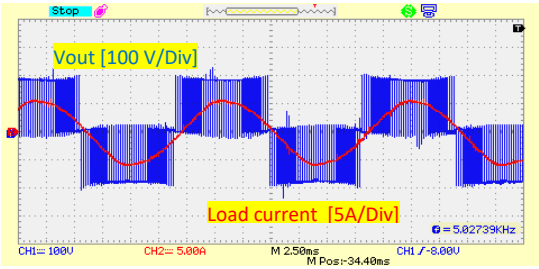
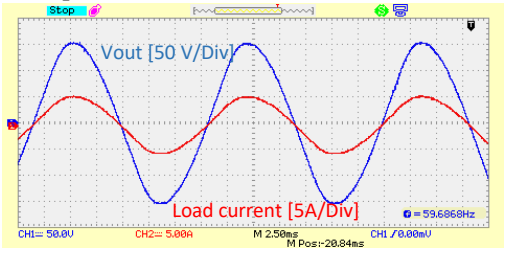
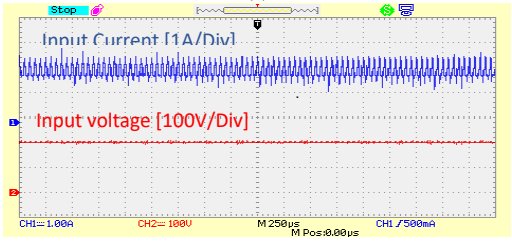


Fig. 21. Output voltage and load current under an inductive-resistive load.

Additionally, the performance of the proposed topology is tested in the presence of an LC filter and a pure load of 30 Ω. The result is shown in Fig. 22. As seen in this figure the, the load power is 375 W and the input power is 405 W. Thus, the efficiency for the mentioned power is 92.5%.



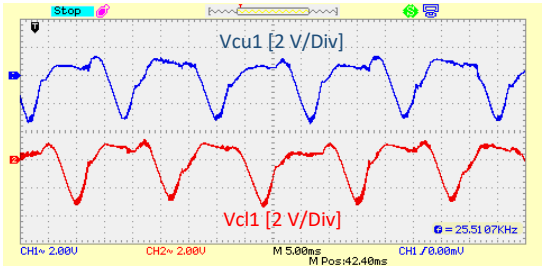
(a)



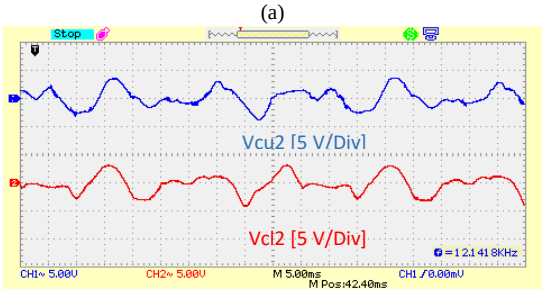
(b)

Fig. 22. Performance in the presence of an LC filter and pure resistive load, (a) output voltage and load current, and (b) input voltage and current.

One of the challenging issues in switched-capacitor-based converters is the inrush current that appears when charging the capacitors. This current has a direct relation with the voltage ripple across the capacitors. In order to investigate the inrush current, the voltage ripple (ac components) of the capacitors and charging current of the switched capacitors are investigated. Figs. 23 (a) and (b) show the voltage ripple in the input capacitors.



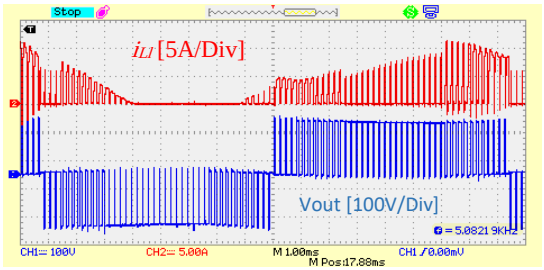
(a)



(b)

Fig. 23. Voltage ripple of the capacitors (ac components) (a) C_{u1} & C_{l1}, and (b) C_{u2} & C_{l2}.

Further, the charging current of the capacitors (charging inductor current) along with the output voltage is depicted in Fig. 24 (a). By referring to Figs. 23 and 24, whereas the proposed inverter has a short discharging duration, the inrush current in this inverter is limited. For more clarity, the charging current and voltage across the charging inductor during one switching cycle are exhibited in Fig. 24(b). this figure proves the analysis provided for Fig. (5).



(a)

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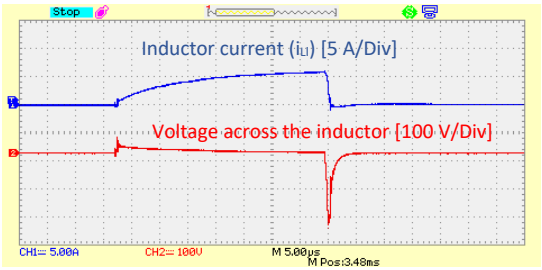
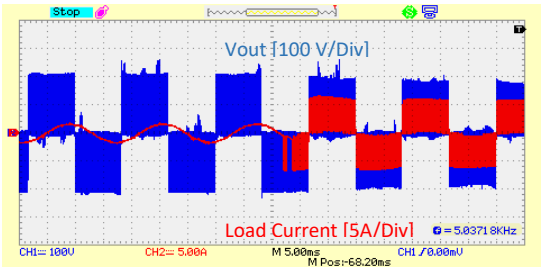


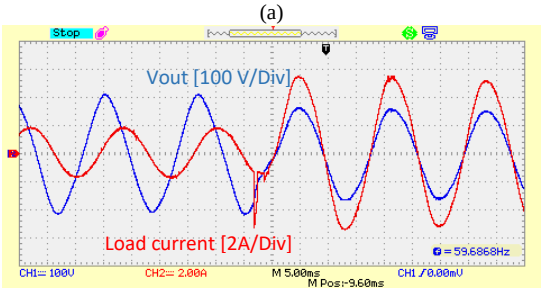
(b)

Fig. 24. Charging current and output voltage, (a) charging current (i_{Ll}) of one of the capacitors and output voltage during a cycle of line frequency, and (b) charging current and voltage of one of the inductors during a switching cycle.

It is worth mentioning that using small inductors along the charging current path not only reduces the inrush current and its effect on power loss, but also they provide zero current switching condition for the diodes resulting in eliminating the switching losses in these devices. Furthermore, the performance of the proposed inverter under the condition of a dynamic load change is exhibited in Fig. 25. As seen in this figure, the proposed inverter can easily response any dynamic load change.



(a)



(b)

Fig. 25. Dynamic performance of the proposed inverter.

As a PV inverter, the proposed inverter should be able to reduce the leakage current which stems from the parasitic capacitors. In order to assess this capability, an impedance of 300 nF + 2 Ω was connected between the mid pint and negative polarity of the input dc source. The current passing through this impedance is shown in Fig. 26. As it is evident, the leakage current is under 25 mA.

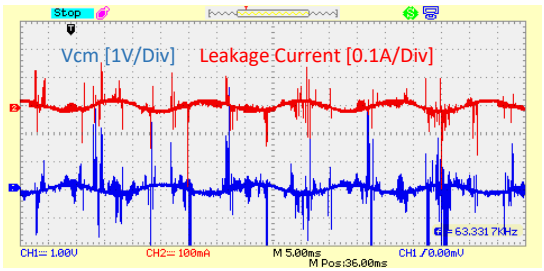


Fig. 26. Leakage current and common-mode voltage curve.

VIII. CONCLUSION

A new three-level inverter with the ability to reduce voltage stress of components, leakage current reduction capability and possibility to configure as a three-phase inverter was proposed. The proposed inverter was constructed by using four switches, two diodes, four low voltage capacitors and two small inductors. In the proposed inverter topology, the common-mode voltage varies with the grid-frequency, and parasitic capacitors of PV panels are in parallel with the input capacitors, so the leakage current in grid-tied PV applications of the proposed inverter will be mitigated. The tiny inductors, which are placed in the charging current path of the switched-capacitors provide zero current switching for the diodes leading in reduction in switching losses. By taking into account the above mentioned feature, the proposed inverter was compared with the state-of-the-art three-level inverters in PV applications. For compactness, only the features of the proposed inverter were investigated in a grid-tied PV system, however this inverter can address many problems in other industrial applications like motor drives. In order to prove the feasibility of the proposed inverter, a lab-scale prototype it was tested under different loading conditions.

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