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Stability Enhancement of Battery-Testing DC Microgrid: An ADRC Based Virtual Inertia Control Approach

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***Abstract*—Power batteries play a vital role in electric vehicle (EV) industry. To evaluate their charging and discharging performance and achieve energy recovery, a power accumulator battery testing system (PABTS) based DC-microgrid (DC-MG) is proposed. However, during battery testing, frequent charging and discharging current test may endanger the stability of the PABTS DC-MG. Although, the traditional virtual inertia control (VIC) approach can stabilize the DC-bus voltage, its anti-interference ability is still limited. To solve this problem, an active disturbance rejection control (ADRC) based VIC control scheme is proposed, wherein the VIC approach provides virtual inertia for the system, and the ADRC is derived and modeled using the first-order virtual inertia equation. The external and uncertain internal disturbances in the system are considered for the total disturbance estimation. This disturbance is suppressed by feedback compensation, thereby greatly improving the system robustness. Finally, the effectiveness of the proposed ADRC-VIC method is further verified by experimental results on the laboratory hardware prototype under different scenarios.**

***Index Terms*—Active disturbance rejection control (ADRC), battery testing system (BTS), DC-microgrid (DC-MG), power accumulator battery testing system (PABTS), virtual inertia control (VIC).**

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NOMENCLATURE

P_{out}	Output power of BGCC.
P_{in}	Injected dc-bus power.
C_{vir}	Virtual capacitor.
u_{vir}^{*}	Virtual reference for dc-bus voltage.
C_{dc}	dc-link capacitance.
u_0	Rated dc-bus voltage.
i_0	Output current of BGCC.
i_{dc}^{ref}	Virtual dc-link current reference.
ΔP	Power fluctuation at DC-bus.
D_b	Damping coefficient.
k_d	Droop coefficient.
u_{dc}	dc-link voltage.
$i_{a,b,c}$	Three-phase grid current in *abc*-frame.
$v_{a,b,c}$	Three-phase grid voltage in *abc*-frame.
i_{dq}, u_{dq}	Grid voltage and current under *dq*-frame.
Δi	Virtual capacitor current.
P_{ref}	Active power reference of virtual synchronous machine (VSM).
P_e	Electromagnetic power of VSM.
D_p	Damping coefficient of VSM
ω	Angular frequency of the VSM
ω_n	Rated angular frequency of the utility grid.
J	Virtual moment of inertia.

I. Introduction

OWING to the energy crisis and environmental problems caused by the extensive use of conventional fuel vehicles, electric vehicles have become increasingly popular in recent years and have been developed rapidly [1]. Batteries are the key factor affecting the dynamic performance of electric vehicles, which include maximum speed, acceleration, and climbing ability. For now, battery test system is the only way to measure the battery parameters (e.g., voltage, current, internal resistance, state-of-charge (SOC), etc.). Traditional battery test system wastes the energy during the test process through dissipative resistance. To save the test energy, considering that DC-MG is a low-cost and efficient integrated microgrid [2, 3] for renewable energy sources, energy storage systems, and DC loads [4-6], a power accumulator battery testing system (PABTS) based DC-MG is proposed (as shown in Fig.1), where the charging and discharging test control of the

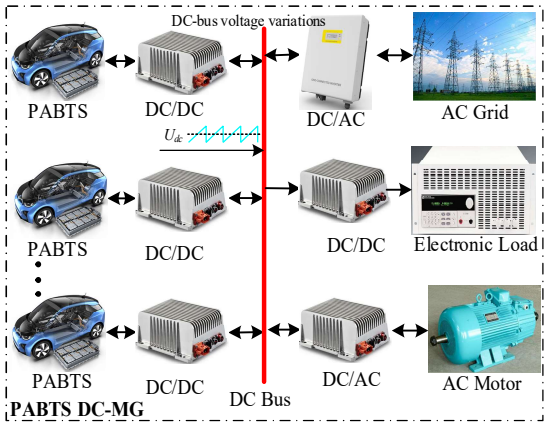


Fig.1. Configuration of the energy recovery PABTS DC-MG.

battery is achieved through the bidirectional DC/DC converter, and the DC/DC converter obtains and releases the battery energy through the DC-bus. The bidirectional grid-connected converter (BGCC) is the interface of the DC-bus and ac grid. However, due to the absence of energy storing devices, DC-MG composed by power electronic devices lacks inertia support similar to a mechanical rotor [7, 8]. Additionally, the battery test system itself is an interference for the PABTS DC-MG when continuously charge and discharge tests of the batteries are performed. Thus, for PABTS DC-MG, maintaining the stability of DC-bus voltage under disturbances is challenging.

The existing techniques for stabilization of DC-bus voltage can be categorized by two methods: (1) Droop control and (2) Inertial control.

Droop control has been widely used in microgrids [9-11]. Its primary functions include realization of power sharing between AC-DC microgrids, and between energy storage units [12, 13]. In addition, hierarchical control and droop control in DC-MG are the most basic control methods [14, 15], which standardize the operation of microgrid and improves the performance of microgrid. An observer was applied to the droop control to overcome the limitations of the traditional droop control. This also improved the current sharing accuracy and regulation of the output voltage [11]. It is difficult to balance the voltage regulation accuracy and current sharing accuracy of parallel DC/DC converters in the DC-MG. In [16], a communication free coordinated droop control energy management method was proposed to improve system reliability. In [17], to compensate the voltage deviation in dc-bus due to the droop-control, a distributed secondary control scheme was presented for both current sharing and voltage restoration. A key part of [17] was the integration of a new parameter 'virtual voltage-drop' defined from droop gain and line resistance. However, PABTS DC-MG is different from traditional DC-MG. The charge and discharge test control of battery pack is realized by bidirectional DC/DC converter. The specification of the control parameter varies according to the test requirements. Since each battery pack is tested independently, there is no correlation between each DC/DC converter and no current sharing control. Therefore, droop control may not be suitable for DC/DC converter in PABTS.

Beside droop control, inertia control is also applied for dc-bus voltage stabilization of DC-MG, which usually has two methods, one is adding an energy storage system (ESS) [16, 18-20]. Nowadays, the use of energy storage units to compensate for the inertia of the distributed intermittent renewable energy microgrid has been widely discussed. In [18], N. Zhi, K. Ding, *et al*. proposed a virtual DC motor control of a distributed battery energy storage system to regulate the fluctuation of the DC-bus voltage. To quickly restore the DC-side voltage and achieve power sharing, in [19], hybrid energy storage (e.g. power battery combined with supercapacitor) was also used in to provide inertia support. The static operation of a power electronic converter has no physical inertia, similar to that of a mechanical rotor. The virtual synchronous machine proposed by simulating the rotor equation has been widely used in photovoltaic and wind power generation systems [4, 21]. For example, in [4], a virtual synchronous generator (VSG) is applied as the interface of the energy storage component in wind-storage power generation system, where model predictive controller (MPC) timely changes the reference active power of the VSG according to the change in frequency, which further suppresses the fluctuation of the microgrid's voltage and its frequency. Nevertheless, supercapacitors and batteries only provide inertial support in the transient state of power disturbance and remain idle when the system is stable, resulting in wasted resources and increased costs.

In addition to inertia control with ESS, another technique is virtual inertia control (VIC) without any ESS. Analogy with the VSG rotor equation, a VIC suitable for DC-MG was derived to stabilize the DC-bus voltage on the bidirectional converter [21]. In [22], virtual capacitance was proposed to enhance the system inertia, and droop and damping control were added to analyze the small-signal model of the system, and the feedforward control is used to improve the system stability. On this basis, the stability of the DC-bus voltage was further enhanced by changing the virtual current reference in VIC [23]. Additionally, traditional VIC usually adopts proportional-integral (PI) control (PI-VIC). Owing to its slow time response, its dynamic disturbance cannot be rapidly attenuated, and its linear weighting is not the optimal combination [24, 25]. Generally speaking, PI-VIC is not robust to external interference. Furthermore, the DC-bus voltage fluctuation cannot be minimized. In addition to PI controller for VIC control, there have been some control strategies to obtain high-quality current, such as repetitive control (RC) [26], proportional-resonant (PR) control [27], and sliding-mode control (SMC) [28]. Although RC and PR control schemes can achieve infinite gain at the selected frequencies and achieve zero steady-state error, their robustness is still poor, and the inherent chattering problem in SMC cannot be fully eliminated. In summary, the above controllers are difficult to replace PI controller in PI-VIC to stabilize DC-bus voltage.

Active disturbance rejection control (ADRC), known as a robust control method, can estimate the generalized disturbance, integrate the unknown dynamics, and eliminate the disturbance through feedback compensation, which greatly improves the anti-interference ability of the system [29, 30]. In [31], an

ADRC controller was applied to a power electronic converter to estimate the total power demand and reduce the steady-state error of the output voltage. In [32], a robust voltage control method for a floating interleaving boost converter with a high voltage gain, was proposed. The reference current was obtained by the ADRC controller in the outer loop, whereas the inner loop adopted the super-twisting sliding-mode control (ST-SMC), which greatly improved the voltage tracking and anti-interference ability of the boost converter. Motivated by the advantages of ADRC control, it is a good idea to replace the PI controller in PI-VIC with ADRC controller to stabilize the DC-bus voltage under large and unknown disturbances.

Considering the stability problem of the PABTS DC-MG due to the low inertia of power electronic devices and the severe challenges caused by frequent charge and discharge test interferences, a method combining the merits of VIC and ADRC, named ADRC-VIC, is proposed for BGCC converter to enhance the system inertia and improve the anti-interference ability. In the proposed ADRC-VIC control, VIC is used for inertia support, and ADRC is served as the outer loop controller for disturbance rejection. In ADRC-VIC, the neglected system dynamics, uncertainties, and non-repetitive factors caused by non-repetitive disturbances, are defined as a part of the total disturbance to be estimated and compensated. These disturbances are eliminated by feedback compensation, thereby, the anti-interference ability is improved. In summary, the main contributions of this paper are as follows:

1) The ADRC controller in the inner loop of ADRC-VIC control is designed according to the virtual inertia equation. The external disturbances (e.g., changes in the grid voltage and load changes) and internal parameter perturbations are regarded as the total estimated disturbance, which are suppressed by feedback compensation of the inner loop ADRC controller. This significantly improves the anti-interference ability of the system.
2) The ADRC-VIC on the outer loop is proposed, and the inertia enhancement and robustness improvement of the PABTS DC-MG are realized. This provides a new solution for dc-bus voltage stabilization under frequent charge and discharge tests of the battery test systems.

The remainder of this paper is organized as follows. Section II describes the PABTS DC-MG and its existing problems. To achieve strong robustness against uncertainties and unknown disturbances, an ADRC-VIC scheme is proposed. Section III introduces the concept of VIC and the virtual capacitor configuration for inertia support of a DC-MG. Section IV describes the design of the ADRC controller for internal and external disturbances that may exist in PABTS DC-MG, which greatly enhance the system robustness. In Section V, stability of the system is analyzed. In Section VI, the effectiveness of the proposed method is compared with other techniques by experimental results. Finally, Section VII concludes this article with a future scope of work.

II. System Description

A. Problem Description

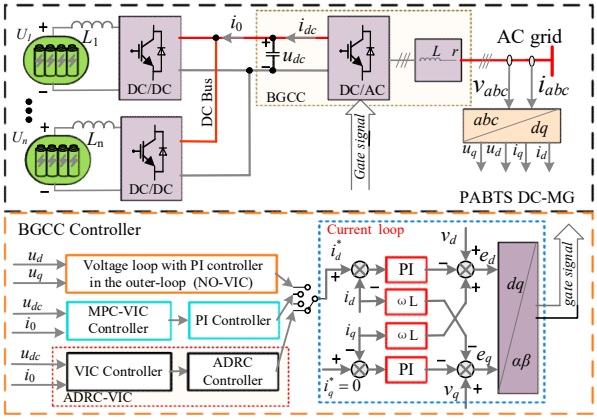


Fig.2. Control block diagram of the BGCC for PABTS DC-MG.

In this paper, we primarily study the control strategy of the bidirectional converter in the PABTS DC-MG used to suppress the DC-bus voltage fluctuations under different interferences. The power module in Fig.2 is a simplified model of the PABTS DC-MG. U_1 to U_n represent different battery test units, and L_1 to L_n represent the boost inductors. The battery pack is charged and discharged through a bidirectional DC/DC converter, and each DC/DC converter is connected to a DC-bus. Then, it is connected to the grid through a bidirectional grid-connected converter (BGCC). C_{dc} represents the DC bus capacitance, u_{dc} is its terminal voltage, i_0 is the DC-link output current, i_{dc} is the DC-link input current, r is the parasitic resistance of the inductor L, i_{abc} is the grid current, and v_{abc} is the grid voltage. u_d and u_q are the voltage components of v_{abc} under dq-frame, respectively. i_d and i_q are the current components of i_{abc} under dq-frame, respectively, after the Clark and Park transformation. i_d^* and i_q^* are the current references of i_d and i_q, respectively. If the BGCC operates with a unit power factor, namely, $i_q = 0$, $u_q = 0$.

To stabilize the DC-bus voltage, inertia support as well as strong robustness are required. Fig.2 shows three different control schemes for the PABTS DC-MG. These are voltage and current double PI loop controls, namely, inertia-free control (NO-VIC). The MPC-VIC of inertia is increased by compensating for the reference current in the virtual inertia control through the MPC and the ADRC-VIC proposed in this paper. To analyze the suppression effect of the first two schemes on the DC-bus voltage fluctuation in the PABTS DC-MG, the experimental results in [23] were analyzed.

Fig.3 shows the DC-bus voltage fluctuation transient diagrams with different control strategies under charging conditions, in which A-VIC represents adaptive virtual inertia control. When t = 0.16 s, a charging test is performed. The voltage drop is caused by the decrease in power at the DC-bus, and the voltage drop reaches 14 V without inertia support. Evidently, this fluctuation result is large, and NO-VIC strategy is not suitable for the PABTS DC-MG. The A-VIC can automatically release the inertia in the virtual capacitor to maintain the voltage balance, based on the voltage fluctuation. Hence, the voltage drop is reduced to 10 V.

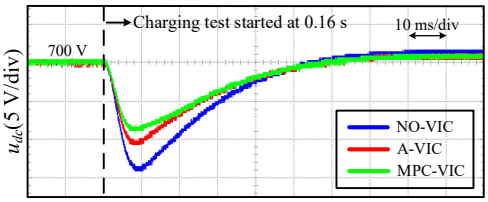


Fig.3. Response of the DC-bus voltage with different strategies.

In addition to A-VIC, the MPC-VIC calculates the optimal compensation in real time along with the change in the external environment, and superposes the system inertia to the virtual reference current to reduce the voltage fluctuation to 8 V. Although the MPC-VIC method can predict and compensate for the DC-bus current to suppress the DC-bus voltage fluctuation, frequent charge and discharge will still have some impact on the PABTS. Therefore, minimizing the system interference is challenging. This will be elaborated in the subsequent sections.

B. Proposed Control Scheme

The traditional VIC method includes a virtual inertia link and a current inner loop control. Both the outer-loop controller and inner-loop controller adopt the PI controller, but the PI controller has inherent limitations. For example, it is difficult to select appropriate parameters, and the inherent contradiction between rapid response and overshoot is difficult to overcome. In this paper, a controller that can reduce external interference and avoid excessive fluctuation of the DC-bus voltage is designed to suppress the disturbance in the DC-bus voltage. It also improves the robustness of the PABTS DC-MG.

Fig.4 shows a simplified schematic diagram of the PABTS DC-MG with the ADRC-VIC strategy, including the power supply and control strategy parts. The outer loop of the control strategy adopts VIC to enhance the inertia of the system, and the inner loop is the current control. Because the current reference of the inner loop comes from the outer loop, the external interference is primarily introduced into the control system through the sampled voltage and current. However, the traditional PI-VIC method, which adopts proportional-integral (PI) controller for outer-loop voltage control and VIC controller in the inner-loop for inertia support, cannot eliminate the interferences [21, 22]. Different with the traditional PI-VIC, Fig.4 shows the derivation of the external loop controller (ADRC) based on VIC method, which replaces the traditional PI controller to eliminate the interference and suppress the DC-bus voltage fluctuation.

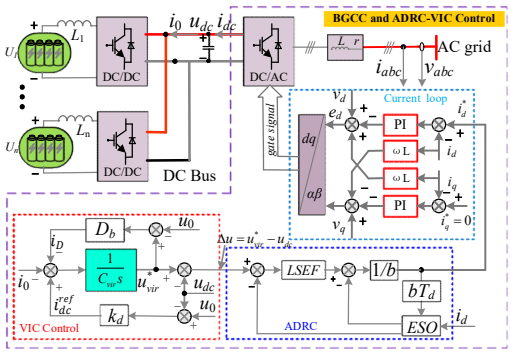


Fig.4. Block diagram of the proposed ADRC-VIC method.

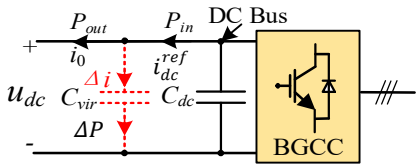


Fig.5. Virtual capacitor configuration.

Mechanical equation of the VSM

$$P_{set}-P_e-D_p\left(\omega-\omega_n\right)=J\omega\frac{d\omega}{dt}\approx J\omega_n\frac{d\omega}{dt}$$

Analogy

Virtual inertia equation of the BGC

$$i_{dc}^{ref}-i_o-D_b\left(u_{vir}^*-u_0\right)=C_{vir}u_{vir}^*\frac{du_{vir}^*}{dt}\approx C_v u_0\frac{du_{vir}^*}{dt}$$

Fig.6. Virtual inertia equation of the BGCC via analogizing with the VSM.

For the proposed ADRC-VIC control scheme in Fig.4, a detailed design and explanation of the VIC controller in the outer-loop and ADRC controller in the inner-loop will be given in Section III and IV, respectively.

III. VIC Control of BGCC

In the DC microgrid shown in Fig. 1, there is no rotating rotor or special energy storage system to provide additional transient compensation power. The AC grid can improve the inertia support for the DC grid, which is realized by implementing a VIC strategy on the bidirectional converter. Under different control strategies, the relationship between the output power of the inverter and the power injected into the DC-bus can be expressed as:

$$P_{out}-P_{in}=\Delta P \tag{1}$$

where ΔP is the power fluctuation at the DC-bus. When the microgrid is stable, $P_{out}=P_{in}$, that is, $\Delta P=0$. When the PABTS performs charge and discharge tests and load switching occurs in the DC-MG, changes in P_{out} and P_{in} lead to an increase in the power fluctuation ΔP. This unbalanced power fluctuation leads to an increase or decrease in the DC-bus voltage. Excessive power fluctuations greatly threaten the stable operation of the DC-MG. The DC bus capacitor C_{dc} will release or absorb power according to the DC-bus voltage fluctuation; however, the suppression effect is limited by the actual capacity. If the additional power is absorbed by a virtual capacitor C_{vir} (see Fig. 5), (1) can be changed to:

$$P_{out}-P_{in}=\Delta P=C_{vir}u_{vir}^*\frac{du_{vir}^*}{dt} \tag{2}$$

where u_{vir}^* is the virtual reference for the DC-bus voltage. Equation (2) shows that the DC-bus power change ΔP, which is interfered with by external power, is finally absorbed or released by the DC-link virtual capacitance, thereby stabilizing the DC-bus voltage.

Additionally, as shown in Fig. 5, the virtual capacitor current Δi_0 can be derived by the virtual DC-link current reference i_{dc}^{ref} and the output current i_0 is calculated by:

$$\Delta i_0=C_{vir}\frac{du_{vir}^*}{dt}=i_{dc}^{ref}-i_0 \tag{3}$$

To achieve power sharing, droop control is usually introduced in the virtual reference current i_{dc}^{ref} as the primary voltage regulator, where $i_{dc}^{ref} = k_d(u_0 - u_{dc})$, and damping is introduced in the output current i_0 to prevent power oscillation, where $i_0 = D_b(u_{vir}^* - u_0)$.

Thus, by analogizing the virtual inertia equation of the BGCC with the virtual synchronous machine (as shown in Fig.6) in AC-MG, the virtual inertial control equation can be written as:

$$C_{vir}\frac{du_{vir}^*}{dt} = k_d(u_0 - u_{dc}) - i_0 - D_b(u_{vir}^* - u_0) \tag{4}$$

where k_d represents droop coefficient, u_0 is rated DC voltage, D_b is damping coefficient. Under the traditional droop control, the output current i_0 is solely influenced by the equivalent resistance $1/k_d$ of the droop loop. The output current in virtual inertia control is jointly determined by $1/k_d$, C_{vir} and D_b.

IV. Design of ADRC Controller for BGCC

The design of ADRC controller in Fig.4 contains the expanded-state-observer (ESO) and the linear-state-error-feedback (LSEF), which are explained as follows.

A. Block Diagram of the ADRC Controller

Fig. 7 shows the typical structure of an ADRC controller. In traditional current controllers, for any dq -axis signal, the extraction of the differential signal and tracking of the reference signal can be realized. However, for the first-order ADRC controller, there is only one input signal. Thus, the differential of the input signal is not required. In addition, the input signal of ADRC controller in this paper is the dc-link voltage variation Δu ($\Delta u = u_{vir} - u_{dc}$) of virtual reference voltage and sampling voltage, and the expected Δu is 0. In view of this special situation, the tracking differentiator (TD) in the first-order ADRC can be omitted. The state variable x and disturbance f are estimated by the ESO through the output $u(t)$ of ADRC controller and sampled grid current i_d. Then, the state error feedback compensation control is carried out with LSEF. Finally, the reference current i_d^* for the inner-loop current controller is obtained. The results show improvement in the anti-interference capability of the system and enhancement of the system robustness.

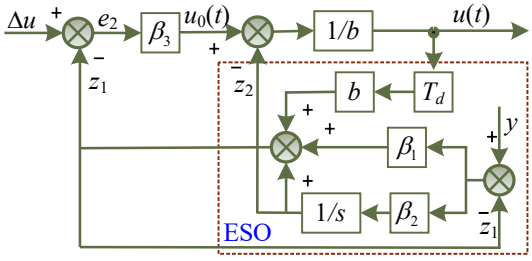


Fig.7. Block diagram of ADRC controller.

B. Expanded State Observer (ESO)

As the core component of linear active disturbance rejection control technology, a linear extended state observer (LESO) can not only estimate the state variables of the system in real time, but also accurately observe the total disturbance of the system. Therefore, the proposed extended state observer reduces the system model requirements, especially for difficulties in establishing an accurate mathematical model of the controlled system, further amplifying its advantages.

For the bidirectional converter, when ignoring the energy loss of the bridge arm and the loss of the parasitic resistance of the inductance and capacitance, the power balance on both sides of the BGCC can be obtained by:

$$\frac{3}{2}(u_d i_d + u_q i_q) = u_{dc} i_{dc} = u_{dc}(C_{dc}\frac{du_{dc}}{dt} + i_0) \tag{5}$$

For a three-phase symmetrical AC power supply, $u_q = 0$. To realize the unity power factor control of the three-phase voltage converter, it is necessary to set $i_{qref} = 0$. Thus, (5) can be written as:

$$1.5u_d i_d = u_{dc} i_0 + u_{dc} C_{dc}\frac{du_{dc}}{dt} \tag{6}$$

Combining (6) and (4) yields:

$$\frac{du_{vir}^*}{dt} = \frac{1}{C_{vir}}\left(\left(k_d + D_b\right)u_0 - k_d u_{dc} + C_{dc}\frac{du_{dc}}{dt} - D_b u_{vir}^* - 1.5\frac{u_d i_d}{u_{dc}}\right) \tag{7}$$

Taking $x = u_{vir}^*$, the dynamic voltage state equation can be obtained from (7) as:

$$\begin{cases} \dot{x}(t) = f(x, u_{dc}(t)) + bu(t) \\ y(t) = x(t) \end{cases} \tag{8}$$

where

$f\left(x, u_{dc}(t)\right) = \frac{k_d}{C_{vir}}(u_0 - u_{dc}) + \frac{C_{dc}}{C_{vir}}\frac{du_{dc}}{d_t} - \frac{D_b}{C_{vir}}u_{vir}^* + \frac{D_b}{C_{vir}}u_0$, $u(t) = i_d$, and $b = -\frac{3u_d}{2C_{vir}u_{dc}}$.

The input of the system is set to $u(t)$, that is, the given value i_d^* of the current inner loop. The coefficient b is determined by the output voltage u_d of the DC-AC converter and the DC-bus voltage u_{dc}. In $f\left(x, u_{dc}(t)\right)$, u_0 is the rated DC-bus voltage and is a constant, and there is no interference with the system. The sampling DC-bus voltage u_{dc} changes with the interference of power fluctuation at the DC-bus in DC-MG, which can be generalized as a phenomenon reflecting the strength of external interference. The state variable u_{vir}^* is the final output result of the VIC link, which changes with the variations in the DC-bus voltage and current, and directly affects the input of the ADRC controller, thereby affecting the reference current i_d^* in the current loop. Therefore, $f\left(x, u_{dc}(t)\right)$ not only contains the disturbance of the external system, but also the perturbation of the parameters of its own control system that affect the output results of the system. Therefore, $f\left(x, u_{dc}(t)\right)$ is regarded as the sum of all system disturbances. The voltage response of (8) can be simplified using a first-order link.

The design of the first-order ADRC-VIC is based primarily on the nonlinear system of (8). To facilitate the understanding of the derivation process, we first assume that an accurate estimation of the total disturbance $f\left(x, u_{dc}(t)\right)$ of the system can be achieved, and the estimated value is z_2, which is given by:

$$z_2 = f(x,\ u_{dc}(t)) \tag{9}$$

An ESO is the core of the ADRC controller, and its advantage is its low model dependence. In addition to providing the observation values of each order state variable of the system, the ESO can also estimate and compensate for the total disturbance of the system in real time. It has the characteristics of an integral link, which can improve the steady-state accuracy of the system and avoid the stability problem caused by the integral link.

To estimate the total disturbance of the system, it is necessary to expand the state variables. The total disturbance $f(x, u_{dc}(t))$ in (8) is replaced by the expanded state quantity x_2, and we obtain:

$$\begin{cases} \dot{x}_1(t) = x_2(t) + bu(t) \\ \dot{x}_2(t) = G(t) \\ y(t) = x_1(t) \end{cases} \tag{10}$$

where $x_1 = u^*_{vir}$, $x_2 = f(x, u_{dc}(t))$ are expansion variables, and $G(t)$ is an unknown function. Real-time observation of state variables can be achieved through the ESO. Rewrite (10) into a state-space form:

$$\begin{cases} \dot{x}(t) = Ax(t) + Bu(t) + EG(t) \\ y(t) = Cx(t) \end{cases} \tag{11}$$

where

$$A = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}, B = \begin{bmatrix} b \\ 0 \end{bmatrix}, E = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, C = \begin{bmatrix} 1 & 0 \end{bmatrix}.$$

The specific algorithm given is:

$$\begin{cases} e_1 = z_1 - y \\ \dot{z}_1 = z_2 - \beta_1 fal_1 + bu(t) \\ \dot{z}_2 = -\beta_2 fal_1 \end{cases} \tag{12}$$

where z_1 and z_2 are the observation results of x_1 and $f(x, u_{dc}(t))$, respectively. e_1 represents the tracking error, and β_1 and β_2 are the controller parameters.

The nonlinear functions are $fal_x = fal(e_x, \alpha_x, \delta)$ and $x = 1, 2$. The expression for $fal(e, \alpha, \delta)$ is as follows:

$$fal(e,\alpha,\delta) = \begin{cases} \dfrac{e}{\delta^{1-\alpha}}, & |e| \le \delta \\ |e|^{\alpha}\, sign(e), & |e| > \delta > 0 \end{cases} \tag{13}$$

where δ and α are constants; $sign(e)$ is the sign function.

When $\alpha = 1$, $fal(e, \alpha, \delta) = e_1$. Considering that it is easier to implement control strategies and adjust parameters in industry, e_1 can be used instead of fal_1 in practical engineering to meet the control effect, thus simplifying (12) to

$$\begin{cases} e_1 = z_1 - y \\ \dot{z}_1 = z_2 - \beta_1 e_1 + bu(t) \\ \dot{z}_2 = -\beta_2 e_1 \end{cases} \tag{14}$$

Equation (14) is the realization of the linear extended observer of the system, and it is rewritten as the state space expression to obtain

$$\begin{cases} \dot{z}(t) = Az(t) + Bu(t) + L(y(t) - \hat{y}(t)) \\ \hat{y}(t) = Cz(t) \end{cases} \tag{15}$$

where $\boldsymbol{L} = [\beta_1 \quad \beta_2]^T$ is the observer gain vector.

When the communication time-delay exists in the control system, the output of the system can be considered as a signal that has lagged, as shown in Fig. 8. To solve this problem, the control signal can also be delayed when it reaches the extended state observer [33], so that the control signal and the system input signal can be resynchronized into the extended state observer, this can accurately estimate the delayed system state and disturbance.

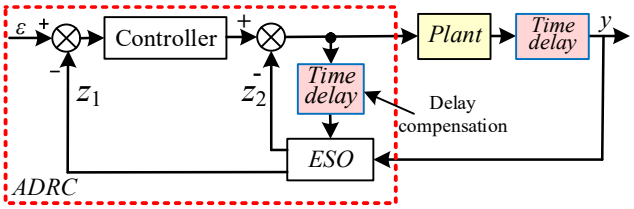


Fig. 8. ADRC controller with delay compensation.

Therefore, the state equation of ESO considering time-delay T_{d} should be

$$\begin{cases} \dot{z}(t) = Az(t) + Bu(t - T_d) + L(y(t) - \hat{y}(t)) \\ \hat{y}(t) = Cz(t) \end{cases} \tag{16}$$

Where T_d denotes the one period delay. Compared with conventional ADRC controller, the ESO considering time-delay can effectively improve the bandwidth of the system observer, and can calculate the total disturbance of the system in a wider frequency range [34], thus improving the accuracy of error estimation and the anti-interference capability.

C. Linear State Error Feedback (LSEF)

Introducing the disturbance estimator z_2 as the compensation to the control system.

$$u(t) = (u_0(t) - z_2)/b \tag{17}$$

Formula (17) is introduced into (8). Since z_2 is the total disturbance estimator $f(x, u_{dc}(t))$ of the system, when the total disturbance estimation value is close to its real value, $z_2 \approx f(x, u_{dc}(t))$, then $\dot{y} \approx u_0(t)$ can be used to eliminate the error.

$$\dot{y} = f(x, u_{dc}(t)) + u_0(t) - z_2 \approx u_0(t) \tag{18}$$

The nonlinear state error feedback (NLSEF) rate refers to the nonlinear relationship between the input of the feedback system and the error of the state variable. The control objective of ADRC is to force the voltage fluctuation change $\Delta u = 0$, and the control law can be expressed as

$$\begin{cases} e_2 = \Delta u - z_1 \\ u_0(t) = \beta_3 fal_2 \\ u(t) = (u_0(t) - z_2)/b \end{cases} \tag{19}$$

where e_2 is the difference between the Δu and z_1, and β_3 is the controller parameter.

Similar to the design in ESO. Considering the realization of control algorithm in industry and the easy adjustment of parameters, we take $\alpha = 1$, namely $fal_2 = e_2$, so (19) can be expressed as the linear error feedback control.

$$\begin{cases} e_2 = \Delta u - z_1 \\ u_0(t) = \beta_3 e_2 \\ u(t) = (u_0(t) - z_2)/b \end{cases} \tag{20}$$

D. Parameter Tuning of ADRC Controller

The rationality of parameter setting of ESO and LSEF in ADRC controller directly affects the control effect. The parameters of each link are set separately through the separation principle. Parameters to be tuned include gain matrix $\boldsymbol{L} = [\beta_1 \quad \beta_2]^T$ in ESO, and β_3 in LSEF control.

The parameter tuning of the observer by pole assignment is one of the common methods [35]. The pole assignment of ESO expression (15) is carried out and its characteristic equation is obtained according to $(A - LC)$

$$D(s) = s^2 + \beta_1 s + \beta_2 \tag{21}$$

The stability condition of the observer is that the characteristic roots of (21) are located in the left-half-plane (LHP) of the s-domain. According to Routh criterion, stability is satisfied as long as $\beta_1 > 0$ and $\beta_2 > 0$ are true for (21). When the characteristic root is farther away from the virtual axis, the stability margin of the system is larger. In order to keep β_1 and β_2 away from the imaginary axis as far as possible, the root of the characteristic equation (21) should be equal, that is, $\beta_1^2 = 4\beta_2$. In addition, the characteristic root (pole) should be set at $-\omega_0$, and ω_0 is the bandwidth of the observer. Thereby, $\beta_1 = 2\omega_0$, $\beta_2 = \omega_0^2$.

Similarly, β_3 can be configured by the closed-loop transfer function poles of the feedback control system. In (20), the output of LSEF can be expressed as

$$u_0(t) = \beta_3(\Delta u(t) - z_1(t)) \tag{22}$$

Substituting (22) into (18), we can get

$$\dot{y} + \beta_3 y = \beta_3 \Delta u \tag{23}$$

From (23), the transfer function of the closed-loop control system after disturbance compensation can be derived as

$$G_{yu}(s) = \frac{y(s)}{\Delta u(s)} = \frac{\beta_3}{s + \beta_3} \tag{24}$$

The pole $-\beta_3$ of (24) should be set at $-\omega_c$, and ω_c is the control bandwidth. Therefore, $\beta_3 = \omega_c$. ω_c can be determined by choosing the controller bandwidth based on common experience [35], thus, $\omega_0 = (1/5 \sim 1/2)\omega_c$.

Through the above analysis, the appropriate initial bandwidth is preliminarily selected, and then further optimized in the experiment. The parameter tune results are shown in Table II.

V. Stability Analysis

ADRC controller as the most popular of disturbance suppression strategy, its capability to estimate the disturbances and state variables as well as its stability will directly affect the DC-bus voltage fluctuation suppression effect of the whole control system. Therefore, it is necessary to analyze the system stability with ADRC controller.

To facilitate the study of the system stability in s-domain, by simplifying (16), z_1 and z_2 can be derived as

$$z_1 = \frac{\beta_1 y + \beta_3 \Delta u}{s + \beta_1 + \beta_3} \tag{25}$$

$$z_2 = \frac{\beta_2 y s + \beta_2 \beta_3 (y - \Delta u)}{s(s + \beta_1 + \beta_3)} \tag{26}$$

Combining (17), (22), (25) and (26), the ADRC control law can be expressed as

$$u(s) = G_a(s) \cdot \Delta u(s) - G_b(s) \cdot y(s) \tag{27}$$

Where G_a and G_b are expressed as

$$G_a(s) = \frac{\beta_3(s^2 + \beta_1 s + \beta_2)}{bs(s + \beta_1 + \beta_3)} \tag{28}$$

$$G_b(s) = \frac{(\beta_1\beta_3 + \beta_2)s + \beta_2\beta_3}{bs(s + \beta_1 + \beta_3)} \tag{29}$$

After converting the dynamic voltage state equation (8) of the controller in s-domain, and substitute (27) into (8), the output of ADRC controller is obtained as

$$\begin{aligned} y(s) &= \frac{1}{s}(f(s) + bu(s)) \\ &= \frac{1}{s}(f(s) + b(G_a(s) \cdot \Delta u(s) - G_b(s) \cdot y(s))) \end{aligned} \tag{30}$$

where $f(s)$ is the total disturbances in s-domain, simplify (30) to obtain

$$\begin{aligned} y(s) &= \frac{(s + \beta_1 + \beta_3) \cdot s}{(s + \beta_3)(s^2 + \beta_1 s + \beta_2)} f(s) + \frac{\beta_3}{s + \beta_3} \Delta u(s) \\ &= G_{yf}(s) f(s) + G_{yu}(s) \Delta u(s) \end{aligned} \tag{31}$$

In (31), the output of ADRC controller is affected by the total disturbance $f(s)$ and the voltage error $\Delta u(s)$. Combined with the analysis in Section IV-D and (31), it is obvious that the system stability is closely related to the observer and control bandwidth, and the system stability can be improved by selecting the appropriate bandwidth.

When the influence of disturbance on the output is ignored, system (31) is simplified to (24), and its output only contains Δu. At this time, the control performance is only determined by ω_c, which is independent of ω_0. The Bode diagram of $G_{yu}(s)$ is plotted in Fig. 9, indicating that the increase of broadband ω_c not only reduces the phase-delay, but almost does not affect the high frequency characteristics, and the stability margin and tracking speed of the system are improved.

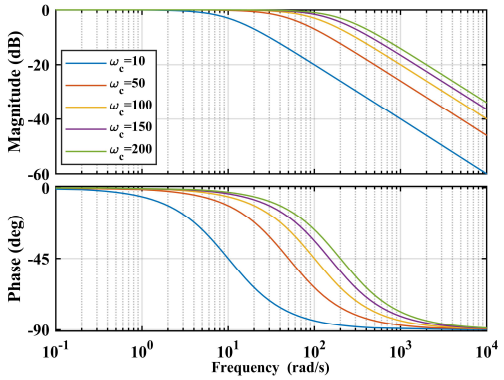


Fig. 9. Block diagram of $G_{yu}(s)$ by changing the control bandwidth ω_c.

When ignoring Δu and only considering the influence of total disturbance $f(s)$ on the system, the transfer function from y to f is $G_{yf}(s)$, and its Bode diagram is shown in Figs. 10 and 11. The system stability is jointly determined by the control bandwidth and the ESO bandwidth. Increasing ω_0 or ω_c can reduce the disturbance gain to enhance the anti-disturbance capability of the controller.

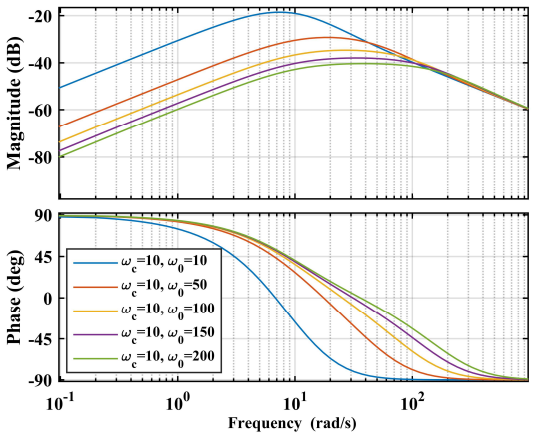


Fig. 10. Block diagram of $G_{yf}(s)$ by changing the observer bandwidth ω_0.

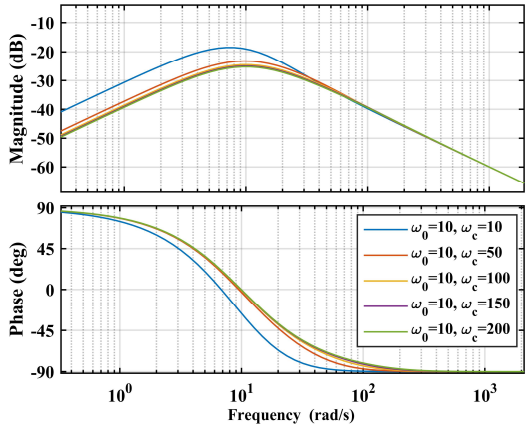


Fig. 11. Block diagram of $G_{yf}(s)$ by changing the control bandwidth ω_c.

VI. Experimental Results

A. Hardware Setup

To successfully demonstrate the effectiveness of the proposed ADRC-VIC for DC-link voltage stabilization, experimental verifications are carried out. The experiments are conducted in a laboratory PABTS DC-MG prototype shown in Fig.12. The DC-MG is constituted by a BGCC converter, two DC-DC converters for charging and discharging test control, two Lithium-Ion power battery packs for Tesla Motors (Model-S 85), and a programmable Chroma 63208 DC electronic load which is designed to test the DC power supplies, power electronic devices, automotive batteries, and components.

The experimental BGCC is composed by a 20-kW SiC-based two-level grid-connected converters. The control scheme in Fig.8 is implemented with a 32-bit float-point digital signal processor (DSP) TMS320F28377D from Texas Instruments, which is usually used for fast, complicated mathematics calculations and control algorithm implementation. All the SiC

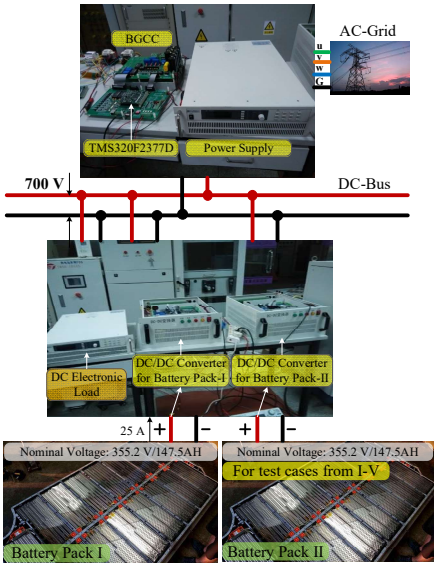


Fig. 12. Configuration of the PABTS DC-MG in experiment.

TABLE I
Parameter Specifications of the Power Battery in Tesla Model3S

Parameters	Value
Nominal voltage	355.2 V
Rated capacity (Ah)	147.5 Ah
Initial state-of-charge	50%

TABLE II
Parameter Specifications of the ADRC-VIC Controller

Parameters	Values	Parameters	Values
U_{dc}	700 V	k_d	38
V_g	220 V	D_b	30
f_o	50 Hz	k_p	20
L	10 mH	k_i	22
C_{dc}	1350 μF	ω_0	40 rad/s
C_{vir}	0.5 mF	ω_c	175 rad/s
L	10 mH	k_i	22

power MOSFETs (LSIC1M120E0080 with 1200V/25A and $R_{ds(on)} = 80$ mΩ) from Littelfuse power semiconductors are driven by the isolation driver ISO5852S. The switching frequency is 10 kHz. Three hall current sensors (HCS-LTS-06A) are used for grid-side current measurements.

The verification of PI-VIC (the outer loop adopts virtual inertia control, and the inner loop controller adopts a PI controller, which is the current control) [21], MPC-VIC [23], and ADRC-VIC are performed. To simplify the battery testing, all battery discharge and charge modes are set to have a constant current during the experiment. The parameters of the power battery for charging and discharging test, ADRC-VIC, and PI controller are listed in Tables I and II. The battery parameters are referenced to the widely used batteries (Lithium iron phosphate battery) in electric vehicle TESLA MODEL3S. Fig.12 gives the configuration of a PABTS DC-MG in

experiment, in which two batteries are parallel connected, thus the parallel DC-DC converters and the BGCC form a DC-MG. The initial state of the DC-MG is defined as that there is battery-I for a 25A discharge test, and the system enters steady state. Based on this, the experiments contained the following scenarios, each comparing two cases. (1) Charging and discharging current tests of the batteries (Cases I and II). (2) The DC-bus voltage under grid voltage and load changes (Cases III and IV).

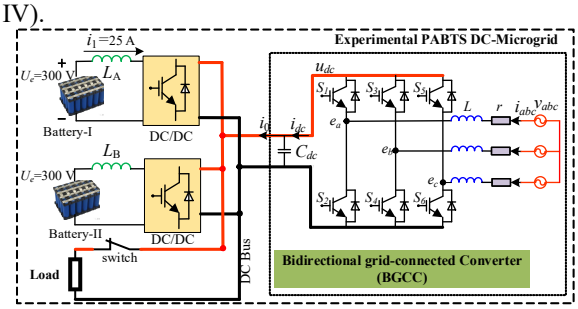


Fig. 13. Configuration of the PABTS DC-MG in experiment.

B. Result and Analysis

Case I: Charging Current Test

Assuming the PABTS DC-MG is in initial state, Battery-II was added to the system during the battery charging test, as shown in Fig.14 (a). The rechargeable battery-II is added to the system for charging at 0.16 s. The state-of-charge (SOC) gradually increases from the initial 50%, charging current stabilizes at 5 A, and terminal voltage of the battery is as large as 355.5 V. Fig.14 (b) shows the DC-bus voltage fluctuations under different control strategies. After the charging test was performed at 0.16 s, the power at the DC-bus was reduced and the DC-bus voltage dropped. Under the PI-VIC, despite providing inertia support, the maximal voltage-drop reached about 9 V. In the MPC-VIC proposed in [23], the MPC compensates for a suitable virtual reference current at the instance of charging transient to improve the inertial support capability of the VIC, and the voltage fluctuation is reduced to 5.6 V. MPC-VIC increases inertia to reduce DC-bus voltage fluctuations by changing the virtual current. Although the virtual reference current compensation can be appropriately increased to improve the suppression voltage fluctuations, this method still has an upper limit. The given reference current of the inner loop in VIC comes from the outer loop, and the outer loop input comes from the real-time sampled DC-bus voltage and current. The interference in the system can only come from the collected voltage and current; thus, the proposed ADRC-VIC uses the estimation of the system and outer loop error. It then uses feedback compensation to eliminate disturbance and suppresses the fluctuation of the DC-bus voltage by eliminating the interferences. The DC-bus voltage fluctuation with ADRC-VIC is significantly reduced (approximately 2.3 V), which proves its effectiveness.

Case II: Discharge Current Test

In initial state, to evaluate the discharging behavior of the batteries, battery-II was added for the discharge test at 0.16 s. Fig. 15 (a) shows the waveforms of the SOC, current, and voltage of the batteries during the discharge test. The SOC

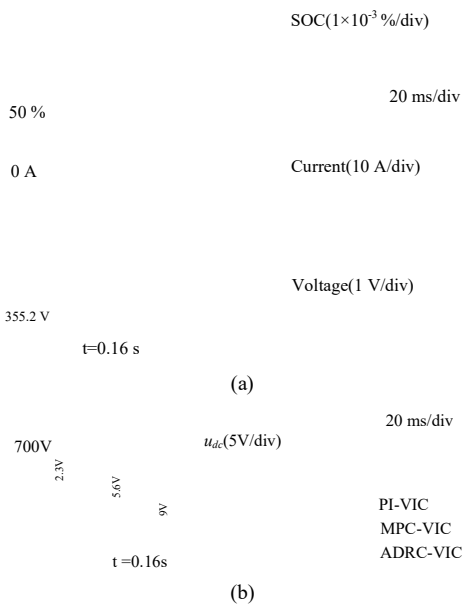
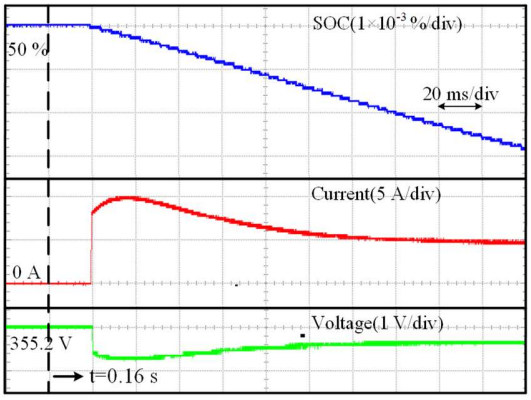
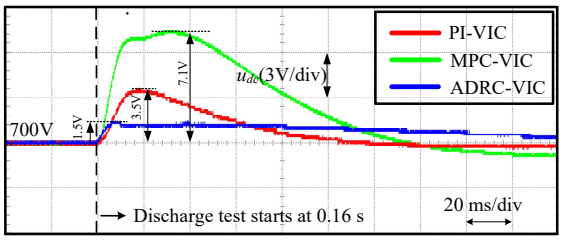


Fig. 14. DC-bus voltage under charging test of battery-II. (a) SOC, battery current, and voltage; (b) Dynamic response of the DC-bus voltage with different control methods.

gradually decreases from the initial 50%, charging current is 5 A, and terminal voltage of battery-II is stable at 354 V. Fig. 15 (b) shows a comparison of the DC-bus voltage fluctuations under different control strategies. Owing to the addition of the discharge test, the power at the DC-bus and the voltage fluctuation increase. Under VIC, the DC-bus voltage fluctuation caused by battery discharge is 7.1 V. Based on this, virtual current compensation (MPC-VIC method) was included in [23] to further improve the voltage fluctuation suppression ability, and the results show that the voltage fluctuation is reduced to 3.5 V. In the proposed ADRC-VIC, the interference from the discharge input power is reflected in the voltage and current input controlled by the VIC. The ADRC controller uses the input disturbance of the external loop voltage and the system disturbance estimation. The feedback compensation is used to eliminate the disturbance and suppress the voltage fluctuation. The results show that the voltage fluctuation is only 1.5 V under the discharge interference. This demonstrates its effectiveness in discharging disturbance.



(a)

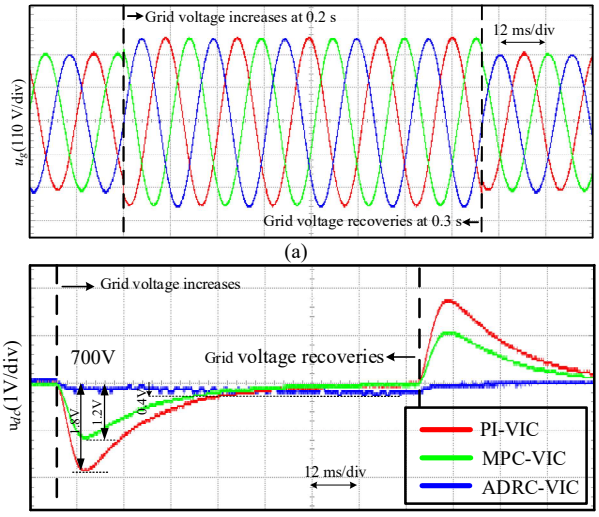


(b)

Fig. 15. DC-bus voltage under discharging test of battery-II. (a) Discharge current test; (b) DC-bus voltage with different control methods.

Case III: DC-bus Voltage under Grid Voltage Changes

The fluctuation of the grid voltage also causes interference in the PABTS DC-MG. Fig. 16 (a) shows the voltage fluctuation of the power grid. The voltage increases by 22% at t = 0.2 s, and the voltage recovers at t = 0.3 s. The results of the DC-bus voltage fluctuations under different control strategies are shown in Fig. 16 (b). It is evident that when the grid voltage fluctuates, the system has relatively obvious DC-bus voltage fluctuations under the control of the traditional VIC and MPC-VIC. In the ADRC, the impact of grid voltage fluctuations is limited to under 0.4 V, thus, demonstrating strong anti-interference suppression capability. The proposed strategy is significantly better than the other methods, that proves its effectiveness.



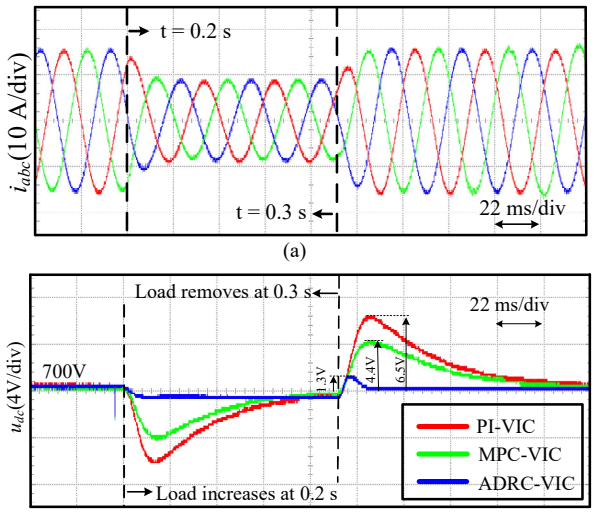
(a)

(b)

Fig. 16. DC-bus voltage under the change of grid voltage. (a) Grid-voltage; (b) DC-bus voltage.

Case IV: DC-bus Voltage under Load Changes

The load switching on the DC-bus also affects the voltage fluctuation at the DC-bus. As shown in Fig. 17, when the system is in initial state and battery-II is disconnected from the DC-MG, a resistive load of 4 kW is added at t = 0.2 s, and it is removed at t = 0.3 s. Fig.17(a) shows the experimental results. In initial state, the discharge test was performed for battery-I, and the power is delivered to the DC-bus. After the load is added, the DC-bus power decreases, resulting in a voltage drop and decrease in the grid current. When the load is removed, the DC-bus power is restored, voltage increases and current is restored. Fig. 17 (b) shows the voltage fluctuations under different control strategies. In the traditional VIC and MPC-VIC, the voltage fluctuations caused by load addition and removal are almost equal, but the MPC-VIC fluctuations are small. In the proposed ADRC-VIC, the interference caused by load fluctuations can be eliminated. The DC-bus voltage fluctuation is 1.3 V, which greatly suppresses the interference. The experiment verifies the effectiveness of the proposed scheme.



(a)

(b)

Fig. 17. Grid current and DC-bus voltage under load changes. (a) Three-phase grid current. (b) DC-bus voltage with different control methods.

C. Enhancement on DC-bus Voltage Stability

To clearly demonstrate the effectiveness of the proposed method, the aforementioned experimental results are analyzed and compared in Tables III and IV.

TABLE III
DC-BUS VOLTAGE FLUCTUATION PERCENTAGE WITH DIFFERENT METHODS

Methods	Case I	Case II	Case III	Case IV
PI-VIC [21,22]	9 V (1.29%)	7.1 V (1.00%)	1.8 V (0.26%)	6.5 V (0.93%)
MPC-VIC [23]	5.6 V (0.8%)	3.5 V (0.5%)	1.2V (0.17%)	4.4 V (0.63%)
ADRC-VIC	2.3 V (0.33%)	1.5 V (0.24%)	0.4 V (0.06%)	1.3 V (0.19%)

TABLE IV
DC-BUS VOLTAGE STABILITY ENHANCEMENT OF ADRC OVER OTHER CONTROL METHODS

Methods	Case I	Case II	Case III	Case IV
$D_{MPC-VIC}$	3.3 V (58.9%)	2V (57.1%)	0.8 V (66.6%)	3.1 V (70.4%)
D_{PI-VIC}	6.7 V (74.4%)	5.6V (78.8%)	1.4 V (77.8%)	5.2 V (80%)

Table III shows the DC-bus voltage fluctuations with different control strategies and their proportions to the reference (700 V here). Their proportions to the dc-link reference is calculated by (32), where $V_{peak}(t_p)$ and $V(t_\infty)$ represent the peak and steady-state DC-bus voltage. D is the dc-bus voltage fluctuation percentage. Table IV shows the DC-bus voltage fluctuation reduction and the percentage of ADRC relative to PI-VIC and MPC-VIC methods. The increased percentage is calculated by $D_{MPC-VIC}$ in (33) and D_{PI-VIC} in (34), where V_{PI-VIC}^{DC}, $V_{MPC-VIC}^{DC}$ and $V_{ADRC-VI}^{DC}$ represent the DC-bus voltage with PI-VIC, MPC-VIC and ADRC-VIC control methods. As

shown in Table III, under different disturbances, the DC-bus voltage fluctuation with ADRC-VIC will not exceed 0.5% of its reference. Table IV shows that, the DC-bus voltage fluctuation suppression effect with the proposed ADRC is increased by 58.9 %, 57.1 %, 66.6 % and 70.4 % when compared with MPC-VIC in four scenarios. Moreover, compared with traditional PI-VIC, the improvements are about 74.4 %, 78.8 %, 77.8 % and 80 %, respectively. Therefore, when external interference occurs, traditional VIC is not sufficient for stabilizing the DC-bus voltage. Although the virtual reference current compensation is provided in MPC-VIC, voltage fluctuation suppression cannot be minimized. Compared with MPC-VIC and PI-VIC, the proposed ADRC-VIC is obviously more robust in anti-interference, and is recommended for PABTS DC-MG where frequently charging and discharging test of the electric vehicle batteries are required.

$$D = \frac{\left|V_{peak}(t_p) - V(t_\infty)\right|}{V(t_\infty)}\% \tag{32}$$

$$D_{MPC-VIC} = \frac{\left|V_{MPC-VIC}^{\mathrm{DC}} - V_{ADRC-VIC}^{DC}\right|}{\left|V_{MPC-VIC}^{DC}\right|}\% \tag{33}$$

$$D_{PI-VIC} = \frac{\left|V_{PI-VIC}^{DC} - V_{ADRC-VIC}^{DC}\right|}{\left|V_{PI-VIC}^{DC}\right|}\% \tag{34}$$

VII. Conclusion

This paper presents an ADRC-VIC method to enhance the robustness of the PABTS DC-MG. The ADRC-VIC adopts the VIC to enhance system inertia, and the outer loop controller adopted the ADRC. It is modeled by the VIC equation, considering the fluctuations of the DC-bus voltage and current, and the influence of the grid current. The known charge and discharge interference, load switching, neglected system dynamics, and uncertainty interference are defined as the estimated total disturbances. Feedback compensation control is carried out, which reduces the sensitivity of the external and system parameters and stabilized the DC-link voltage of the DC-MG. Compared with traditional PI-VIC and MPC-VIC methods, the proposed ADRC-VIC control significantly suppresses the interference of external disturbances with the system. Finally, its effectiveness is verified under different scenarios.

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