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Single-Source Cascaded Multilevel Inverter with Voltage-Boost Submodule and Continuous Input Current for Photovoltaic Applications

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***Abstract*—Cascaded multilevel inverter produces a step-up output voltage by series-connection of several submodules supplied by isolated dc sources which can be implemented by photovoltaic (PV) sources. The unbalanced power provided by different PV sources may however distort the output voltage. To use a single dc source while retaining the voltage boosting, this paper proposes a novel cascaded multilevel inverter based on a four-switch submodule. It is conditioned by an input inductor, which discharges with boosted voltages across the submodules. Furthermore, a continuous input current is achieved by the inductor. The proposed inverter can be extended to higher voltage-level operations using capacitors to supply its extended submodules. To avoid switched-capacitive charging, a two-phase configuration where capacitors are directly charged by the inductive input current is presented. The voltages of capacitors are well balanced at the same average value and feature a similar ripple. The operating principles and pulse-width modulation scheme of the two-phase inverter are described. Theoretical analysis, calculations, and comparisons with the prior-art cascaded multilevel inverters illustrate the superiorities of the proposed inverter. Simulation and experimental results agree well with each other and verify the feasibility of the proposed inverter for PV power applications.**

***Index Terms*—Cascaded multilevel inverter, continuous input current, PV applications, single dc source, voltage boosting.**

I. Introduction

WHILE two-level voltage-source inverters have reached maturity and presented certain limitations for medium-voltage applications, many attempts to advance multilevel inverters (MLIs) with reduced voltage stresses on power switches have been made [1]–[3]. Additionally, the low total harmonic distortion (THD) of the output voltage achieved by MLIs has made them more and more commonly seen in applications requiring a high-quality output voltage. To date, MLIs are widely used in power electronics systems such as the ac adjustable speed drives [4], flexible ac transmission [5], and renewable energy generation [6].

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In general, the traditional MLIs are categorized into three groups including the cascaded multilevel inverter (CMI) [1], neutral-point-clamped (NPC) [2], and the flying capacitor (FC) inverters [3]. Among them, the CMI, which is mostly based on the series-connection of several full-bridges to form the cascaded H-bridge (CHB) inverter has been demonstrated to be advantageous over other MLIs in terms of producing a boosted voltage. However, it sometimes suffers from a large number of isolated dc sources [7]–[10].

For renewable energy applications such as PV power generation, the source requirement can be easily met due to the widespread PV sources that can be installed separately. The CMIs, however, still face certain challenges related to the variable voltage/power of the PV sources. If each series-connected submodule (SM) is directly supplied by an individual PV source, the same output current flowing through all of the SMs causes mismatching issues, since, in most cases, the active powers provided by different PV sources are unbalanced. The ac output voltage may be over-modulated, thus deteriorating the waveform quality [11].

Despite that, the boosted output voltage of the CMIs makes them suitable for PV systems to reduce the requirement for high step-up transformers, as illustrated in Fig. 1 [11], [12]. Fig. 1(a) shows that a dc-dc front-end converter is used to boost the low-voltage dc (LVDC) link to a medium-voltage dc (MVDC) link for supplying a rear-end inverter. The two-stage power conversion, however, may require a larger number of components [12]. Alternatively, the low-voltage ac (LVAC) link can be interfaced with the medium-voltage ac (MVAC) link using a high step-up line transformer with a large turns-ratio (Fig. 1(b)). It is therefore promising to obtain a step-up voltage at the inverter output (Fig. 1(c)) and one straightforward solution is to use CMIs. But the mismatch problems among many of the PV sources need to be addressed [11].

Recently, reduced dc-source CHB inverter using capacitors to supply its SMs are presented [13]–[14]. However, the voltage balance of the capacitors becomes crucial and additional voltage sensing circuits cooperating with modified pulse-width modulation (PWM) scheme are required. Moreover, the voltages of the capacitors must be balanced at different values lower than the dc voltage. Different voltage-rating devices are used and the total output voltage is lowered [15]. Nonetheless, due to reduced source requirement, using capacitors for supplying some of the SMs has been proven to be an effective strategy [16]–[21].

With capacitors as the intermediate energy-storage devices, one alternative is to cascade several switched-capacitor (SC)

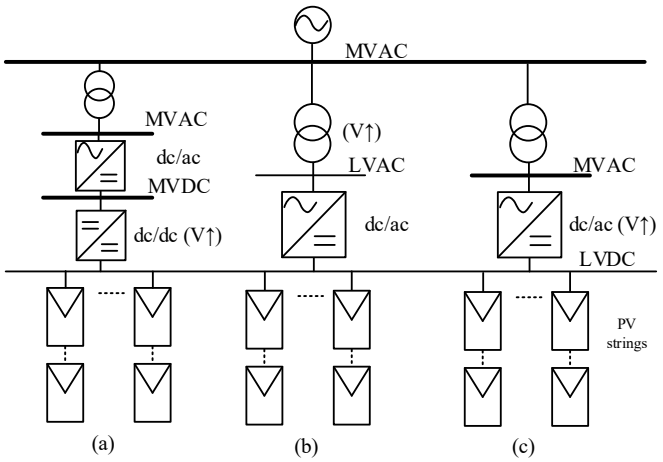

Fig. 1. Diagrams of PV power generation interfacing with MVAC link: voltage boosting (V↑) achieved by (a) step-up dc-dc converter, (b) step-up transformer, and (c) step-up dc-ac inverter.

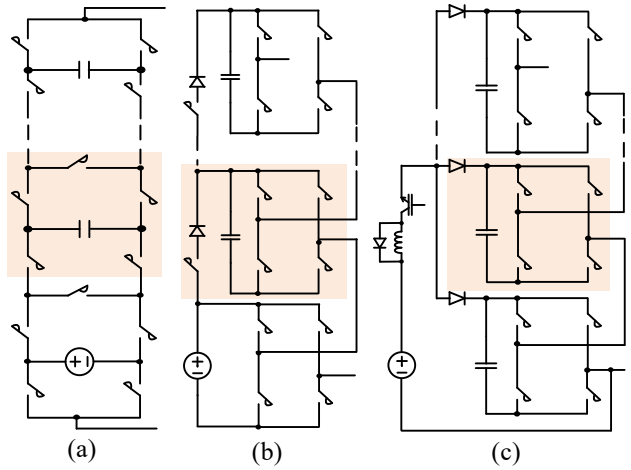

Fig. 2. Prior-art CMIs using (a), (b) SCs with a single dc source [19], [20], and (c) SCs with a single dc source and auxiliary charging circuits [23].

SMs that generate different output voltages from a series-parallel conversion. Despite that, switches used for the rear-end HB have to withstand the maximum output voltage, which requires high-voltage devices [16]−[18].

Cascaded SC MLI without the rear-end full-bridge is presented in [19], where a unique switching cell consisting of 5 power switches is used, as shown in Fig. 2(a). It exhibits an inherent polarity reversal capability and induces a uniform voltage on its devices. A similar approach is presented in [20] based on an extendable SC circuit (Fig. 2(b)). Both inverters use a single dc source and a number of floating capacitors. Different from the single-source CHB inverter [13]–[15], the charging currents of the capacitors are independent of the output current, and thus, the voltages across the capacitors can be maintained close to the dc voltage. However, the source-voltage regulation is not investigated and a voltage drop in the dc source essentially lowers the voltages across SMs. As a result, the total attainable voltage becomes lower. Additional dc-dc voltage stages may be required to address the source-voltage deficiency, as discussed in [21]–[23]. Note that, in [23] (Fig. 2(c)), a basic boost stage

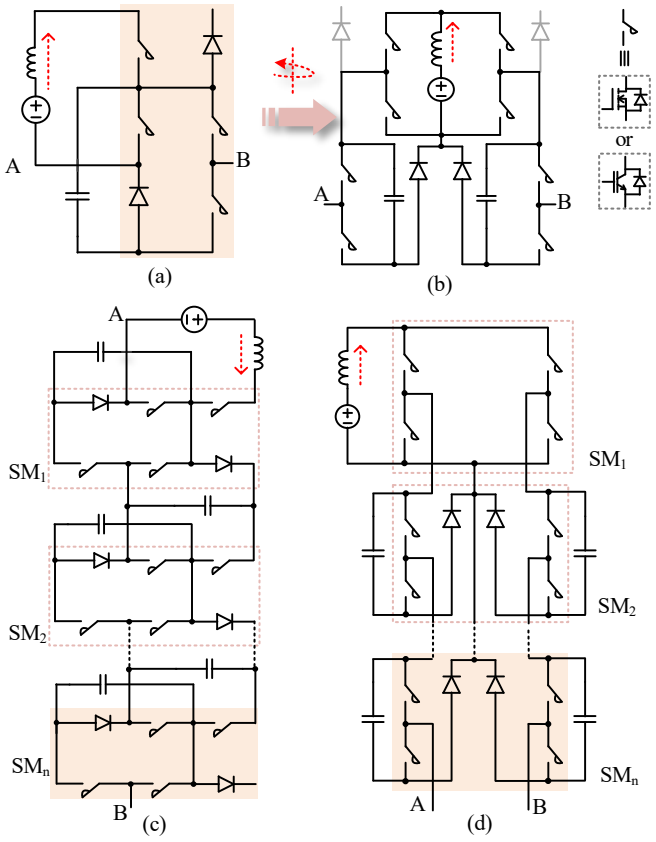

Fig. 3. Illustrations of the (a) proposed SM and (c) the one-phase (1ϕ) extension of the proposed CMI; (b) two-phase (2ϕ) symmetrical inverter topology and (d) the 2ϕ extension.

with multiple outputs is used to supply all capacitors. However, the switch and output diodes in the boost stage experiences high voltages.

In light of the above issues, this paper proposes a novel CMI, which is fed by a single dc source and uses capacitors to supply its SMs. The derivation of the proposed CMI begins with a basic SM that can be implemented by two half-bridges, as shown in Fig. 3 (a). It can be extended for a high voltage-level operation, using SC technique (see Fig. 3(c)) [24], [25].

In addition, the proposed CMI can be extended in a two-phase (2ϕ) configuration. For that, a five-level inverter is preliminarily derived as shown in Fig. 3(b). The resultant 2ϕ five-level inverter is extended using a SM consisting of 4 switches and 2 diodes (see Fig. 3(d)). Both extensions in Fig. 3(c) and (d) have the following key features.

1) A single dc source for multiple series-connected SMs;
2) Built-in voltage boosting for stepping up the SM voltage and achieving source-voltage regulation;
3) Voltages across the capacitors remain steady and balanced among the SMs automatically;
4) A continuous input current suitable for interfacing with renewable energy sources.

Circuit configurations of 1ϕ and 2ϕ seven-level inverters are exemplified as in Fig. 4. It is noticed that the 1ϕ topology uses one less switch since it maintains a continuous input current and thus, S_{11} is no longer necessary. However, the 1ϕ topology causes inrush switched-capacitive current, which remains a

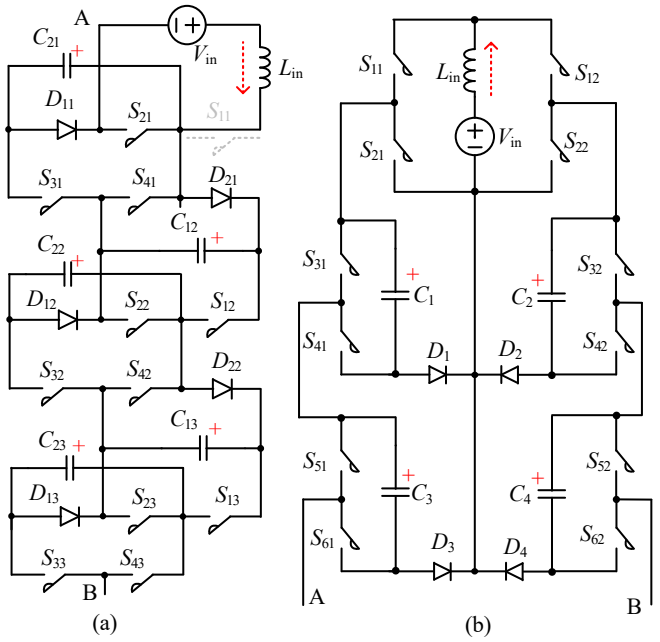

Fig. 4. Proposed cascaded seven-level inverter configured in (a) 1ϕ topology (one less switch) and (b) 2ϕ topology.

concern for MV applications. Differently, the 2ϕ topology is directly charged by the inductive input current. Therefore, the operating principles of the 2ϕ CMI are discussed in detail in this paper. As for circuit components, the 2ϕ CMI uses the same number of switches as that of the conventional CHB inverter. The complexity of the proposed CMI is not high. An input inductor is required to step up the SM voltage, which is illustrated in Section II. The operating states and PWM scheme of the 2ϕ seven-level inverter are also presented. Theoretical analyses of voltage/current ratings, power losses, and common-mode voltage are presented in Section III. Section IV compares the proposed CMI with the prior-art MLIs to discuss the pros and cons. Simulation and experimental results are then given in Section V before a conclusion is drawn in Section VI.

II. Two-Phase Extension of the Proposed CMI

A. Operating States

Assuming that the capacitors are with relatively large capacitances so that voltages across them remain steady with the same average value of V_C, to be illustrated in Subsection C. Voltage levels across the output terminals (v_{AB}) during the positive half-cycle are 0, V_C, $2V_C$, and $3V_C$. To produce them, eight switching states are exemplified and described next.

Level 0 ($v_{AB} = 0$): Fig. 5(a) shows the operating state where the inductor L_{in} is discharged to all capacitors, forming thus four discharging loops. Which discharging loop is established depends on the instantaneous voltages of capacitors. When capacitors C_1 and C_3 present lower voltages during the positive half-cycle, they are charged by L_{in}. Otherwise, C_2 and C_4 are charged. When switches S_{21} and S_{22} are turned on, L_{in} is charged by the dc source, and the operating state is shown in Fig. 5(b).

Level 1 ($v_{AB} = V_C$): Fig. 5(c) shows the operating state where the capacitor C_4 is discharged by the load current, maintaining the voltage of V_C across the output terminals. Similarly, the inductor enters its charge state by turning on S_{21} and S_{22}. Moreover, aiming to keep voltages of C_2 and C_4 close to each other, C_2 is made to discharge to the output in this state as shown in Fig. 5(d).

Level 2 ($v_{AB} = 2V_C$): Fig. 5(e) and (f) show two operating states when C_2 or C_4 is placed at the output current path. Different from the previous states, the load current flows through the dc source. When the input current (I_{in}) is larger than the load current (i_o), the inductor keeps discharging to the capacitors C_1 or/and C_3, and the voltage across the output is equal to $2V_C$. When I_{in} is equal to i_o, the inductor does not provide energy to the capacitors and the output voltage is reduced to ($V_C + V_{in}$). The latter could occur under light load conditions, which occupies a relatively small duration since for the proposed single-source boost inverter, the average input current I_{in} is larger than the maximum output current i_{omax}, to be illustrated in the next subsection. When the inductor is charged in Fig. 5(g), the two capacitors C_2 and C_4 both discharge to the output to maintain the voltage level of $2V_C$.

Level 3 ($v_{AB} = 3V_C$): Fig. 5(h) shows the operating state when the output voltage is $3V_C$. Similarly, the load current flows through the dc source. At light load conditions, the output voltage drops to ($2V_C + V_{in}$). Both capacitors C_2 and C_4 discharge to the output with their voltage dropping quickly in this state. As the discharging currents of C_2 and C_4 are the same (i_o), their voltages keep close to each other.

Due to the symmetrical structure, capacitors C_1 and C_3 discharge during the negative half-cycle, which implies that the average voltages of capacitors and their ripples are the same. Moreover, the average voltage of capacitors can be regulated by controlling the charging duty ratio of the L_{in} through the level-shift (LS) PWM scheme.

B. LS PWM Scheme

To implement the LS PWM scheme for the 2ϕ seven-level inverter, three carriers (T_1–T_3) with the same frequency, phase, and peak-to-peak amplitude are deposited as shown in Fig. 6. A half-wave sinusoidal signal ($0 < t < 1/(2f_l)$) is used as the modulation signal which is expressed as

$$v_{ref} = M_{ac} \sin(2\pi f_l t) \tag{1}$$

where M_{ac} is the amplitude of the modulation signal, and f_l is the fundamental frequency.

Additionally, a stepped dc signal (M_{dc}) is used to produce the shoot-through duty ratio for charging L_{in} whenever M_{dc} is less than the carrier in each carrier band. Considering that a constant dc signal M_{dc} ($0 < M_{dc} \leq 1/3$) is used and that the magnitude between two adjacent steps is 1/3, a constant inductive-charge duty ratio $d = (1-3M_{dc})$ can then be obtained in each switching period (T_s). As seen from Fig. 5, when L_{in} is discharged, the average discharging voltage of the inductor is found as (V_{in}–V_C). Applying volt-second balance to L_{in}, the following equation is written

$$V_{in} dT_s + (V_{in} - V_C)(1 - d)T_s = 0 \tag{2}$$

Consequently, the voltage V_C is found as

$$V_C = V_{in}/(3M_{dc}) \tag{3}$$

Using Eq. (3), the ac voltage gain is calculated by

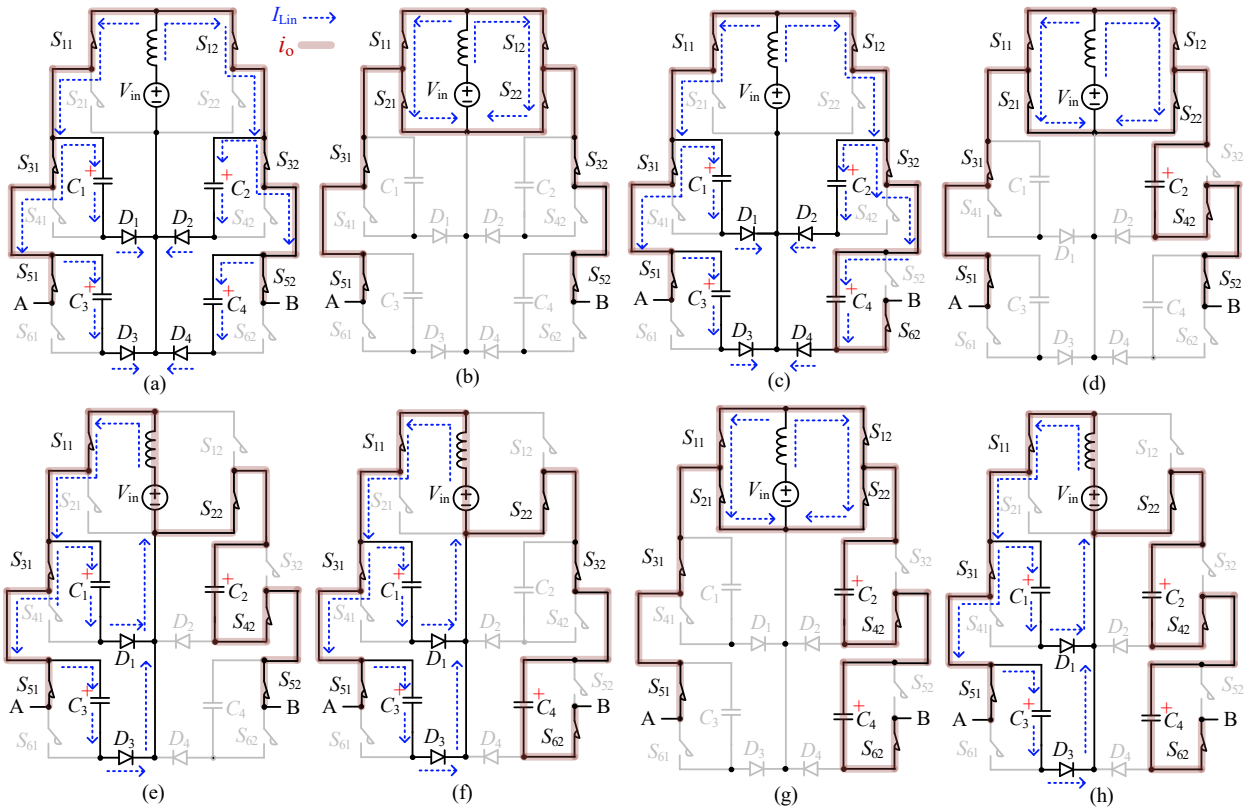

Fig. 5. Operating states of the 2ϕ seven-level inverter during positive half-cycle: (a), (b) Level 0; (c), (d) Level 1; (e), (f), (g) Level 2; and (h) Level 3 with possible input inductor current (I_{Lin}) and output current (i_o) paths.

$$G_{ac} = 3M_{ac}V_C/V_{in} = M_{ac}/M_{dc} \tag{4}$$

Furthermore, for a unity power factor operation, the relationship between the input current (I_{in}) and the maximum output current (I_{omax}) can then be established as

$$I_{in} = I_{omax}M_{ac}/(2M_{dc}) \tag{5}$$

To generate a seven-level output voltage, M_{ac} should fulfill $2/3 < M_{ac} < 1$. Additionally, M_{dc} is confined to 1/3, i.e., $0 < M_{dc} < 1/3$. Therefore, it implies that the average input current should be larger than the maximum of the output current of the proposed 2ϕ CMI, which agrees well with the operating states in Fig. 5(e), (f), and (h). Though the output current flows through L_{in}, it can still discharge to capacitors to maintain a boosted V_C. Furthermore, both the inductive currents I_{in} and i_o are not disrupted abruptly when transiting from any inductor-charge to -discharge states.

Additionally, due to the cascaded feature, the phase-shift (PS) PWM scheme can also be applied to the 2ϕ CMI. Notably, the switching frequency for each SM can then be reduced while maintaining relatively high-quality output waveforms using the PS PWM scheme. However, the input current features a higher ripple if the switching frequency of SM_1 is too small.

Under the LS PWM scheme, the positive half-cycle is divided into five zones Z_1 to Z_5. It is observed that capacitors are charged or discharged at a low frequency, featuring a low-frequency ripple as analyzed next.

C. Capacitor Voltage Ripple

Letting the modulation reference v_{ref} be 1/3, the duration of zone Z_1 can then be calculated by finding t_1, according to

$$t_1 = arcsin(3M_{ac})^{-1}/2\pi f_l \tag{6}$$

The same analysis applies to other zones by finding t_2 to t_4. As seen in Fig. 5 (d) and (e), the capacitor C_2 discharges to the output during Levels 1 and 2. Its reflection in Fig. 6 is that when the modulation reference $v_{ref} > (M_{dc}+1/3)$ in zone Z_2, the capacitor C_2 keeps discharging to the output with its voltage dropping. The charge transferred from C_2 to the output is calculated by

$$Q_{C2\_Z2} = \int_{t_x}^{t_2} i_o(t)dt \tag{7}$$

where t_x is expressed as $t_x = t_1 + 3M_{dc}(t_2 - t_1)$.
Furthermore, the capacitor C_2 discharges intermittently during zone Z_3 which includes states in Fig. 5(f), (g), and (h). Since the three states account for $(3v_{ref} - 3M_{dc} - 1)$ of the total duration $(t_3 - t_2)$ of zone Z_3, the discharge of capacitor C_2 during zone Z_3 is thus calculated by

$$Q_{C2\_Z3} = \int_{t_2}^{t_3} i_o(t)(3v_{ref} - 3M_{dc} - 1)\,dt \tag{8}$$

Using Eqs. (7) and (8), the total charge loss of the capacitor C_2 during the positive half-cycle is calculated by

$$Q_{C2} = 2Q_{C2\_Z2} + Q_{C2\_Z3} \tag{9}$$

The voltage drops across the capacitor C_2 and the associate voltage ripple is calculated by

$$\Delta V_{C2} = Q_{C2}/2C_2 \tag{10}$$

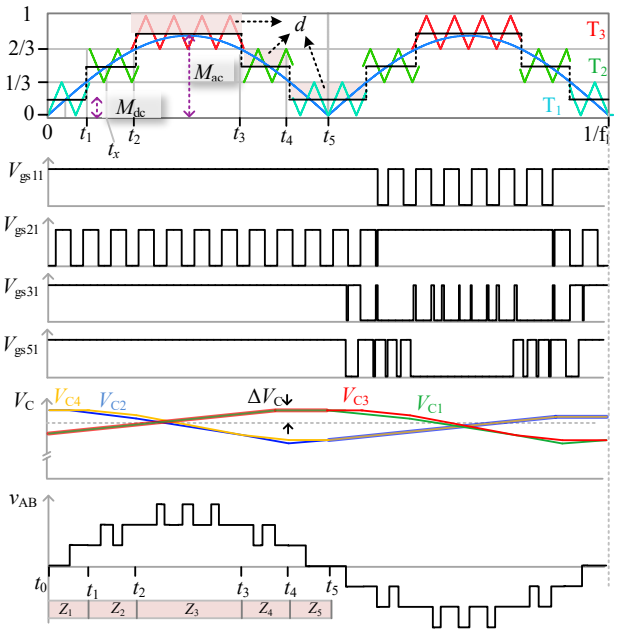

Fig. 6. Level-shift (LS) PWM scheme for the 2ϕ seven-level inverter (gating signals of $S_{41} = \overline{S}_{31}$ and $S_{61} = \overline{S}_{51}$) and the resultant key voltages.

The same analysis applies to the capacitor C_4, whose voltage keeps close to that of C_2. For the other two capacitors (C_1 and C_3), their voltage ripples can also be analyzed following the same procedure. In fact, due to the symmetrical structure of the 2ϕ CMI, it can be deduced that the voltage ripples of capacitors C_1 and C_3 are equal to those of the C_2 and C_4, respectively. If a low ripple voltage such that $\Delta V_C \le 10\,\% V_C$ must be ensured, the capacitances should be selected according to

$$C_1(C_2) \ge 5\frac{Q_{C2}}{V_C}, \text{ and } C_3(C_4) \ge 5\frac{Q_{C4}}{V_C} \qquad (11)$$

Based on the above criterion and under the nominal operating power of 1 kW, the theoretical capacitances should fulfill C_1 (C_2) ≥ 0.46 mF and C_3 (C_4) ≥ 0.43 mF, respectively.

Accordingly, the numerical calculations of the ripple voltages of the four capacitors (0.47 mF each) versus the output power are studied in Fig. 7. As seen, the voltage ripples of capacitors are at a similar level. They increase as the output power rises, which is expected since the output current becomes larger. Therefore, to maintain a low voltage ripple across each capacitor, it is reasonable to use large capacitances suggested by Eq. (11). Furthermore, the total installed energy of capacitors is

$$\mathrm{E} = \frac{1}{2}CV^2 \times 4 = 37.6\ \mathrm{J/kW} \qquad (12)$$

It should be mentioned that when the allowable voltage ripples of capacitors are larger, smaller capacitances can be considered to reduce the total installed energy, which is demonstrated in the simulated MV PV power generation using 0.25-mF capacitors.

III. Theoretical Analysis of the Two-Phase CMI

A. Voltage and Current Stresses

According to the eight operating states shown in Fig. 5, the switches are clamped by the voltages across capacitors when they are turned off. The voltage stresses on the switches are thus

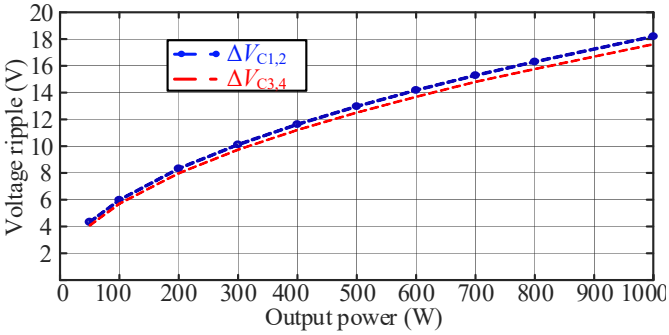

Fig. 7. Calculated voltage ripples of the capacitors versus output power.

the same, as given by $V_{ds} = V_C$. The blocking voltages of diodes are however different. The peak inverse voltages of D_3 and D_4 are $2V_C$, higher than those of D_1 and D_2 (V_C). Furthermore, the currents flowing through switches are different as discussed next.

Assuming that the 2ϕ CMI operates with unity power factor, it is observed from Fig. 6 that the capacitors C_1 and C_3 are charged during the positive half-cycle when the input and output currents flow in the same direction. Due to the cascaded feature, the charging current of the capacitor in SM_n must be transferred by switches in $SM_{(n-1)}$. It should however be mentioned that the current stresses of switches in SM_n are smaller than those of $SM_{(n-1)}$. That is, the maximum current stress is induced on switches of SM_1, which is estimated as the sum of the maximum input and output currents ($I_{in} + i_{omax}$). During the positive half-cycle, assuming that the inductor current is discharged to the two capacitors C_1 and C_3 equally. The maximum current through switches in SM_2 is then given by ($1/2I_{in} + i_{omax}$). For SM_3, it conducts only the output current, the current stresses on switches in SM_3 are i_{omax}.

With different conducting currents, switches may present different switching losses. Assuming that the 2ϕ CMI operates under the unity power factor, the switching losses of switches are analyzed according to the five zones shown in Fig. 6.

B. Switching Losses Under the LS PWM Scheme

Zone Z_1 (t_0 to t_1): in this zone, switches S_{22}, S_{52}, and S_{62} are switched at the carrier frequency f_s. The current flowing through switch S_{22} is $I_{s22} = 1/2(I_{in} + i_o)$, while the currents of switches S_{51} and S_{61} are the output current: $I_{s51} = I_{s61} = i_o$. Therefore, the switching losses of switches S_{22}, S_{52}, and S_{62} in this zone are respectively calculated by

$$P_{sw22\_1} = \frac{V_{ds}f_s(t_{on}+t_{off})}{2(t_1-t_0)} \int_{t_0}^{t_1} \frac{1}{2}(I_{in} + i_o(t))\mathrm{d}t \qquad (13)$$

and

$$P_{sw52\_1} = P_{sw62\_1} = \frac{V_{ds}f_s(t_{on}+t_{off})}{2(t_1-t_0)} \int_{t_0}^{t_1} \frac{1}{2} i_o(t)\mathrm{d}t \qquad (14)$$

where t_{on} and t_{off} are the turn-on and turn-off durations of the switches, respectively.

Furthermore, when $v_{ref} > M_{dc}$, switches S_{32} and S_{42} begin to operate at the carrier frequency from ($2t_1 - t_x$) to t_1. Their conducting currents are $I_{s32} = I_{s42} = i_o$. The switching losses of them in zone Z_1 are respectively calculated by

$$P_{sw32\_1} = P_{sw42\_1} = \frac{V_{ds}f_s(t_{on}+t_{off})}{2(t_x-t_1)} \int_{2t_1-t_x}^{t_1} i_o(t)\mathrm{d}t \qquad (15)$$

Zone Z_2 (t_1 to t_2): switches S_{12}, S_{52}, and S_{62} are switched at the carrier frequency. The current of switch S_{12} is $0.5(I_{in} - i_o)$, while switches S_{52} and S_{62} conduct the output current i_o. The switching losses of them are thus calculated by

$$P_{sw12\_2} = \frac{V_{ds} f_s (t_{on}+t_{off})}{2(t_2-t_1)} \int_{t_1}^{t_2} \frac{1}{2}(I_{in} - i_o(t))\mathrm{d}t \quad (16)$$

and

$$P_{sw62\_2} = P_{s52\_2} = \frac{V_{ds} f_s (t_{on}+t_{off})}{2(t_2-t_1)} \int_{t_1}^{t_2} i_o(t)\mathrm{d}t \quad (17)$$

Furthermore, from t_1 to t_x, switches S_{22}, S_{32}, and S_{42} still operate at the carrier frequency, their switching losses are, respectively, calculated by

$$P_{sw22\_1} = \frac{V_{ds} f_s (t_{on}+t_{off})}{2(t_x-t_1)} \int_{t_1}^{t_x} \frac{1}{2}(I_{in} + i_o(t))\mathrm{d}t \quad (18)$$

$$P_{sw32\_2} = \frac{V_{ds} f_s (t_{on}+t_{off})}{2(t_x-t_1)} \int_{t_1}^{t_x} i_o(t)\mathrm{d}t \quad (19)$$

and

$$P_{sw42\_2} = \frac{V_{ds} f_s (t_{on}+t_{off})}{2(t_x-t_1)} \int_{t_1}^{t_x} i_o(t)\mathrm{d}t \quad (20)$$

Zone Z_3 (t_2 to t_3): switches S_{12}, S_{32}, and S_{42} operate at the carrier frequency. The conducting current of S_{12} is $0.5(I_{in} - i_o)$ while for switches S_{32} and S_{42}, their conducting currents are both i_o. Therefore, the switching losses are calculated by

$$P_{sw12\_3} = \frac{V_{ds} f_s (t_{on}+t_{off})}{2(t_3-t_2)} \int_{t_2}^{t_3} \frac{1}{2}(I_{in} - i_o(t))\mathrm{d}t \quad (21)$$

and

$$P_{sw32\_3} = P_{s42\_3} = \frac{V_{ds} f_s (t_{on}+t_{off})}{2(t_3-t_2)} \int_{t_2}^{t_3} i_o(t)\mathrm{d}t \quad (22)$$

Switching losses in zones Z_4 and Z_5 can be found due to the symmetry. Throughout the positive half-cycle, the switch S_{21} operates at the carrier frequency. As seen from Fig. 5(b), (d), and (g), the inductor-charge and output currents flow through the switch S_{21}, whose conducting current is $I_{s21} = 0.5(I_{in} - i_o)$. The switching losses of S_{21} are thus calculated by

$$P_{sw21} = \frac{V_{ds} f_s (t_{on}+t_{off})}{2} \frac{f_l}{2} \int_{t_0}^{t_5} \frac{1}{2}(I_{in} - i_o(t))\mathrm{d}t \quad (23)$$

Under the LS PWM scheme, although all switches need to operate at the carrier frequency during some zones of a fundamental cycle, it is deduced from Fig. 6 that except for the switches S_{21} and S_{22}, all other switches remain on/off in one half-cycle. The total switching loss is reduced, which will be examined through simulations, together with conduction losses analyzed as follows.

C. Conduction Losses and Diode Reverse-Recovery Loss

Average currents of devices are considered to estimate their conduction losses. In each carrier period, the current flowing through switch S_{11} is $(I_{in} + i_o)$ in the inductor-discharge state, or $1/2(I_{in} + i_o)$ in the inductor-charge state. The average current flowing through S_{11} during the positive half-cycle is given by $(I_{in} + i_o)(1 - 0.5d)$. During the negative half-cycle, the average current of S_{11} can then be estimated as $0.5(I_{in} + i_o)d$. Therefore, the conduction loss of S_{11} is calculated by

$$P_{con,s11} = \frac{f_l R_{on}}{2}\left[\int_0^{0.5/f_l} \left(1 - \frac{1}{2}d\right)^2 \left(I_{in} + i_o(t)\right)^2 dt + \int_{0.5/f_l}^{1/f_l} \frac{1}{4}d^2 (I_{in} + i_o(t))^2 dt\right] \quad (24)$$

where R_{on} is the on-state resistance of the switch.

The same conduction-loss analysis can be applied to other switches, whose details are not repeated here.

Similarly, the conduction loss of the inductor caused by the parasitic resistance r_L can be calculated according to

$$P_{Lin} = {I_{Lin}}^2 r_L = {I_{in}}^2 r_L \quad (25)$$

Capacitors are assumed to have the same conduction loss since they experience a similar charge/discharge current. Taking the capacitor C_1 as an example, its conduction loss during the positive half-cycle when it is charged is expressed as

$$P_{C1\_phc} = [\frac{1}{2} I_{in}(1-d)]^2 r_{Lin} = \frac{1}{4}{I_{in}}^2 (1-d)^2 r_C \quad (26)$$

where r_C is equivalent-series-resistance (esr) of the capacitor.

During the negative half-cycle, the capacitor C_1 discharges to the output. Using Eq. (9), and assuming $Q_{C1} = Q_{C2}$, the average current of the capacitor C_1 during the negative half-cycle is

$$I_{C1} = 2Q_{C1} f_l \quad (27)$$

based on which, the conduction losses of the capacitor C_1 during the negative half-cycle is calculated by

$$P_{C1\_nhc} = [2Q_{C1} f_l]^2 r_{Lin} = 4{Q_{C1}}^2 {f_l}^2 r_C \quad (28)$$

The total conduction loss of the capacitor C_1 is summarized as

$$P_{C1} = 1/2(P_{C1\_phc} + P_{C1\_nhc}) \quad (29)$$

The diodes D_1 and D_3 (or D_2 and D_4) are turned on to conduct the inductor-discharge current during one of the half-cycles. Assuming that the forward voltage of a diode is V_{Fd}, the conduction loss is expressed as

$$P_D = \frac{1}{2}[\frac{1}{2} I_{in}(1-d)]V_{Fd} \quad (30)$$

Additionally, the reverse-recovery current of the diode induces additional power loss which can be calculated by

$$P_{drr} = \frac{1}{2} V_d Q_{rr} f_s \quad (31)$$

where V_d is the peak-inverse voltage and Q_{rr} the reverse-recovery charge of the diode.

To verify the effectiveness of the theoretical calculations, power losses of different kinds of components are simulated through *PLECS*. During the simulation, parameters obtained from the datasheets of devices are considered, while the parasitic resistances of the reactive components are 0.1 Ω. Simulation results of switching losses are shown in Fig. 8(a), which indicates that theoretical losses are close to the simulations. The total switching loss (12 switches) is very low at 3.82 W. This is because only a few switches operate at the carrier frequency (10 kHz) concurrently (see Fig. 6). Similarly, power losses of different components are shown in Fig. 8(b), where the similarity between the calculated and simulated values is seen. The conduction loss of L_{in} is relatively large since for the boost CMI, its I_{in} is several times larger than the rms output current.

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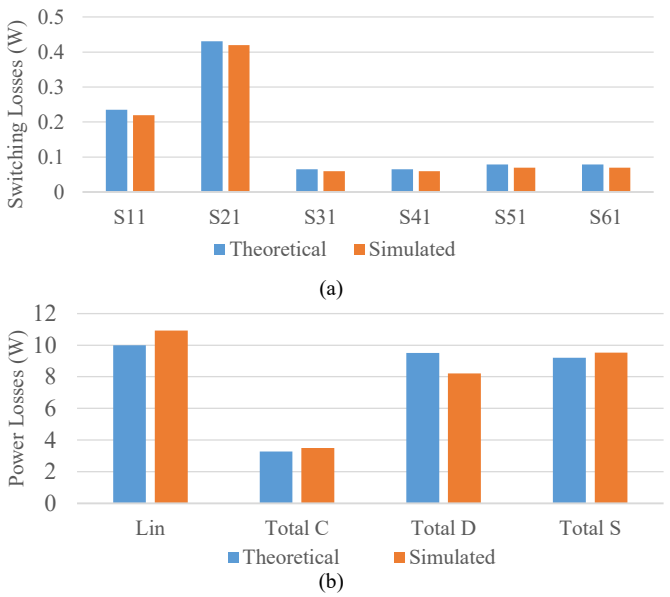

Fig. 8. Theoretical and simulated (a) switching losses and (b) power losses of different kinds of components under 1 kW (r_C = r_L = 0.1Ω; considering switches *IRF300P227* and diodes *DPG60I300HA*).

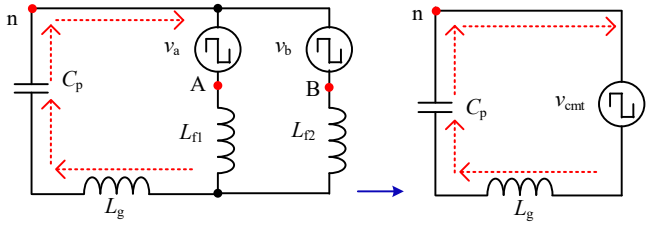

Fig. 9. Common-mode model of the 2ϕ seven-level inverter (v_{cmt} is the total excitation voltage of C_p and L_g).

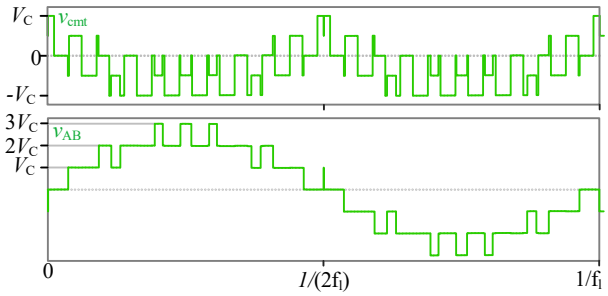

Fig. 10. The total common-mode voltage (v_{cmt}) with respect to v_{AB} under the LS PWM scheme.

D. Common-Mode Voltage

The common-mode model of the proposed 2ϕ seven-level inverter is shown in Fig. 9, considering the parasitic capacitance (C_p) that is connected between the negative terminal (point n) of the dc source and the ac neutral of the transformerless PV grid-tied system. The ground stray inductance is notated as L_g. Accordingly, the common-mode voltage (v_{cm}) is written as

$$v_{cm} = \frac{1}{2}(v_A + v_B) \tag{32}$$

where v_A (v_B) is the voltage of the output terminal A (B) with respect to the negative terminal of the dc source.

Both the common-mode and differential-mode voltages contribute to the total excitation voltage (v_{cmt}) of C_p and L_g, expressed as [27]

$$v_{cmt} = \frac{1}{2}(v_A + v_B) + \frac{1}{2}(v_A - v_B)\frac{L_{f2}-L_{f1}}{(L_{f1}+L_{f2})} \tag{33}$$

where L_{f1} and L_{f2} are line inductors of the two phases, respectively.

Assuming that the two inductances are close to each other, which usually is the case, the total excitation voltage can then be simplified as

$$v_{cmt} = v_{cm} = \frac{1}{2}(v_A + v_B) \tag{34}$$

Fig. 10 depicts the total common-mode voltage under each voltage level. The maximum value is $v_{cmt,max} = V_C$, lower than the maximum output voltage ($3V_C$). The suppression of the ground leakage current of CMIs for transformerless grid-tied applications is discussed in [27], where passive common-mode filters are mentioned. Details are however not included in this paper. Instead, the simulated leakage current is given and discussed in Section V considering the common-mode filters [27]. Before proceeding with it, a comparative study of the proposed CMI is presented next.

IV. Inverter Comparison and Design Considerations

A. Qualitative Comparison among the MLIs

A qualitative comparison among the conventional MLIs, prior-art CMIs, and the proposed CMI is illustrated in Table I. As seen, to produce the same number of voltage levels of (2*n*+1), the proposed CMI uses the same numbers of switches and gate drivers as those of the conventional CHB inverter. However, the proposed CMI uses a single dc source compared to the conventional CHB inverter, which requires multiple isolated dc sources. For PV applications where the isolated dc sources are no longer a major challenge, the conventional CHB inverter may use the smallest number of power devices [11].

Additionally, for low voltage-level applications, the proposed CMI can also be configured with fewer SMs. The numbers of the components used are thus at a similar level with those of the conventional NPC or FC inverter. The NPC/FC inverter may have difficulty in balancing the voltages of the dc-link or flying capacitors. Unlike the conventional multilevel inverters, however, the reverse-power flow is not allowed for the proposed CMI. Similarly, the reverse-power flow is not supported by the prior-art CMIs presented in [20] and [23]. The SC technique is used in [19], [20], and the proposed 1ϕ CMI shown in Fig. 3(c). Their devices are thus burdened by the inrush currents of capacitors. They may be less suitable for higher voltage/power applications [24], [25]. Differently, for the CMI in [23] and the proposed 2ϕ CMI shown in Fig. 3(d), the floating capacitors are charged by an inductive input current, and therefore free of the inrush currents.

The total capacitances of the compared MLIs are also given in Table I. As can be seen, for CMIs in [19], [20], and [23], large capacitances are used. Its total installed energy (total E) is thus

TABLE I
COMPARISON WITH AVAILABLE MLIS PRODUCING A (2n+1)-LEVEL VOLTAGE

MLIs	The number of					Total C(mF) /Volt.	Total E J/kW	V_C	Contin-uous I_{in}?	Inrush current?	Reverse power?	Remarks
	N_S / N_{dr}	N_D	N_C	N_L	N_{dc}							
CMI [19] Fig. 2(a)	5n-1	0	n-1	0	1	3.3/100 V	N.I.	V_{in}	No	Yes	Yes	SM using 5 switches, SC voltage balancing
CMI [20] Fig. 2(b)	5n-1	n-1	n-1	0	1	4×4.7/100 V	88.13	V_{in}	No	Yes	No	SM using 5 switches and a diode, SC voltage balancing
CMI [23] Fig. 2(c)	4n+1	n	n	1	1	4×4.6/80 V	58.88	> V_{in}	No	No	No	Capacitor charged by input inductor, requiring high-voltage diodes
CHB	4n	0	0	0	n	/	/	V_{in}	No	No	Yes	Series-connected two-level inverters, multiple isolated and balanced dc sources
1ϕ CMI Fig. 3(c)	4n	2n-1	2n-1	1	1	5×0.47/200 V	47	> V_{in}	Yes	Yes	No	SM using 4 switches and 2 diodes, SC voltage balancing
2ϕ CMI Fig. 3(d)	4n	2(n-1)	2(n-1)	1	1	4×0.47/200 V or 4×0.25/2000 V	37.6 or 20*	> V_{in}	Yes	No	No	SM using 4 switches and 2 diodes, requiring high-voltage diodes (2 > 1)
NPC	4n	2n	2n	0	1	/	/	/	Yes	No	Yes	Unbalanced dc-link voltage and requiring high-voltage diodes (n > 1)
FC	4n	0	2n	0	1	2×10/1100 V	18.15**	/	Yes	No	Yes	Non-uniform capacitors voltages require series-connected capacitors

Notes: "N.I." means no information; "/" not applicable; "*" simulation value; "**" excluding the dc-link capacitors [28].

higher. Similarly, the total *E* of the proposed CMI is relatively high compared to the conventional FC MLI [28]. Smaller capacitances can be used to reduce the total E if a lesser stringent voltage-ripple requirement is met.

B. Discussions on Voltage- or Power-Level Extension

The proposed single-source CMI can be extended for higher voltage-level operations with proper design and selection of the semiconductor devices. Since the maximum current (I_{inmax} + i_{omax}) arises in SM_1, it is feasible to apply the switches in SM_1 to other SMs for generating higher voltage levels. Switches in the rear-end SMs are however over-designed. Such a characteristic of the proposed CMI however does not render it less superior compared to the counterparts including the prior-art single-source CMIs [19], [20], and [23]. One common feature of these CMIs is that different currents/voltages are induced on switches in different SMs which share the same circuit structure. Therefore, different current-rating switches may be required to optimize the overall circuit for these CMIs.

In terms of a high-quality waveform, the feasibility of the proposed CMI for higher voltage-level extensions is thus not limited. Higher voltage-level (7, 9, 11, …) operations require higher voltage-rating diodes, which can be implemented by series-connected diodes similar to the conventional NPC MLI. As for power-level extension, however, unlike the multi-source CMIs whose total output power can be increased by increasing the number of SMs and their associated dc sources while maintaining the same voltage and current stresses, one limitation of the proposed single-source CMI is the operating power must be confined to the input power. It means scaling up the number of SMs does not necessarily enlarge the output power level. Raising the single input power necessitates an increase in the voltage or current rating of the devices. It is therefore imprudent to raise the output power by increasing the number of SMs indefinitely. Thus, the capability of the power-level extension of the proposed single-source CMI is indeed limited.

It is worth mentioning that for PV applications since the operating power of the inverter is confined to the maximum power point, it is reasonable to use and design a few SMs to achieve a boosted and regulated output voltage. Moreover, like any of the CMIs, the cascaded feature of the proposed CMI somewhat reduces the maintenance effort.

C. Component Design Consideration

Selections of the switches and diodes can be attained according to their voltage/current ratings. For the capacitors, their capacitances are designed according to the voltage-ripple requirements as mentioned in Section II.C. The design considerations of the input inductor are detailed below.

The boost inductor should ensure that it operates in the continuous conduction mode (CCM). In practice, the inductor current is coupled with high-frequency and low-frequency ripples. The high-frequency ripple during each carrier period is expressed as

$$\Delta I_{\text{HF}} = \frac{V_{\text{in}} d}{2 L_{\text{in}} \text{f}_\text{s}} \tag{35}$$

Assuming a constant shoot-through duty ratio is used in the LS PWM scheme, the voltage across L_{in}, when it is charged, is V_{in}. When it is discharged in series with the dc source to any of the capacitors (C_1 to C_4), the voltage across it (v_{L}) is coupled with a second-order harmonic. The low-frequency current ripple of the inductor is expressed as

$$\Delta i_L = \frac{1}{2L_{in}} \int_0^{1/(4\text{f}_\text{l})} v_L \, dt \approx \frac{1}{2L_{in}} \frac{1}{2} \left(\frac{\Delta V_c}{2} \frac{1}{4\text{f}_\text{l}} \right) = \frac{\Delta V_c}{32 L_{in} \text{f}_\text{l}} \tag{36}$$

Using Eqs. (35) and (36), the total current ripple of the input inductor is thus calculated with

$$\Delta I_{L,t} = \Delta I_{\text{Lin}} + \Delta i_{\text{L}} = \frac{V_{\text{in}} d}{2 L_{\text{in}} \text{f}_\text{s}} + \frac{\Delta V_c}{32 L_{in} \text{f}_\text{l}} \tag{37}$$

Assuming that the current-ripple requirement of L_{in} is $\Delta I_{\text{L,t}} < \alpha I_{\text{in}}$, the inductor is designed according to

$$L_{in} > \frac{1}{\alpha I_{in}} \left(\frac{V_{\text{in}} d}{2 \text{f}_\text{s}} + \frac{\Delta V_c}{32 \text{f}_\text{l}} \right) \tag{38}$$

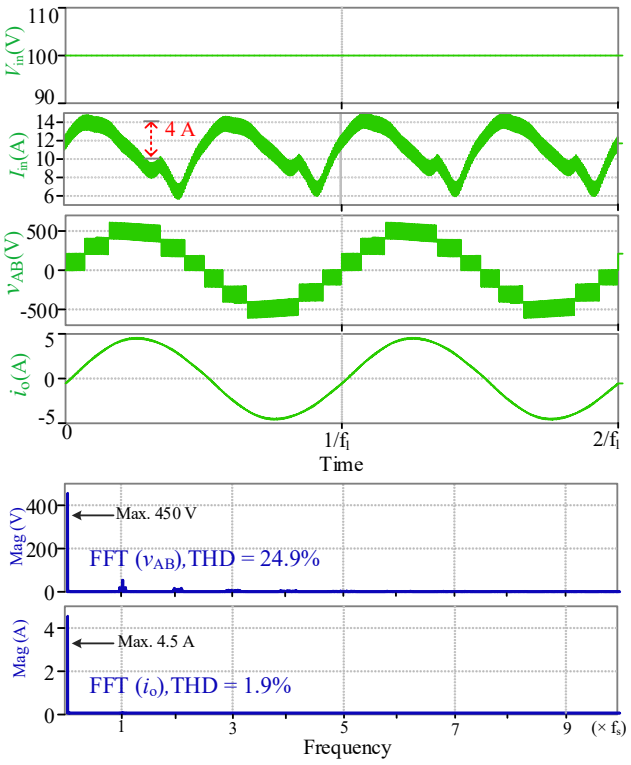

Fig. 11. Simulation results of 2ϕ seven-level inverters including input and output voltages (V_{in}, v_{AB}) and currents (I_{in}, i_o); FFT of v_{AB} and i_o, and their THD values considering high-frequency harmonics (up to 10f$_s$).

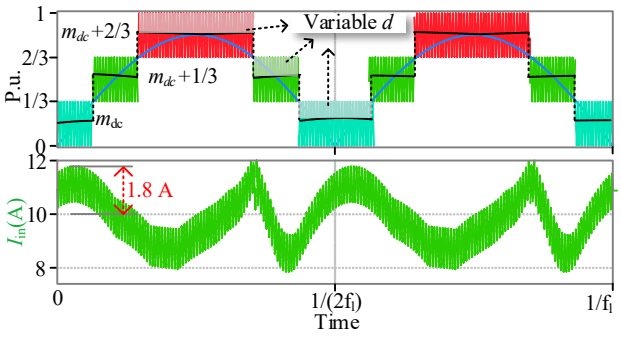

Fig. 12. Reduced input current ripple (ΔI_{in}) by a variable shoot-through duty ratio m_{dc}.

V. Simulation and Experimental Results

A. Simulation Results

The steady-state simulation results of the 2ϕ seven-level inverter are shown in Fig. 11. The inverter is fed by a constant dc source, while its ac output supplies an *RL* load (R = 100 Ω, L = 50 mH) with the nominal output power of 1 kW (f$_l$ = 50 Hz). It is seen that a boosted voltage with the peak value of 600 V is achieved from the 100-V input voltage. The THDs of output voltage and current are investigated through the fast Fourier transform (FFT). The THD of the seven-level output voltage is 24.9%, while the THD of the output current is very low at 1.9% due to the filtering effect of the loading inductance. It is seen that the instantaneous input current of the inverter is coupled with a relatively larger ripple of 4 A due to the single-phase

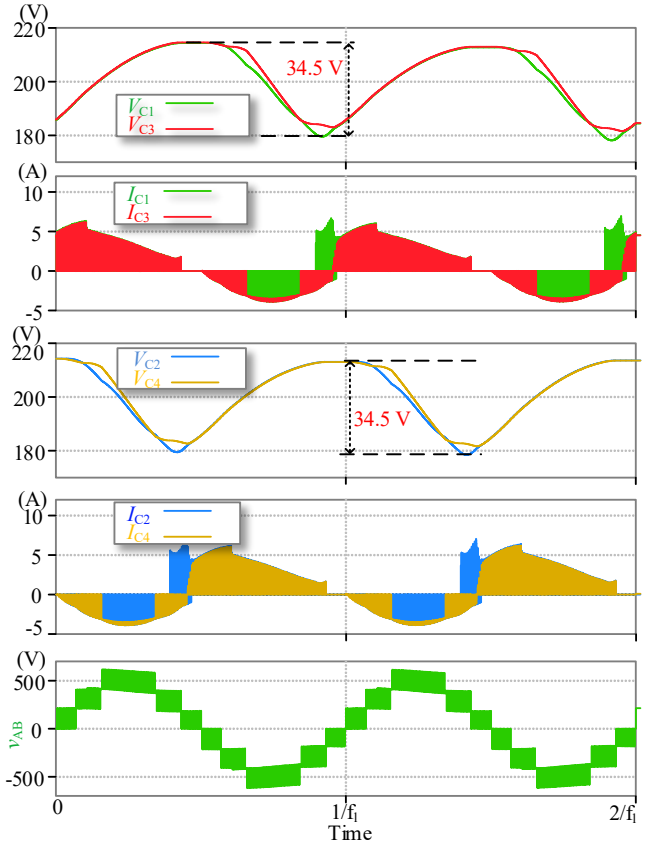

Fig. 13. Simulated voltages and currents of the capacitors C_1 to C_4.

pulsating output power which fluctuates at the double-line frequency. To reduce the low-frequency current ripple, a modified M_{dc} is considered for generating a variable shoot-through duty ratio as shown in Fig. 12, where m_{dc} = 0.16 − 0.01(1−cos(4πf$_l$t)) is used. The ripple current is then reduced to 1.8 A. In addition, power decoupling techniques using additional active or reactive components or control strategies can also be considered to remove the low-frequency input current ripple of a single-phase inverter [26], [29], which being general, is not shown here.

The voltages and currents of capacitors C_1 to C_4 are shown in Fig. 13. Under the nominal operating power, the voltage ripples of four capacitors are kept at a similar level at 17.25 V, which is close to the theoretical calculations presented in Fig. 7. It is evident that capacitors C_1 and C_3 are charged during the positive half-cycle while C_2 and C_4 are charged during the negative half-cycle, which confirms again the theoretical analysis presented in Section II.C. The voltage ripples of capacitors C_3 and C_4 are equal, slightly less than those of C_1 and C_2. The voltages across all capacitors are balanced automatically at the same average value around 200 V. Furthermore, the average/maximum currents of capacitors are close, simplifying the designs and selection of capacitors.

Nevertheless, the current stresses of switches are indeed different as shown in Fig. 14. The maximum and rms values of currents are summarized in Table II. As seen, the maximum current of switches in SM$_1$ is 15.9 A. As expected, the rms currents of switches are not the same either. The switch S_{11} is loaded by the maximum rms current at 6.3 A, while the rms

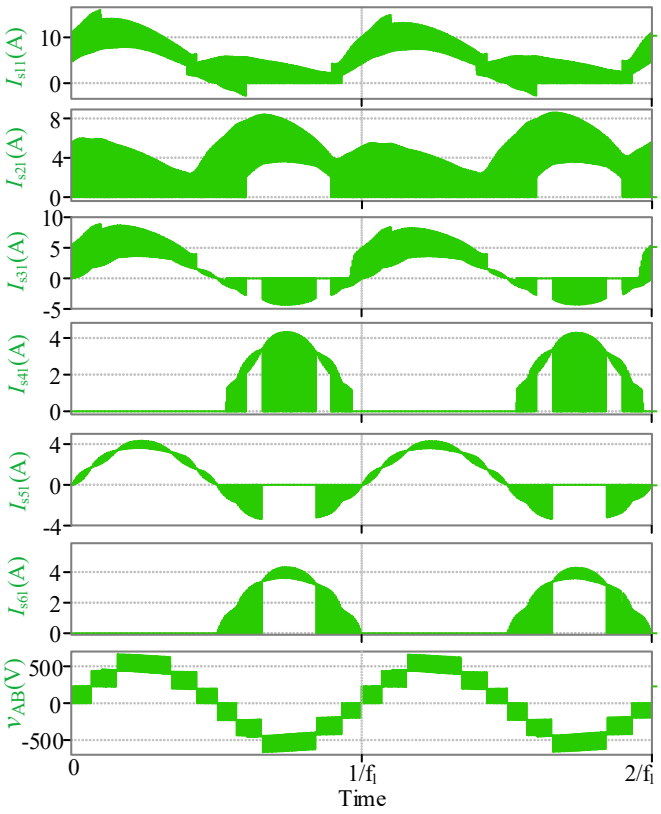

Fig. 14. Simulated currents of switches S_{11} to S_{61} of phase A.

TABLE II
MAXIMUM AND RMS CURRENTS UNDER NOMINAL OUTPUT POWER

Switches	S_{11} / S_{12}	S_{21} / S_{22}	S_{31} / S_{32}	S_{41} / S_{42}	S_{51} / S_{52}	S_{61} / S_{62}
Max. (A)	15.9	8.6	8.9	4.3	4.3	4.3
RMS (A)	6.3	4.1	3.5	1.8	2.2	1.8

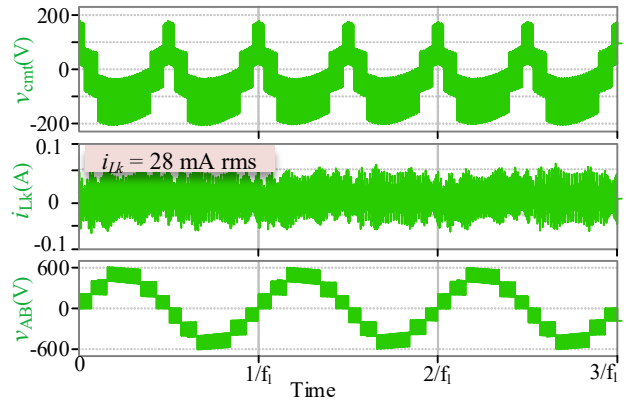

Fig. 15. Simulated common-mode voltage (v_{cmt}) and the leakage current (i_{Lk}) under the operating power of 1 kW.

currents of switches S_{21} and S_{31} are 4.1 A and 3.5 A, respectively. The remaining three switches are loaded with a similar current of around 2 A. Another observation made is that although the maximum current of switches is larger than the average of the input current (10 A), its rms value is smaller.

To examine the feasibility of the proposed CMI for transformerless grid applications, a small capacitor (50 nF) is used to simulate C_p (see Fig. 9). It is connected between the ac neutral and the negative terminal of the dc source with a nominal power of 1 kW. The stray inductance of the ground is assumed to be 1 uH. Additionally, the total common-mode filter used at the input and output is 20 mH [27]. Simulation results are shown in Fig. 15. As seen, the common-mode voltage matches well with the analysis in Section III.D. The leakage current is not zero, but at a low level with the peak value of 58 mA and rms value of 28 mA, which is compatible with the grid codes [27]. It is, therefore, able to apply the proposed CMI to transformerless grid application, especially considering its step-up feature which is further tested through experiment.

Table III
SPECIFICATIONS OF THE EXPERIMENTAL PROTOTYPE

Voltage ratings	V_{in} = 100 V, Max. v_{AB} = 600 V, 50 Hz, 1 kW
Switches	IRF300P227 (300 V, 50A, R_{on} = 0.04Ω)
Diodes	D_1/D_2: DPG60I300HA (300 V, 60A, V_{Fd} = 1.4 V) D_3/D_4: DPG60I300HA × 2
Capacitors	C_1 to C_4 0.47 mF each
Inductors	Input L_{in} = 3 mH; filter L_f = 2 mH;
PWM variables	M_{ac} = 0.8; M_{dc} = 0.16; f_s = 10 kHz

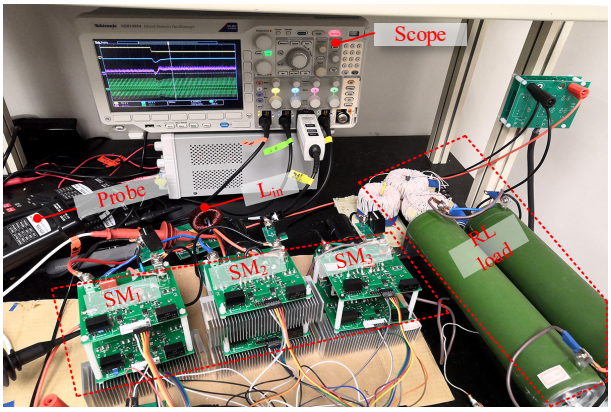

Fig. 16. Photographs of the experimental prototype.

B. Experimental Results

To verify the feasibility of the proposed CMI, two downscale experimental prototypes (1ϕ and 2ϕ) are built and tested. Results obtained from the 2ϕ seven-level inverter are shown here in comparison with the simulations. The components used in the experiment are listed in Table III. A constant dc source (V_{in} = 100 V) is used as the input of the inverter, while an *RL* load (R = 100 Ω, L = 50 mH, see Fig. 16) is connected to the output through a filter inductor L_f (2 mH). The inductor-charge duty ratio for the 2ϕ seven-level prototype is d = 0.52 (M_{dc} = 0.16). Additionally, its ac modulation ratio used is M_{ac} = 0.8. The carrier frequency of the LS PWM scheme is 10 kHz. Steady-state experimental results are shown in Figs. 17−19. Experimental data are also captured and can be rebuilt using *Matlab* to increase the readability.

The key input and output waveforms are shown in Fig. 17(a), where the output voltage feature seven discrete voltage levels with the maximum value of |±600| V obtained from the 100-V dc source. The harmonic contents (up to 40th order) of the output voltages are tested with the maximum value of the third-order harmonic at 9.18 V rms. Furthermore, due to the filtering effect

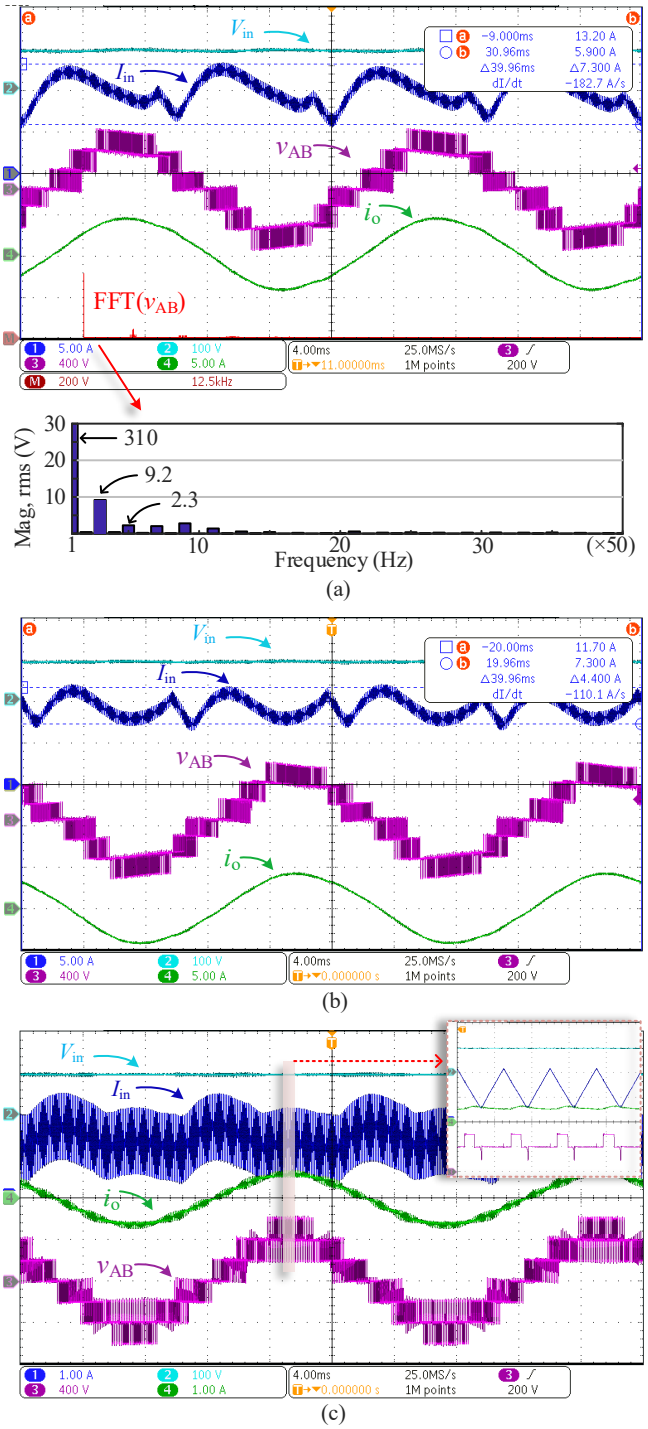

Fig. 17. Steady-state experimental results including (a) input voltage V_{in} (100 V/div), input current I_{in} (5 A/div), output voltage v_{AB} (400 /div), and output current i_o (5A /div), FFT test of the output voltage, low-order harmonics (up to 40th order) measured by the scope; (b) key waveforms with reduced input current ripple; (c) waveforms under light load condition (100 W).

of the loading inductance, the tested THD of the output current is very low at 1.74%. The input current couples a low-order ripple, which can be reduced by using a modified PWM signal m_{dc} that produces a variable shoot-through duty ratio as shown in Fig. 17(b). The results obtained match well with the simulations shown in Fig. 12.

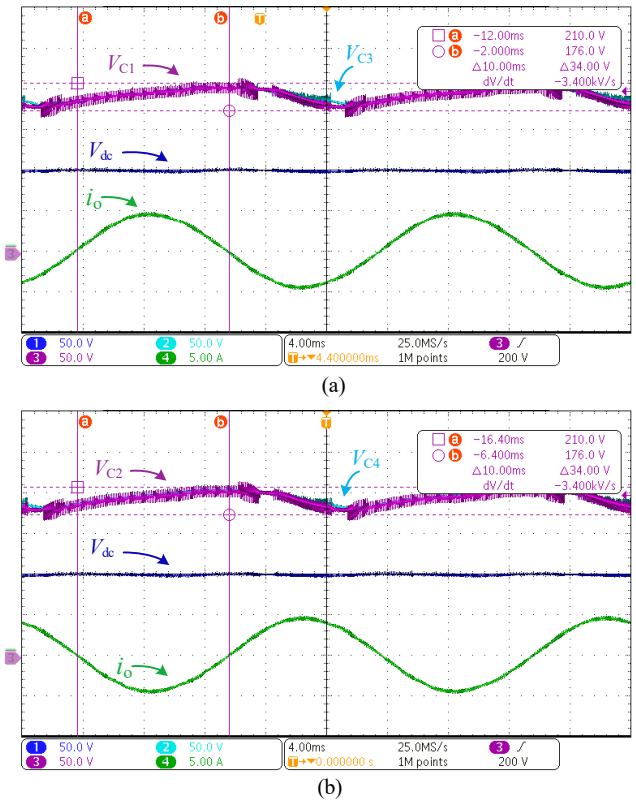

Fig. 18. Steady-state (a) capacitors' voltages V_{C1} (50 V/div), V_{C3} (50 V/div) input voltage V_{in} (50 V/div) and output current i_o (5 A/div), and (b) capacitors' voltages V_{C2} (50 V/div), V_{C4} (50 V/div) input voltage V_{in} (50 V/div) and output current i_o (5 A/div).

The voltage and current waveforms are also measured under the light load condition (100 W) as shown in Fig. 17(c). It is observed that when the inductor discharges and $I_{in} = i_o$ is met, the output voltage drops, which agrees with the analysis described in Section II.A. Such durations are relatively small since L_{in} is charged and its current increases subsequently. The output sinusoidal current is not distorted under such a condition and the THD of the output current measured is 3.9%.

The voltages of capacitors are measured and shown in Fig. 18. It is seen that their voltages are balanced at the same average value. While capacitors C_1 and C_3 are charged during the positive half-cycle, C_2 and C_4 are charged during the negative half-cycle as shown in Fig. 18(b). Nevertheless, their voltage ripples are maintained at a similar level at about 17 V under the nominal output power. These results therefore match with the simulations, confirming again the theoretical analysis. Furthermore, since all the capacitors are charged directly by the input current, the currents flowing through them are relatively smooth, which is evaluated by testing the switch currents.

To illustrate, the current waveforms of switches in phase A are measured and shown in Fig. 19. The switches in the rear-end side (e.g., S_{51} to S_{61}) conduct only the ac output current, whose peak currents, and thus the rms currents are smaller as shown in Fig. 19 (b). Other switches (e.g., S_{11} and S_{21}) need to conduct capacitor-charging currents and the output current, and therefore, their current ratings are relatively large, as shown in Fig. 19(a). Nonetheless, the conducting currents of switches are in accordance with their simulation results shown in Fig. 14.

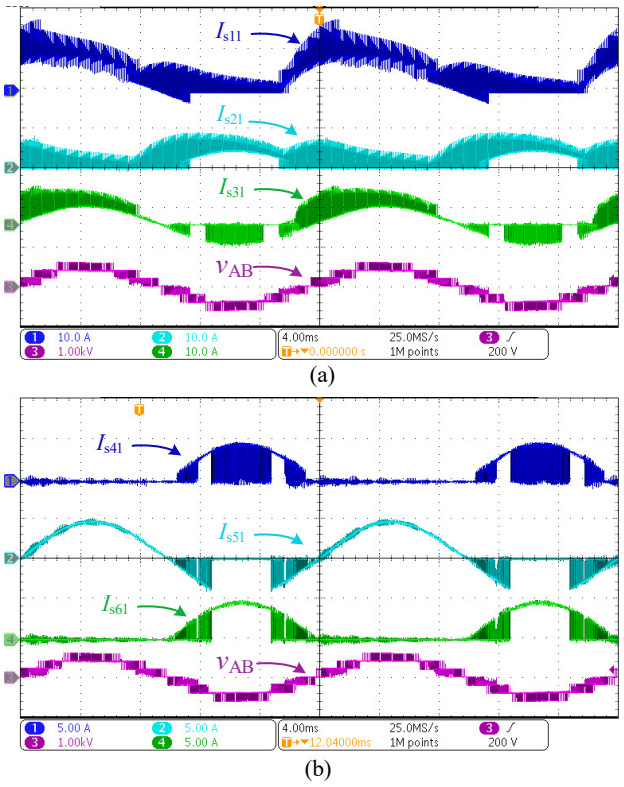

Fig. 19. Steady-state (a) switches currents I_{s11} (10 A/div), I_{s21} (10 A/div) and I_{s31} (10 A/div) and (b) I_{s41} (5 A/div), I_{s51} (5 A/div) and I_{s61} (5 A/div); output voltage v_{AB} (1 kV/div) is used as common reference in both captures.

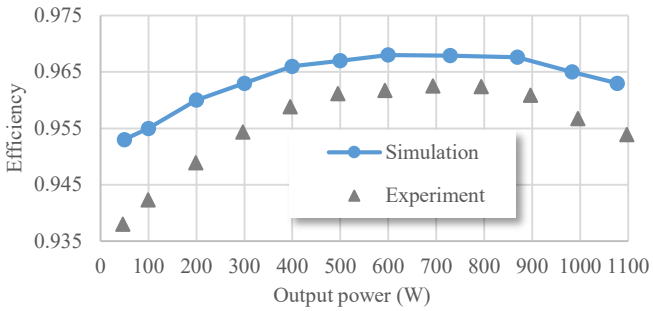

Fig. 20. Experimentally measured efficiency under different power levels (V_{in} = 100 V, V_{omax} = 600 V) in comparison with the simulated values.

The maximum switch current arises in SM_1 ($I_{in} + i_{omax}$), agreeing with the theoretical analysis.

The steady-state efficiency versus output power is measured and shown in Fig. 20. During the experimental tests, the digital power analyzer *WT333E* is used for measuring the input and output power concurrently. By varying the loading resistance R, different sets of data corresponding to different input (P_{in}) and output (P_o) powers are tested and the efficiency is calculated with $\eta = P_o/P_{in}$. As seen from Fig. 20, the measured efficiency is close to the simulated value (differences mostly within 0.5%). It increases steadily as the operating power rises at lower power levels. The maximum efficiency achieved is 96.3% at P_o = 690 W. After reaching the maximum value, the efficiency curve begins to fall. Nonetheless, under a wide range of output power,

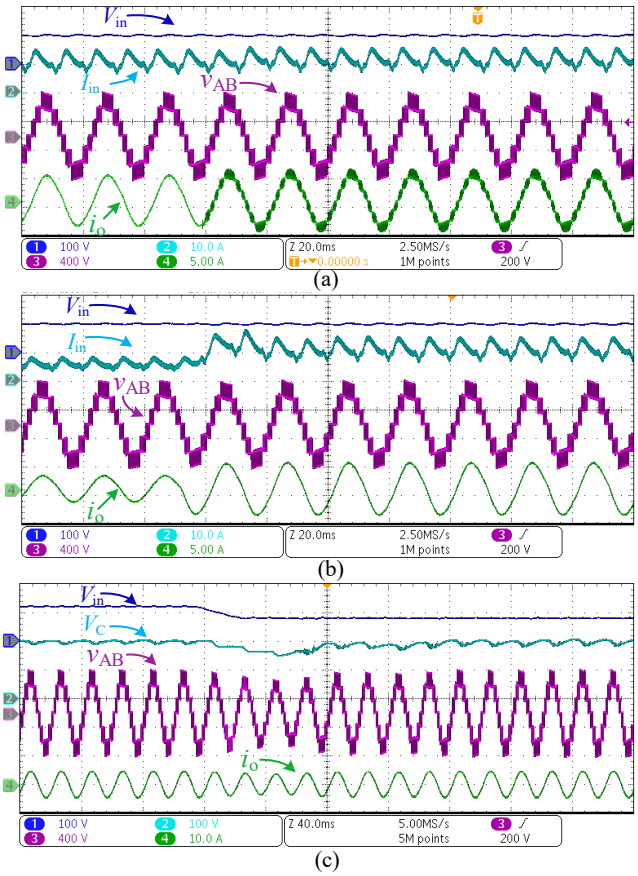

Fig. 21. Dynamic responses of the 2ϕ prototype under (a) a transient from an inductive load to a resistive load, (b) from half-load to full-load, and (c) a step-change of V_{in} from 120 V to 80 V.

the obtained data is well above 95%, demonstrating a high-efficiency dc-ac voltage-boost power conversion.

For verifying the stable operation of the proposed CMI under different loading conditions, the dynamic results of the prototype are tested and detailed in Fig. 21. Fig. 21(a) and (b) show the transient results of the inverter from an inductive load to a resistive load and from half-load to full-load condition. During these transients, the inverter operates properly. Furthermore, to illustrate the voltage regulation of the proposed CMI, the voltage of each series-connected SM and the total output voltage are sensed and a voltage closed-loop control is used to regulate the voltages of the capacitors. A sudden change in the input voltage from 120 V to 80 V is applied, which causes an under-shoot voltage across capacitors. Correspondingly, the output voltage sags during the transient before it returns to its nominal value within several cycles (Fig. 21(c)). Regulation of the ac voltage is achieved, and the proposed CMI can, therefore, operate with a varied dc source while at the same time providing a regulated output voltage.

Overall, the downscale experimental tests confirm the theoretical analysis and demonstrate the advantages of the proposed single-source CMI. Due to the constraint of the prototypes, higher voltage operations of the proposed CMI are not experimentally tested. Instead, a scale-up (voltage and current 10 times scaled up) PV power generation is simulated and discussed in the following.

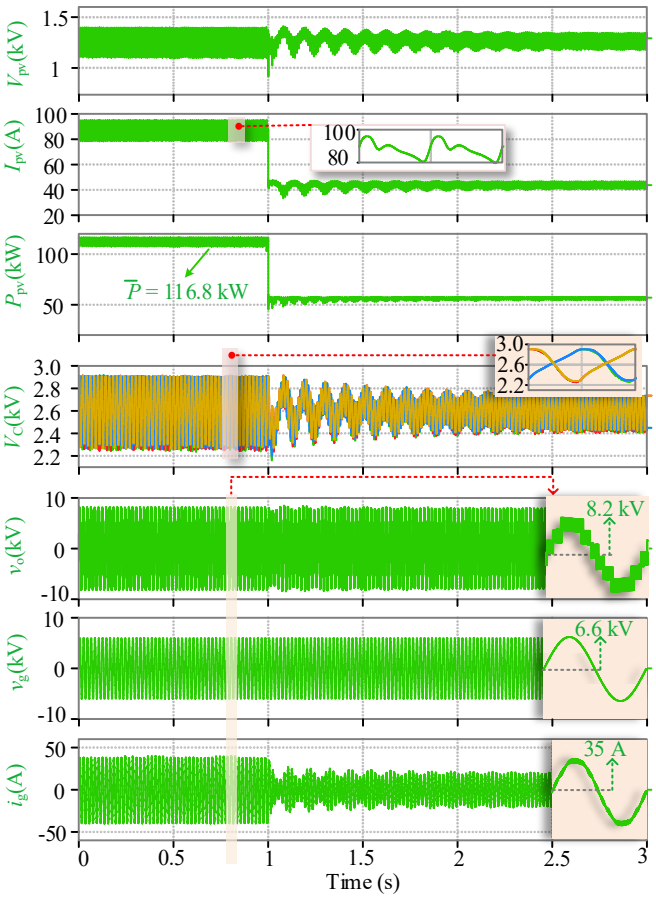

Fig. 22. Simulation results of the MV PV power generation including PV voltage V_{pv} and power P_{pv}, SM capacitor voltage V_C, output voltage v_o, grid voltage v_g, and current i_g under a step-change of the PV irradiance.

C. Simulation of A Scale-up PV Power Generation

A PV power generation system based on a 2ϕ seven-level inverter is studied through *MATLAB/PLECS* co-simulation environment. The PV source is realized by series and parallel connections of PV modules *JKM360M-72-V*. The maximum-power-point (MPP) PV voltage is at about 1.3 kV. A 0.25-mF capacitor is considered for each capacitor (15% ripple requirement), while the input and output line inductors are assumed to be 5 mH. The parasitic resistance of each reactive component is assumed to be 0.1 Ω for loss estimation. Note that since galvanic isolation is usually required in the point of coupling for interfacing with MV grid, the parasitic capacitance and leakage current issues in transformerless PV systems are not considered in the MV simulation.

Under the steady-state operation, the steady-state average voltages across capacitors are boosted to be about 2.6 kV. As a consequence, a step-up seven-level output voltage is produced and the amplitude of the fundamental component of the total output voltage is boosted at 6.6 kV. The peak-to-peak value of the PV current simulated is 14 A (average I_{pv} 86 A), which means the PV current ripple is less than 10% of its average current. The average output power of the PV source ($\overline{P}_{pv}$) is 116.8 kW out of its maximum power of 117.5 kW. The simulated maximum-power-point-tracking (MPPT) efficiency is thus 99.4%. A step-change in the PV irradiation is applied

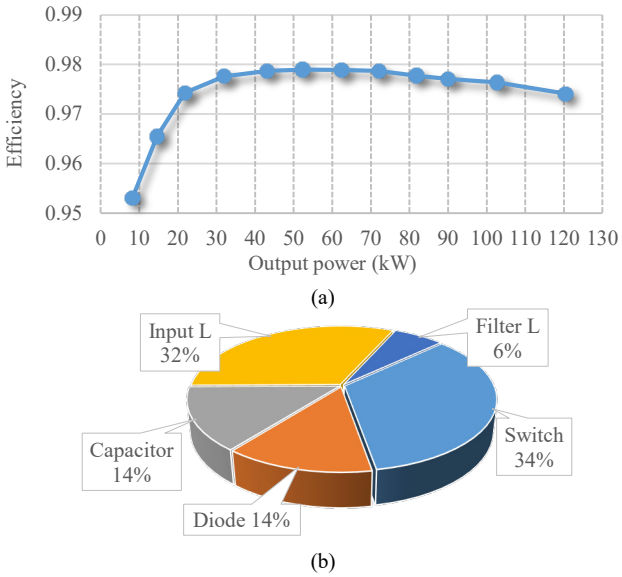

Fig. 23. Simulated (a) efficiency of the scale-up 2ϕ inverter for MV PV applications (V_o = 6.6 kV) and (b) the total loss (2488.1 W) breakdown under output power 100 kW.

which causes the output voltage/power of the PV source to reduce as shown in Fig. 22. During the transient, the output voltage (v_{AB}) keeps steady, while the current injected to the grid (i_g) reduces in accordance with the variation of the input PV power, thereby, maintaining MPPT.

The power losses and efficiency of the proposed CMI are simulated considering the semiconductor power module *SKM450GB33F* (including IGBT and diode) operating under a 2-kHz switching frequency. Its specific loss data are used to evaluate the losses of the switches and diodes. The simulated efficiency under different operating power is depicted in Fig. 23(a), where it can be seen that the efficiency across a wide range of operating power is larger than 97%. The total loss breakdown of the inverter under the rated power of 100 kW is also given in Fig. 23(b). The semiconductor switches cause the largest power loss, taking up 34% of the total loss. The input inductor consumes the second largest proportion of power since for a boost converter/inverter the input current (≈100 A) is several times larger than the output current. Nonetheless, with its boosted output voltage, the proposed CMI, therefore, provides a promising solution for a single-stage MV PV power generation using a single dc source.

VI. Conclusion

A novel CMI fed by a single dc source is proposed, which reduces the requirement of dc sources for boost dc-ac multilevel voltage synthesis. The proposed inverter is conditioned by an input inductor that operates with shoot-through charging and discharges with a boosted voltage to the SMs. The capacitors in each SM are smoothly charged by the inductive input current. A 2ϕ symmetrical structure is presented and assisted by the LS PWM scheme to keep voltages of capacitors balanced in addition to producing a suitable inductive-charge duty ratio and voltage gain. The voltage and current ratings of the devices are analyzed, which shows that the proposed CMI is able to be extended for higher voltage-level operations using the same

circuit structure but with different current-rating switches and additional diodes. Furthermore, a qualitative comparison with the prior-art CMIs is given to illustrate the advantages of the proposed CMI. Simulations and experimental results obtained from downscale inverter prototypes have demonstrated the characteristics of the proposed CMI. In addition, the feasibility of the proposed CMI for MV applications has been tested through simulation of a single-source PV inverter producing a boosted ac voltage for interfacing with the MV grid.

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