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Online Capacitance Monitoring for DC/DC Boost Converters Based on Low-Sampling-Rate Approach

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***Abstract*—Aluminum Electrolytic Capacitor (Al-Cap) is widely used in dc/dc converters to suppress voltage ripple and store energy to stabilize the output voltage. However, Al-Cap is one of the most vulnerable parts in power electronic converters, and its capacitance (*C*) is an important parameter for indicating the health status. For the purposes of condition monitoring, small-signal voltage and current ripples are usually used to estimate the capacitance of Al-Caps. Unfortunately, the ripples of dc/dc converters have the features of small amplitude and high frequency, which increases the complexity for data acquisition and processing. Moreover, the amplitude of ripple changes as the operation condition of converters changes (e.g., the load changes), and it will increase the complexity of sampling circuits. Considering this issue, this paper proposes a transient charging profile-based capacitance estimation scheme for dc/dc boost converters, which aims to reduce the sampling frequency. Taking a 24−48-V boost converter as a case study, simulation and experimental results demonstrate the feasibility of the proposed scheme for converters with different operating conditions and circuit parameters, and the estimation error is less than 3%.**

***Index Terms*—Aluminum electrolytic capacitor (Al-Cap), condition monitoring (CM), capacitance, transient charging profile.**

I. Introduction

DC/DC boost converters are widely used in step-up conversion applications, such as dimmable LED arrays, navy and spacecraft power supplies [2], etc. In such applications, the converter always operates in uncertain conditions with dynamic loading and variable input. Taking a boost converter for space applications as an example, Fig. 1 shows its typical loading profile [3], [4]. Usually, large-capacity low-cost aluminum electrolytic capacitors (Al-Caps) are employed to absorb the current ripple and store energy to stabilize the output voltage during input or load transients [5]. However, Al-Cap is one of the weakest components in converter systems. For reliability reasons, it is essential to monitor the health status of Al-Caps and schedule maintenance before a serious breakdown occurs [6], [7].

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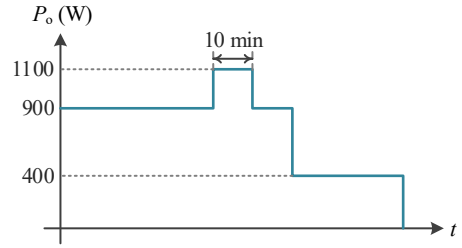

Note: The converter shall have the capability to provide a repetitive instantaneous peak power of 1100 W during 10 min/orbit.

Fig. 1. An example of frequent load perturbation in dc/dc boost converters for space applications, where 10 min is a typical value [3], [4].

Usually, capacitance (*C*) and equivalent series resistance (ESR) are chosen as the health indicators of Al-Caps. Once *C* has reduced to 80% and/or ESR increased to 2.8 times the initial values, the Al-Cap is considered to be failed [8]. Based on this, some efforts have been made to realize the condition monitoring (CM) for Al-Caps in dc/dc converters. One commonly used approach is to estimate *C* and/or ESR based on the relationship between steady-state ripples and capacitor parameters. In [9]−[13], capacitor current ripples were directly sampled to estimate ESR and/or *C*, here, oscilloscopes' current probes [9], [10] and specially designed current sensors [11]−[13] were employed to obtain the high-frequency current ripples. To avoid using a capacitor current sensor, Amaral *et al.* used the input current and output voltage ripples to estimate the ESR of a buck converter based on the operation model [14]. Similarly, *C* and/or ESR could be derived from the output voltage and inductor current of buck converters [15]−[17] and boost converters [18]−[20].

The estimation models of the above-mentioned steady-state ripple-based methods are simple. However, the steady-state ripples of a dc/dc converter have the characteristics of high frequency and small amplitude. In order to accurately sample the ripples, specially designed high-bandwidth current sensors [11]−[13], ripple extraction circuits [20], and high-speed sampling devices [9]−[20] were required (e.g., the sampling frequency was more than 300 times of the switching frequency of converters in [20]), which increases the complexity of data acquisition. Besides, powerful data processing tools, such as personal computers (PCs), were required to process a large amount of ripple data. Although Yao *et al.* [21]−[23] sampled the output voltage at several particular instants of one switching cycle to reduce the sampling frequency, additional ripple extraction circuits and pulse capture circuits were needed. To avoid using a pulse capture circuit, Ahmad *et al.* [24] applied a similar scheme in a digital-controlled boost converter, however,

additional ripple extraction circuits were still required. Moreover, considering the variation of the ripples amplitude depending on the converter loading condition would further increase the complexity of the sampling circuits.

Another approach is based on the circuit model or transfer function model of converters. In [25], an adaptive model observe-based method was proposed to estimate the circuit parameters of a PV buck converter. Similarly, hybrid model and modified hybrid model-based methods were presented in [26]−[28] to monitor the parameters degradation of dc/dc converters. The above-mentioned methods could realize the CM of all the passive components in converters. However, high-rate sampling devices and powerful data processing tools were also required to obtain the circuit model. In [29]−[31], a pseudo-random binary sequence was injected into the duty cycle to realize the full-parameters monitoring of converters based on the transfer function model. Unfortunately, substantial time was needed to run the complex identification algorithm, which limits its application in high-frequency dc/dc converters (the switching frequencies of the converter in [29]−[31] were 20 kHz).

To reduce the sampling frequency and computational complexity of Al-Cap monitoring, some large-signal transient trajectory-based methods were proposed for CM of capacitors in dc/dc converters. In [32], an output voltage transient analysis-based scheme was proposed for a full-bridge converter. However, an accurate estimation model for ESR and/or C has not been provided. Considering this issue, Zhao *et al.* proposed a large-signal load transient trajectory-based method to monitor the Al-Caps in buck converters [33]. Unfortunately, there exists some limitations to apply it in boost converters:

1) The parameters estimation method is based on the case that the duty cycle of buck converters is approximately equal to 0 or 1 during load transients. However, different from the buck converters, boost converters have one right half plane zero, which limits the duty cycle from reaching 0 or 1 during transients. Therefore, the introduced calculation model is not applicable for boost converters.
2) Only load transient is considered for capacitor monitoring, which does not prove the feasibility of CM based on the input perturbation.
3) Additional transient detection circuits are required, which increases the hardware cost and introduces new reliability risk.

To verify the applicability of transient-profile-based CM schemes in converters with one right half plane zero and to overcome the above-mentioned limitations, this paper presents a low-sampling-rate transient charging profile-based capacitance monitoring scheme for dc/dc boost converters. Considering a microcontroller unit (MCU) is widely used in CM systems to realize the parameter estimation, which can also be used for the control purpose. Hence, a digital controlled dc/dc boost converter is built to verify the proposed CM scheme. The main contributions are given as follows.

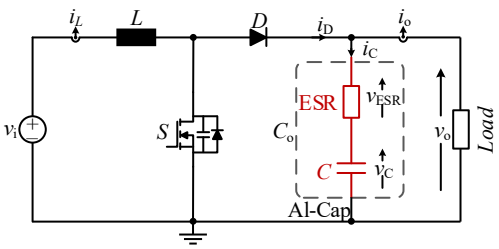

Fig. 2. Main circuit of a dc/dc boost converter.

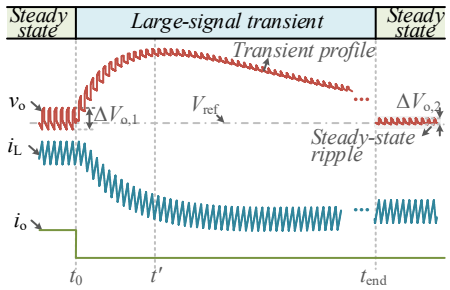

Fig. 3. Unloading transient response waveforms of v_o, i_L, i_o (t_0 and t_{end} are the start and end instants of the transient, t' is the end instant of the voltage-rise period, $\Delta V_{o,1}$ and $\Delta V_{o,2}$ are the peak-to-peak values of the voltage ripple at different powers).

1) The relationship between capacitance and transient charging profile of boost converters is analyzed and a capacitance estimation model is built.
2) The single-rate sampled signal for control purposes is also used for CM, which does not need additional ripple amplification circuits and high-frequency sampling devices.
3) The proposed scheme is feasible for both input and output perturbations, and its feasibility is verified on converters with different parameters and operating conditions.

The rest of this paper is organized as follows: Section II describes the background of the proposed scheme. The proposed capacitance monitoring scheme is introduced in Section III. Simulation and experimental studies are presented in Section IV and Section V. Section VI analyzes the robustness and provides a comparison between the proposed scheme and the existing schemes. Finally, conclusions are drawn in Section VII.

II. Background

Fig. 2 shows the main circuit of a conventional dc/dc boost converter consisting of a power switch S, a power diode D, an inductor L, and an output filter capacitor C_o (Al-Cap), where C_o is equivalent to a series connection of a pure resistance ESR and a pure capacitance C. i_L, i_D, i_C, i_o, v_o represent the inductor current, diode current, capacitor current, load current, and output voltage, respectively. v_{ESR} and v_C indicate the voltage components across the ESR and C, respectively.

Taking an unloading transient as an example, Fig. 3 shows the transient response waveforms of v_o, i_L, and i_o. Before the instant t_0, the converter works in steady state and v_o equals to the reference voltage V_{ref}. At t_0, a negative current step occurs and the converter starts to work in a transient. Assuming v_o recovers to V_{ref} and the converter reaches a new steady state at the instant t_{end}. One can see the transient voltage profile has the

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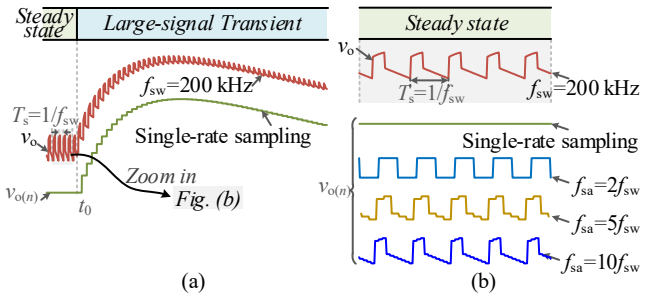

Fig. 4. Sampling waveforms of transient voltage profile and steady-state ripple (v_o ,$v_{o(n)}$, T_s, f_{sw}, f_{sa} represent the output voltage, sampled output voltage, switching cycle, switching frequency, sampling frequency, respectively). (a) Transient voltage profile. (b) Steady-state ripple.

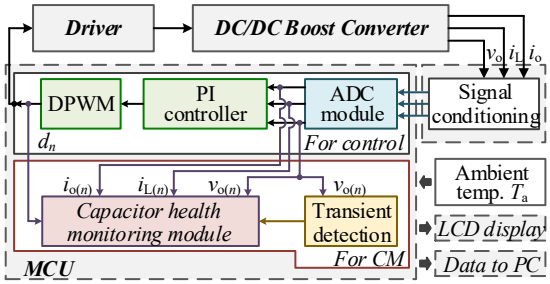

Fig. 5. DC/DC boost converter with the proposed monitoring scheme ($v_{o(n)}$, $i_{L(n)}$, $i_{o(n)}$ represent the sampling signals of v_o, i_L, and i_o, d_n is the duty cycle).

characteristics of large amplitude and long time scale when compared with the high-frequency small-amplitude steady-state waveforms.

To compare the difference of the sampling of steady-state ripples and transient profile, Fig. 4(a) shows the sampling waveforms of transient voltage profile and steady-state ripples, where v_o, $v_{o(n)}$, T_s, f_{sw}, f_{sa} represent the output voltage, sampled voltage, switching cycle, switching frequency, sampling frequency, respectively. Assuming the switching frequency f_{sw} = 200 kHz, it is found that the sampling signals $v_{o(n)}$ can represent the transient trajectory of v_o when using a single-rate sampling (usually for control). However, the sampling signal cannot represent the steady-state ripple in this case.

Fig. 4(b) shows the enlarged sampling waveforms of steady-state ripple. Here, three different sampling frequencies f_{sa} are employed, i.e., f_{sa} = 2f_{sw}, f_{sa} = 5f_{sw}, and f_{sa} = 10f_{sw}. It is easily found that $v_{o(n)}$ can accurately represent the steady-state voltage ripple only in the case that $f_{sa} \geq 10f_{sw}$. Moreover, referring to Fig. 3, it is known that the peak-to-peak value of the steady-state ripple ΔV_o changes as the load current changes, i.e., $\Delta V_{o,1} \neq \Delta V_{o,2}$, which increases the design difficulties of ripple extraction circuits.

Therefore, it is relatively easy to sample the transient profile rather than to sample the steady-state ripple. The main idea of the proposed monitoring scheme is to use the large-signal long-time-scale transient profile to online estimate the capacitance of Al-Caps, which does not need a relatively high sampling frequency.

III. Proposed Online Capacitance Estimation Scheme

The proposed capacitance monitoring scheme is shown in Fig. 5. Usually, the microcontroller unit (MCU) is used for digital control. Once a transient is detected, the MCU starts to

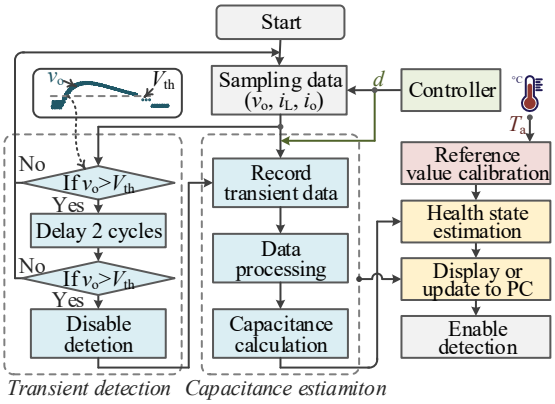

Fig. 6. Flowchart of the online capacitance monitoring scheme (V_{th} is the threshold voltage).

run the proposed CM algorithm. Here, the transient is detected based on the comparison results of the output voltage and the designed threshold voltage V_{th}, as shown in the monitoring flowchart in Fig. 6. In order to sample data during the voltage rise period, V_{th} should be larger than V_{ref}, i.e., $V_{th} > V_{ref}$. Actually, a whole process of capacitance estimation is considerably short compared with the transient occurrence period (e.g. 10 min, as shown in Fig. 1) and capacitor aging [23]. Therefore, the threshold voltage V_{th} can be stetted relatively large (e.g. $V_{th} > V_{ref} + 4$), and a transient with a relatively large amplitude is selected for CM.

In the proposed scheme, the voltage-rise period during transients (c.f., the period t_0–t' in Fig. 3) is chosen to estimate C. Referring to Fig. 6, when a transient occurs, the MCU starts to record the transient data $v_{o(n)}$, $i_{L(n)}$, $i_{o(n)}$ from the analog-to-digital conversion (ADC) module, and the duty cycle d_n from the controller, in order to estimate C. Here, $v_{o(n)}$, $i_{L(n)}$, $i_{o(n)}$ represent the sampling signals of v_o, i_L, and i_o, respectively. At the same time, the ambient temperature T_a is sampled for the health status assessment, which is measured using the internal temperature sensor of the MCU.

Notice that two times comparison are introduced to avoid an error trigger of CM in the proposed scheme. And the transient detection function is disabled when one transient is detected, in order to ensure the sampling and calculation are not affected by other processes, such as the next transient or the voltage ringing.

A. Capacitance Estimation Model

Fig. 7 gives the detailed transient waveforms of two switching cycles during the voltage rise period (i.e., the period from t_0 to t' shown in Fig. 3). Before the instant t_0, the converter works in steady state. At t_0, a transient occurs, the controller starts to recover the output voltage v_o. Assuming at arbitrary instant t_1, the converter operates in a new switching cycle (defined as Transient Period I and the duty cycle is d_1). The switch S turns ON and the diode D turns OFF. The inductor current i_L rises with the slope of v_i/L, here, the diode current i_D = 0 and the capacitor starts to discharge. At t_2, S turns OFF, the capacitor ends discharging. After the period of $(1-d_1)T_s$, the switch S turns ON again at t_3. The converter operates in a new transient period (i.e., Transient Period II) and the duty cycle is defined as d_2.

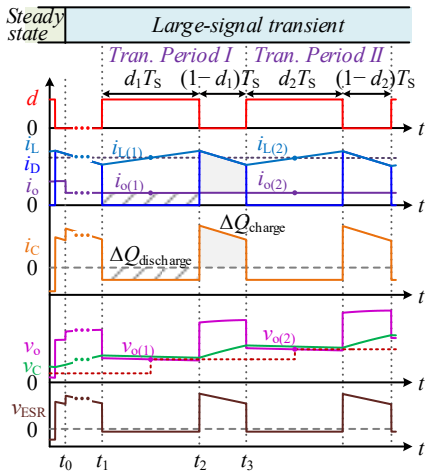

Fig. 7. Detailed transient response waveforms of two transient switching cycles (t_0 is the start instant of a transient, t_1, t_3 represent the start and end instants of Transient Period I, t_2 is the turn-OFF instant of the switch).

In Fig. 7, $\Delta Q_{discharge}$ and ΔQ_{charge} are the discharge and charge areas during Period I. $v_{o(1)}$, $i_{L(1)}$, and $i_{o(1)}$ represent the sampling signals of v_o, i_L, and i_o during Period I, respectively. $v_{o(2)}$, $i_{L(2)}$, and $i_{o(2)}$ are the sampling signals during Period II. Notice that the sampling frequency equals to the switching frequency. To avoid a sampling error at the switching instant, the signals are sampled at the middle instant of the switch S turns ON. In order to analyze the voltage variation during transients, the following symbols are defined. $\Delta v_{C,[t1,t2]}$, $\Delta v_{C,[t2,t3]}$, $\Delta v_{C,[t1,t3]}$ represent the voltage variation of v_C during the periods t_1–t_2, t_2–t_3, and t_1–t_3. $\Delta v_{ESR,[t1,t3]}$, $\Delta v_{o,[t1,t3]}$ are the voltage variation of v_{ESR} and v_o during the period t_1–t_3,

From Fig. 7, the charge released from the capacitor during t_1 to t_2, i.e., the area of striped shadow region is calculated as

$$\Delta Q_{discharge}=\int_{t_1}^{t_2} i_C(t)\mathrm{d}t=\int_{t_1}^{t_2}\left|i_D(t)-i_o(t)\right|\mathrm{d}t=\int_{t_1}^{t_2} i_o(t)\mathrm{d}t. \quad (1)$$

Using the sampled load current $i_{o(1)}$ to represent the actually load i_o during Transient Period I, (1) can be expressed as

$$\Delta Q_{discharge}=(t_2-t_1)i_{o(1)}=d_1\cdot T_S\cdot i_{o(1)}. \quad (2)$$

Due to the discharge of the capacitor, the pure capacitor voltage v_C decreases. The voltage variation $\Delta v_{C,[t1,t2]}$ from t_1 to t_2 is calculated as

$$\Delta v_{C,[t_1,t_2]}=v_C(t_2)-v_C(t_1)=\Delta Q_{discharge}/C=d_1\cdot T_s\cdot i_{o(1)}/C. \quad (3)$$

From t_2, the switch S turns OFF, the diode D turns ON. The inductor current i_L equals to the diode current i_D, and it decreases with the slope of $(v_o-v_i)/L$. Here, the capacitor starts to charge and v_C increases. At t_3, S turns ON, the capacitor ends charging. The charge absorbed by the capacitor is

$$\Delta Q_{charge}=\int_{t_2}^{t_3} i_C(t)\mathrm{d}t=\int_{t_2}^{t_3}\left|i_D(t)-i_o(t)\right|\mathrm{d}t=\int_{t_2}^{t_3}\left|i_L(t)-i_o(t)\right|\mathrm{d}t. \quad (4)$$

As $i_{L(1)}$ is sampled at the middle instant during t_1 to t_2, it can approximately represent the average value of i_L during t_1 to t_3. The trapezoidal region ΔQ_{charge} can be approximated as a rectangle, whose length and width are $T_s(1-d_1)$ and $i_{L(1)}-i_{o(1)}$, respectively. Then, ΔQ_{charge} is

$$\Delta Q_{charge}\approx(t_3-t_2)\left(i_{L(1)}-i_{o(1)}\right)=(1-d_1)\cdot T_s\cdot\left(i_{L(1)}-i_{o(1)}\right) \quad (5)$$

The voltage variation $\Delta v_{C,[t2,t3]}$ of v_C from t_2 to t_3 is calculated as

$$\begin{aligned}\Delta v_{C,[t_2,t_3]}&=v_C(t_3)-v_C(t_2)=\Delta Q_{charge}/C\\&\approx(1-d_1)T_s\left(i_{L(1)}-i_{o(1)}\right)/C.\end{aligned} \quad (6)$$

According to (3) and (6), the difference value of Δv_C from t_1 to t_3 is

$$\Delta v_{C,[t_1,t_3]}=\Delta v_{C,[t_2,t_3]}-\Delta v_{C,[t_1,t_2]}. \quad (7)$$

Referring to Fig. 7, it is easily found that $i_C(t_3)=i_C(t_1)$ when i_o is constant during Transient Period I. The variation of v_{ESR} is

$$\Delta v_{ESR,[t_1,t_3]}=\mathrm{ESR}\cdot\left[i_C(t_3)-i_C(t_1)\right]=0. \quad (8)$$

Because of $v_o=v_C+v_{ESR}$, hence, during Transient Period I, the variation of output voltage v_o is derived as

$$\Delta v_{o,[t_1,t_3]}=\Delta v_{C,[t_1,t_3]}+\Delta v_{ESR,[t_1,t_3]}=\Delta v_{C,[t_1,t_3]}. \quad (9)$$

Similarly, the voltage variation of v_o from two sampling instants is approximately calculated as

$$\begin{aligned}v_{o(2)}-v_{o(1)}&=\begin{pmatrix}0.5(1-d_1)T_s\left(i_{L(1)}-i_{o(1)}\right)\\-0.5d_1T_si_{o(1)}-0.5d_2T_si_{o(2)}\end{pmatrix}\Big/C\\&=T_s\left(i_{L(1)}-i_{o(1)}-d_1i_{L(1)}+0.5d_1i_{o(1)}-0.5d_2i_{o(2)}\right)/C\end{aligned} \quad (10)$$

It is found that C can be derived from the transient voltage variation. Similarly, for n transient switching cycles ($n\geq1$), C can be estimated from the total voltage variation, i.e.,

$$C=\frac{T_s}{v_{o(n)}-v_{o(1)}}\sum_{j=2}^{j=n}\begin{pmatrix}i_{L(n-1)}-i_{o(n-1)}-d_{n-1}i_{L(n-1)}+\\0.5d_{n-1}i_{o(n-1)}-0.5d_ni_{o(n)}\end{pmatrix} \quad (11)$$

where $i_{L(n-1)}$, $i_{o(n-1)}$ are the sampling signals of i_L and i_o at $(n-1)$th transient cycle. d_{n-1} denotes the duty cycle at $(n-1)$th transient cycle.

B. Data Processing

Although v_o, i_L, i_o are sampled at the middle instant of S turning ON, it cannot avoid the sampling error completely. Here, a least mean square (LMS) based data reconstructed method is used for signal processing. Assuming n points of v_o, i_L, i_o, and d are obtained during transients, they can be reconstructed using a quadratic function, i.e.,

$$y_n=a_0+a_1n+a_2n^2 \quad (12)$$

where y represents the reconstructed data of v_o, i_L, i_o, and d. The coefficients a_0, a_1, a_2 can be derived from the LMS algorithm, which is detailed discussed in [36], [37].

Considering the CM is taken during the voltage rise period, the sampling data $v_{o(n)}$ should be larger than $v_{o(1)}$. Here, the restrictive conditions for capacitance estimation are defined as $v_{o(n)}>v_{o(1)}$ and $v_{o(n)}>v_{o(n-1)}$.

C. Reference Value Calibration

Generally, the health status of capacitors is assessed based on the comparison of the estimated capacitance and the reference value, i.e., the initial value C_0. However, the capacitance is easily affected by the ambient temperature T_a. Assuming the capacitance is estimated at T_a, C_0 needs to be calibrated using the following equation, in order to acquire a fair comparison, i.e.,

TABLE I
ASSUMED CAPACITOR PARAMETERS IN THE SIMULATION

Capacitors	Reference values (Assumed values)
Simulated Cap. 1	C = 220 μF, ESR = 50 mΩ
Simulated Cap. 2	C = 100 μF, ESR = 50 mΩ
Simulated Cap. 3	C = 330 μF, ESR = 50 mΩ
Simulated Cap. 4	C = 220 μF, ESR = 10 mΩ
Simulated Cap. 5	C = 220 μF, ESR = 100 mΩ

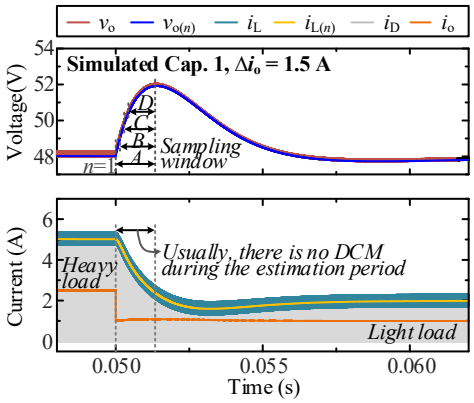

Fig. 8. Simulated response for the built dc/dc boost converter.

$$C_0\left(T_a\right) = \chi_{Al} + \lambda_{Al} e^{-T_a/\nu_{Al}} \tag{13}$$

where, χ_{Al}, λ_{Al}, and ν_{Al} are characteristics coefficients of capacitors, which are determined experimentally [6].

IV. SIMULATION STUDY

To verify the proposed capacitance estimation scheme, a dc/dc boost converter with different capacitor parameters is built in PSIM simulation environment. The main circuit parameters are given as follows: V_i=24 V, V_o=48 V, L=100 μH, f_s=200 kHz. A digital double closed-loop controller is chosen as a case study, the crossover frequency of current loop is set to 10 kHz with a phase margin of 55° and the crossover frequency of voltage loop is set to 100 Hz with a phase margin of 45° [34], [35]. Based on the small-signal modeling, the proportional coefficient k_{pi} (interior loop), k_{po}(outer loop) and integral coefficient k_{ii} (interior loop), k_{io} (outer loop) are 0.01, 0.02, 7.5×10^{-3} and 7.5×10^{-6}, respectively. Five different capacitors are assumed in the simulation to verify the estimation model, as shown in Table I.

A. Sampling Windows Selection

Taking a 1.5-A load transient as a case study, Fig. 8 shows the simulation waveforms of output voltage v_o, sampling voltage $v_{o(n)}$, inductor current i_L, sampling current $i_{L(n)}$, diode current i_D, and load current i_o. Here, the sampling frequency equals the switching frequency, and Cap. 1 is chosen as an example. Because the proposed scheme samples the transient profile during the voltage rise period, which is usually occurred during the transient from a heavy-load mode to a light-load mode. Therefore, there is no discontinuous current mode (DCM) in the estimation process, which does not need to be considered.

Referring to Fig. 8, four sampling windows A, B, C, and D are chosen as examples to illustrate the appropriate sampling region for parameter estimation. Using (11), the estimation results are shown in Fig. 9, where n represents the number of transient switching cycles used for parameter estimation. Here, we define the starting cycle of sampling window A as n=1. It is found that the estimation error reduces as n increases due to the accumulated charge Q_{charge} on the output capacitor increases as n increases. And, Q_{charge} is relatively small when n is small, which results in a relatively large error.

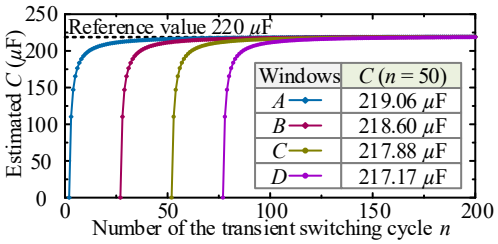

Fig. 9. Estimated results for different sampling windows.

For Window A, the estimation result tends to constant when $\Delta n \geq 30$, however, it tends to constant for Window D when $\Delta n \geq 50$. Because the voltage rise rate for Window A is larger than that for Window D. According to the obtained results, it is known that 50 sampling points are suitable for the capacitance estimation and the estimation error is less than 2%. Moreover, the simulation results illustrate that the sampling start time has no effect on parameter estimation.

B. The Effect of Transient Change Amplitude

Considering the availability of the proposed scheme for converters with a relatively small transient amplitude. Fig. 10(a) shows the sampling voltage profiles for converters with different transient change amplitudes, i.e., Δi_o = 0.5 A, Δi_o = 1 A, and Δi_o = 2 A. It illustrates that the maximum voltage deviation increases as the transient amplitude decreases when the capacitance is constant. Using (11), the estimated results are given in Fig. 10(b). Here, 50 transient switching cycles are chosen to estimate C. It is found that the proposed scheme is feasible for converters with different transient amplitudes. However, for a small-amplitude transient, the error at the estimation point (i.e., n = 50) is slightly larger than that for a large transient.

C. The Effect of Capacitor Parameters

1) The Effect of Capacitance: To verify the proposed scheme for converters with different capacitances, Fig. 11(a) shows the sampling voltage profiles when Caps. 1, 2, and 3 are used. It is found that the maximum voltage deviation increases as the capacitance decreases when the load current step is constant. The estimation results in Fig. 11(b) illustrates the feasible of the proposed scheme, and the estimation error at n = 50 is less than 2%.

Moreover, assuming the capacitance of Cap. 1 has been degraded to 98% and 96% of the reference value (i.e., 215.6 μF and 211.2μF), Fig. 12 shows the sampling voltage profiles and estimation results for a 1.5-A unloading transient. It is found that the proposed scheme can identify a slight change of capacitance, and the estimation error at n = 50 is less than 1%.

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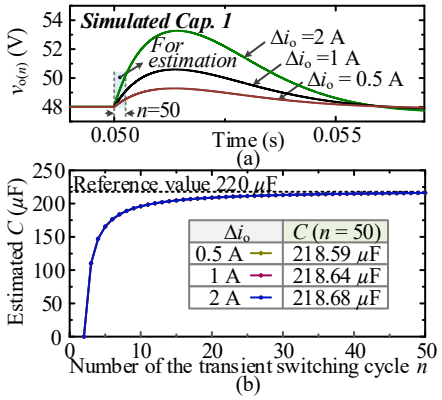


Fig. 10. Simulation waveforms and estimated results for converters with different transient change amplitudes. (a) Simulation waveforms. (b) Estimated results.

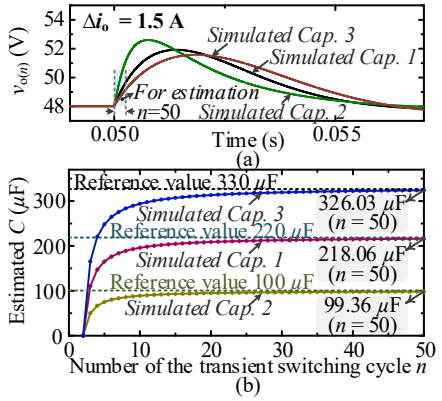


Fig. 11. Simulation waveforms and estimated results for converters with different capacitances. (a) Simulation waveforms. (b) Estimated results.

2) The Effect of ESR: In order to verify the effect of ESR on capacitance estimation, Fig. 13 shows the transient response waveforms and estimation results for two types of capacitors, where the ESR of Cap. 4 and 5 are assumed as 10 mΩ and 100 mΩ, respectively. Referring to Fig. 13(a), the sampled waveforms of transient voltage are similar for these two cases. The estimated results of capacitance are given in Fig. 13(b), it is found that the estimation error of the cases that ESR = 10 mΩ and ESR = 100 mΩ when n = 50 are 1.1% and 0.7%, respectively.

3) The Effect of ESL: Furthermore, Fig. 14(a) shows the simulation waveforms for converters with two different values of ESL, i.e., ESL = 10 nH and ESL = 50 nH. Here, Cap. 4 is used and Δi_o = 1.5 A. Fig. 14(b) gives the sampling waveforms of v_o, i.e., $v_{o(n)}$, it is found that the ESL has almost no effect on the sampling signals. Because the signals are sampled at the middle instant of the switch S turns ON, the switching noises caused by ESL have not been recorded. Furthermore, Fig. 14(c) shows the estimation results, it illustrates that there is little difference between these two cases due to the sampling signals are similar. Therefore, the effect of ESL on capacitance estimation can be ignored.

D. The Effect of Transient Profile

In addition, Fig. 15(a) shows the simulation waveforms for the converter with different control parameters, where k_{pi}, k_{po}, k_{ii}, k_{io} are 0.02, 0.04, 7.5×10^{-3} and 7.5×10^{-6}, respectively.

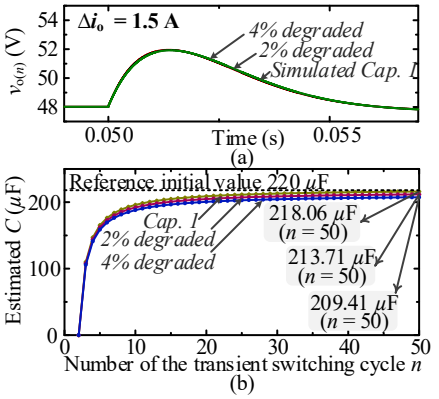


Fig. 12. Simulation waveforms and estimated results for capacitance degradation. (a) Simulation waveforms. (b) Estimated results.

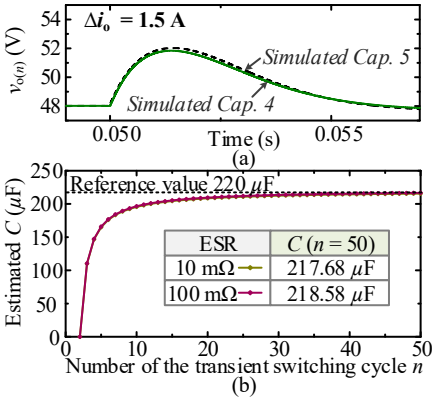


Fig. 13. Simulation waveforms and estimated results for converters with different ESR. (a) Simulation waveforms. (b) Estimated results.

It is found that there exists voltage ringing during transients under these control parameters. Taking six sampling regions (i.e., Regions I, II, III, IV, V, VI) as case studies, Fig. 15(b) shows the capacitance estimation results when n = 50. It is known that the capacitance estimation model is feasible by using different transient profiles, e.g., voltage undershoot and voltage ringing. However, the estimation error for Region VI is larger than that for others due to the rate of change of voltage is relatively small. For simplification, the voltage-rise period during transients is chosen to estimate C in the proposed scheme.

V. Experimental Verification

A. Experimental Platform and Reference Value Calibration

Taking a dual-loop digital controlled boost converter as a case study, Fig. 16 shows the photo of the built experimental platform. Table II lists the detailed circuit parameters and controller parameters. Fig. 17 shows the circuit implementation scheme, where $v_{o,s}$, $i_{L,s}$, $i_{o,s}$ represent the sampling signals of the voltage sensor (type: LV25-P) and current sensor (type: LA 25-NP). Here, the signal conditioning circuits designed for $v_{o,s}$, $i_{L,s}$, $i_{o,s}$ are the same, as shown in the right part of Fig. 17. In the proposed scheme, a dual-core MCU TMS320F28377D is used for digital control and CM. The on-chip and off-chip memories are 204 KB and 256 KB, respectively [38]. In each switching cycle, the PI control algorithm is executed in the ADC interrupt subroutine. After the end of one unloading transient, the

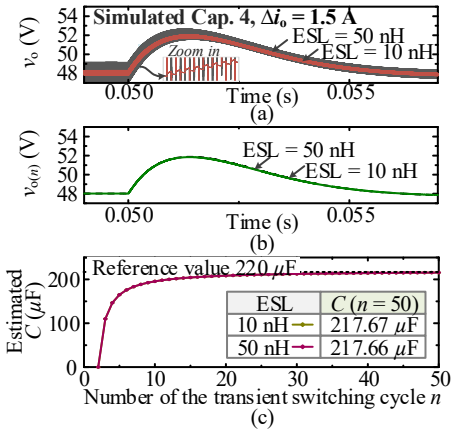


Fig. 14. Simulation waveforms and estimated results for converters with different ESL. (a) Simulation waveforms of v_o. (b) Simulation waveforms of $v_{o(n)}$. (c) Estimated results.

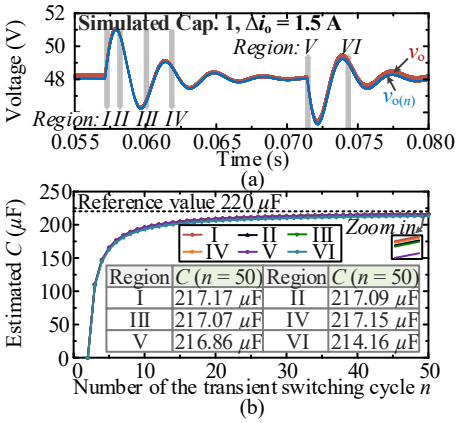


Fig. 15. Simulation waveforms and estimated results for different transient profiles. (a) Simulation waveforms. (b) Estimated results.

TABLE II
KEY PARAMETERS OF THE EXPERIMENTAL PLATFORM

Parameters	Values
Input voltage V_i	24 V
Output voltage V_o	48 V
Inductor L	100 μH, 50 μH
Switching frequency f_s	200 kHz
Controller parameters	k_{pi}=0.01, k_{ii}=1.5×10^{-4} k_{po}=0.024, k_{oi}=3.5×10^{-7}

proposed capacitance estimation algorithm is being executed in the main program. Moreover, a liquid crystal display (LCD) based on serial communication is employed for display.

Table III lists the initial values of capacitors, where the capacitor parameters are tested using an LCR meter at 20 °C (i.e., room temperature). Here, three types of Nichicon UKZ capacitors are selected for experimental verification, i.e., Cap. I, Cap. II, and Cap. III, where Caps. I and II are new capacitors. Cap. III consists of Cap. I and a resistor in series, in order to simulate the ESR change. It is noticed that the C is tested under the frequency of 120 Hz, and the ESR is tested under 200 kHz. The relationship between C and ambient temperature can be derived using (13). Based on the tested data of Nichicon UKZ series capacitors [39], Fig. 18 shows the relationship curve of initial capacitance and temperature, where the coefficients χ_{Al}, λ_{Al}, ν_{Al} for Caps. I, II, and III are also shown in Fig. 18. Then, the estimated capacitance can be compared with the reference value obtained from Fig. 18 when the ambient temperature is

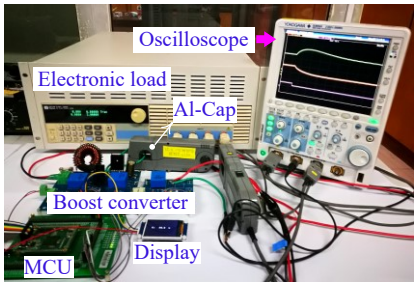


Fig. 16. Photo of the built experimental platform.

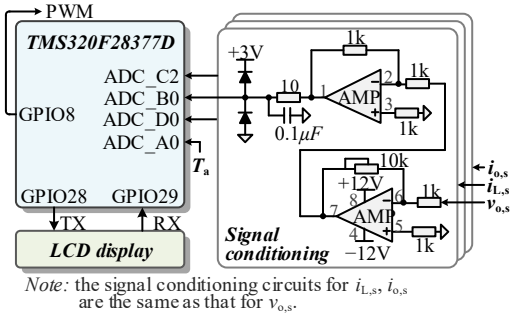


Fig. 17. Circuit implementation of the proposed CM scheme.

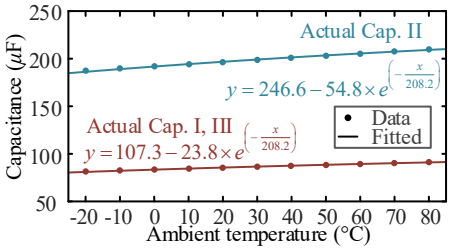


Fig. 18. Capacitance variation versus temperature of used capacitors.

TABLE III
INITIAL VALUES OF ACTUAL CAPACITORS I, II, AND III AT 20 °C

Capacitors	Tested initial values
Actual Cap. I: Nichicon 100μF/100V	85.4μF, 40.2 mΩ
Actual Cap. II: Nichicon 220μF/100V	196.3μF, 13.7 mΩ
Actual Cap. III: Nichicon 100μF/100V	85.4μF, 90.2 mΩ

TABLE IV
SIX CASES FOR LOAD TRANSIENT EXPERIMENTS

Cases	Experimental condition
A	Actual Cap. I, L = 100 μH, Δi_o = 1.5 A (step)
B	Actual Cap. I, L = 100 μH, Δi_o = 2 A (step)
C	Actual Cap. II, L = 100 μH, Δi_o = 2 A (step)
D	Actual Cap. III, L = 100 μH, Δi_o = 2 A (step)
E	Actual Cap. I, L = 100 μH, Δi_o = 2 A (gradual)
F	Actual Cap. I, L = 100 μH, ΔP_o = 100 W (step)

changed, in order to assess the health status of capacitors. Simplistically, all the experimental researches in this section are taken at 20 °C, in order to verify the capacitance estimation scheme.

B. Experimental Results of Load Transients

To verify the proposed scheme is suitable for converters with different transient amplitudes and circuit parameters, six different cases are chosen as case studies, as shown in Table IV. Here, resistive loads are considered in Cases A−D, and the load current i_o is suddenly changed. A gradual load change and a constant power load are considered in Case E and Case F, respectively.

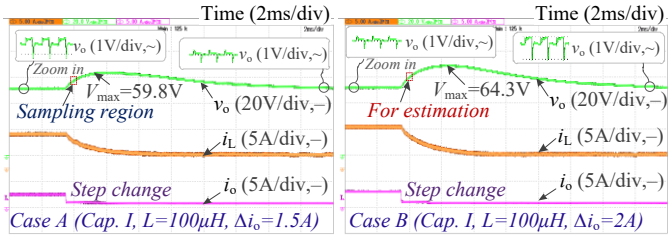


Fig. 19. Experimental waveforms for Cases A and B. (a) Experimental waveform of Case A. (b) Experimental waveform of Case B.

1) Case of Converters with Different Transient Amplitudes: Figs. 19(a) and (b) show the experimental waveforms for Cases A and B, respectively. It is found that the steady-state ripples changes when the operating conditions of converters are changed, and the transient charging profile is changed as Δi_o changes. Moreover, the maximum transient voltage derivation V_{max} increases as the step amplitude increases.

Taking Case A as an example, Fig. 20 shows the sampled data of v_o, i_L, i_o, and d. It illustrates that the single-rate sampled voltage data (i.e., $v_{o(n)}$) can indicate the transient profile, however, there exist noise signals on the sampled data. To reduce the effect of noise and improve the capacitance estimation accuracy, a LMS based data reconstructed method is used for signal processing, as discussed in Section III. Besides, Fig. 20 also gives the reconstructed data (indicated in red), which illustrates that the data processing method can filter the high-frequency noise. Moreover, the execution time of running the LMS algorithm in TMS320F28377D is about 50 μs. The CM algorithm can be executed after the end of transients.

Based on the proposed estimation model, Fig. 21 shows the estimated results of C. Here, the sampling threshold voltage V_{th} is set as 52 V, n is set as 50. To make sure the data are sampled during the voltage rise period, the following conditions need to be satisfied, i.e., $v_{o(n)} > v_{o(n-1)}$ and $v_{o(50)} - v_{o(1)} > 1$. The estimation results demonstrate that the proposed scheme is suitable for converters with different load changes, and the estimation errors are less than 1% when n = 50. Moreover, the estimation error when Δi_o = 1.5 A is slightly larger than that when Δi_o = 2 A.

2) *Case of Converters with Different Capacitor Parameters:* Fig. 22 shows the experimental waveforms for converters with Caps. II and III. Comparing with the experimental waveform in Fig. 19(b), it is known that V_{max} decreases as the capacitance increases, and it is increases as the ESR increases. The estimation results for these two cases are also given in Fig. 21, it is found that the scheme is feasible for converters with different capacitance and ESR. Considering the capacitors with different ESR, the accuracy of Case D is slightly larger than that in Case B due to the transient voltage has a relatively large rise slew rate. Moreover, Caps. II and III have different ESL, the experimental results also illustrate that the ESL has no effect on capacitance estimation.

3) *Case of Converters with Gradual Load Transients:* Considering the converter would endure a gradual load transient, Fig. 23(a) shows the experimental waveform of Case E, where the load current is not suddenly changed and its slew rate is 2 A/ms. According to the estimation results in Fig. 21, it illustrates that the scheme is feasible for converters with a gradual load transient, and the estimation error is less than 1%.

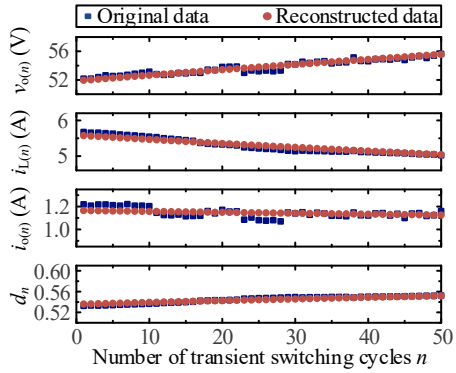
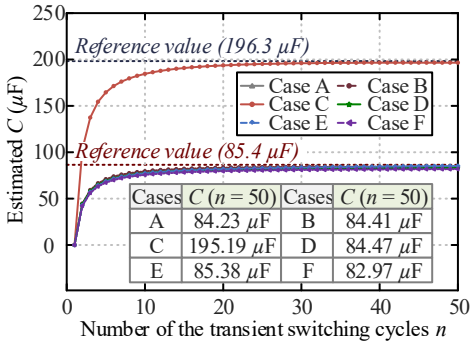


Fig. 20. Sampled data and reconstructed data of v_o, i_L, i_o, and d for Case A.



Cases	C (n = 50)	Cases	C (n = 50)
A	84.23 μF	B	84.41 μF
C	195.19 μF	D	84.47 μF
E	85.38 μF	F	82.97 μF

Fig. 21. Estimated capacitance for Cases A–F.

TABLE V
CASES FOR INPUT PERTURBATION

Cases	Experimental condition
G	Actual Cap. I, L = 100 μH, i_o = 2 A, Δv_i = 4 V
H	Actual Cap. I, L = 100 μH, i_o = 2 A, Δv_i = 8 V

4) *Case of Converters with Constant Power Loads:* Considering converters with different load types [e.g. constant power loads (CPLs)], Fig. 23(b) shows the waveform of Case F. Here, the step power ΔP_o is 100 W. The estimation results in Fig. 21 demonstrate that the proposed scheme is suitable for a converter with CPLs, and the estimation error is less than 3%.

C. Experimental Results of Input Perturbation

The proposed estimation scheme is also suitable for the converter with an input voltage perturbation. Taking 4-V and 8-V input-voltage change as case studies (c.f. Table V), Fig. 24 gives the experimental waveforms, where the slew rate of the input voltage is 3 V/ms. The estimation results in Fig. 25 illustrate that the proposed capacitance estimations scheme is suitable for the input perturbation of converters, and the estimation error is less than 1%. Notice that Case G requires a relatively large n to enable the estimate result tends to constant, because of the voltage rise rate during the estimation period is relative small, as discussed in Part A of Section IV.

VI. DISCUSSION

The effect of transient amplitude, load types, capacitor parameters on CM has been discussed in Section V. In order to further evaluate the proposed scheme, the effects of converter

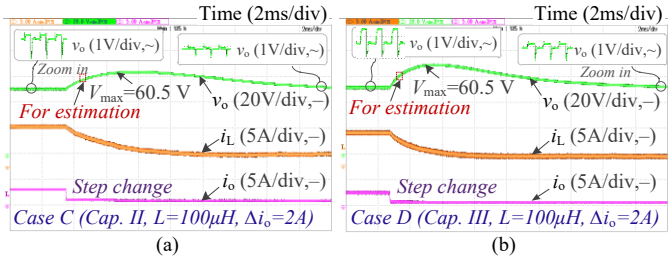


Fig. 22. Experimental waveforms for Cases C and D. (a) Experimental waveform of Case C. (b) Experimental waveform of Case D.

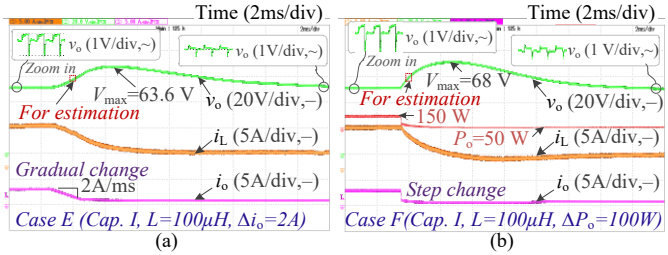


Fig. 23. Experimental waveforms for Cases E and F. (a) Experimental waveform of Case E. (b) Experimental waveform of Case F.

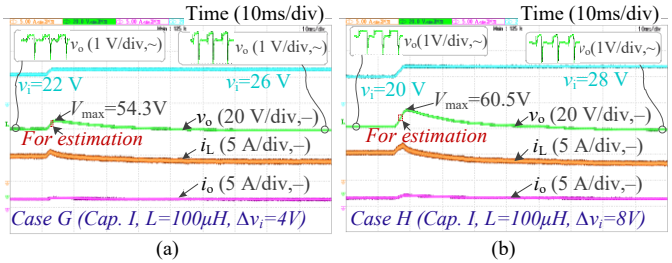


Fig. 24. Experimental waveforms for Cases G and H. (a) Experimental waveform of Case G. (b) Experimental waveform of Case H.

parameters (e.g., inductance, input and output voltage), capacitance variation, and change of sensor are discussed in this section.

A. Robustness Analysis

1) The Case of Different Inductances: In order to investigate the effect of converter parameters on the proposed scheme, Fig. 26(a) shows the experimental waveform of the built converter with a 50-μH inductance (i.e., Case J). Comparing with the waveform in Fig. 19 (b), it is known that the maximum voltage derivation and transient setting time reduce when a small inductance is used. According to the estimation results in Fig. 27(a), it is found the proposed scheme is suitable for converters with a small-amplitude transient profile when a small inductance is used, and the estimation error is less than 2%.

2) The Case of Different Loads: In Cases A−E and J, the load current is 1 A during the light load period. Considering different loads, Fig. 26(b) shows the experimental waveform of the built converter with a 1.5-A unloading transient (i.e., Case K). Here, the load current is 0.4 A during the light load period. Fig. 27(a) gives the estimation results, which illustrate that the proposed scheme is suitable for converters with different loads.

3) The Case of Capacitance Variation: The experimental results in Section V illustrate that the proposed scheme is feasible to identify different capacitances. In order to simulate the small-range capacitance variation, a small-capacity Al-Cap

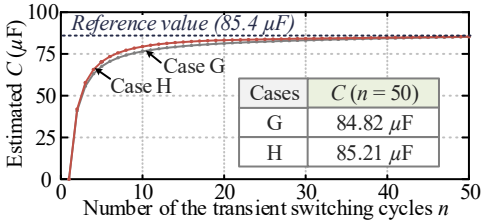


Fig. 25. Estimated capacitance for Cases G and H.

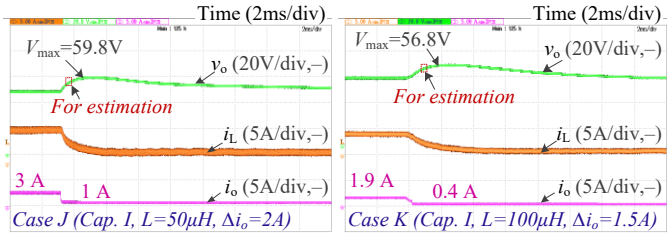


Fig. 26. Experimental waveforms for Cases J and K. (a) Experimental waveform of Case J. (b) Experimental waveform of Case K.

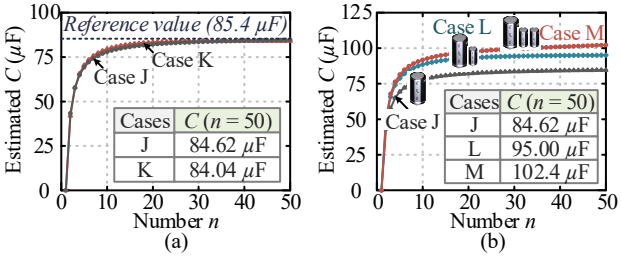


Fig. 27. Experimental results for Cases J−M. (a) Cases J and K. (b) Cases J, L and M.

(type: Nichicon 10 μF/100 V) is connected in parallel with Cap. I, whose actual capacitance is 9.8 μF (tested at 120 Hz). Referring to Fig. 27(b), one small-capacity Al-Cap is connected with Cap. I in Case L, and two are connected with Cap. I in Case M. The reference values are 95.2 μF and 105 μF, respectively. Under the same experimental condition with Case K, Fig. 27(b) gives the experimental results. It can be seen that the proposed scheme has the ability to identify the small-range capacitance variation. Notice that the experimental waveforms of Cases L and M are similar to that in Case K, which are not given in this part.

4) The Case of Different Input and Output Voltages: Considering different input and output voltages, Fig. 28(a) shows the experimental waveform for an 18−42-V converter (i.e., Case M). Here, the sampling threshold voltage V_{th} is defined as 46 V. The estimation results are shown in Fig. 28(b), which illustrates that the prosed scheme is not affected by the input and output voltage changes.

5) The Case of Different Sensors: In order to analyze the effect of voltage and current sensors, the sensors LV25-P and LA25-NP are replaced by two similar ones, i.e., HNV025A and HNC025A. Taking the inductor current sensor as an example, Fig 29(a) shows the sampling calibration results, where the horizontal axis represents the results of 12-bit ADC. Here, the operation condition of the converter is the same as that in Case K, and the experimental waveform is similar to Fig. 26(b).

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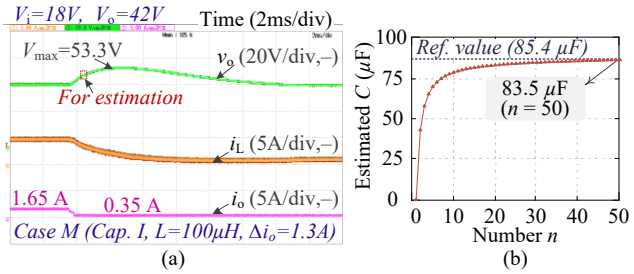

Fig. 28. Experimental waveform and estimation results for Case M. (a) Experimental waveform. (b) Estimation results.

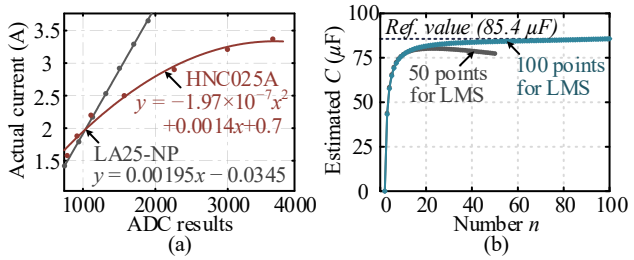

Fig. 29. Sampling calibration and estimation results when the sensor HNC025A is used. (a) Sampling calibration. (b) Estimation results.

For comparison, the calibration results of LA25-NP are also shown in Fig. 29(a). It is found that the sensor HNC025A has poor linearity. Although the calibration can improve the estimation accuracy, the estimation error is relatively large when 50 points are sampled, as shown in Fig. 29(b). Fortunately, the accuracy can be improved by increasing the sampling number for LMS, as shown in Fig. 29(b). Because the degree of similarity between an original signal and reconstructed data has been increased in this case, which can reduce the error.

Similarly, the estimation accuracy for other cases can be further improved by increasing the sampling number for LMS.

B. Comparison with the Existing Schemes

To compare the proposed scheme with the existing schemes, Table VI summarizes the additional hardware and software demands for CM in dc/dc boost converters, where f_{sw} is the switching frequency and N represents the number of sampling points during one switching cycle. Here, the oscilloscope and PC are used for signal sampling and processing of high-frequency small-signal ripples. The remarks are given in the following.

1) To acquire the high-frequency small-amplitude ripples, the steady-state ripple-based methods [9], [10], [12], [13], [18]−[20], [24] and circuit model-based methods [27], [28] require high-frequency sampling devices, such as oscilloscopes, data acquired cards, and/or ripple extradition circuits. Moreover, a powerful data processing device, such as a PC, is needed to process an amount of sampling data. Comparing with them, the hardware and software demand in the proposed scheme is relatively low.

2) The scheme in [24] can reduce the sampling frequency of steady-state ripple, however, the magnification of ripple extraction circuits cannot adapt to the change of ripples. Especially, the amplitude of steady-state ripple in boost converters is changed when the operation condition changes (e.g., the load changes), which leads a limitation to apply them in boost converters. Comparing with them, the proposed scheme does not have this limitation.

3) From the perspective of applicability, the proposed capacitance estimation model is specifically designed for a dc/dc boost topology, which is similar to that in [18]−[20], [24], [27], [28]. For other topologies, the same transient charging profile-based concept can be applied but need to be altered depending on the selected topology. In [33], a transient trajectory-based method is presented to monitor the Al-Cap of buck converters, however, additional transient detection circuits are required. Comparing with that in [33], the proposed scheme for boost converters does not need additional transient detection circuits, and the estimation accuracy is relatively high.

In a summary, comparing with the existing schemes, the proposed scheme does not need high-frequency sapling devices and ripple extraction circuits. The volume of sampled data is small, and the estimation algorithm is relatively simple. However, the transient period is too long when compared with the steady-state ripples. Fortunately, the transient is not always occurred. In order to avoid a continuous triggering, the transient detection module is disabled before one CM algorithm has finished. Moreover, the transient period is considerably short when compared with capacitor aging. Therefore, there is no need to execute CM all the time. It is reasonable to enable the CM when a relatively large transient has occurred.

VII. CONCLUSION

In this paper, a transient charging profile based capacitance estimation scheme is proposed for output capacitors of dc/dc boost converters. Taking a 24−48-V boost converter as a case study, experimental results demonstrate the feasibility of the proposed scheme, and the estimation error is less than 3%. The main features of the proposed scheme are given in the following.

1) The proposed scheme uses the large-amplitude long-time-scale transient charging profile to estimate the output capacitance of boost converters, which can reduce the sampling frequency and the volume of data. Moreover, the proposed scheme does not need ripple extraction circuits, which is not affected by operating conditions.

2) It is proved that the transient characteristics-based CM schemes are suitable for converters with one right half plane zero, such as dc/dc boost converters. Moreover, for other topologies, the same transient charging profile-based concept can be applied but need to be altered depending on the selected topology.

3) Although the transient period is too long when compared with the steady-state ripples, the transient is not always occurred. Moreover, the transient time is considerably short when compared with capacitor aging. Therefore, the estimation can be enabled when a relatively large transient has occurred, which does not affect the purpose of CM.

TABLE VI
COMPARISON WITH THE EXISTING CM SCHEMES FOR DC/DC BOOST CONVERTERS

Methods		Ref.	f_{sw} (N)	Additional sampling circuits/ devices	Data processing tool; algorithm (calculation complexity)	Experimental error	Applicability in other topologies
Steady-state ripple-based methods	Capacitor current directly measured	[9]	15 kHz (N=100)	Oscilloscope, current probe	PC with Matlab; N/A (+)	ESR: <2.8%	+ + +
		[10]	20 kHz (N=26)	Oscilloscope, current probe	PC with Matlab; CS-DWT (+ + + +)	ESR: <3%	
		[12], [13]	20 kHz (N=50) 100 kHz (N=10)	Oscilloscope	PC with Matlab; N/A (+)	ESR: <4.1% [12] C: <5.4% [12]	
	Operation mode of converters	[18]	20 kHz (N/A)	Oscilloscope	Not mentioned; LMS (+ +)	ESR: <15%	+
		[19]	20 kHz (N=25)	N/A	MCU (controller); LMS (+ +)	ESR: <10.5% C: <15.8%	
		[20]	30 kHz (N=333)	Ripple extraction circuit, PCI card	PC with Matlab; WTD (+ + +)	ESR: <3.1%	
		[24]	10 kHz (N=4)	Ripple extraction circuit	MCU (controller); N/A (+)	ESR: <6.2%	
Circuit mode-based methods		[27]	20 kHz (N=200)	PCI card	PC with Matlab; N/A (+)	ESR: <13.3% C: <7.5%	+
		[28]	100 kHz (N=100)	Oscilloscope	PC with Matlab; WTD(+ + +)	ESR: <11.7% C: <9.2%	
Discharging/ charging profiles based-methods		[33]	200 kHz (N=1)	Unloading transient detection circuit, load current sensor	MCU (controller); N/A (+)	ESR: <7.4% C: <9.6%	+
		Proposed	200 kHz (N=1)	Load current sensor	MCU (controller); LMS (+ +)	C: <3%	

Note: The topology in [33] is a buck converter, others are dc/dc boost converters.

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