Heat cycle failure point prediction by 3D thermal stress analysis for medium voltage power module

Takahashi, Masaki; Jørgensen, Jannick Kjær; Jørgensen, Asger Bjørn; Munk-Nielsen, Stig; Uhrenfeldt, Christian

Published in:
2023 IEEE Applied Power Electronics Conference and Exposition (APEC)

DOI (link to publication from Publisher):
10.1109/APEC43580.2023.10131157

Publication date:
2023

Document Version
Accepted author manuscript, peer reviewed version

Heat cycle failure point prediction by 3D thermal stress analysis for medium voltage power module

Masaki Takahashi
Department of Energy
Aalborg University
Aalborg, Denmark
mata@energy.aau.dk

Jannick Kjær Jørgensen
Department of Energy
Aalborg University
Aalborg, Denmark
jkj@energy.aau.dk

Asger Bjørn Jørgensen
Department of Energy
Aalborg University
Aalborg, Denmark
abj@energy.aau.dk

Stig Munk-Nielsen
Department of Energy
Aalborg University
Aalborg, Denmark
smn@energy.aau.dk

Christian Uhrenfeldt
Department of Energy
Aalborg University
Aalborg, Denmark
chu@energy.aau.dk

***Abstract*—The structural optimization of power modules for reliability can be performed without physical prototyping if the structural weakness in modules can be assessed on a 3D model. In this study, 3D thermal stress simulation is investigated as a predictive tool for the heat cycle test (HCT) failure point of the medium voltage power module. The module has a multi-layer structure of two different ceramics (Al2O3 and AlN) to reduce the parasitic capacitance. In this complex structured module, the failure point of actual test samples are shown to coincide with weakness points of the thermo-mechanical stress in the 3D simulation. The heat cycle test (125/-40°C) was used for simulation and testing. The failure point of the module was predominantly copper delamination from the AlN substrate surface after HCT 100 cycles. The delaminated locations were matched to points in the simulation that has 2 characteristics, high peeling stresses points and high shape deformation of copper pattern at the simulation results. This observation applies to copper patterns only connected to the ceramics, while copper patterns connected to other adjacent layers did not follow this trend.**

***Index Terms*—10kV SiC-MOSFET power modules, heat cycle, 3D modeling, Finite Element Method, thermo-mechanical stress**

I. Introduction

Silicon carbide metal oxide semiconductor field effect transistors (SiC-MOSFETs) are expected to expand the power device applications such as medium voltage range in the 10kV or higher, because SiC-MOSFETs show superior performance in the high voltage and frequency range compared to conventional silicon Insulated Gate Bipolar Transistors (Si-IGBT) [1] [2]. On the other hand, it is necessary to optimize the package structure of medium voltage power modules for the application. One example of a module structure for medium voltage is a power module with four SiC-MOSFETs (10kV 350mΩ, Wolfspeed) connected in parallel (80A) as presented in [3]. The module has a structure to reduce the switching loss and EMI risks at high voltage operation [3]. A structural feature is that it has a stacked direct copper bonding (DCB) substrates design with a large AlN and a small Al2O3 on the output terminal side. This is to reduce parasitic capacitance from the output plane to the base plate. The structure is shown in Fig. 1 compared to a conventional power module [4].

However, the thermo-mechanical characteristics have not been sufficiently analysed for this advanced structure power module that was optimised mainly with respect to its electrical performance for medium voltage application. In general, the thermo-mechanical performance defines the reliability of power modules. Power module reliability characteristics are directly linked with the time to fail under long-term stress tests. The failure of modules often occur due to the coefficient of thermal expansion (CTE) mismatch between different materials such as the structure in Fig. 1. The heat cycle test (HCT) is used to identify the weakness point of modules for the thermo-mechanical stress from CTE mismatch between the component materials [5]. However, HCT needs a lot of time since 1 cycle may require 2 hours and always more than 100 cycles are required as a test criteria [6]. Therefore, for new product design engineers, designing while minimising the number of actual HCTs has a significant effect on reducing design lead time.

Through digital design using 3D modeling, a new design

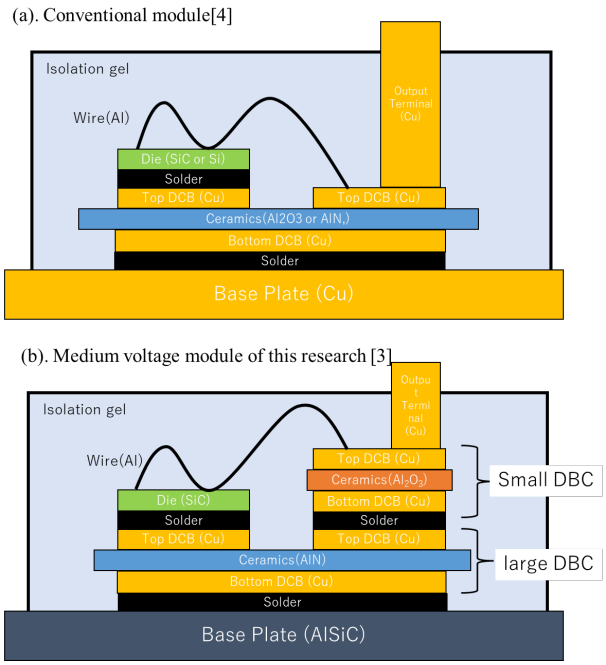

Fig. 1. Schematic cross section of power module structure (a). conventional module [4], (b). module structure in this research [3]

method that has been gaining attention in recent years, it is possible to realize an efficient product design with a small number of samples, and minimum testing [7]. It is necessary to perform 3D simulation analysis combined with a suitable failure mode theory to apply the digital design method for thermo-mechanical performance assessment.

Typically, HCT leads to the large solder layer degradation for conventional power modules [8]. This has been ascribed to the solder crack growth due to fatigue caused by repeated solder creep [9]. According to previous research, design parameters of solder layer required for digital design utilising the finite element method (FEM) are proposed by a more practical model [10]. On the other hand, from other experimental testing results, two failure modes of HCT are observed at the same time; solder cracking and copper layers delamination from the DCB substrate ceramic layer [11]. Especially, even though the solder cracks are still contained to a level where they still be safe of their connection, the coppers delamination causes the failure of modules. In addition, some advanced structured power modules for medium voltage showed the delamination of copper and aluminium layers from the ceramics substrate after HCTs [12] [13]. One feature of them is a jointed 2 ceramic substrates by soldering or sintering. However, detailed analysis of the influence of HCT failure modes by the ceramics stacked structure has not been reported.

Therefore, it is difficult to predict whether the modules under study will have the same failure points as these results due to their new characteristics of being base-joined modules with DCBs of different sizes and ceramic types (Al2O3, AlN). In order to quantitatively estimate the structural weak points for power modules, it is necessary to correlate the analysis results from simulations with the actual failure points.

In this study, the HCT failure point of the power module with partly DCB stacked structure shown in Fig. 1 (b) was investigated. First, the points of highest thermo-mechanical stress between the different materials comprising the module were simulated to predict the failure layer. Next, HCT failure mode was revealed by experiments, especially difference between DCB substrates with and without stacking. Then, an attempt was made to estimate the points of high failure risk from thermo-mechanical stress simulation in 3D modeling.

II. Methodology

A. 3D thermo-mechanical stress simulation

In this study, 3D models and actual samples were fabricated without power device chips, wires, isolation gel, terminals, and a case. The actual sample picture and the 3D model are shown in Fig. 2.

The material thicknesses of the module and physical properties of each component used in this study are summarised in Fig. 3 below. Two ceramics (Al2O3, AlN) and AlSiC are assumed to be linear elastic. On the other hands, copper and solder (Sn-Ag-Cu:SAC305) were applied to non-linear elasticity adopted from each reference [14] [18]. Fig. 4 below shows the behaviour of the non-linear elasticity used in this simulation.

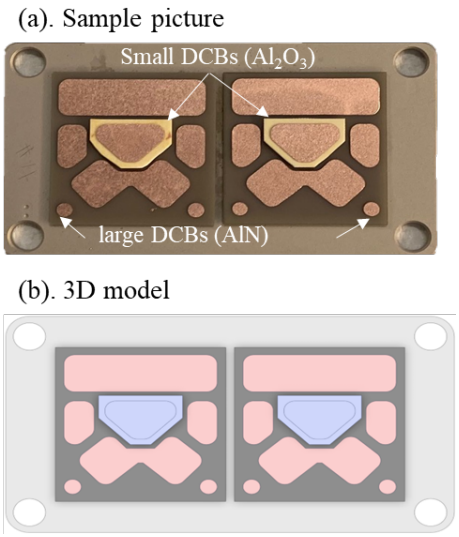

Fig. 2. Schematic images of module and test sample in this research

Structure	Material	Thickness	Function	Density [kg/m3]	Thermal expansion coefficient[K^{-1}]	Young's modulus [GPa]	Poisson's ratio	Ref.
Small DCB	Cu	300μm	Upper side Connection	8940	1.8E-05	110	0.34	[14]
	Al2O3	630μm	Isolation	3970	6.5E-06	400	0.22	[15]
	Cu	300μm	Bottom side Connection	8940	1.8E-05	110	0.34	[14]
Solder	Sn-Ag-Cu	50μm	Connection	7370	2.3E-05	34.3	0.4	[16]
Large DCB	Cu	300μm	Upper side Connection	8940	1.8E-05	110	0.34	[14]
	AlN	630μm	Isolation	3300	4.5E-06	340	0.24	[15]
	Cu	300μm	Bottom side Connection	8940	1.8E-05	110	0.34	[14]
Solder	Sn-Ag-Cu	50μm	Connection	7370	2.3E-05	34.3	0.4	[16]
Base	AlSiC	1.5mm	Protection	3010	8E-06 @ 30-100°C	188	0.24	[17]

Fig. 3. Material property for the simulation [14]- [17]

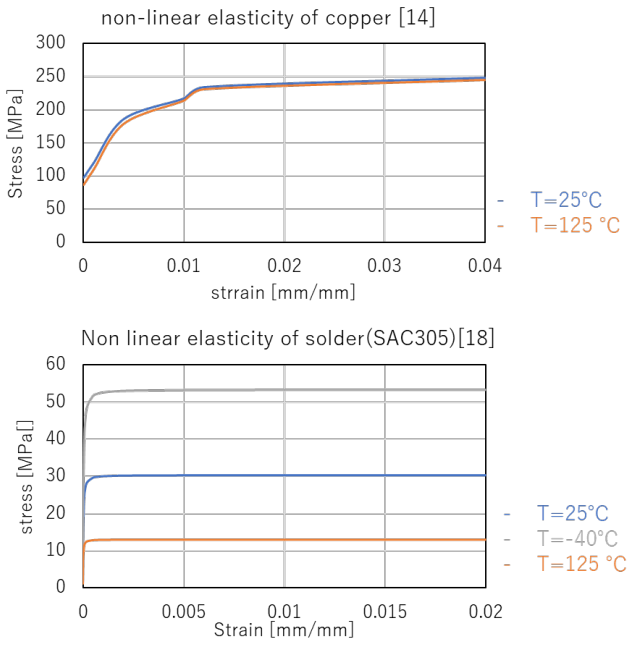

Fig. 4. Non-linear elasticity behavior of copper and solder [14] [18]

Thermo-mechanical stresses were calculated in ANSYS Mechanical 2021 by 3D modeling during one HCT consisting of a temperature rise, a high temperature hold, a temperature drop, and a low temperature hold. The model was meshed with 173462 elements and 759035 nodes by the automatic mesh generation in this simulation. The initial condition of the simulation was defined as the zero stress point during the solder processing at a temperature of 217°C, which is the lowest liquidus temperature of the solder (SAC305) [19]. The initial temperature profile was then followed by a cooling process to room temperature (25°C) to simulate the temperature profile during the actual solder process. The rate of temperature cooling to room temperature was 0.3°C/sec, and the holding time at room temperature 25°C was 10 seconds. After the soldering process profile, HCT conditions were 125°C / -40°C, a holding time of 10 minutes at each temperature, a temperature rising rate of 3.3°C/min, and a falling rate of 2.1°C/min. These temperature change rates are fixed with the test chamber used in the actual test [20].

B. Heat cycle test with actual samples

HCT was conducted using an Espec Test Chamber SH-262 with the same conditions as simulations. Sample evaluation during and after the HCT was carried out using sample appearance optical photographs and Scanning Acoustic Microscopy (SAM) analysis to monitor the degradation phenomena of each component.

III. Result and Discussion

A. Thermo-mechanical stress simulation result

In estimating failure points due to HCT at conventional power module structures, von Mises stress is an often used analytical parameter because the dominant failure mode is the copper delamination [11]. Thus, the results of the von Mises stress simulation are presented at first. Fig. 5 below shows the results of plotting the maximum value of the von mises stress for the entire module for each time in the virtual HCT, together with the module temperature profile.

The initial von Mises stress is zero at the solder melting temperature (as expected since this condition was defined as the stress-free initial point in the simulation), and it was changing with the temperature cycling due to the fact that upon cooling from solder temperature the CTE mismatch in the structure leads to stress build-up. It is observed that the von Mises stress at the second holding time at -40°C exceeds that of the previously highest value also observed at the -40C holding. This can be ascribed to the strain hardening of the copper, which increases the stress level with each cycle and which is included in the model through the non-linear elasticity of the copper used [11].

Next, the cross sectional images of von Mises stress distribution of module are demonstrated at the second 125°C and -40°C in Fig. 6.

The highest layer of von Mises stress is the interface between the copper layer of the AlN substrate at -40°C. These are thermo-mechanical stresses sufficient to cause delamination

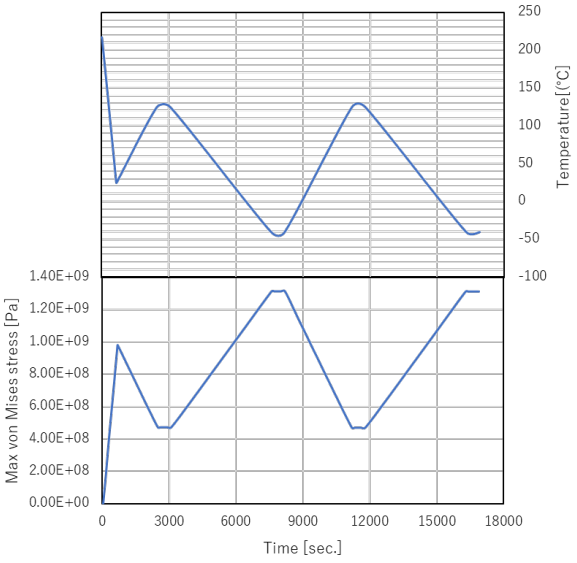

Fig. 5. The time profile of maximun von Mises stress value of the power module and temperature

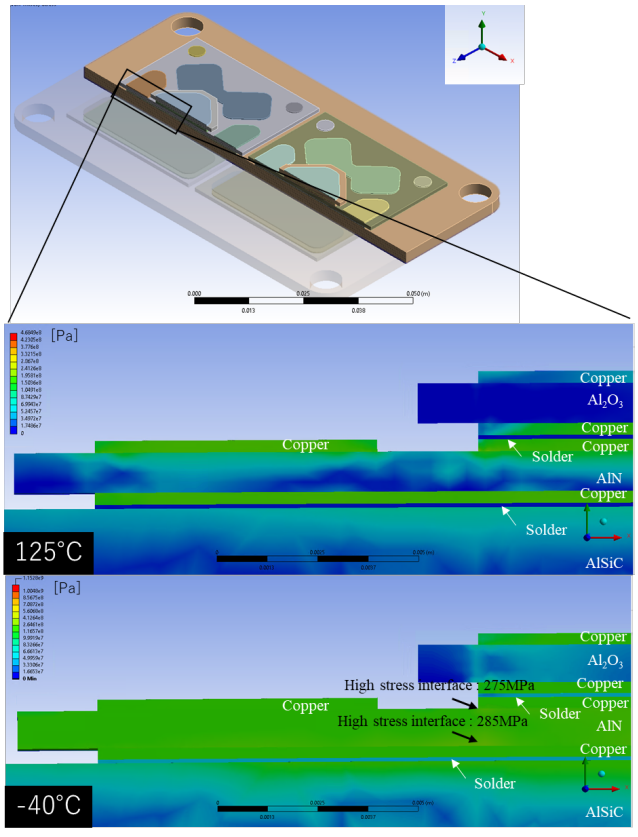

Fig. 6. Cross sectional images of von Mises stress distribution

between copper and AlN due to cracking on the AlN surface, as the stresses exceed the AlN tensile strength of 270 MPa [11]. It is assumed that the layer with the highest thermal stress is the HCT failure point. In other words, it is predicted to be the failure mode where the copper on the AlN delaminates.

On the other hand, the solder layer is also subjected to thermal stress, and at the same time to strain. Therefore, failure modes due to solder crack growth may occur. In the next section, the dominant failure mode is identified by actual HCT results.

B. Heat cycle test result

To evaluate the prediction from von Mises stress simulation, actual samples were fabricated and failure points after HCT were analysed. Fig. 7 shows the test results with sample pictures SAM images of the interface of copper layers and AlN substrate, and 2 solder layers under large (AlN) and small (Al2O3) DBC substrates in Fig. 1(b).

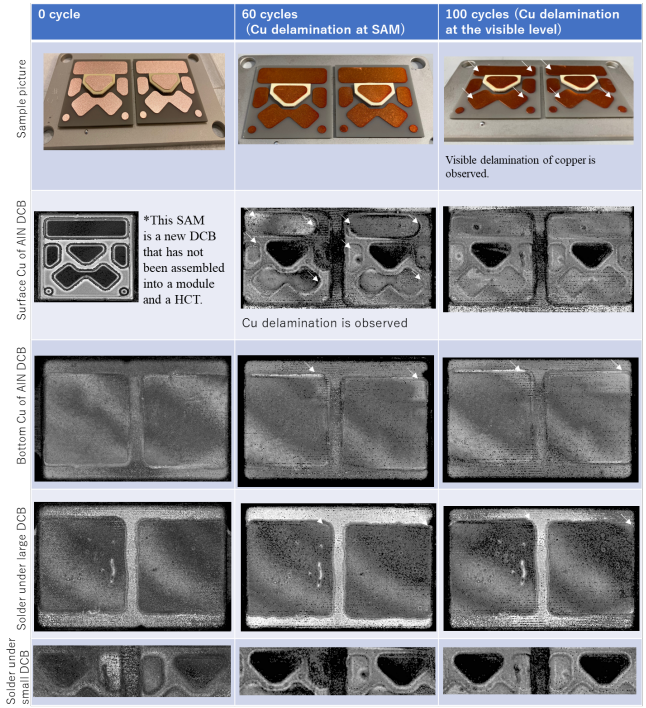

Fig. 7. Actual sample measurement results of HCT until 100cycles

Upon closer inspection of SAM images obtained, it was revealed that the delamination phenomena started at the edges of some copper patterns from the AlN surface as the HCT cycles increased from exceeded 60 cycles. These results indicated the main HCT failure mode in this module structure is copper delamination from the AlN surface. This is considered to be the result of delamination between copper and AlN, as shown the simulation in Fig. 6, developing to a level observable by SAM at the end of HCT 60 cycles and to a level of copper pattern delamination that can be observed visually at the end of HCT 100 cycles. However, there were no delaminations of the copper at the center copper pattern that has stacked ceramics after 100 cycles. It is proven that copper patterns on AlN have different driving force of peeling during HCT. In addition, SAM observations showed no significant degradation of the solder layer up to 100 cycles. A slight white contrast can be seen at the edge of each pattern, but it is difficult to determine whether this is due to contrast changes caused by degradation or measurement error due to the unclear contrast.

In order to estimate all failure and degradation points for this module, further HCT was performed on the samples shown in Fig. 7, and detailed SAM images with larger fractures at the end of 500 cycles are shown below Fig. 8. These SAM observations were conducted after HCT from the topside which allows better contrast since samples can be scanned without going through the AlSiC composite base plate first. These measurements were not possible during HCT testing since the immersion of the DBC layers into water for SAM scanning might have affected the failure mode development.

As a result, the subsequent SAM investigations confirmed the massive delamination of the top copper islands. Only the black spots on the copper islands indicate points of no delimantion on the copper islands. (yellow arrows in Fig. 8 (b)) In addition, degradation was identified at the pattern edges indicated by red arrows in Fig. 8 (b) and shown by white contrast. Note the timing of the gating giving the contrast points marked by red arrows in Fig. 8 (b) corresponds to the interface between the bottom copper and the lower solder layer in these parts of the image. As shown in Fig. 8 (c), the SAM result of the copper layers of DCB bottom side was observed no degradation between the ceramic and the copper layer. On the other hands, Fig. 8 (d) the SAM image of the solder layer between the DCB and base plate shows degradation that appears to be crack growth from the edge. Therefore, top side SAM data in Fig. 8 clearly shows that copper delimantion is not occurring at the bottom copper pattern. SAM observation from the bottom of samples is not a good way to asses this once solder degradation has been observed.

The results suggest that the dominant failure mode occurring in the early stages of the HCT cycle is delamination of some copper layers on the AlN surface, with solder degradation also occurring in addition at a later stage in the HCT tests. This result is consistent with the failure mode of the common module (Fig. 1 (a)), where solder degradation and copper delamination of the DCB occur simultaneously, at which point copper delamination becomes the dominant failure mode [11]. The results show that the soldered copper pattern on the backside of the DCB does not delaminate unlike the copper pattern on the surface, causing degradation of the solder layer. This result is identical to the failure mode identified in conventional modules [21]. In addition, a copper pattern on the surface is also soldered to another smaller DCB substrate in the module studied here. No degradation of the soldered copper pattern was observed because the solder was considered to be small and of high HCT capability.

Accordingly, the dominant failure point for this module in HCT is the copper layer delamination from the AlN. This is consistent with the interface with the highest thermal stress

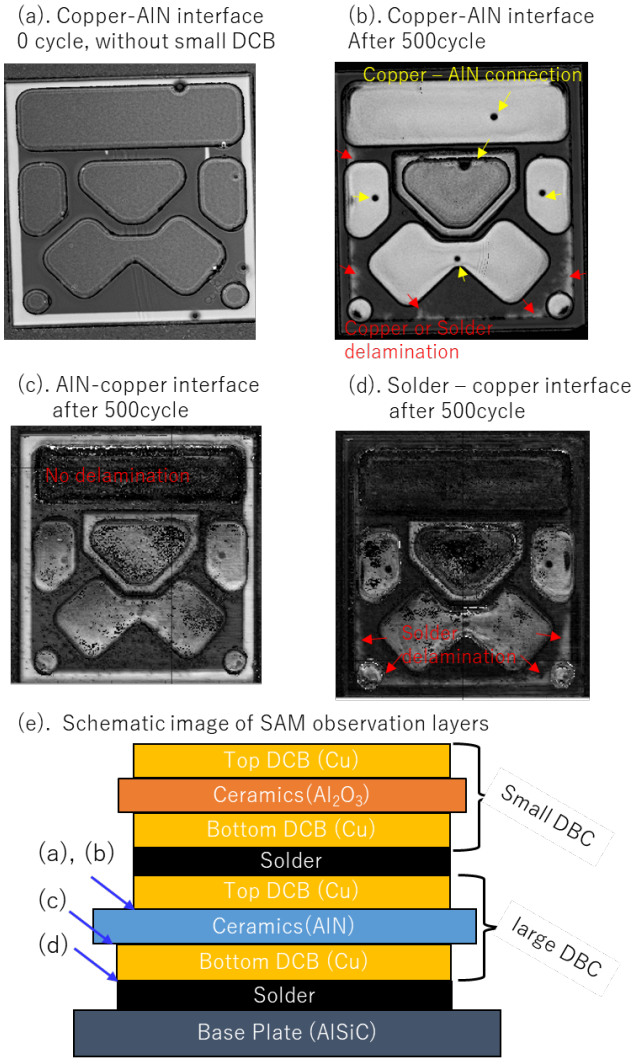

Fig. 8. Detailed SAM images after HCT (a). Copper-AlN interface on the top side at 0 cycle (without a small DCB), (b). Copper-AlN interface on the top side after 500 cycles, (c). AlN-copper interface on the bottom side after 500 cycles, (d). Copper-solder interface after 500 cycles, (e). Cross sectional image of SAM observation layers

in the von Mises stress analysis. There are no difference in the failure mode between the this DCB stacked module and conventional one.

On the other hand, the surface copper delamination identified after 100 cycles was only observed in some parts of patterns. In particular, the von Mises stress distribution in Fig. 6 shows strong thermal stresses on the copper patterns under the small DCB substrates and bottom side of DCB substrates, which are not actually delaminated in the visible level even after 500 cycles. Therefore, assuming that von Mises stress analysis, which is effective for thermal stress analysis due to CTE mismatch between different materials, is not suitable for predicting the dominated failure points of HCT, i.e. where optical visible level delamination occurs between copper patterns, the parameters for predicting failure points by 3D simulation are further investigated.

In the next section, it will be discussed how to estimate from thermo-mechanical simulations the difference between copper patterns in which optical visible-level delamination occurred and those in which it did not. This means that the simulation will validate a method for estimating copper patterns that are at high risk of developing to a visible level delamination between the copper and the AlN.

C. Failure point prediction from thermo-stress simulation

To predict the failure point by the 3D thermo-stress simulation, the peeling stress (same with normal stress to the Y-axis direction [22]) of the copper as a more practical parameter than von Mises stress was tested. Fig. 9 shows the comparing result between the von Mises stress and Peeling stress of surface copper layers on AlN. In order to compare their intensity distributions, the line profile of stress was compared. The stress values shown where normalised to maximum value along the individual line profiles.

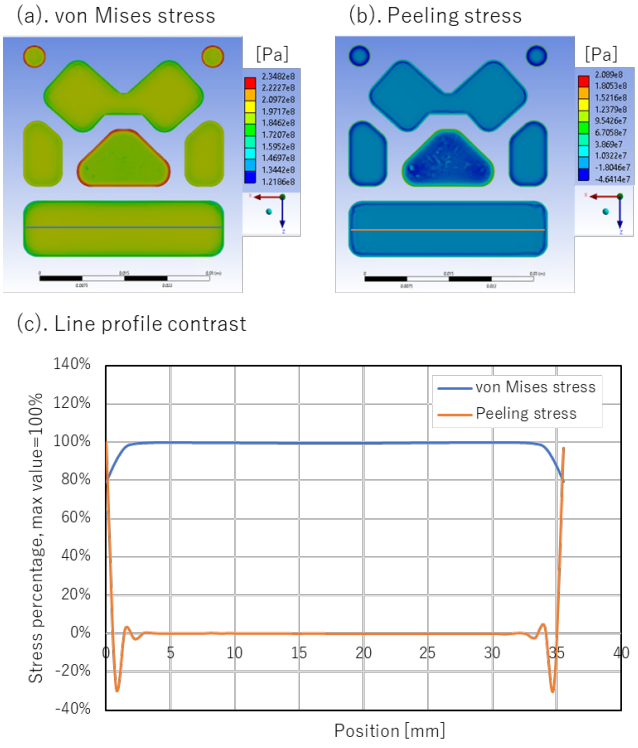

Fig. 9. Comparison of von Mises stress and peeling stress (a). von Mises stress distribution of copper patterns, (b). Peeling stress distribution of copper patterns, (c). Line profile comparison of relative line profile stress distribution

Comparison of von Mises stress and peeling stress distributions reveals that peeling stress is a good representation of the actual failure phenomena. This is because the measured results in Fig. 7 and 8 suggest that delamination progresses from the edge of the copper pattern, and the peeling stress demonstrates the highest stress distribution on the pattern edges. Compared to von Mises stress, which calculates stress in all directions as a scalar quantity, peeling stress shows a greater contrast between the delaminated area (copper pattern edge) and other

areas (copper pattern centre) because it shows stress in the direction of copper delamination. The contrast of the peeling stress makes it easier to estimate the copper delamination point from the AlN substrate. This means that peeling stress analysis is better suited than von Mises stress to describe the delamination progression from the edge of the copper pattern, as confirmed by actual measurements. On the other hand, it is difficult to distinguish between visible delaminated and non-visible delaminated copper patterns as indicated by actual measurements from even with these thermo-mechanical stresses analysis.

Upon closer inspection of delaminated copper patterns, they were larger in size than the other patterns. Therefore, the shape change of each copper pattern due to thermo-mechanical stress was investigated from the 3D thermo-mechanical simulation. Fig. 10 below shows the simulation results of shape deformation value of Y-axis direction at the the AlN top and bottom copper patterns. (-40°C : the shape deformation value was the largest.) In this figure, shape changes are shown on a larger scale than the actual values to make it easier to understand the direction of shape change.

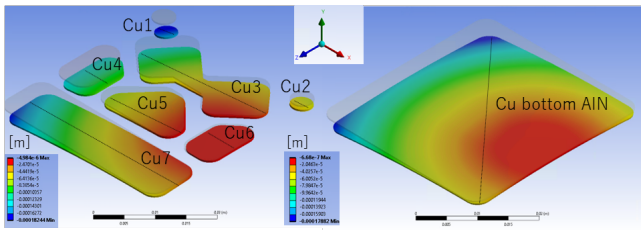

Fig. 10. The simulation results of shape deforming value for every copper patterns

To further quantitatively evaluate the shape change value for each copper pattern, the shape difference from the initial shape was calculated in terms of the angle made by the pattern before and after the change due to thermo-mechanical stress : the shape deforming angle. An example of the calculation of a pattern shape deforming angle is shown in Fig. 11 below.

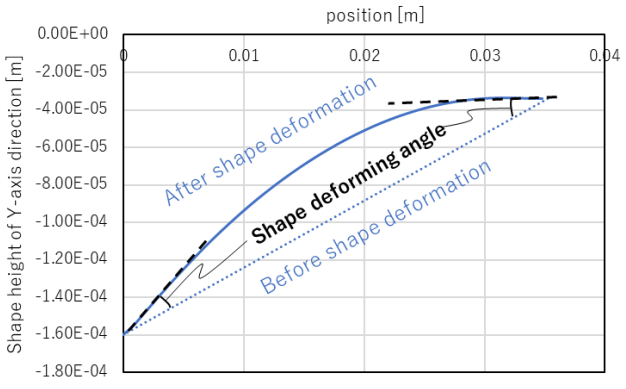

Fig. 11. shape deformation angle definition on Cu7 in Fig. 10

For the pattern shapes before and after the shape deforming by thermal stress, their height line profiles are plotted on the same graph. The angle formed by the pattern after the shape change with respect to the initial shape (straight line) was calculated. This was calculated by finding the tangent line made by the pattern after the shape change at the nodes made by the two patterns before and after the shape change, and the angle between the tangent line and the initial shape was determined from the following equation.

$$tan\theta = \frac{tan\beta - tan\alpha}{1 + tan\beta tan\alpha} \tag{1}$$

θ is the shape deforming angle, and $tan\alpha, tan\beta$ are slopes of 2 lines.

Fig. 12 below shows the shape deforming angle for all copper patterns that are calculated by (1).

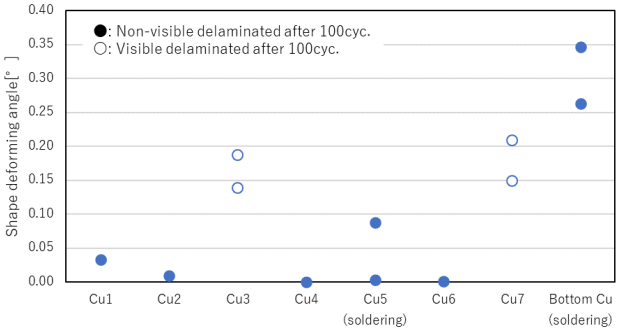

Fig. 12. Shape deforming angle calculation result of every copper patterns

Cu 3 and Cu 7, where delamination occurred after 100 cycles, showed a larger shape change angle during HCT than the other copper patterns. On the other hand, Cu 5 and Bottom Cu of AlN showed their large shape change angles but did not show visible delamination in the actual test results (in Fig. 7). This is considered to be because both of these two copper patterns are laminated by the AlN substrate and the solder layer, and the copper patterns are fixed by solder, especially in the direction of delamination, so that no visible delamination of the copper pattern occurred.

The results indicate two parameters that predict the location of copper delamination. First, it is the peeling stress distribution which represents the aspect that pulls the copper-AlN bond separation in the non-visible level delamination. On the other hand, it is the pattern of large shape deformation due to thermo-mechanical stresses that causes visible level delamination. However, if the copper pattern is fixed by solder, no significant visible level delamination occurs in spite of observing solder layer degradation.

From these results, the risk estimation of HCT failure locations by thermo-mechanical stress simulation is estimated from the calculation of peeling stress and shape deforming angle only for the unsoldered copper pattern. In other words, copper patterns with a relatively high shape deforming angle can be assumed to cause earlier copper pattern delamination than others, and the delamination initiation point is the point where the peeling stress distribution in the pattern is high

provided they are not soldered to additional adjacent layers. However, a different failure mode, solder degradation was observed for soldered copper patterns after larger HCT cycles. This means that the rate of progression of solder degradation during HCT cycles may be slower for copper pattern peeling, but the rate of progression of failure modes for these different materials could not be predicted by the 3D thermo-mechanical stress simulations in this paper.

IV. Conclusion and future works

In this research, practical method to predict the HCT failure point of power modules with a DCB stacked structure was proposed by 3D thermo-mechanical simulation.

At first, a two-dimensional analysis of the von Mises stress distribution between each module component suggests that the interface between the AlN and copper layers may be the structural weak points that are subject to the highest thermo-mechanical stress.

Next, the HCT results from the actual sample showed that the dominated failure point was the copper pattern on the AlN and that visible delamination occurred in a specific pattern. They were observed as an earlier and more significant failure than the solder degradation at the DCB-base plate solder. The experimental results suggest that both copper pattern delamination and solder degradation, which were previously reported as failure modes of HCT, occur in the present module, and that copper pattern delamination is the dominant failure mode with a faster rate of progression.

The prediction of the copper pattern delamination point, which is the dominant failure mode, by simulation was attempted using the peeling stress and shape deforming angle obtained from thermo-mechanical stress simulation. The peeling stress distribution of copper patterns well represents the aspect of delamination from the AlN of some copper patterns (delamination progression from the pattern edge). On the other hand, it was found that the parameters separating visible and non-visible delamination were the presence or absence of fixation of the copper pattern by the solder layer and the magnitude of the shape change of the copper pattern due to thermo-mechanical stress. However, the prediction of delamination locations by this shape change simulation is only applicable to unsoldered copper patterns.

The results may be applicable to the shape design of the power module design, especially of the surface (the surface on which the chip is mounted), e.g. as it reduces the shape of the copper pattern so that the shape change due to thermal stresses is smaller. On the other hand, prediction of failure points for all structures of the module, including soldered copper, is not possible with these results. This requires a physical model that can assess the rate of progression of two different failure modes; solder degradation rate and copper delamination rate, and compare them within a module. This is the future challenge based on this result.

V. ACKNOWLEDGMENT

This research is carried out as a part of the Center of Digitalized Electronics (CoDE) project at Aalborg university, funded by the Poul Due Jensen Foundation (Grant number 2020-070).

References

[1] Jeffrey B. Casady, Vipindas Pala, Daniel J. Lichtenwalner, Edward Van Brunt, Brett Hull, Gang-Yao Wang, Jim. Richmond, Scott T. Allen, Dave Grider, John W. Palmour, “New generation 10kV SiC power MOSFET and diodes for industrial applications,” Proceedings of PCIM Europe 2015

[2] Asger Bjørn Jørgensen , Thore Stig Aunsborg, Szymon Beczkowski, Christian Uhrenfeldt, Stig Munk-Nielsen, ”High-frequency resonant operation of an integrated medium-voltage SiC MOSFET power module”, IET Power Electron., 2020, Vol. 13 Iss. 3, pp. 475-482, 2020

[3] Jannick Kjær Jørgensen, Dipen Narendra Dalal, Szymon Beczkowski, Stig Munk-Nielsen, Christian Uhrenfeldt, “Multi-chip Medium Voltage SiC MOSFET Power Module with Focus on Low Parasitic Capacitance.” CIPS 2020 - 10th International Conference on Integrated Power Electronics Systems, 2020

[4] Josef Lutz, Heinrich Schlangenotto, Uwe Scheuermann, Rik De Doncker, ”Semiconductor Power Devices Physics, Characteristics, Reliability”, Springer, p.390-392, 2011

[5] Josef Lutz, Heinrich Schlangenotto, Uwe Scheuermann, Rik De Doncker, ”Semiconductor Power Devices Physics, Characteristics, Reliability”, Springer, p.380-383, 2011

[6] Fuji Electric Co., Ltd., ”Fuji IGBT modules application manual chapter 11 reliability of power module”, REH984e p.11-3, 2017

[7] Asger Bjørn Jørgensen, Stig Munk-Nielsen and Christian Uhrenfeldt, ”Overview of Digital Design and Finite Element Analysis in Modern Power Electronic Packaging”, IEEE Transactions on Power Electronics, 35(10), 10892- 10905., 2020

[8] SEMIKRON International GmbH, ”Application Manual Power Semiconductors”, p.118, 2015

[9] Robert Darveaux, ”Effect of simulation methodology on solder joint crack growth correlation and fatigue life prediction”, Journal of Electronic Packaging Vol. 124, p.147-154, 2002

[10] Gary Chi, Ian Chen, Andy Liao, ”Development of TCT Life Prediction Model of Solder for Power Module”, Proceedings of PCIM Europe 2019, 7-9 May 2019, Nuremberg, Germany

[11] L. Dupont, R. Meuret, Z. Khatir, B. Parmentier, S. Lefebvre, S. Bontemps, “Evaluation of thermo-mechanical stresses of a power module dedicated to high temperature applications,” Proceedings of International Conference on High Temperature Electronics, Paris, 2005

[12] Bassem Mouawad, Jianfeng Li, Alberto Castellazzi, C. Mark Johnson, ”On the reliability of stacked metallized ceramic substrates under thermal cycling”, Proceedings of CIPS 2018 10th International Conference on Integrated Power Electronics Systems

[13] M. Bouarroudj, Z. Khatir, S. Lefebvre, L. Dupont, ”Thermo-mechanical investigations on the effects of the solder meniscus design in solder joint lifetime for power electronic devices”, Proceedings of 2007 International Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems. EuroSime, 2007

[14] Tingrui Gong , Feng Qin, Xinzhu Yan, Lei Gao, Yingkun Yang, Zhicheng Lei, Haoshu Tan, Juntao Li, ”Thermo-mechanical optimization of ceramic substrate with through ceramic vias by Taguchi-Grey method”, Microelectronics Reliability, Volume 132, 114535, 2022

[15] Borong Hu , Jose Ortiz Gonzalez, Li Ran, Hai Ren, Zheng Zeng, Wei Lai, Bing Gao, Olayiwola Alatise, Hua Lu, Christopher Bailey, Phil Mawby, ”Failure and Reliability Analysis of a SiC Power Module Based on Stress Comparison to a Si Device”, IEEE Transaction on device and materials reliability, vol.17, No. 4, 2017

[16] Mingxing Dua, Qiuya Guoa , Ziwei Ouyanga , Kexin Weia , William Gerard Hurley, ”Effect of solder layer crack on the thermal reliability of Insulated Gate Bipolar Transistors”, Case Studies in Thermal Engineering 14, 100492, 2019

[17] CPS Technologies, ”AlSiC IGBT Baseplates, AlSiC 9 Material Properties”, datasheet

[18] Mohammad Motalab, Zijie Cai, Jeffrey C. Suhling, Pradeep Lall, ”Determination of Anand constants for SAC Solders using Stress-Strain or Creep Data”, Proceedings of 13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2012

[19] Jasbir Bath, ”Lead-Free Soldering” New York, USA, Springer, p.93., 2007

[20] Espec, ”SH, SU specs(SH-262)”, CAT. NO.13111-T2112

https://www.espec.co.jp/english/products/catalog/sh
(November 7th, 2022 viewed)

[21] Laurent Dupont, Zoubir Khatir, Stéphane Lefebvre, S. Bontemps, "Effects of metallization thickness of ceramic substrates on the reliability of power assemblies under high temperature cycling", Microelectronics Reliability, 46 (9) 1766-1771, 2006

[22] Yiyi Chena, Bo Lia, Xin Wanga, Yuying Yana, Yangang Wangb, Fang Qi, "Investigation of heat transfer and thermal stresses of novel thermal management system integrated with vapour chamber for IGBT power module," Thermal Science and Engineering Progress, vol. 10, pp.73-81, 2019