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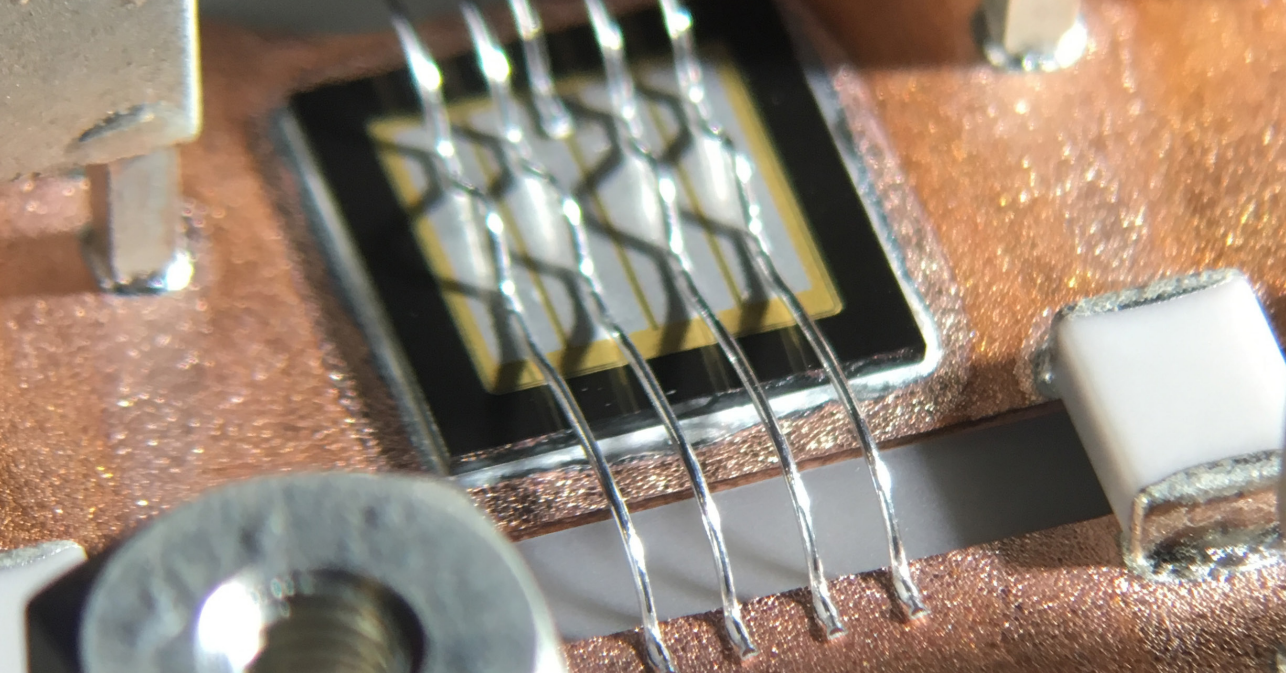

PACKAGING OF WIDE BANDGAP POWER SEMICONDUCTORS USING SIMULATION-BASED DESIGN

BY
ASGER BJØRN JØRGENSEN

DISSERTATION SUBMITTED 2019

AALBORG UNIVERSITY
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Packaging of Wide Bandgap Power Semiconductors using Simulation-based Design

Ph.D. Thesis

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in honor of my late father...

Abstract

Power electronics are used for the conversion of electric energy in applications such as wind turbines, pumps, solar arrays and many industrial processes. The main unit of any power electronic device is the semiconductor die which traditionally has been made from silicon. For past decades wide bandgap semiconductors, such as silicon carbide and gallium nitride, have matured. They can be operated at higher voltages, higher frequencies and reduce losses by switching faster. To fully utilize these benefits the semiconductor die must be properly packaged and integrated with other parts of the power electronic converter.

The thesis initially presents a simulation framework for detailed modelling of electro-thermal behavior of 3D power module packaging and printed circuit board stackups used in integrated packaging. This enables rapid digital prototyping and accurate prediction of the performance, prior to manufacturing and testing of the real device.

The thesis studies several aspects related to packaging of wide bandgap semiconductor power semiconductors. The parasitic capacitive coupling in conventional power modules is analyzed with new medium voltage dies that switch at high $\mathrm{d}v/\mathrm{d}t$. A concept is investigated where the gate driver is integrated in the power module to enable fast switching and high power dissipation of the gate driver. The gate driver is operated at 2.5 MHz and its thermal resistance is reduced by 45 % compared with conventional placement on a printed circuit board outside the package. The experience gained from the two studies is combined to design and test the worlds first 10 kV SiC MOSFET power module driven in the MHz-range.

A new power module structure is proposed for new gallium nitride power devices, which is significantly easier to manufacture compared with other integrated structures. The package has a power loop inductance experimentally verified at 2.65 nH and switching transients of 64 V/ns without any overshoot. The new power module with gallium nitride devices is more expensive than conventional silicon power modules, but reduces switching losses up to 75 - 90 % and thus is regarded a viable choice for future power electronics applications.

Dansk resumé

Effektelektronik benyttes til konvertering af elektrisk energi i applikationer som vindmøller, pumper, solpaneler og i mange industrielle processer. Hjertet i effektelektronikken er halvlederchips som de sidste mange årtier har været lavet af silicium. I de senere år er nye halvledermaterialer blevet modnet, herunder siliciumkarbid og galliumnitrid. De kan opereres ved højere spændinger, højere frekvenser eller sikre lavere skiftetab end traditionelle siliciumchips. Men disse fordele kan kun udnyttes hvis halvlederen indpakkes rigtigt og integreres med andre dele af effektelektronikken.

Indledningsvis præsenteres en simuleringsprocedure, som giver mulighed for en detaljeret beskrivelse af både elektriske og termiske aspekter af selv avancerede 3D strukturer og printlag i integreret effektelektronik. Det tillader hurtig udvikling af digitale prototyper og præcist design af elektronikkens opførsel, inden de fremstilles og testes fysisk.

I denne afhandling undersøges forskellige aspekter i forbindelse med indpakning af de nye halvlederchips til effektelektronik-formål. Problemer med kapacitiv kobling i traditionel elektronikindpakning undersøges med de nye højspændings-chips. Herefter indlejres styrekredsen tæt på halvlederchippen, hvilket sikrer hurtig tænd/sluk karakteristik, samtidig med at styrekredsens termiske modstand nedsættes med 45 %. Erfaringerne med højspændings-chips og indlejringsteknikken kombineres, og afhandlingen præsenterer verdens første forsøg på at drive en 10.000 V siliciumkarbid halvlederchip ved frekvenser i MHz-området.

Slutteligt præsenteres en helt ny indpakningsstruktur af galliumnitrid-baserede chips, som er meget nemmere at fremstille end den nuværende førende teknologi. Indpakningen har lav induktans på 2.65 nH hvilket sikrer at chippen kan tænde/slukke med spændingshældninger på op til 64 V/ns helt uden oversving i blokeringsspændingen. Den nye indpakning baseret på galliumnitrid-halvledere er dyrere end traditionel silicium-teknologi, men kan reducere skiftetab med op til 75 - 90 %. Derfor anses den nye teknologi som et realistisk valg i fremtidens effektelektroniske apparater.

Contents

Preface

This thesis is prepared at the Department of Energy Technology, Aalborg University as partial fulfillment of the PhD degree. The research was conducted in the time period between August 2016 and April 2019. The research is funded by the Intelligent and Efficient Power Electronics (IEPE) project, Advanced Power Electronics Technology and Tools (APETT) project and the Department of Energy Technology, Aalborg University.

The thesis was supervised by Professor Stig Munk-Nielsen and Associate Professors Christian Uhrenfeldt and Szymon Beczkowski. Part of the research was conducted at the FREEDM Systems Center at North Carolina State University, USA during Fall 2018 under supervision of Professor Douglas C. Hopkins, Head of the Packaging Research in Electronic Energy Systems (PREES) laboratory. I would like to express my gratitude to all of them for their trust and giving me the freedom to pursue new research ideas along the way. I would also like to thank the industrial partners of the IEPE and APETT projects for valuable discussions and feedback throughout the project period. I appreciate the discussions with Niels Høgholt Petersen and Søren Jørgensen from Grundfos A/S and their contributions to the research. I would like to thank my colleagues at the Department of Energy Technology, Aalborg University for making it a great and inspiring place to work.

Special thanks to my family for their support in times where some things in life are more important than research.

Asger Bjørn Jørgensen

Part I

Extended summary

Chapter 1

Introduction

Power electronics is used in the conversion of electrical energy. It is employed for all power levels and includes applications such as wind turbines, photovoltaics, motor drives, pumps and lighting. Its main task is to control the flow of power from a source or to a load. This is done using a semiconductor die by switching it between its conducting and blocking state. At lower power levels (<1 kW) the semiconductor die is typically packaged as a single discrete device, and is then interfaced with other components to form a switch mode power supply (SMPS) unit [1]. At higher powers, typically several power semiconductor devices are packaged together in a standalone component called a power module. The interconnections between devices are then arranged inside the power module and only a few external terminals points are available for the end user. Achieving a good performance of the semiconductor die depends on how well it is interfaced with the other semiconductors as well as other parts of the SMPS, including gate driver integrated circuits (ICs), measurement circuitry, filter inductors and capacitors. In addition, the packaging must be designed to also ensure that the semiconductor die is cooled adequately and enclosed properly to avoid contaminants. These interactions of a semiconductor die with surrounding parts of the power electronic system are shown in Figure 1.1.

Traditionally the semiconductor die has been based on silicon (Si) material. Other advantageous wide bandgap (WBG) semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) have been known for decades without significantly impacting the market of power semiconductor devices [2], [3]. However, in recent years new low voltage (typically 650-1200 V) WBG devices with advantageous properties have been introduced to the market at competitive prices [4], [5]. When compared to Si devices, some of the advantages highlighted for new available WBG devices are higher voltage breakdown strength, higher thermal conductivity and reduced on state resistance [6]–[9]. Some advantages of the WBG semiconductor materials and the trade offs in a

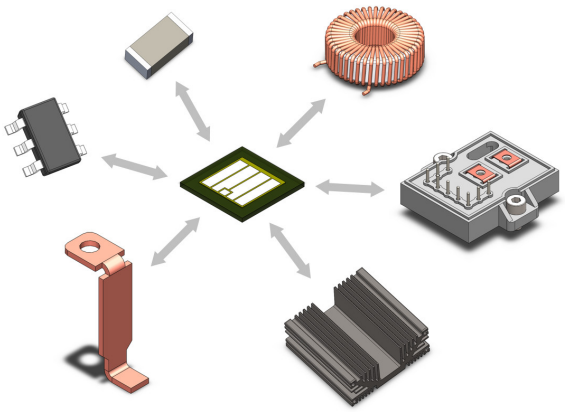


Fig. 1.1: Performance of the power semiconductor device depends on its interconnections with other parts of the power converter.

Table 1.1: Material properties for selected semiconductors [12], [13]

Material	**Si**	**SiC**	**GaN**
Band gap [eV]	1.12	3.26	3.39
ϵ, relative permittivity	11.7	9.7	8.9
μ, electron mobility $\left[\frac{\mathrm{cm}^2}{\mathrm{V \cdot s}}\right]$	1360	900	2000
E_C, critical electric field $\left[\frac{\mathrm{V}}{\mathrm{cm}}\right]$	$2 \cdot 10^5$	$22 \cdot 10^5$	$15 \cdot 10^5$

power semiconductor can be understood by studying the equation for the on resistance, R_on, of a power semiconductor. The following equation is valid for the on resistance of the drift region in a unipolar device such as the Schottky diode, but also applies to MOSFETs, and is given by [10].

$$R_\mathrm{on} = \frac{4 \cdot V_\mathrm{br}^2}{\epsilon \cdot \mu \cdot E_\mathrm{C}^3 \cdot A} \tag{1.1}$$

where V_br is the breakdown voltage, A is the cross sectional area. ϵ is the relative permittivity, μ the electron mobility and E_C the critical electric field of the semiconductor material. The denominator $(\epsilon \cdot \mu \cdot E_\mathrm{C}^3)$ is often referred to as the Baliga figure of merit (BFOM) of a semiconductor material [11].

For high voltage power electronics (1.1) shows that increasing the breakdown voltage of a device from 1 kV to 10 kV results in a 100x increase of R_on. Using Si as semiconductor material, this would require an impractical large die area or result in a device with too high on resistance. In recent years, high voltage SiC devices with ratings of 10 and 15 kV have been developed and made available for research teams and universities [14], [15]. By using the higher BFOM of SiC,

Wolfspeed has developed a 10 kV 350 mΩ SiC MOSFET with a die area of 8.1 x 8.1 mm [16].

Increasing the die area results in a reduction in on resistance, but to achieve high frequency operation of the device it must also be appropriately sized. Increasing the die area results in larger capacitance of the devices, such as the input and output capacitance of the device. Generally the switching time for transitioning between the on and off states increases as the output capacitance of the device becomes larger [17]. Similarly, a larger input capacitance puts more demand on the gate driving circuit as more power is required to charge and discharge the gate of the device [18]. This balance between on resistance and input capacitance is depicted by Baligas high frequency figure of merit (BHFFOM) [19], given by

$$\text{BHFFOM} = \frac{1}{R_{\text{on}} \cdot C_{\text{in}}} \tag{1.2}$$

where C_{in} is the input capacitance of the device. Due to the properties of WBG, these devices are smaller when compared with a Si device of similar voltage and current ratings. Due to the smaller die area, the WBG devices also have lower input capacitance which potentially allows operation at higher frequencies [19], [20].

Thus in summary the new WBG materials used for semiconductor devices, when compared with conventional Si devices, allows for higher voltage operation, faster switching performance and higher frequency driving. The balance between these attributes depends on the design of the semiconductor die itself. Furthermore, the benefits can only be utilized in the power electronics converter design if the semiconductor die is properly packaged and interfaced with the remaining power electronics system.

1.1 State of the art packaging

The following section reviews and presents a state of the art of packaging of power semiconductors, as packaging is identified as a key element to benefit from the advantages WBG power semiconductors potentially bring.

With Si being the dominant technology for the past decades, the most widely used power module structure is shown in Fig. 1.2. It is estimated to be used in 70 to 80 % of all power modules [4]. The assembly typically starts with a baseplate at the bottom. The baseplate ensures mechanical support and allows for mounting the power module to a heat sink, which is the reservoir used for dissipation of the generated power losses of the power module. Soldered to the baseplate is a direct bonded copper (DBC) substrate, which is a sandwich structure of a ceramic with copper on either side. The ceramic is typically aluminum oxide (Al_2O_3) or aluminum nitride (AlN). The DBC ensures electrical

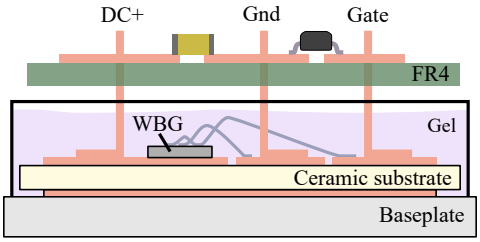


Fig. 1.2: Typical structure of a conventional power module. [Paper D]

insulation while allowing a relatively effective heat transfer from the top copper layers to the base plate [21]. The top copper layer of the DBC has tracks which routes the electrical signals and interconnects the different semiconductor dies, which are soldered to the top copper layer. For most Si power semiconductor dies, such as MOSFETs and IGBTs, the drain/collector-connection is at the bottom side and is soldered to the copper. Source/emitter and gate-connections are located on the top side of the die. The top side of the die is interconnected with the DBC top side copper using bond wires. The bond wires are typically attached to the die metallization and the DBC copper by ultrasonic welding and does not require soldering. Power terminals to interface with the external circuits are either soldered or ultrasonic welded to the top side copper. Following these steps the power module is encapsulated typically with epoxy or silicone gel. The encapsulation has a higher electric breakdown strength than air, and thus allows a more compact power module design with reduced risk of partial discharges or flashovers. Additionally, the encapsulation protects the semiconductor dies from humidity and other contaminants. Connected to the power module terminals on the outside is a printed circuit board (PCB), which holds the other important electrical components that is required to operate the power module, such as DC-link capacitors, gate driver circuit and voltage/current measurements. The advantage of this power module structure is its capability to dissipate high powers through the large baseplate and its attached heat sink. Also, the use of DBC and encapsulation enables for high voltage design [22]. Its disadvantage is its large parasitic inductances due to the long copper terminals, single-layer copper traces and the use of bond wires. This is a reported as an issue in terms of utilizing the fast switching speed of the new emerging WBG power devices. Power modules using this conventional structure typically has a parasitic inductance in the power loop of 10-30 nH [23]–[26]. Such high inductance results in large voltage overshoots and ringings when subjected to the high $\mathrm{d}i/\mathrm{d}t$ produced by the WBG power devices in some applications [27]. Similar noise issues may arise during fast switching of the gate-source loop because the gate driver is located outside the power module [28]. To fully utilize the fast switching capabilities of WBG power devices, research has been put into new power module packaging structures which minimize the

parasitic inductance in both the power and gate loop. From a theoretical point of view the optimum solution is to include the gate driver structure directly in the semiconductor switch structure. But such a solution is not economical, as the structure required to do the driver is more intensive than making the power structure [29]. For now the performance achieved by co-packing driver and switch is deemed good enough, with new packaging concepts to narrow the gap to the theoretical limit.

A proposed structure to minimize the parasitic inductance is by embedding the power semiconductor device inside the PCB and placing the gate driver and other circuitry on the outside layers, as shown in Fig. 1.3. First of all this eliminates the use of bond wires and secondly the gate driver is placed very close to the gate of the device which it has to drive. A prototype of this concept has been presented with a power loop having only 2.8 nH of parasitic inductance [25].

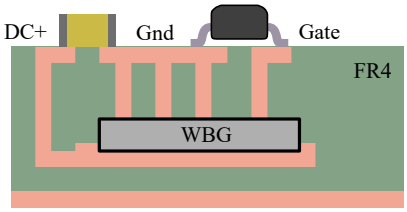


Fig. 1.3: Power module structure using PCB embedded die technology. [Paper D]

An issue of this structure is that the FR4 material has a relatively low thermal conductivity. To improve the thermal performance, designers might use larger copper planes and via arrays to distribute the generated losses to the outside copper layers. For further improvement of the thermal resistance the FR4 layers must be kept as thin as possible. However, as the FR4 layers become thinner it then may result in electrostatic issues such as partial discharge or sparking [30]. An example of this phenomenon is described by D. Kearney *et al.* during testing of a PCB embedded switching cell [31]. At 3.5 $\frac{\mathrm{kV_{rms}}}{\mathrm{mm}}$ partial discharges are detected, which for an insulation layer thickness of 130 μm corresponds to 455 $\mathrm{V_{rms}}$. The team experienced electric breakdown at approximately 14 times that voltage at an edge where field concentration occurred, as shown in Fig. 1.4. The geometry of the structure can be modified to reduce the peak electric field stress [32], but the critical dielectric field strength of the material must be obeyed. Thus while the embedded power module structure allows for a very low inductive design, it may cause difficulty in maintaining a good performance of both the thermal and electrostatic aspects simultaneously.

For good thermal performance it is advantageous to place the semiconductor device on a DBC, but it is often desired to achieve lower parasitic inductance than what is possible with the conventional power module structure. A proposed

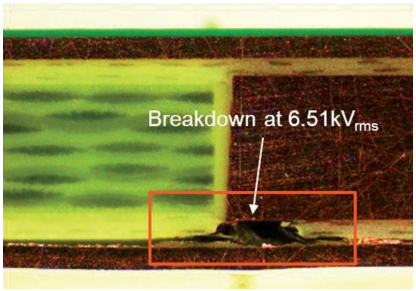


Fig. 1.4: Electric breakdown in 130 μm isolation layer of an embedded PCB solution [31].

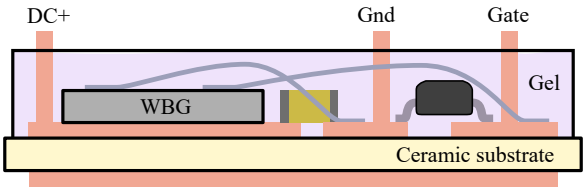


Fig. 1.5: Diagram of integrated DBC power module structure. [Paper D]

power module structure [28], [33] utilizes more of the DBC by including most of the important components inside the power module, as the power module structure shown in Fig. 1.5. Here both the semiconductor device, DC-link and gate driver are soldered to the top side copper layer, and literature presents a power loop inductance in the range of 7-11 nH [34]. Good electrostatic performance can still be obtained as the module can be encapsulated in silicone gel. Additionally, if compared with the conventional power module structure, this technology does not require any new manufacturing steps. However, it is difficult to obtain the same level of integration and compactness as with the PCB technology because the circuit is limited to the single copper layer on the top side of the DBC. [26], [35] has proposed a solution to address this issue by using a printed copper thick-film approach. While more compact circuitry can be integrated in the power module by using this approach, it is still not as dense as what is possible with PCB technology.

With the advantages and disadvantages observed from the PCB embedded and DBC integrated power module structures, a new proposed solution is to combine the two technologies [18], [36], [37]. It solves the problem of the weak thermal performance from the PCB embedded structure, while allowing a low inductive and compact design compared with the DBC. The structure is shown in Fig. 1.6. The PCB is molded directly on top of the DBC, which enables a very low inductive design reported at 1.5 nH for the power loop [38]. G. Feix *et al.* [37] have proven fast switching speeds of both gate and power loops, of the module shown in Figure 1.7(a). Using hybrid DBC and PCB technology is

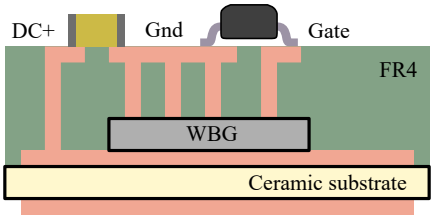
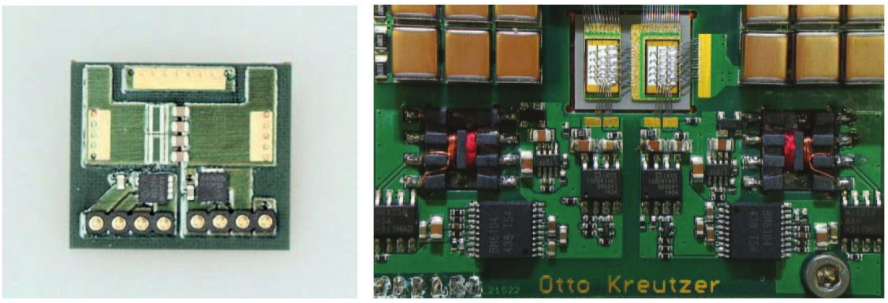


Fig. 1.6: Diagram of a PCB/DBC hybrid power module structure. [Paper D]

an effective solution to achieve low electrical parasitics, high heat dissipation and good electrostatic performance. But in terms of manufacturability the complexity is increased significantly. An alternative solution is proposed by O. Kreutzer *et al.* [18], which decreases the complexity of manufacturing, but still combines the PCB and DBC as shown in Figure 1.7(b). Instead of molding the PCB layers on top of the DBC, bond wires are used to connect the chip to the PCB. Long copper planes and terminals are avoided compared with a conventional power module structure. The bond wires inevitably adds some inductance to both the power and gate loops. However, some inductance can be allowed as there is a limit to the switching speed of the gate structure, as discussed in Section 3.2.



(a) (b)

Fig. 1.7: Two examples from Fraunhofer IZM Berlin of combinations of DBC and the PCB either (a) molded on top [37] or (b) connected by bond wires [18].

The literature review shows the various packaging approaches available to achieve high voltage operation and fast-switching of WBG power semiconductors. It has highlighted that research is put into the improvement of current power module packaging techniques. However, it also shows that packaging technology of the new WBG is far from as mature as the known silicon technology. When investigating the papers, various issues are encountered during experimental tests. The designs fail or are limited in performance due to weak electrostatic design [31], wrong gate design [18] or low thermal performance [33]. Some

challenges found in literature is that the fast $\mathrm{d}i/\mathrm{d}t$ produced by the WBG devices increase the noise originating from the device source inductance, while high $\mathrm{d}v/\mathrm{d}t$ may increase the displacement current of the Miller capacitance causing a false parasitic turn-on of a device [39], [40]. The issue is reinforced as the new WBG devices are decreasing in size meaning that they have lower input capacitance, which may make them more susceptible for noise issues such as the parasitic turn-on and ringing of the gate-source voltage. As devices become smaller and the packaging more compact it decreases parasitic inductance and capacitance in both power and gate loops. Especially reported in the case of GaN enhancement high electronic mobility transistors (eHEMTs), the result is that the resonance frequencies of power and gate loops move closer to one another, creating a scenario where it can cause for a continuous oscillatory triggering making the circuit unstable [41]–[44].

The risk of issues appearing in the experimental test phase can potentially be reduced by using a proper design method involving three-dimensional (3D) computer-aided design (CAD), multi-physics simulation, device modelling and circuit simulation. Limited usage of simulation methods prior to manufacturing may result that the performance of designs sometimes seem like a “hit” or “miss”. Further discussion and reasoning for the use of simulation tools is elaborated further in Chapter 2.

1.2 Research objectives

The project has two main research objectives. The new emerging WBG power semiconductor devices offer benefits for designers of power electronic converters. To fully utilize the benefits it is necessary to package and properly integrate the semiconductor device to achieve robust operation. To close the gap between an ideal switch and a physical semiconductor die, a fast-switching WBG device must integrated with its peripheral components, including gate drivers and DC-link capacitors etc. The first research objective is

> **To investigate and design packaging prototypes to push the operating range, improve the fast-switching or high voltage switching capabilities of WBG power semiconductors.**

To achieve the first research goal, it is necessary to understand and use accurate simulation models of both the semiconductor devices and the influence of the packaging. The second research objective is

> **To develop and build a digital design framework used for virtual prototyping of new integrated packaging solutions.**

Gaining fidelity of the combined 3D multi-physics simulations, device modelling and circuit simulation will aid in the design of working prototypes and push the performance of new power modules based on WBG semiconductor devices.

1.3 List of publications

The thesis is based on the following papers, which have also been appended at the back of the thesis.

A "Reduction of Parasitic Capacitance in 10 kV SiC MOSFET Power Modules using 3D FEM." Asger Bjørn Jørgensen, Nicklas Christensen, Dipen Narendrabhai Dalal, Simon Dyhr Sønderskov, Szymon Beczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen. *Published in "Proceedings of 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)"*, Warsaw, Poland, 2017.

B "A SiC MOSFET Power Module With Integrated Gate Drive for 2.5 MHz Class E Resonant Converters" Asger Bjørn Jørgensen, Unnikrishnan Raveendran Nair, Stig Munk-Nielsen and Christian Uhrenfeldt *Published in "Proceedings of CIPS 2018; 10th International Conference on Integrated Power Electronics Systems"*, Stuttgart, Germany, 2018.

C "High Frequency Resonant Operation of an Integrated Medium Voltage SiC MOSFET Power Module." Asger Bjørn Jørgensen, Thore Stig Aunsborg, Szymon Beczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen. *Submitted for publication in "IET Power Electronics"*, 2019.

D "A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices" Asger Bjørn Jørgensen, Szymon Beczkowski, Christian Uhrenfeldt, Niels Høgholt Petersen, Søren Jørgensen and Stig Munk-Nielsen *Published in "IEEE Transactions on Power Electronics, vol. 34, no. 3, pp. 2494-2504"*, March 2019.

E "Thermal Characteristics and Simulation of an Integrated GaN eHEMT Power Module." Asger Bjørn Jørgensen, Tzu-Hsuan Cheng, Douglas Hopkins, Szymon Beczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen *Accepted for publication in "Proceedings of 2019 21th European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)"*, Genoa, Italy, 2019.

In addition to the appended papers which are included in the thesis, there is a main authorship/co-authorship of the following papers which have been published during the PhD-project period.

1. "Novel Screening Techniques for Wind Turbine Power Converters." Asger Bjørn Jørgensen, Simon Dyhr Sønderskov, Nicklas Christensen, Kristian Linding Frederiksen, Eddy Iciragiye, Anders Eggert Maarbjerg, Stig Munk-Nielsen and Bjørn Rannestad. *Published in "Proceedings of 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)"*, Karlsruhe, Germany, 2016.

2. "Test Bench for Thermal Cycling of 10 kV Silicon Carbide Power Modules." Simon Dyhr Sønderskov, Asger Bjørn Jørgensen, Anders Eggert Maarbjerg, Kristian Linding Frederiksen, Stig Munk-Nielsen, Szymon Beczkowski and Christian Uhrenfeldt. *Published in "Proceedings of 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)"*, Karlsruhe, Germany, 2016.

3. "Switching Current Imbalance Mitigation in Power Modules with Parallel Connected SiC MOSFETs." Szymon Beczkowski, Asger Bjørn Jørgensen, Helong Li, Christian Uhrenfeldt, Xiaoping Dai and Stig Munk-Nielsen. *Published in "Proceedings of 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)"*, Warsaw, Poland, 2017.

4. "Performance Analysis of Commercial MOSFET Packages in Class E Converter Operating at 2.56 MHz" Unnikrishnan Raveendran Nair, Stig Munk-Nielsen and Asger Bjørn Jørgensen *Published in "Proceedings of 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)"*, Warsaw, Poland, 2017.

5. "Gate Driver with High Common Mode Rejection and Self Turn-on Mitigation for a 10 kV SiC MOSFET Enabled MV Converter" Dipen Narendrabhai Dalal, Nicklas Christensen, Asger Bjørn Jørgensen, Simon Dyhr Sønderskov, Szymon Beczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen. *Published in "Proceedings of 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)"*, Warsaw, Poland, 2017.

6. "Common Mode Current Mitigation for Medium Voltage Half Bridge SiC Modules" Nicklas Christensen, Asger Bjørn Jørgensen, Dipen Narendrabhai Dalal, Simon Dyhr Sønderskov, Szymon Beczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen. *Published in "Proceedings of 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)"*, Warsaw, Poland, 2017.

1.4 Thesis outline

The thesis is structured in the following way. Chapter 1 introduces the state of the art within packaging and defines the research objectives. Part of fulfilment of the research goals includes understanding the use of simulation software and tools. The simulation software and the design methodologies used throughout the thesis are presented in Chapter 2.

Chapter 3 presents several power module prototypes demonstrating packaging design changes to better utilize some benefits of the SiC devices. A 10 kV

SiC MOSFET half bridge power module, as shown in Fig. 1.8(a), has been designed to study the influence of parasitic capacitances for high voltage and high $\mathrm{d}v/\mathrm{d}t$ operation. The design of a power module with low parasitic capacitance is the topic of Section 3.1, and the design and experimental validation is published as the main content of Paper A. The work was carried out as part of the Intelligent and Efficient Power Electronics (IEPE) research project.

To study the design of high frequency power electronics, a SiC MOSFET power module with integrated gate driver circuit was designed, as shown in Fig. 1.8(b). The work was carried out as part of the Advanced Power Electronics Technology and Tools (APETT) project, as a contribution of how to achieve MHz-range switching using conventional gate driver ICs. The design, simulation and validation at 2.5 MHz in a Class-E converter of the designed power module is published in Paper B.

The experience gained from working with both the high voltage and the high frequency packaging is combined in Section 3.3. A medium voltage, high frequency power module based on a 10 kV SiC MOSFET die and integrated gate driver is designed as shown in Fig. 1.8(c) and tested. It is the first documented attempt of operating a 10 kV SiC MOSFET die in the MHz range, and the work is included in Paper C

Chapter 4 presents the work on a fast-switching GaN eHEMT power module, which uses a new integrated packaging structure. The power module is shown in Fig. 1.8(d). Due to its compact form factor it is carefully simulated and tested for both its electrical and thermal performance, which is included as the main content of Paper D and E. The research is part of the APETT project. Due to the successful results a new three phase power module prototype, as shown in Fig. 1.8(e), is build and is currently being prepared for tests in a real pump application.

The thesis is concluded in Chapter 5 and the main research contributions are summarized. Future work is discussed in Section 5.1.

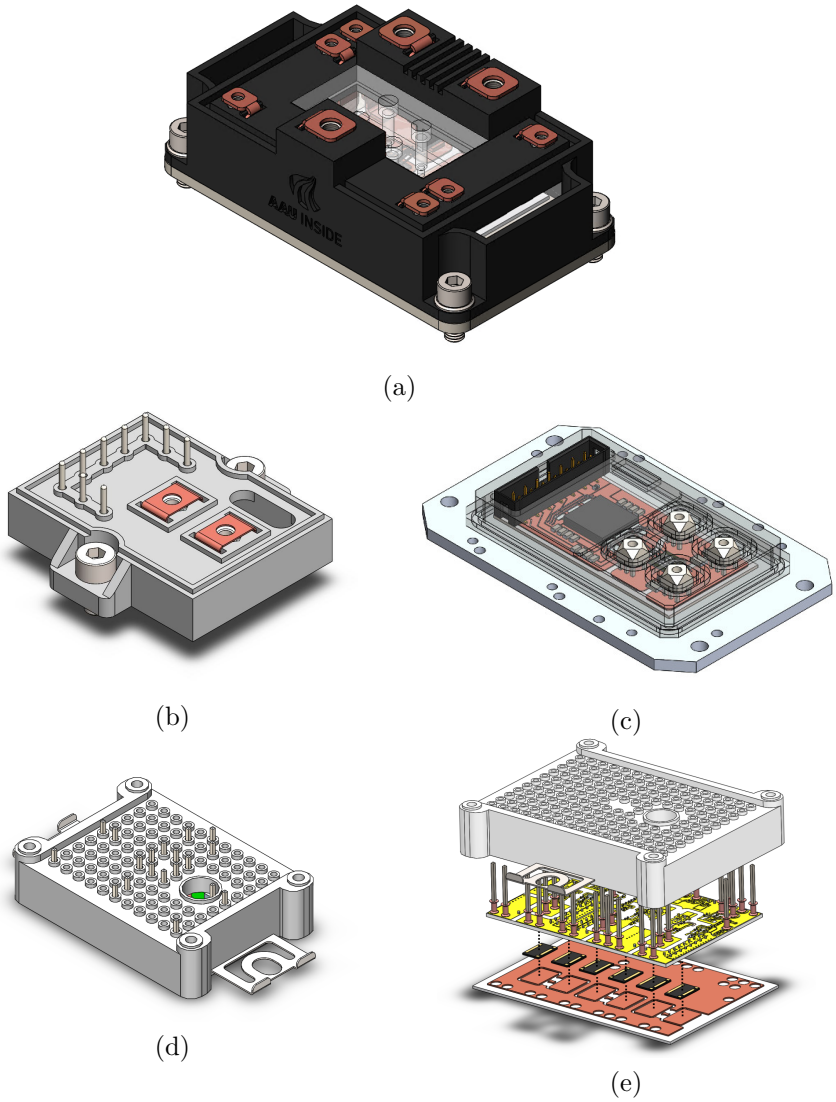


Fig. 1.8: 3D renderings of power module designs developed throughout the project, including: (a) 10 kV SiC MOSFET halfbridge power module (b) SiC MOSFET RF power module with integrated gate driver (c) integrated RF power module with 10 kV SiC MOSFET die (d) integrated GaN eHEMT full-bridge power module (e) exploded view of integrated GaN eHEMT three phase power module.

Chapter 2

Simulation tools & methods

Simulation tools have been used extensively for the presented research and designs in this thesis. This chapter summarizes the motivation for using the simulation softwares and presents how they are used[1]. The chapter concludes with the presentation of an overall simulation framework, that has been used throughout the project period for the design of power modules. The simulation tools mainly include finite element method software suites to solve problems involving complex geometries exposed to physics such as electromagnetic fields, electrostatics, heat transfer and thermomechanical stress. The use of such simulations have become more valuable and more easily accessible due to a number of reasons.

Computing power The number of computations per second is continuously increasing, resulting in reductions of the simulation time. Combined with increasing memory available it allows for continuously larger and more complex geometries to be solved for. To increase simulation speed and being able to store the problem in memory, users have often been required to reduce and simplify the geometries to only small sections or cross-sectional 2D problems to study. The importance of having knowledge and understanding the physics on a simplified model cannot be understated. However, it also limits the trust a designer has of how well the simplified model represents the real-world behavior. With the availability of work stations with quad core computing power and memory of 32 GB/64 GB often allows for fast solving of the original geometry with only minor simplifications [45].

[1]Some of the software is chosen as it is regarded the superior software for the specific problem to solve, while in other cases the choice of software is based solely on prior experience and what licenses are available. Note that the author has no personal interest or benefit in the promotion of any of software packages.

Difficulty of measuring Getting measurements on wide bandgap semiconductor devices which are encapsulated and integrated in compact power modules and packages is difficult. To utilize the fast-switching speeds of SiC and GaN, the inductance of commutation loops are as low as only a few nH. Most current sensing techniques are intrusive as they need to be inserted in or around the current path, which may add up to several nH of insertion inductance in the path and thus deteriorates the fast switching performance that was aimed for in the first place [46]–[49]. Due to the compactness of many power modules and integrated packages, measurement of internal voltages in the circuit such as gate-source voltages may be impossible. Likewise, prediction of issues such as cross-coupling between internal PCB layers, ground plane bounce etc. can be hard or impossible to measure [50], [51], in which case simulation of the original geometries is an important tool for designers.

Accuracy of measurements In the cases where measurement of the current and voltages is possible, the accuracy of such measurements is of concern. The reason is that the devices are switching so fast and has frequency content of hundreds of MHz. Voltage probes rated at several hundreds volts are typically limited by a bandwidth in the range of 100-200 MHz for differential probes [52]–[54] and 400-500 MHz for passive probes [55]–[57]. When measuring signals which are approaching this limit, designers may start to lose trust in their measurements [58]. For this reason, a second layer of validation through accurate simulation of the original geometry is useful to validate that the experimental measurements are correct.

Digital prototyping A simulation based design approach has been used to enable rapid digital prototyping, where several iterations of designs are quickly simulated and tested, before settling on a final design to manufacture. Silicon technology and power modules have been matured over decades, which provides a big pool of knowledge and many previous designs. However, when using new WBG semiconductors there is less experience and limited designs to build upon. Due to the duration of this PhD project, it was considered time inefficient to build several iterations of prototypes before landing the final design.

2.1 Electromagnetic finite element software

One of the main tasks for this thesis is to extract the electrical parasitics in terms of resistances, inductances and capacitances in the designed 3D power module structures. A widely used simulation software suite for extraction of electrical parasitics is the ANSYS Electronics Desktop. The ANSYS Electronics Desktop software suite includes three environments: ANSYS Maxwell, ANSYS Q3D Extractor and ANSYS HFSS - each specifically designed to speed up simulations

for different areas of electromagnetic problems encountered in power electronics. The difference is what approximations are used to ensure convergence and enabling faster solving without necessarily suffering significant reduction in accuracy for a type of problem. **ANSYS Maxwell** is designed for simulation of low frequency magnetics such as inductors, transformers or induction machines. It includes non-linear material properties and temperature dependencies [59]. **ANSYS Q3D Extractor** is used for higher frequencies, typically in range from DC to <1.5 GHz. It solves near-field magnetic and electric fields to calculate inductive and capacitive coupling between conductors. Material properties are linear and solving of magnetic and electric fields are decoupled problems. These simplifications allows calculation of RLC-parasitics for rather complex geometries often found in power modules and multilayer PCBs [60]. **ANSYS HFSS** is designed for very high frequencies, typically from MHz to hundreds of GHz, and solves the coupled magnetic and electric fields propagating into far field. It is well suited for simulating antenna structures or assess electromagnetic interference issues for different packages or casings [61].

For this PhD thesis the ANSYS Q3D Extractor has been used as the main software tool for computing the RLC parasitics encountered in power module packaging and PCBs. When reviewing literature using ANSYS Q3D Extractor [22], [62]–[67], it becomes apparent that different simulation approaches are employed within the ANSYS Q3D Extractor tool itself. The following paragraphs describe the different simulation methodologies used and discusses the advantages/disadvantages.

Method A In this method the inductances are calculated piece-wise for each conductor/trace on the circuit, as shown in Fig. 2.1. For the TO 247 4-pin device in this example, the model simply includes the extraction of the self-inductance for each individual lead. The advantage of this method is that setting up the simulation is simple and solving of the problem is fast, because it is reduced to single decoupled problems. The result is easily read and implemented as a lumped inductor in any circuit simulator such as PLECS, LTSpice, Saber or Simplorer. The disadvantage is that the result does not take into account the influence of cross-coupling due to flow of current in the other conductors of the net. There is no magnetic cancelling effects, or for instance how the gate-leads are influenced by a high current flowing in the drain-source path. Despite this fact, many SPICE component models of relatively compact packages only include lead self-inductances with no consideration to the coupling between.

Method A is the easiest to understand and to implement. It is useful in cases where it is not critical to fully model the magnetic field cancelling effects. Examples could be for single layered power electronic modules, especially if working at low $\mathrm{d}i/\mathrm{d}t$ where the contribution from inductances is less dominant.

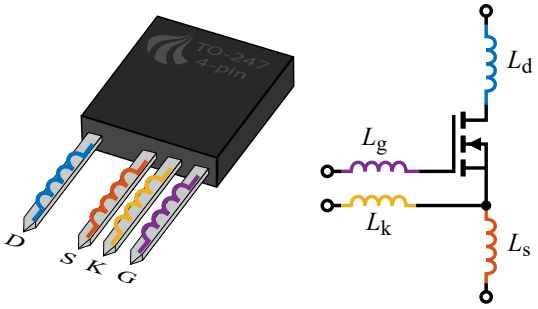


Fig. 2.1: Simulation method A calculating single piece-wise inductance values excluding coupling.

Method B To take into account the magnetic field cancelling effects, a method is to change the problem from a lumped element, into calculating a full current path, as shown in Fig. 2.2. When calculating the full loop during

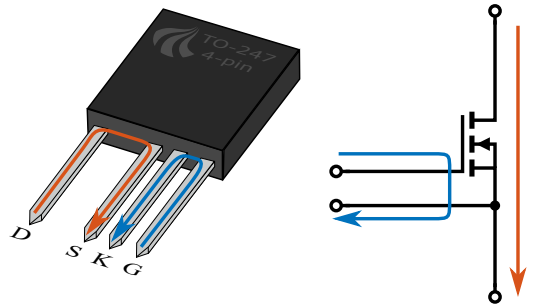


Fig. 2.2: Simulation method B calculating entire loops including coupling.

a simulation cycle, it takes into account the magnetic coupling for that entire loop. In practice, this is then often achieved by shorting the terminals of the semiconductor die, so that it is a perfect conductor. The disadvantage of this method is that now the inductance is calculated for a full loop. It is not easy to implement in the circuit simulator, because the inductances are not split into lumped components that can be easily placed around the semiconductor model. The method can be advantageous in optimization problems as loops are quantified by a single loop value read from the software. For instance, if the main focus is to reduce the inductance of the power loop or gate loop. In such a case, it is easy to visualize and method B provides more accurate results of the effective inductance when compared to Method A.

Method C This method uses the same self-inductances as in method A, with the addition of coupling between the self-inductances, as shown in Fig. 2.3. The

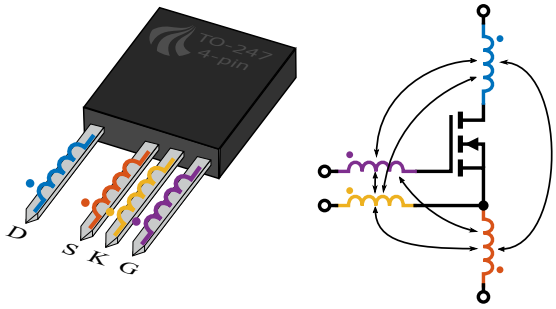


Fig. 2.3: Simulation method C calculating inductances and all couplings.

advantage is that the accuracy is similar to method B, because the magnetic field cancelling effects are included. In addition to that, when compared to method B, it now enables the designer to include the self-inductance and coupling into a circuit diagram. The disadvantage is that the effective inductance of a loop is not as easily available as in the case of method B, and thus during an initial design phase it is not as useful for design optimizations. For small systems, the couplings could be entered to a circuit simulator manually. However, for larger systems describing all couplings quickly approaches hundreds/thousand of entries. Thus, in practice ANSYS Q3D Extractor allows for the export of the full coupling matrix in a SPICE format. Thus to use the result, this method requires the use of a SPICE compatible circuit simulator, which may exclude a few circuit simulation softwares, such as PLECS. LTSpice, Saber and Simplorer are all compatible with this method. The definition of the coupled SPICE lumped circuit model of a power electronic component is described further in Section 2.1.1.

2.1.1 SPICE lumped models from ANSYS Q3D Extractor

For the case of three to four coupled nets it is easy to have an overview of how couplings are interconnected. However, for a case with 30-40 nets or more, extracting and keeping track of the interconnections manually is a tedious task prone to mistakes. Having at least 30-40 coupled impedances is not uncommon. In this case we need another way to describe the circuit dynamics in a more compact form. A three-layer PCB stack, as shown in Fig. 2.4, is used to describe how the SPICE lumped circuit model is interpreted. Each copper layer is defined as a net, which is all geometries of a conductive material type which is in contact with one another. Each net is separated by an isolating material type, either explicitly defined as the FR4 material layers included in Fig. 2.4 or just the surrounding air/vacuum. Each net has two terminals on its surface, a current input and current output, also known as a source and sink in ANSYS

Q3D Extractor. The current sources and sink are indicated by the arrows in Fig. 2.4. Thus, for currents flowing through each net, they create a voltage drop, that we wish to solve for, and can be represented in matrix form as

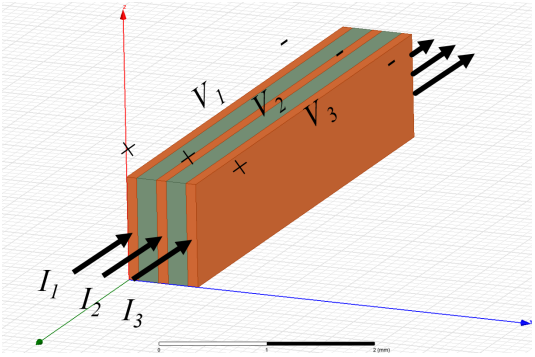


Fig. 2.4: Example of a three layer stack coupled electromagnetically in ANSYS Q3D.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} & R_{13} \\ R_{21} & R_{22} & R_{23} \\ R_{31} & R_{32} & R_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} + j\omega \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \tag{2.1}$$

ANSYS Q3D Extractor solves the problem at two frequencies. At DC the problem is solved with the current distributed uniformly in the volume of the conductor, until convergence at the current path which results in the lowest resistance, R_{ij}. Based on this current distribution the magnetic couplings, L_{ij} are calculated. The second solution is obtained at high frequency AC with the assumption that skin effect is well developed, thus the current density is focused on the conductor surfaces. To speed up the solver the problem is regarded as a surface problem. When solving the high frequency AC part it is solved as a coupled problem, meaning that the current distribution is dependent on the inductive part. ANSYS Q3D Extractor also solves for the capacitive coupling between nets. This is done by assuming equipotential nets, and the capacitance values are calculated as an independent problem with no influence of frequency or the magnetic coupling.

The extracted resistance, inductances and capacitance values, are implemented in the SPICE circuit simulator as lumped circuit elements. The inductance and resistance values are halved and the capacitance is placed in between. Thus the parasitics are arranged symmetrically in terms of the defined input/output ports. This may of course not be the case in the real device where capacitance might be distributed differently. ANSYS Q3D Extractor allows for automatic export of the calculated RLC-matrices into a SPICE circuit model using the circuit diagram as depicted in Fig. 2.5.

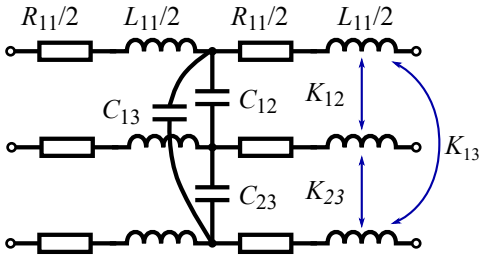
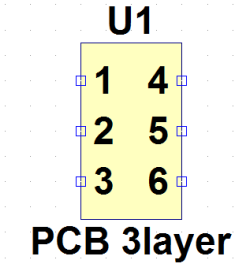


Fig. 2.5: Equivalent lumped circuit model of Fig. 2.4 .




```
.subckt Project1_half 1 2 3 4 5 6
V1 1 7 dc 0.0
V2 2 8 dc 0.0
V3 3 9 dc 0.0
R1 7 10 0.000431034482758
R2 8 11 0.000431034482759
R3 9 12 0.000431034482759
L1 10 4 1.26439744292e-009
L2 11 5 1.25035367724e-009
L3 12 6 1.26450847076e-009
K1_2 L1 L2 0.823488
K1_3 L1 L3 0.702289
K2_3 L2 L3 0.823483
.ends Project1_half
```

(a) (b)

Fig. 2.6: (a) the LTSpice circuit symbol and (b) part of the SPICE code used to describe the terminal.

For fast solving of a large netlist it is useful to use as few elements as possible, and solve a simplified set of equations to speed up the simulation. However, for systems of high frequencies and where it is required to achieve higher accuracy the ANSYS HFSS software package could be the simulation tool of choice. ANSYS Q3D Extractor enables the lumped circuit model of Fig. 2.5 to be directly exported into a SPICE circuit symbol as shown in Fig. 2.6(a). The symbol includes the SPICE code to define Fig. 2.5 and is partly shown in Fig. 2.6(b)

2.2 Software framework

The following section describes the main software packages which have been used for the research in this thesis. Additionally, some discussion is given in regard to which design tasks are being carried out at each step. A flow diagram shown in Fig. 2.7 depicts how the different software are interfaced with one another.

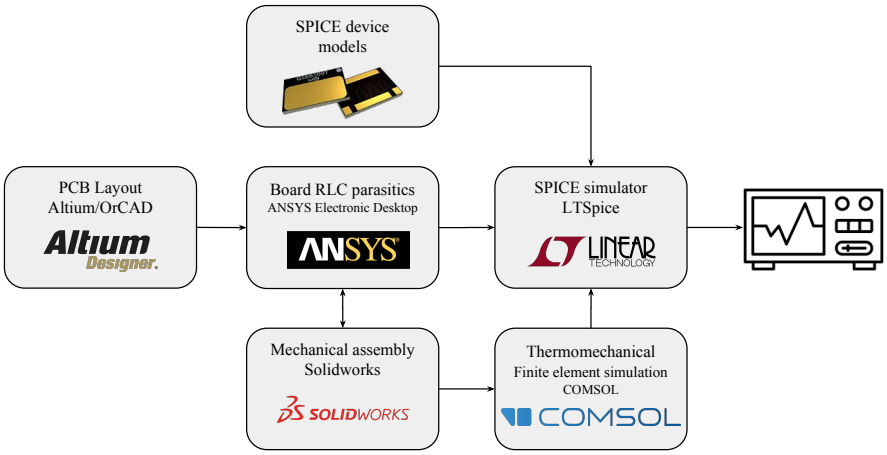


Fig. 2.7: The simulation software tool roadmap used for designed prototypes.

The simulation process starts out by setting up a model of the semiconductor. Almost all semiconductor manufacturers provide SPICE models of their devices, and thus a SPICE solver is required. For this thesis LTSpice has been used exclusively due to its accessibility and for being freeware. Alternatives could be Saber and Simplorer. Initially, just the main circuit elements and the die models are used to gain insight to the overall functionality of the circuit. It is important to insert some of the parasitic inductances and capacitances that are expected to be in the final power module. By changing the values of the parasitics, the designer gains some insight into what paths of the power module are critical. Some paths might allow hundreds of nH without significantly effect on the resulting switching waveforms, while 1-2 nH in the wrong path can seriously deteriorate the performance.

Once the circuit is understood, a draft of the 3D design power module is proposed. For a conventional power module structure it is mainly the traces of the DBC, which for this thesis is designed using Solidworks. For more integrated packaging the electrical design is done in a PCB editor, such as Altium or OrCAD. As a draft design is done, it is imported to ANSYS Electronics Desktop. The circuit is simulated using the ANSYS Q3D Extractor and an electrical parasitics model, as described in Section 2.1, is exported for use in LTSpice. If the electrical performance is satisfactory in LTSpice, the next step is to verify the power module in terms of other aspects in a multi-physics finite element method simulation software such as COMSOL Multiphysics, ANSYS workbench or Abaqus.

From ANSYS Electronics Desktop the full PCB layer stackup and its traces can be exported as a 3D model, which in this thesis is assembled in Solidworks

with the 3D models of baseplates, DBCs and semiconductor die models. From Solidworks a full 3D model is now available to verify the electrostatic or thermal performance of the power module. From the electrical waveforms in LTSpice we may have obtained some critical information such as expected power losses and peak voltage that can be used as input information. Furthermore, the finite element method software can also be used for a transient simulation i.e. used for obtaining a thermal response for the power module. If the SPICE model of the component is temperature-dependent, the thermal characteristics can be implemented in LTSpice to finalize a full electro-thermal model.

Using this detailed simulation process allows the engineer to assess a design for several aspects before spending valuable time on manufacturing a prototype. Using the real 3D geometries and accurate SPICE die models provides more accurate results as opposed to rough calculations or simplified 2D structures to estimate semiconductor losses, thermal resistances and electric field strengths early in the design process. Additionally, having the 3D models and using finite element method simulations provides a visualization of phenomena such as current crowding, thermal spreading and electric field concentrations. This enables the engineer to make quick adjustments and digitally iterate on a design much faster.

2.3 Digital prototyping

As an example of digital prototyping, some early versions of designs for an integrated RF power module are presented in this section. The design of the module is presented in more detail in Chapter 3.2. For now the focus is on a single inductance of the power module.

In this example an initial power module layout, shown in Fig. 2.8(a), has been designed in the 3D CAD software Solidworks. In ANSYS Q3D Extractor the inductance is calculated using Method B. The inductance is from the drain to the source terminals - thus the path is through the semiconductor die and its bondwires. For the initial design the inductance equals 11.5 nH. To understand the origin of the inductance, a new 3D model is designed in Fig. 2.8(b), where the lengths of the three pin terminals are reduced from 14 mm to 1 mm. The inductance is then reevaluated as 4.6 nH, revealing that more than 50 % of the inductance is caused by the terminals. By gaining inspiration from looking at some discrete RF packages [68] and high current power modules [69] that rely on low inductive packaging, a new set of power terminals based on wide flat copper terminals are designed. The drain-source inductance of the new design in Fig. 2.8(c) is then increased again to 10.5 nH. The new terminals are slightly better than the original design, but the main inductance was not caused by the shape of the terminals. It is noticed that the current must flow from the exterior of the DBC to the center before conducting through the semiconductor die.

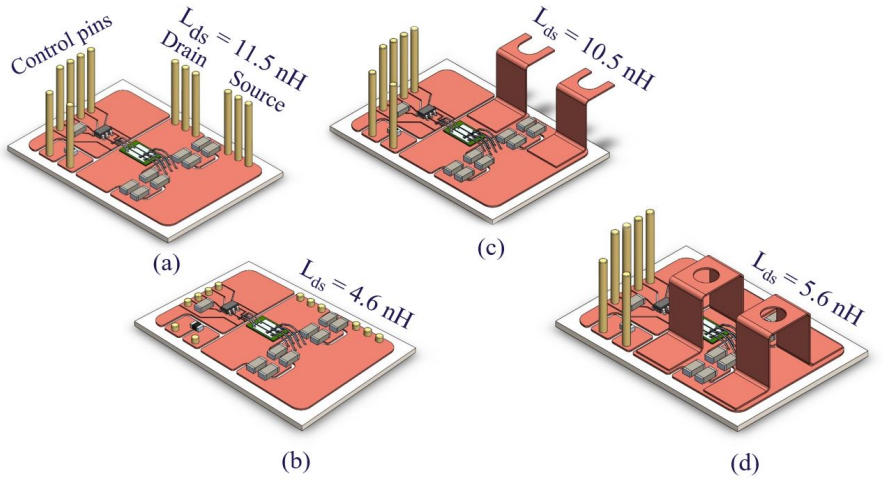


Fig. 2.8: Rapid prototyping enable quick trial of design layouts, as (a), (b), (c) and (d) represents four different iterations of the design.

Additionally, the ~5-6 nH contributed from the height of the power terminals itself can be reduced by paralleling more conductors. The final power module layout, shown in Fig. 2.8(d), has achieved a drain-source inductance of 5.6 nH.

This example shows how the power module inductance in an important path of the power module has been reduced to half of its initial value. The four different designs have been designed and simulated in about a 1-2 days of work. Without the use of 3D CAD tools and finite element simulation software, there would have been limited information to assess the design before it was build.

This chapter has presented several simulation strategies when using the finite element method software. Some of the approaches have advantages during early design iterations and for parametric sweeps of design variables to optimize the layout. Some methods are more suited for accurate circuit modelling in later stages. The use of the simulation tools are an important part in the design of the power module packages presented in the following chapters of this thesis. The time required in experimental testing is reduced, because the prototype being manufactured has already been through extensive digital verification.

Chapter 3

Wide bandgap power module prototypes

The following chapter presents power module prototypes that each treats an issue related to the full utilization of WBG power semiconductor devices. Issues related to fast $\mathrm{d}v/\mathrm{d}t$ in switching of medium voltage devices are presented in Section 3.1. Section 3.2 investigates the gate-driver circuit if WBG power devices are to be switched at potentially higher frequencies without the use of resonant gate drivers. The knowledge gained from the two first prototypes are combined in Section 3.3 to present the worlds first documented attempt of medium voltage, high frequency operation of a 10 kV SiC MOSFET.

3.1 Challenges in medium voltage operation of SiC MOSFETs

Medium voltage SiC devices have received increasing interest as the semiconductor technology is improving and samples are being released for engineers and research institutions. A potential application, once the medium voltage semiconductor technology has matured, is the wind turbine industry where power levels has scaled to several megawatts within a decade. For increasing power levels the typical method for increasing the power handling capability is to increase the current rating by paralleling converters [70]. Associated with the very high current levels is increasing joule losses and increasing size of the transformer required to step up the voltage for distribution [71]. An alternative solution to reach the required power is by removing the bulky transformer in the nacelle and increase the voltage at converter level [72], [73]. A proposal is to use the conventional two-level converter topology and increase the voltage rating by using 10 kV SiC MOSFETs instead of low voltage Si IGBTs. Currently, the

packaging of medium voltage devices is not mature and this research is set out to investigate critical issues when designing packaging for such high voltage ratings.

Conventional Si IGBT power modules have several hundreds or thousands of amperes in rating, meaning that they are experiencing a large $\mathrm{d}i/\mathrm{d}t$ during switching. For the medium voltage operation the $\mathrm{d}i/\mathrm{d}t$ stress is reduced, thus despite the faster switching of WBG devices the inductance of conventional packaging is not a limiting factor. As discussed in Section 1.1, the conventional packaging structure has advantageous properties in terms of electrostatics. The conventional packaging structure is deemed advantageous for medium voltage operation. However, in terms of medium voltage operation increased focus on the issues related to high $\mathrm{d}v/\mathrm{d}t$ is critical, which is the parasitic capacitances shown in Fig. 3.1.

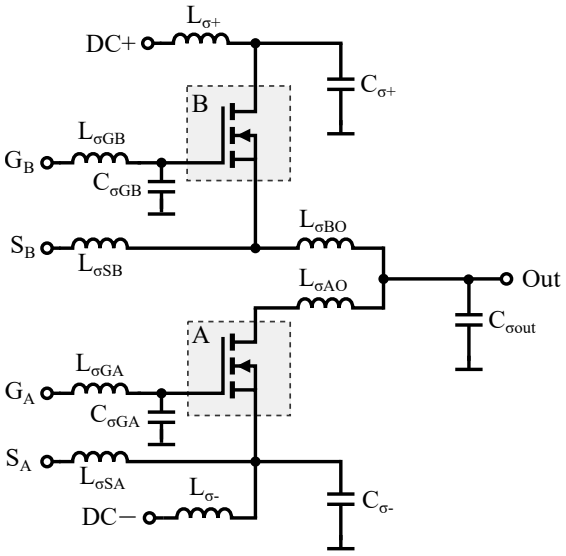


Fig. 3.1: Parasitics of a half-bridge conventional module structure. [Paper A]

3.1.1 Parasitic capacitance in conventional power modules

In early versions of a 10 kV SiC MOSFET half-bridge power module, as shown in Fig. 3.2, it is observed that during switching, the high $\mathrm{d}v/\mathrm{d}t$ of the switching output causes current to flow in the heat sink due to the parasitic capacitance of the power module [74]. The copper layers of the DBC are only separated by a 0.63 mm thick aluminum nitride (AlN) ceramic, so the Cu-AlN-Cu sandwich structure makes a capacitance. For safety the heat sink is grounded and due

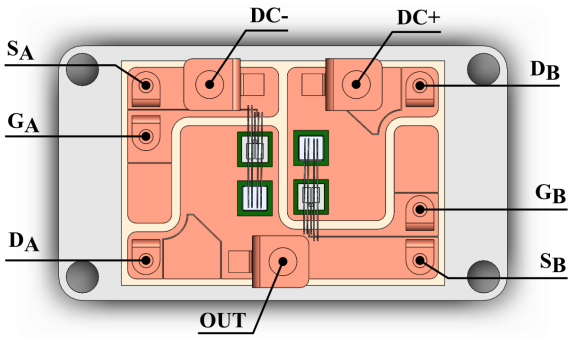


Fig. 3.2: Previous 10 kV SiC MOSFET power module layout.

to the grounding impedance there is a voltage ringing on the heat sink as current flows [40]. The current conducts through critical gate driver circuitry of the power module, which causes electromagnetic interference issues limiting the achievable switching speed [74]. Rearranging the parasitic capacitances of Fig. 3.1 and including the grounding impedance and auxiliary parasitic capacitance of the experimental setup results in a SPICE simulation schematic as shown in Fig. 3.3. In this schematic the inductances have been neglected, because for the experimental tests the di/dt is relatively low and only slightly influences the result. The schematic highlights that the root cause of the

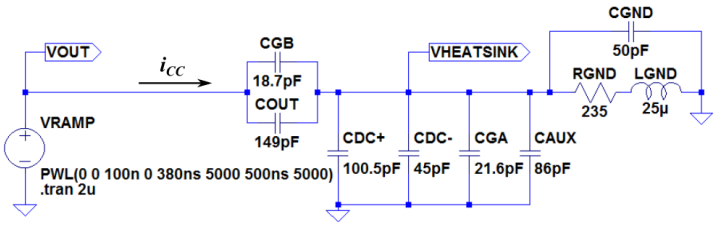


Fig. 3.3: SPICE model of the capacitive coupling to the heat sink. [Paper A]

currents are the capacitances $C_{\sigma\mathrm{GB}}$ and $C_{\sigma\mathrm{out}}$. As the voltage $(V_{out} - V_{heatsink})$ changes, a current flows given by

$$i_{\mathrm{CC}}(t) = (C_{\sigma\mathrm{GB}} + C_{\sigma\mathrm{out}}) \cdot \frac{\mathrm{d}(V_{\mathrm{out}} - V_{\mathrm{heatsink}})}{\mathrm{d}t} \tag{3.1}$$

where $C_{\sigma\mathrm{GB}}$ is the parasitic capacitance of the gate plane for MOSFET B, $C_{\sigma\mathrm{out}}$ the parasitic capacitance of the output plane, V_{out} the voltage of the switching output plane and V_{heatsink} the voltage of the heat sink. It is not desirable to slow down the switching speed of the SiC MOSFET, as we wish to have as fast $\frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t}$ as possible. We may limit the rate of change of voltage on the

heat sink, by changing the grounding impedance. Having a very high resistance is dangerous as the heat sink is not properly grounded and can be dangerous when working with the test bench after a switching test if voltage is build up in the capacitance. On the other hand a very low resistance results in an undamped oscillation. In this experiment the resistor has been chosen such that it gives a nearly critically damped response of the heat sink voltage, ensuring that heat sink voltage oscillation diminishes fast. This is shown for a double pulse switching test in Fig. 3.4, which also demonstrates the validity of the SPICE model in Fig. 3.3. The simulation is run both with and without the influence of 86 pF from auxiliary circuitry on the experimental setup. This highlights how the parasitic capacitance can be indirectly verified by measurement of on the heat sink voltage.

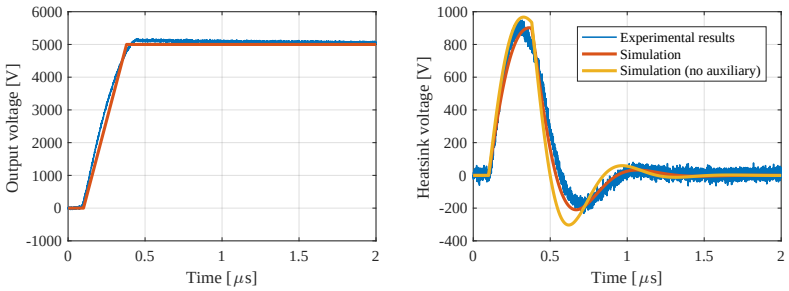


Fig. 3.4: Heatsink voltage during a double pulse switching test. [Paper A]

3.1.2 Design and test of prototype with low parasitic capacitance

The most effective way to solve the electromagnetic interference (EMI) issue is to decrease the common mode current by reducing the parasitic capacitances. The initial power module layout is shown in Fig. 3.2, which has a total output capacitance ($C_{\sigma out} + C_{\sigma GB}$) of 168 pF. Some of the main changes for a new layout is that the ability for paralleling dies is removed. The gate driver connection points are kept in the same location, but the terminals are rotated such that the connection point is outside the perimeter of the DBC. This reduced the parasitic output capacitance to 98 pF.

A relatively large part of the output copper plane is used for the connection to the source terminal, S_B. Floating copper planes are utilized to reduce the copper area of the output plane. When choosing the size of one of these floating planes, it is noted that it is close to the expected current paths, and thus might affect the parasitic inductances. An ANSYS Q3D Extractor simulation is setup, which includes a parametric sweep of the size of the area which is to be converted to a floating area, as indicated by the marked area in Fig. 3.5.

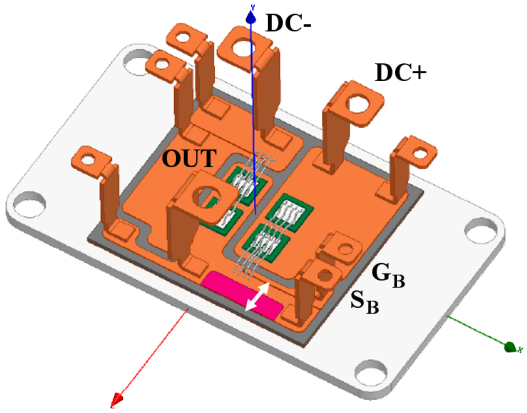


Fig. 3.5: The width of indicated area is swept using ANSYS Q3D Extractor. [Paper A]

The three paths which are considered are from DC+ to the output terminal, from DC- to the output and the gate-source loop of MOSFET B. The inductances are evaluated according to Method B of Section 2.1. While increasing the width of the removed area, the parasitic inductance, parasitic resistance and output capacitance are monitored. The results are shown in Fig. 3.6. The results show that the parasitic capacitance is linearly decreasing as the width of the region removed is increased, while the parasitic inductance and resistance are nearly unaffected.

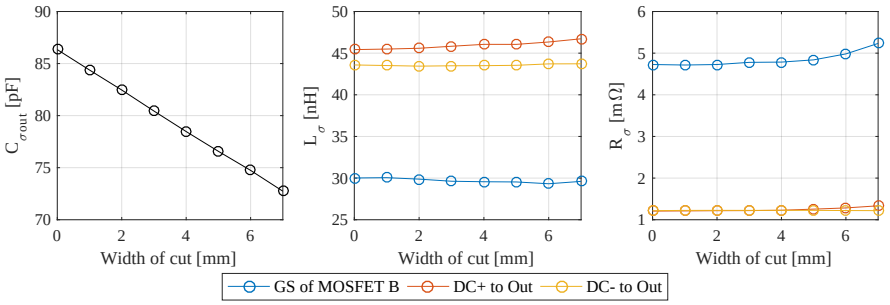


Fig. 3.6: Simulated $C_{\sigma out}$, L_σ and R_σ for three critical paths as the width of the floating area is increased. [Paper A]

The final power module layout is shown in Fig. 3.7. An experimental setup is designed to perform a double-pulse test of the new power module. Gate driver boards and a medium voltage experimental test bench are designed and build by Nicklas Christensen, Dipen Narendrabhai Dalal and Simon Dyhr Sønderskov *et al.* as described in [40], [74].

The new power module is tested in the medium voltage test bench and

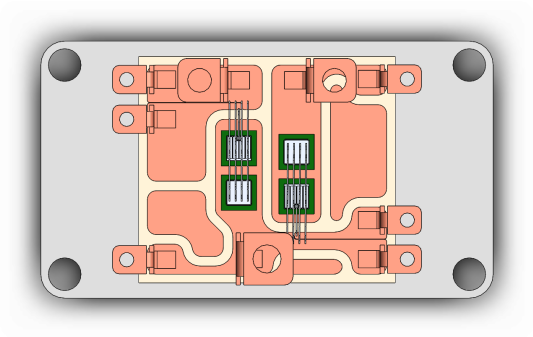


Fig. 3.7: Updated 10 kV SiC MOSFET power module design with lowered parasitic capacitance.

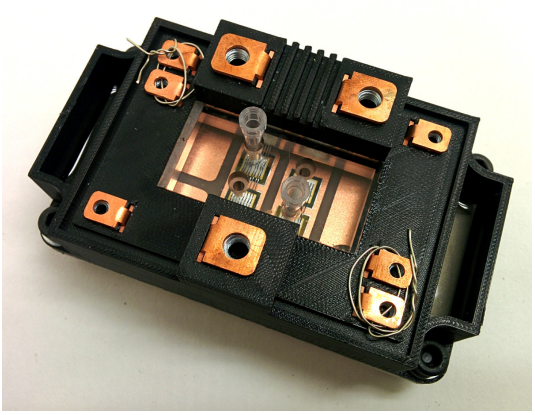


Fig. 3.8: Picture of manufactured 10 kV SiC MOSFET power module.

the switching output voltage and the generated heat sink voltage is compared with the previous module, as shown in Fig. 3.9. The results highlight that the reduction in total parasitic output capacitance from 167 pF to 85 pF (73 pF from $C_{\sigma out}$ and 12 pF from $C_{\sigma GB}$) results in a reduction in switching time of 15 %, while the amplitude of the heat sink voltage has been reduced by 26 %.

3.2 An integrated high frequency power module

One of the benefits of the WBG semiconductor devices, is the ability to be operated at higher frequencies. Smaller device area is required to obtain the same voltage and current ratings as a Si device, which results in reduced device capacitances. Often for high frequencies resonant gate driver circuits are used,

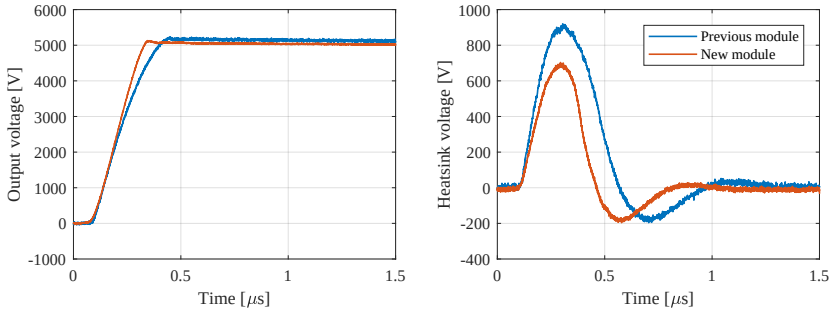


Fig. 3.9: Comparison of output voltage and generated heat sink voltage during 5 kV / 5 A switching of the previous and new 10 kV SiC MOSFET power modules.

as they enable recovery of some of the gate charge. Resonant gate drivers have less strict requirements of the gate-source loop inductance, as it is included as a part of the resonant oscillating loop [75]. Resonant gate drivers use more components, such as capacitors and inductors, which distribute the gate losses and reduces overheating of gate driver circuitry [76]. But it comes at the cost of resonant gate drivers being more complex to design. A hard switched gate driver IC is advantageous for many applications because of its increased control flexibility, increased power density and simpler implementation [77], [78]. But two main prerequisites for the solution is the capability of handling the increased gate losses of a hard-switched gate driver and strict requirements that the inductance is low enough to avoid oscillations due to a steep slope of the gate voltage input waveform.

S. Guo *et al.* [28], [33] have shown good performance of a 650 V SiC MOSFET power module with integrated gate driver. The gate driver is soldered to the DBC inside the power module, meaning it has a structure similar to what was shown in Fig. 1.5. Good switching performance of the SiC MOSFET device was demonstrated.

In this section, two aspects are further studied in detail. First of all it is analyzed how low inductance is required in the gate-source loop to achieve the clean switching. Secondly, the change in thermal performance of the gate driver IC is analyzed when placed on DBC inside the power module versus a typical placement on a PCB. Without these two assessments it could prove that the SiC MOSFETs perform very well on their own and that discrete packages are sufficient [79]. If relatively high inductance is allowed and the thermal performance is good enough on a PCB, it would mean that there is no requirement for integration of the gate-driver circuit inside the power module to achieve high switching frequencies of SiC MOSFETs.

This is investigated using a platform of a Class E resonant converter to be operated at a frequency of 2.5 MHz. A custom SiC MOSFET power module with integrated gate driver IC is designed. The components to be integrated

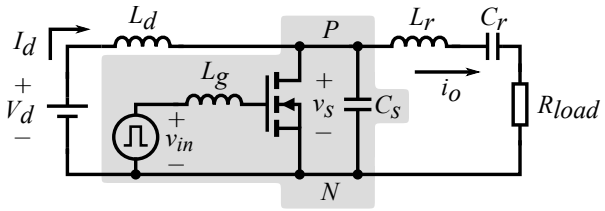


Fig. 3.10: Class E schematic with integrated components marked [Paper B].

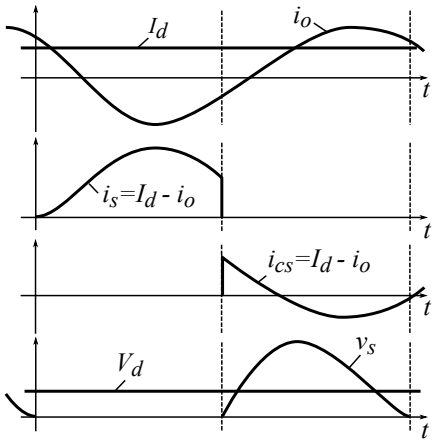


Fig. 3.11: Class E converter waveforms.

inside the power module are marked in Fig. 3.10. The ideal Class E resonant converter waveforms are shown in Fig. 3.11. When the switch turns on/off the current is abruptly shifted between the external parallel capacitance, C_s and the switch. Thus, to reduce the noise generated the external parallel capacitance is also included inside the package.

3.2.1 Analysis of gate driver dynamics for fast switching

Part of achieving fast switching speeds, is to ensure the correct dynamics of the gate-source voltage. Often a gate resistor is placed between the gate driver IC and the MOSFET, which helps dampening the gate-source loop and results in a robust but slow transient of the gate-source voltage. If a too small resistance is used it leads to oscillations of the gate-source voltage, which may propagate as undesirable high frequency noise on the drain-source voltage of the MOSFET [18], [80]. The purpose of this section is to describe the dynamics of the gate-source loop, to achieve a fast and non-oscillating gate-source voltage. The parasitics included in the gate-source loop are shown in Fig. 3.12

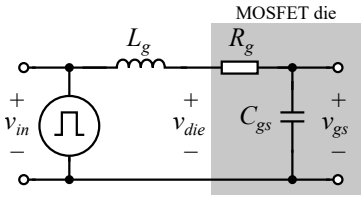


Fig. 3.12: Parasitics included in the gate-driving loop [Paper C]

Kirchoffs voltage law is applied to the circuit in Fig. 3.12

$$v_{\mathrm{in}}(t) = L_{\mathrm{g}}\frac{\mathrm{d}i(t)}{\mathrm{d}t} + i(t)R_{\mathrm{g}} + v_{\mathrm{gs}}(t) \tag{3.2}$$

Taking the Laplace transform of (3.2) results in

$$V_{\mathrm{in}}(s) = L_{\mathrm{g}} \cdot s \cdot I(s) + I(s)R_{\mathrm{g}} + V_{\mathrm{gs}}(s) \tag{3.3}$$

By inserting $I(s) = C_{\mathrm{gs}} \cdot s \cdot V_{\mathrm{gs}}(s)$ to (3.3) and rearranging

$$V_{\mathrm{in}}(s) = V_{\mathrm{gs}}(s)(L_{\mathrm{g}} \cdot C_{\mathrm{gs}} \cdot s^2 + C_{\mathrm{gs}} \cdot R_{\mathrm{g}} \cdot s + 1) \tag{3.4}$$

From (3.4) the transfer function becomes

$$\frac{V_{\mathrm{gs}}(s)}{V_{\mathrm{in}}(s)} = \frac{1}{L_{\mathrm{g}} \cdot C_{\mathrm{gs}} \cdot s^2 + C_{\mathrm{gs}} \cdot R_{\mathrm{g}} \cdot s + 1} \tag{3.5}$$

The standard form for a 2nd order system is shown in (3.6)

$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_{\mathrm{n}}s + \omega_{\mathrm{n}}^2} \tag{3.6}$$

By rewriting (3.5) to the standard form of (3.6) we obtain

$$\frac{V_{\mathrm{gs}}(s)}{V_{\mathrm{in}}(s)} = \frac{\frac{1}{L_{\mathrm{g}} \cdot C_{\mathrm{gs}}}}{s^2 + \frac{R_{\mathrm{g}}}{L_{\mathrm{g}}}s + \frac{1}{L_{\mathrm{g}} \cdot C_{\mathrm{gs}}}} \tag{3.7}$$

From this we can get the natural frequency and damping ratio as

$$\omega_n = \sqrt{\frac{1}{L_{\mathrm{g}} \cdot C_{\mathrm{gs}}}} \qquad \zeta = \frac{R_{\mathrm{g}}}{2 \cdot L_{\mathrm{g}}} \frac{1}{\sqrt{\frac{1}{L_{\mathrm{g}} \cdot C_{\mathrm{gs}}}}} = \frac{R_{\mathrm{g}}}{2}\sqrt{\frac{C_{\mathrm{gs}}}{L_{\mathrm{g}}}} \tag{3.8}$$

Once a damping ratio is determined, the required inductance is obtained from

$$L_{\mathrm{g}} = \frac{C_{\mathrm{gs}} \cdot R_{\mathrm{g}}^2}{4\zeta^2} \tag{3.9}$$

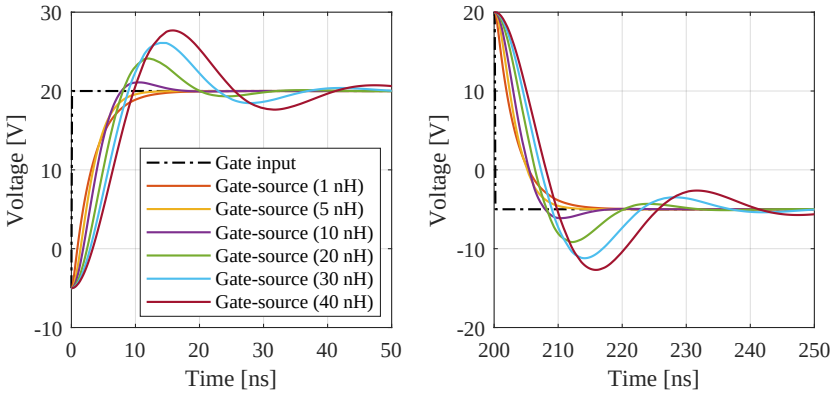


Fig. 3.13: Gate-source voltage of CPM2-1200-0160B for various gate-source loop inductances when subjected to a step input.

For this demonstration the 1200 V, 160 mΩ SiC MOSFET bare die CPM2-1200-0160B [81] from Wolfspeed is used and no external gate resistance is added to achieve faster switching. The gate-source voltage due to a step-input for various gate loop inductances are shown in Fig. 3.13.

For damping ratio $\zeta = 1$ (critically damped) the required inductance is

$$L_g = \frac{521\,\text{pF} \cdot (6.5\,\Omega)^2}{4 \cdot 1^2} = 5.5\,\text{nH} \tag{3.10}$$

An inductance below is value results in a overdamped response, while anything above gives some slight oscillation. The absolute maximum rating of gate-source voltage for CPM2-1200-0160B are stated as +25/-10 V. Thus for safe operation it is necessary for the inductance to be less than 20 nH.

3.2.2 Design of power module with integrated gate driver

A power module prototype is designed with an integrated gate driver circuit to achieve a low gate-source loop inductance, as shown in Fig. 3.14. Before settling on this final design, several iterations were tested as described in Chapter 2. The gate driver is a UCC27531 from Texas Instruments, and it is placed very close to the SiC MOSFET die. An additional auxiliary source bond wire is used to get a Kelvin connection for the gate circuitry. This ensures decoupling between the gate and the power loop. Capacitors for the gate driver are placed inside the power module as well, to ensure a robust +20 V and -5 V supply voltage. Four 1812 SMD capacitors making up a total $C_s = 880$ pF are placed symmetrically to obtain good current sharing during operation. The capacitors are of type NP0/C0G, as this type maintains its capacitance at varying voltage bias and high frequency operation. The disadvantage of the NP0/C0G capacitors is a low capacitance density [82], [83].

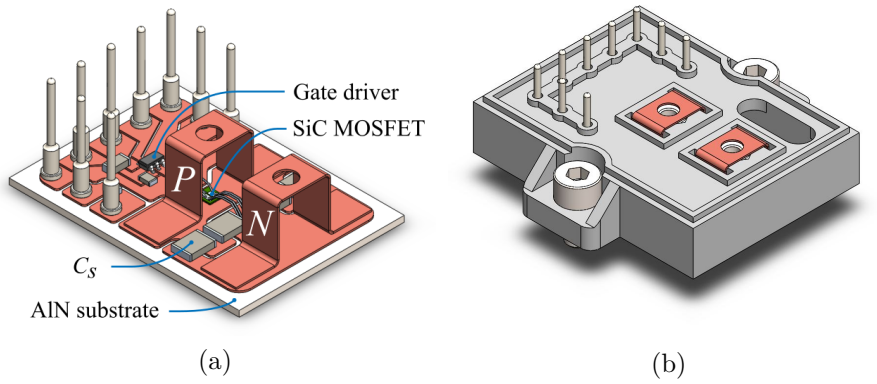


Fig. 3.14: 3D model of the designed integrated SiC MOSFET power module (a) without and (b) with housing.

The 3D model of the power module from Solidworks is imported into ANSYS Q3D Extractor to evaluate the loop inductances. The inductances are evaluated using the Method B as described in Section 2.1, to evaluate a full current loop. First, for this case the gate-source terminals of the SiC MOSFET die are modelled as shorted circuited in ANSYS Q3D Extractor. The gate-source loop inductance is evaluated as 4.6 nH, which results in a slightly overdamped gate-source voltage of the SiC MOSFET. The drain-source pads of the SiC MOSFET die are short-circuited to calculate the drain-source loop inductance, which is found to be 6.3 nH. At last, a very crucial inductance is between the SiC MOSFET die and the parallel capacitors. The loop input is placed on the drain pad of the SiC MOSFET, the capacitors are modelled as a short and the loop output is placed on the source pad. This results in a loop inductance of 2.1 nH. The three paths are shown in Fig. 3.15.

3.2.3 Thermal performance of gate driver IC

The power module of Fig. 3.14 is manufactured. Traces are etched to the top side of the 1 mm thick AlN DBC. All components and pins are soldered in a single step to the DBC. At this point the power module is not yet encapsulated and covered, and thus the temperature of the gate driver IC inside the power module can be observed using a thermographic camera. During the experiment the power module is clamped down to a heat sink using a custom cut acrylic plastic holder, similar to when the final housing is mounted, as shown in Fig. 3.16(a). Supply voltages of +20 V and -5 V are given to the gate driver IC from a laboratory power supply. A control signal of 2.5 MHz is given from a National Instruments CompactRIO. The SiC MOSFET die has no drain-source bias, meaning all power delivered from the laboratory power supply goes to the gate-driving circuit and the gate-source of the SiC MOSFET. Thermal

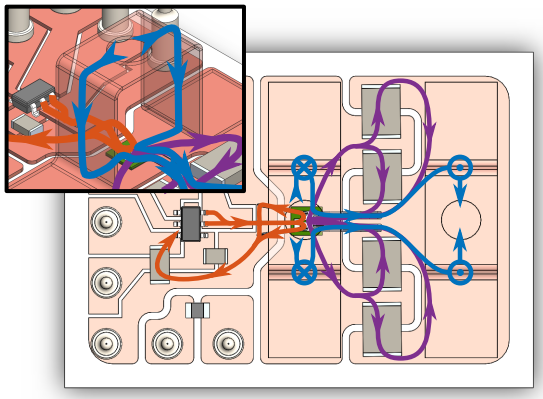
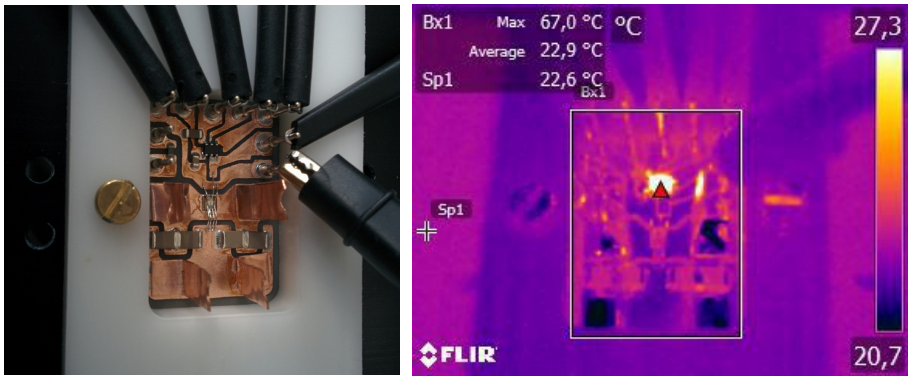


Fig. 3.15: Paths of die to external capacitance (purple), drain-source (blue) and gate-source (red), where $\otimes$ is direction inward and $\odot$ is outward. [Paper B]

contact resistance between DBC and heat sink is reduced by the use of thermal interface material. Another prototype is also manufactured, where the DBC has been replaced by a conventional double-layer PCB, having FR4 thickness of 1.5 mm and a copper layer of 35 μm on either side. This is to compare the two cases. The measured case temperatures of the two gate driver ICs are shown in



(a) (b)

Fig. 3.16: Picture of (a) test setup and (b) output image from FLIR E40.

Fig. 3.17, which also shows the temperature on the heat sink during one of the tests. From Fig. 3.17 the maximum case temperatures measured during the experiment are 120 °C and 69 °C, for the case where the gate driver is mounted on a PCB and DBC, respectively. It is concluded that there is a significant gain by placing the gate driver IC on the DBC. Despite the small form factor and

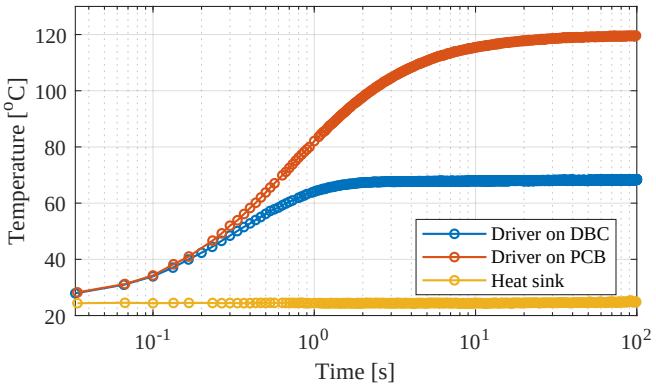


Fig. 3.17: Measured temperature of prototype with gate driver on DBC, gate driver on PCB and heat sink temperature during the experiment.

that the gate driver is only thermally connected to the DBC/PCB by six pin legs, the thicker copper and good thermal conductivity of the DBC is enough to make a significant difference between the two experiments. However, the measured temperatures are the case temperature. To further investigate the actual operating margin for the maximum junction temperature of 150 °C [84], it is useful to estimate the junction temperature. A thermal network is used for these calculations[1], as shown in Fig. 3.18.

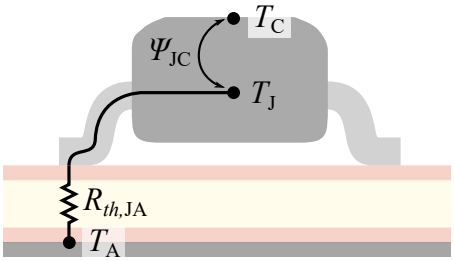


Fig. 3.18: Thermal network for the integrated gate driver IC.

[1]Note that this way of calculating the junction temperature T_J is different from what is presented in the accepted manuscript of Paper B. Mistakenly, the thermal resistance value used for R_{JC} in Paper B is instead a thermal characteristic parameter ψ_{JC}. Despite this error, the appended Paper B has been kept in its accepted manuscript form. The reason is to keep consistency between the appended papers of this thesis and the submitted/accepted versions at the publishers. IEEE Xplore does not allow changes to already published conference paper files, as they only deal with the files provided from the conference organizers. Only changes to metadata or abstract are possible, as seen in the support center resources: https://supportcenter.ieee.org/app/answers/detail/a_id/1012/kw/error in pdf

The junction temperature is calculated from

$$T_{\mathrm{J}} = T_{\mathrm{C}} + \Psi_{\mathrm{JC}} \cdot P_{\mathrm{IC}} \tag{3.11}$$

where T_{J} is the junction temperature, T_C is the top case temperature, Ψ_{JC} is the thermal characteristic parameter from junction to case and P_{IC} is the power dissipated in the junction of the IC. For the UCC27531 the Ψ_{JC} is 14.7 K/W as given in the datasheet [84].

The thermal characteristic parameter, Ψ, describes the temperature difference between the two points given a certain power dissipation in the IC junction. Note that the thermal characteristic parameter, Ψ, has the same unit as a thermal resistance, R_{th}, and they look similar in their definition. However, it is important to distinguish the two. For the thermal resistance, R_{th} we use the temperature difference between two points and requires that we know the power flow in the path between these two points. Using Ψ is often of more value in practical cases, because the exact power flow in different paths is often unknown and difficult to measure [85].

From the junction temperature calculated in (3.11), the thermal resistance from junction to ambient, $R_{th,\mathrm{JA}}$ is determined by

$$R_{th,\mathrm{JA}} = \frac{T_{\mathrm{J}} - T_{\mathrm{A}}}{P_{\mathrm{IC}}} \tag{3.12}$$

In this case the thermal resistance is used correctly, because all power is dissipated in the junction of the gate driver IC and must all flow to the ambient. Shown in Fig. 3.17 is that the heat sink temperature is constant during the experiment, meaning it can be used as a constant reference ambient temperature at an equipotential as the surrounding air.

During the experiment the power is measured from the laboratory power supply as 1.83 W. This power is shared between the gate driver IC and some power loss in the gate structure of the SiC MOSFET. The circuit of Fig. 3.12 is used and the measured 2.5 MHz voltage from the gate-driver, v_{die} is used as the input to the die model in SPICE. The power loss in the gate structure of the SiC MOSFET is simulated in SPICE as 0.78 W when being run at 2.5 MHz. Thus, the remaining 1.05 W is assumed to be dissipated in the gate driver IC. Using the estimated power dissipation in the gate driver IC, the maximum junction temperatures are calculated using (3.11) after steady state is reached, which results in 84 °C and 136 °C for the DBC and PCB, respectively. This results in a $R_{th,\mathrm{JA}}$ of 57 K/W and 105 K/W for the gate driver mounted on a DBC and PCB, respectively. Thus, despite of the gate driver IC having relatively small pins that could be a thermal bottle neck, the experiment has demonstrated a 45 % reduction in the thermal resistance by placing the gate driver IC on the DBC inside the power module compared to on a PCB.

3.2.4 Experimental results at 2.5 MHz in Class E converter

Following the gate driver test, the power module is encapsulated in silicone gel for it to withstand a higher drain-source bias. A custom housing is milled from a block of acrylic plastic. The final power module is shown in Fig. 3.19, after curing of the silicone gel. The power module is inserted in a Class E resonant converter test setup shown in Fig. 3.20.

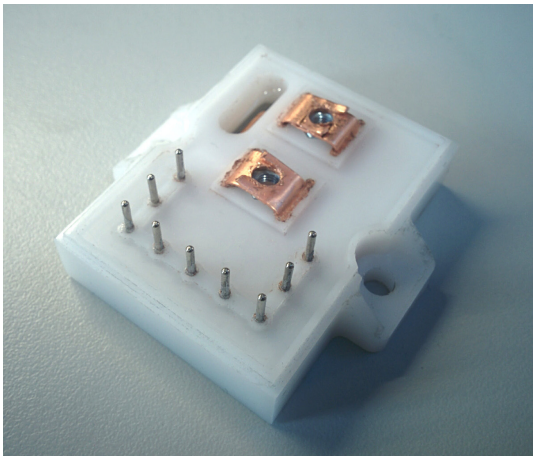


Fig. 3.19: Picture of the final power module after assembly [Paper B].

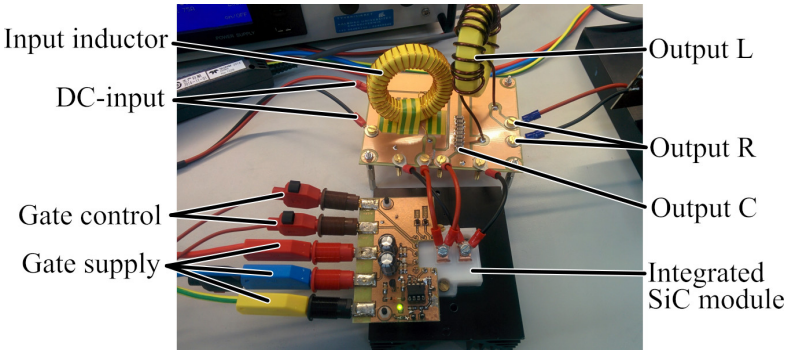


Fig. 3.20: Picture of experimental setup used to test the integrated module.

The output resonance LCR tank is designed for a resonance frequency of 2.5 MHz. By parallel connecting NP0 ceramic capacitors a total output capacitance of C_r = 2.08 nF is achieved. The resonance output inductor is wound on a powdered iron core to achieve L_r = 3.84 μH. Similarly, the input inductance L_d = 25 μH is also wound on a powdered iron core. Finally, an output resistance of

$R_{load} = 16.7\ \Omega$ is achieved by a parallel connection of three RF power resistors each of 50 Ω. The components for the experimental resonance tank are based on a design by Unnikrishnan Raveendran Nair *et al.* [86]. The results shown here are performed at an input voltage, V_d, of 150 V.

The experiment is compared with a simulation model, based on the inductances extracted. The inductances calculated using Method B are assumed to be only weakly coupled and thus are inserted in a simulation diagram as shown in Fig. 3.21. The simulation is compared to the experimental waveforms

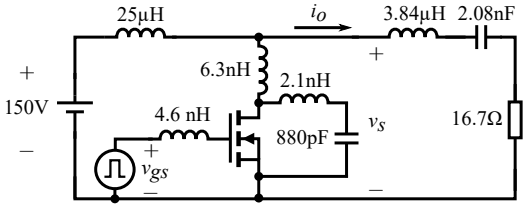


Fig. 3.21: Simulation model of Class E resonant circuit [Paper B].

in Fig. 3.22. There is a very good coherence between the experimental and simulation waveforms. The gate-source voltage is nearly undisturbed by the switching, meaning that both the right damping is obtained and that the auxiliary source connection decouples the gate from the power loop as intended. This also results in no higher order oscillation observed on the measured drain-source voltage waveform. This has been observed in other Class E converters with discrete packages, caused by no auxiliary source connection or too high interconnection inductances [79]. The coherence between experiment and simulation verifies the design methodology and demonstrates the clean switching that can be obtained when the loop inductances are designed correctly.

3.3 Making vacuum tubes obsolete?

The following section describes the work done on combining the learnings from building both medium voltage power modules in Section 3.1 and high frequency operation of a low voltage SiC MOSFET in Section 3.2.

The purpose is to investigate the feasibility of creating a solid state semiconductor solution, which can replace current vacuum tube solutions in some applications. More specifically, it is resonant converters that operate at medium voltage (a few kV) and in a frequency range of hundreds kHz to tens of MHz. This include industrial processes such as induction and dielectric heating used for drying, processing of food or melting metals [87]–[91]. These industrial applications still rely on vacuum tubes to run converters. Conventional silicon power devices have not yet shown capabilities to operate in this domain. Replacing the vacuum tubes with a solid state device could result in higher

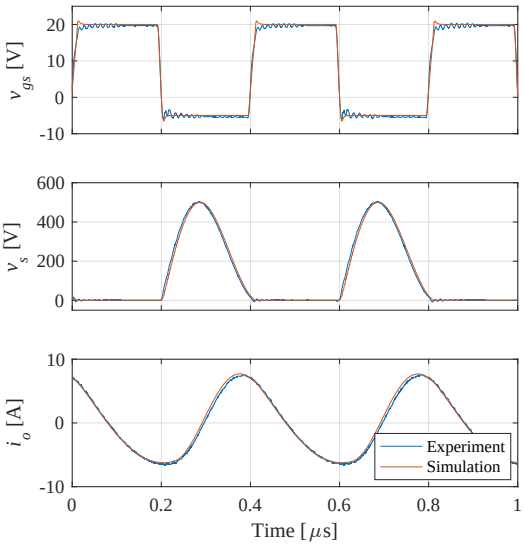


Fig. 3.22: Comparison of experimental waveforms and simulation [Paper B].

efficiency and higher power density [92], [93]. With the benefits of wide bandgap semiconductors, as highlighted in Chapter 1, there is a potential that devices with medium voltage ratings and relatively low device capacitances are now capable of operating at the required specifications for the industrial RF applications. The superior performance of 900-1700 V SiC MOSFETs has already been demonstrated in low voltage RF converters [28], [33], [79], [94]. The fast dv/dt switching of 10 kV SiC MOSFETs has mostly been demonstrated in single event switching such as in double pulse tests [74], [95]–[100] and short circuit characteristics [101]–[103]. The continuous operation of a 10 kV SiC MOSFET die has been demonstrated in boost converters [104]–[107] or inverters [108]–[112] up to a few tens of kHz. However, at this point in time there has been no documented attempts at switching medium voltage SiC MOSFETs in the MHz range. This section describes the work done of designing and testing a medium voltage high frequency integrated power module to work at 2-3 kV and targeted at a few MHz.

3.3.1 Power module design and manufacturing

The power module prototype is based on the DBC integrated structure, similarly to what was used in Section 3.2. A 3D model of the power module is designed using Solidworks as shown in Fig. 3.23. Wolfspeed bare dies are available in the voltage range 900-1700V and 10-15 kV. A 10 kV 17 A SiC MOSFET die from Wolfspeed is used to reach the targeted 2-3 kV operation range. The

power module has an IXRFD630 gatedriver from IXYS integrated in the power module, which has a current source capability of 30 A and is designed for RF applications. The gate driver has a solderable bottom which allows for high power dissipation of the gate driver. This is required to drive the 6 nF gate-source capacitance of the 10 kV SiC MOSFET die.

The parallel capacitance, C_{p}, consists of four 180 pF capacitors of type NP0. 1812 SMD components are used to allow for a relative compact form factor, but they are only rated for 3000 V. Due to the relatively low capacitance density of NP0 capacitors they quickly reach a size which is hard to integrate. However, the 3000 V is enough to showcase the feasibility of the power module in the target applications.

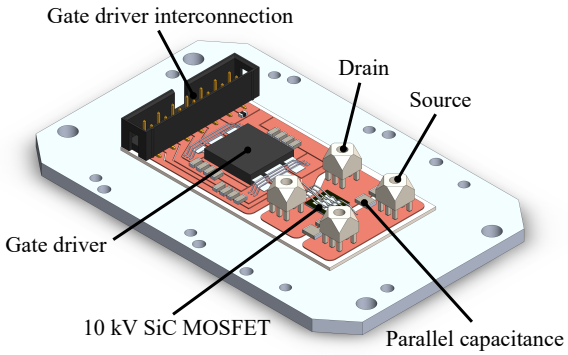


Fig. 3.23: 3D model of designed medium voltage integrated SiC MOSFET power module [Paper C].

Similar to the case of Section 3.2, the critical gate-source, drain-source and SiC MOSFET to parallel capacitance loops are simulated using ANSYS Q3D Extractor. Once again this is done to ensure that the gate-source loop inductance is tuned to the SiC MOSFET gate parameters and mitigates gate-source voltage oscillations during operation.

All the integrated components are soldered to the DBC which consists of 0.3 mm thick copper on both sides of a 1 mm aluminium nitride (AlN) ceramic. Using AlN allows for a very high power dissipation as its thermal conductivity is 150-180 $\frac{\mathrm{W}}{\mathrm{m}\cdot\mathrm{K}}$, which is several times larger than the 24 $\frac{\mathrm{W}}{\mathrm{m}\cdot\mathrm{K}}$ which is the case for traditional aluminium oxide (Al_2O_3) DBCs. The 10 kV SiC MOSFET die is wirebonded and has an auxiliary source connection for the gate driver. At last the power module is packaged in a custom housing made from transparent acrylic plastic and it is potted using WACKER Silicone gel with an insulation strength rated at 23 kV/mm. The final power module is shown Fig. 3.24.

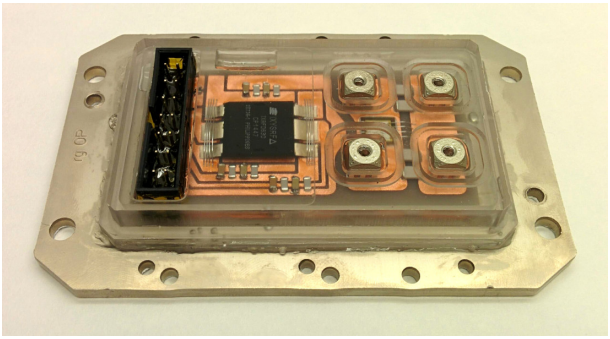


Fig. 3.24: Picture of manufactured medium voltage SiC MOSFET RF module [Paper C].

3.3.2 Experimental results & discussion

For the experimental tests an LC oscillator circuit, as shown in Fig. 3.25(a) is used. The switch, Q, and capacitance, C_p, are contained inside the power module package.

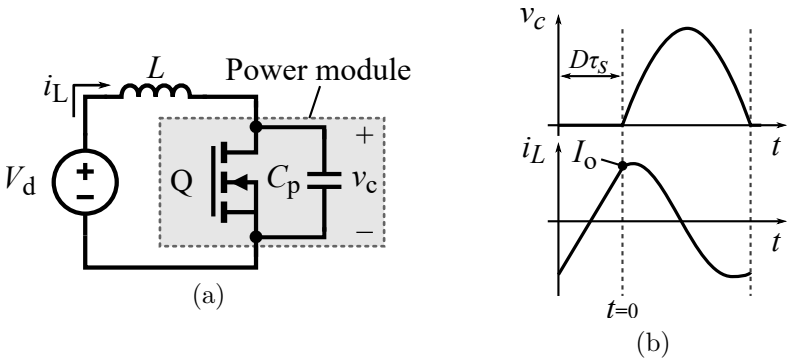


Fig. 3.25: (a) Experimental LC circuit diagram and (b) its analytical waveforms.

The analytical LC oscillator waveforms are shown in Fig. 3.25(b). Initially, the switch, Q, is on for a time period of $D\tau_s$. During this time period the change in current through the inductor is

$$\Delta i_{\mathrm{L}} = \frac{D \cdot \tau_{\mathrm{s}} \cdot V_{\mathrm{d}}}{L} \tag{3.13}$$

The current at $t = 0$ is denoted I_0, and because the inductor current is centered around zero, it is geometrically determined from Fig. 3.25(b) to be

$$I_0 = \frac{D \cdot \tau_{\mathrm{s}} \cdot V_{\mathrm{d}}}{2 \cdot L} \tag{3.14}$$

At the time $t = 0$, the switch is turned off and the voltage starts to build up across the switch, v_c. The voltage, v_c, following $t = 0$ with the initial condition of $i_L = I_0$ is given by [113]

$$v_{\mathrm{c}} = V_{\mathrm{d}} - V_{\mathrm{d}} \cdot \cos(\omega t) + \sqrt{\frac{L}{C_{\mathrm{p}}}} \cdot I_0 \cdot \sin(\omega t) \tag{3.15}$$

The maximum capacitor voltage is determined by differentiating (3.15), which equals

$$\frac{\mathrm{d}v_c}{\mathrm{d}t} = V_d \cdot \omega \cdot \sin(\omega t) + \sqrt{\frac{L}{C_p}} \cdot I_0 \cdot \omega \cdot \cos(\omega t) \tag{3.16}$$

The time, t, where maximum voltage occurs is found by equating (3.16) to zero and then solved for t. The extremes are at $t = \frac{\pi(2n-1)}{2\omega}$ for $n \in Z$. Because the LC circuit is being reset every period, it is only the initial peak which is of interest. This occurs at $n = 1$, and thus maximum capacitor voltage at $t = \frac{\pi}{2\omega}$ is given by

$$V_{\mathrm{c}} = V_{\mathrm{d}} + \sqrt{\frac{L}{C_{\mathrm{p}}}} \cdot I_0 \tag{3.17}$$

The input voltage is ramped up gradually. The results shown in this thesis are done at an input voltage of $V_{\mathrm{d}} = 800$ V. At this voltage the combined drain-source capacitance (the sum of the device output capacitance and the external capacitors) is $C_p = 890$ pF. The input inductance L is 25 μH and thus the resonance frequency of the LC oscillator is 1 MHz. At these experimental tests conditions, the current I_0 is predicted from (3.14) to be 5.0 A, while the drain-source peak voltage, V_C, is 1638 V. The experimental results and the simulated waveforms are shown in Fig. 3.26, which demonstrate the capability of the SiC MOSFET to operate at 1 MHz. The experimental drain-source peak voltage only deviates by 2.4 % of the analytical value calculated. There is a good coherence between analytically derived values, the simulation and the experimental waveforms.

Successful tests have not been performed at higher voltages because the operation is not robust. At the very first switching of the circuit, the resonant operation has not yet been established and thus the DC-link voltage is being hard switched. This creates a very high $\mathrm{d}v/\mathrm{d}t$ of the output node, and causes the gate-signal to flicker. The hypothesis is that the high $\mathrm{d}v/\mathrm{d}t$ of the drain copper plane causes current to flow to the heat sink, which couples to the input node of the gate driver. The input pin of the gate driver is designed for relatively fast response from a weak driving stage (such as an FPGA or DSP), and thus a few mA of noise can greatly affect the input gate signal. This creates a scenario where the gate driver continuously flickers the output until it overheats and

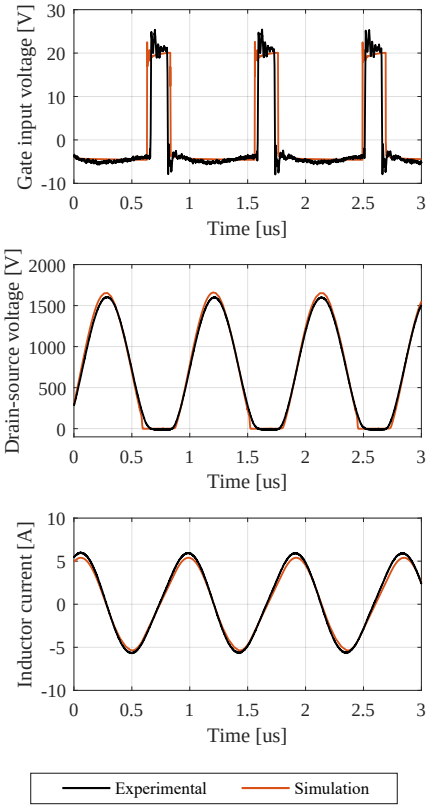


Fig. 3.26: Comparison of experiment and simulation waveforms of the LC oscillator at 1 MHz [Paper C].

causes a short circuit, as shown in Fig. 3.27. Some bubbles due to heating have formed on top of the gate driver IC, and the failure due short circuit of the 10 kV SiC MOSFET is evident.

In conclusion the tests demonstrated the 1 MHz resonant operation of a 10 kV SiC MOSFET. The chosen integrated power module structure allowed for a low inductive gate driver design and did not shown sign of issues related to the medium voltage operation. However, the module showed weak electromagnetic compatibility due to coupling through the DBC during high $\mathrm{d}v/\mathrm{d}t$ switching. The issues related to this were not identified during design because the circuit was only simulated for its drain-source path and the output of the gate driver was assumed independent. The SPICE models of the gate driver IC was not available, which potentially could have given some insight to EMI challenges.

Fig. 3.27: Picture of the integrated power module after failure.

3.4 Conclusion

The issue related to parasitic capacitance in conventional power module structures was identified in Section 3.1. The heat sink voltage used as an indirect measurement of the parasitic capacitance was demonstrated, with clear distinction when 86 pF contributed from the experimental setup was not included. A 10 kV SiC MOSFET half-bridge power module with a 50 % reduction in parasitic capacitance was designed, without penalizing other parameters of the power module. It resulted in a 15 % faster turn-off speed, while the heat sink voltage spike during switching was reduced by 26 %.

Experiments in Section 3.2 showed a reduction of 45 % in the thermal resistance from junction to ambient when the gate driver is integrated on a DBC inside the power module compared to the conventional placement on a PCB. It was found that a gate-source loop inductance of 5.5 nH is required for a CPM2-1200-0160B die for it to obtain a critically damped gate-source voltage when no external gate resistance is added. Designing a power module with an integrated gate driver with this gate-source inductance and using a auxiliary source connection resulted in clean switching with very limited oscillations. The results also showed the usefulness of simulation Method B during the design phase. The method proved adequate to obtain good simulation results for the single layer DBC based power modules used in low current applications.

Section 3.3 demonstrates the capability of switching a 10 kV SiC MOSFET die at a frequency of 1 MHz and peak drain-source voltage of 1.6 kV in a LC oscillator circuit. This is the first documented attempt at switching a 10 kV SiC MOSFET in this frequency range. The achieved operating point is plotted in Fig. 3.28 together with other medium voltage converters using 10 kV SiC MOSFETs presented in literature.

However, at higher operation voltages the parasitic capacitive coupling ruined the safe operation. The integrated DBC method is not regarded as the

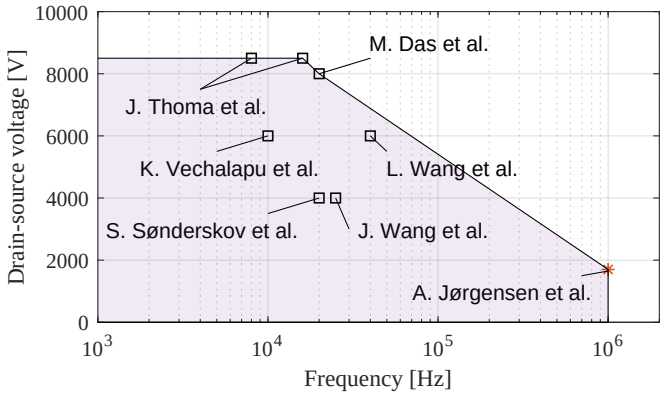


Fig. 3.28: Verified operation of 10 kV SiC MOSFETs at various drain-source voltages and frequencies. Boost converter demonstrators by K. Vechalapu *et al.* [104] and J. Wang *et al.* [105]. Inverter operation demonstrators by M. Das *et al.* [108], S. Sønderskov *et al.* [110], L. Wang *et al.* [111] and J. Thomas *et al.* [112]. The star point indicates the operating point for the experiment presented in this thesis.

most suitable in terms of electromagnetic compatibility, and the low power gate drivers are highly affected by the high $\mathrm{d}v/\mathrm{d}t$ switching. This issue was not predicted in the simulation phase due to the unavailability of SPICE models of the gate driver IC used. Expansion of the range of components included in the simulation framework is regarded as an important future step in terms of accurate and effective digital prototyping.

Chapter 4

Novel integrated packaging of GaN eHEMT devices

The following chapter presents a novel power module structure for fast-switching and high power operation of new GaN enhancement-mode high-electron-mobility transistors (eHEMT) devices.

Integrating the DBC and PCB into the same power module was mentioned in Chapter 1 as the packaging technology currently achieving the lowest inductance while maintaining the good thermal conductivity known from conventional packages. One of the main issues of the integrated modules presented in literature, is that the PCB is molded directly on top of the DBC [36], [37], which significantly increases the manufacturing complexity.

Some new commercially available lateral GaN eHEMT have all electrical connections on their top side, while they have a solderable heat pad on the bottom [114]. This allows for a structure as shown in Fig. 4.1, where the GaN device is sandwiched between a PCB and a DBC. Both the PCB and the DBC can be pre-manufactured independently, and only a vapor phase soldering process is required for the assembly of the stack. The hypothesis is that this solution still enables a low inductive design and good heat dissipation, while the manufacturing is significantly easier.

4.1 Power module design & layout

A proposed power module design is shown in Fig. 4.2, and is configured as a full-bridge. A premanufactured PCB is populated and soldered with all its components, such as DC-link capacitors, gate drivers, voltage regulators and GaN eHEMT devices. The exposed heat pad on the backside of the GaN eHEMT devices are then soldered to aluminium oxide (Al_2O_3) DBC at the bottom. The

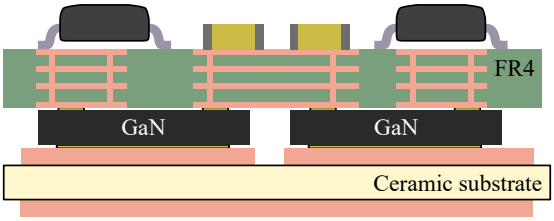


Fig. 4.1: Diagram of the proposed hybrid DBC/PCB power module structure using GaN eHEMT devices. [Paper E]

heat pad of the GaN device is electrically connected to source, thus the DBC has etched islands to isolate each GaN device. Press fit pins are used to interface the power module with DC voltage supply, gate driver signals, shunt resistor voltage signal and switching output. For safety the copper underneath each press fit socket is etched away, to ensure that no pins are shorted through the DBC copper. The assembly is enclosed by a premanufactured plastic housing, which has a hole to allow for potting of protective gel if necessary.

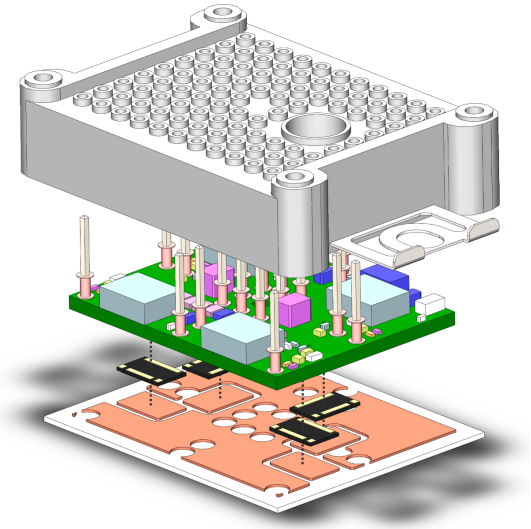


Fig. 4.2: A 3D assembly of the GaN power module. [Paper D]

The schematic for the main power loop of the power module and the gate drivers are shown in Fig. 4.3. Each half-bridge has a decoupling capacitor, C_{De}. A sense resistor is inserted in the power loop path to measure the current, which is useful for control or safety purposes. A 20 nH ferrite bead is inserted in the gate-source loop to suppress high frequency ringing from the source-inductance. For compact switching circuits using WBG it is described in literature that

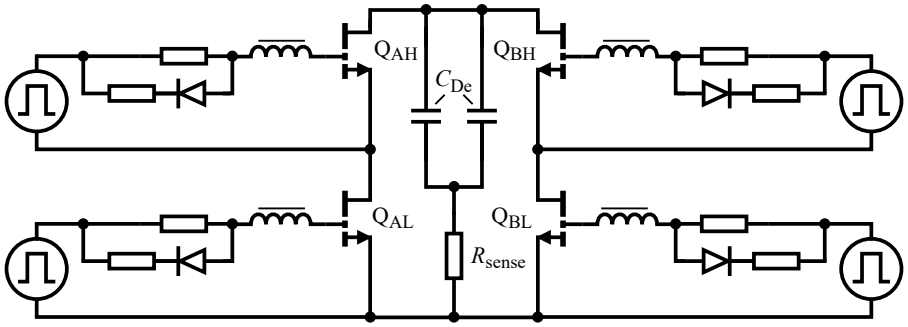


Fig. 4.3: Schematic of the power and gate-drive loop for the integrated GaN eHEMT full-bridge power module.

oscillation issues may occur as the difference between the resonance frequencies of the power loop and gate-source loops are becoming smaller [41], [43], [44]. Placing an additional 20 nH in the gate-source loop significantly shifts the resonance frequency to a much lower region. The size of the gate resistors are designed similarly to the approach presented in Section 3.2.1 and a damping ratio of $\zeta = 0.707$ is chosen, which results in a required gate resistance of 12.4 Ω.

The high-side gate-drivers are powered using a bootstrap circuit and a linear voltage regulator. These components are not included in the simulation framework, and thus are not treated in more detail in this thesis. A circuit diagram of the gate driver is found in Paper D.

The PCB layout of the power module is shown in Fig. 4.4. The PCB layout is done by John Klostergaard Nielsen and Niels Høgholt Petersen at Grundfos A/S. The layout is a compromise between having both low parasitic inductance and low parasitic capacitance, to achieve both fast $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ switching. Parallel planes are often used to achieve low inductance [115], but this would cause the high capacitive coupling. To keep a low parasitic capacitance there is no overlap of the switching output planes and any other planes, as this would otherwise cause unwanted common mode currents to flow during switching [64]. Within the limits of not having any parallel planes, the GaN eHEMT devices have been arranged to keep a relatively small switching loop area. Multiple via arrays are used to connect the top and bottom sides of the PCB, with the decoupling capacitors directly positioned on top of one of the GaN devices. A current shunt resistor array is inserted in the power loop current path, based on the designs presented in [48], [58]. The current shunt resistor array method has relatively low insertion inductance [46], which also increases the measurement bandwidth [47].

The power module is manufactured in the following steps at the packaging laboratory at the Department of Energy Technology, Aalborg University. An

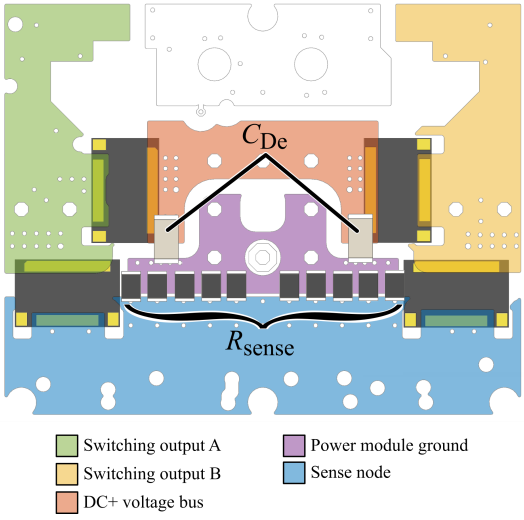


Fig. 4.4: Layout of the PCB planes in the integrated GaN power module.

Al_2O_3 DBC mastercard is aligned with a printed photomask of the layout. A single mastercard holds up to 16 power modules. The entire mastercard is etched with its pattern and cut into smaller segments. The PCB boards arrive premanufactured in a panel. A stencil is aligned with the PCB and solder is applied. The PCB is populated with components using a manual pick and place machine, and the PCB is soldered in a vapor phase reflow soldering oven. As the solder liquefies the surface tension and solder mask design aligns the components correctly on the PCB. A solder stencil pattern is then applied to the DBC, the PCB is placed on top, and the power module is soldered once more. The final power module is shown in Fig. 4.5.

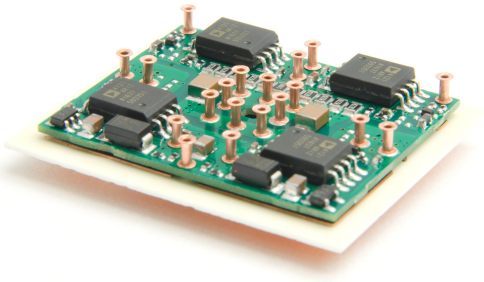


Fig. 4.5: Picture of the manufactured integrated GaN eHEMT power module. [Paper D]

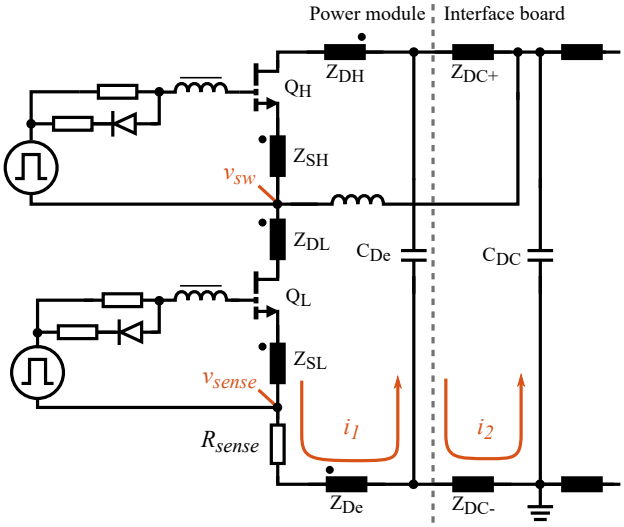


Fig. 4.6: Schematic used for the comparing simulation complexities. [Paper D]

Table 4.1: Level 1 self-inductance of traces [Paper D]

Symbol	Value	Symbol	Value
L_{DH}	0.31 nH	L_{De}	0.23 nH
L_{SH}	0.26 nH	$L_{\mathrm{DC+}}$	1.9 nH
L_{DL}	0.35 nH	$L_{\mathrm{DC-}}$	0.3 nH
L_{SL}	0.86 nH		

4.2 Electrical switching performance and simulation

The following section experimentally demonstrates the switching performance and also investigates the influence of different simulation/modelling. In summary, an electrical simulation model is created of the PCB board based on the Method A and Method C mentioned in Chapter 2. As the PCB board is more compact than conventional single-layer power modules, it is expected that the impact of including the magnetic coupling is pronounced for this power module. The simulation model used for the parasitics of a single half-bridge is shown in Fig. 4.6.

In this chapter Method A is denoted as a Level 1 model. This method extracts the self-inductances of each trace. The self-inductances of the impedances, Z_x, as shown in Fig. 4.6 are listed in Table 4.1.

Table 4.2: Levels of complexity in simulation models [Paper D].

	Board parasitics	Component parasitics
Level 1	L w/o coupling	Ideal R, L or C
Level 2	RLC incl. coupling	Ideal R, L or C
Level 3	RLC incl. coupling	Measured RLC

Method C includes the magnetic coupling between trace inductances and the capacitive coupling between traces. In this chapter this level of simulation complexity is denoted as a Level 2 model. An additional level of complexity is added to this study where RLC-parasitics of the SMD components are included. The SMD components are characterized up to 2 GHz using an Keysight E5016B and Keysight 16192A test fixture and an equivalent RLC model is extracted. The model including both coupling between traces and RLC-parasitics of the SMD components is denoted Level 3. A summary of the three different levels of complexities is listed in Table 4.2.

The three different levels of simulation complexities are compared for a turn-off switching transient as shown in Fig 4.7. For the Level 1 model, the power loop inductance is directly obtained by summation of all the self-inductances in the traces, as listed in Table 4.1. When also including the 0.4 nH of the GaN eHEMT device SPICE models, the power loop inductance equals 2.8 nH. In addition to this the resonance frequency of the Level 1 model is read from Fig. 4.7 to be 325 MHz. For the LC parasitics in the power loop (i_1 in Fig. 4.6), they create a resonance frequency given by

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{4.1}$$

By rearranging (4.1) the output capacitance of the GaN eHEMT device is estimated as

$$C = \frac{1}{(2 \cdot \pi \cdot 325\text{MHz})^2 \cdot 2.8\text{nH}} = 85\text{pF} \tag{4.2}$$

The Level 1 model power loop inductance was calculated just by summation of trace self-inductances. However, Level 2 and 3 models include the mutual coupling between the inductances, and thus it is more cumbersome to calculate the effective loop inductance. Knowing the output capacitance of the GaN eHEMT device and using (4.1) allows us to estimate the power loop inductance in Level 2 and Level 3, just by reading their resonance frequency from the simulation results.

The simulation results of Fig. 4.7 show that the resonance frequency for Level 2 and 3 are slightly higher, which suggest that the power loop inductance is lower. The resonance frequencies are read as 358 MHz and 338 MHz for

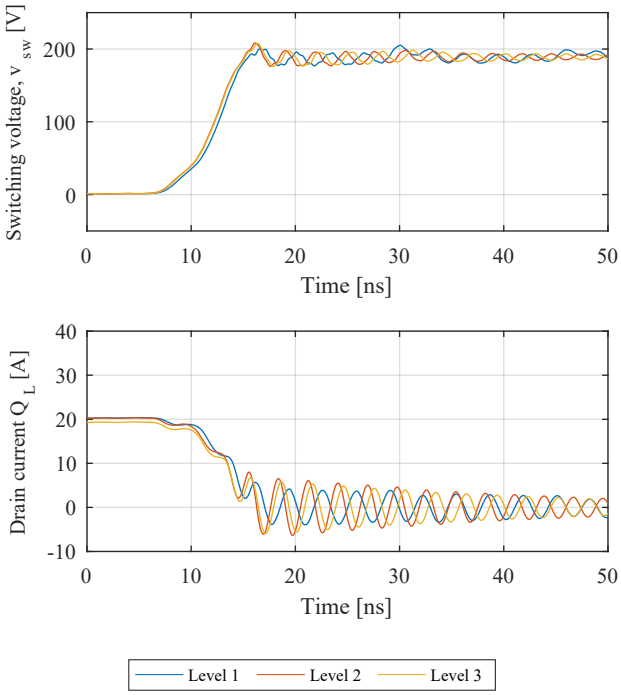


Fig. 4.7: Simulated switching voltage and drain-source current with three levels of simulation complexity. [Paper D]

simulation models Level 2 and 3, respectively. Rearranging (4.1), the effective inductances of Level 2 and Level 3 are 2.32 nH and 2.61 nH. In conclusion the effective power loop inductance is 8 % higher for Level 1 (which only includes self-inductance), when compared to the Level 3 which includes both the mutual coupling and the RLC parasitics of the components on the board.

To verify the simulation results an experimental test setup is constructed. The PCB layout of the test-board is designed by John Klostergaard from Grundfos A/S. The test board is shown in Fig. 4.8. The experimental waveforms at a switching condition of 400 V / 15 A are shown in Fig. 4.9, with the simulation results of Level 3 superimposed. The experimental results and the detailed modelling of both the PCB and SMD components show very good agreement. The voltage fall and rise times are read as 5 ns and 8 ns, respectively. This is equivalent to a voltage transient of 64 V/ns and 40 V/ns, in the two cases. Additionally, the resonance frequency is 335 MHz. If the output capacitance is assumed to be 85 pF as observed in the SPICE device model, this corresponds to an effective power loop inductance of 2.65 nH. In summary, Level 1 which only includes self-inductance of traces predicts a too high inductance compared to experiment. Using Level 2 where magnetic coupling is included, predicts a

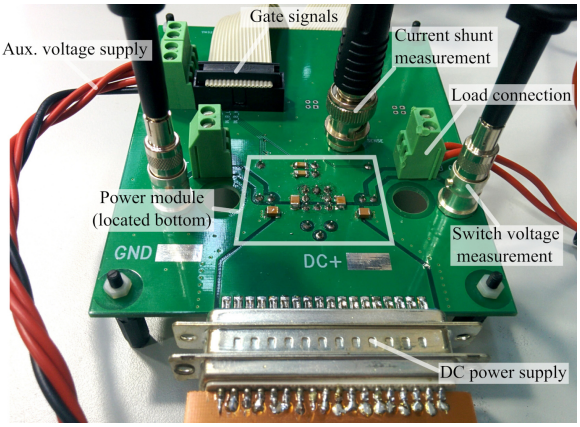


Fig. 4.8: Test board used for the experimental switching test of the GaN power module [Paper D].

too low. Including the RLC parasitics of the SMD components as done for Level 3, adds the required inductance to correctly predict the resonance frequency with very little error.

4.3 Thermal characteristics of integrated packaging

The following section describes the thermal characteristics of the designed integrated power module. Literature on the development of hybrid DBC/PCB integrated power modules present simulations showing that the thermal performance is up to par with conventional power modules [37], [116]. However, these studies have been done by only modelling the dies on the DBC and do not include the copper layers/traces of the PCB. One hypothesis is that the very thin copper layers and the FR4 material has poor heat conductivity, and thus does not impact the thermal characteristics of the power module. In that case it could be ignored without significant error. It could also be the case that the simulation of the PCB is cumbersome and a task that has not been prioritized due to the lack of the right tools. However, in this thesis a simulation software flow diagram has been presented in Chapter 2 which allows the combination of 3D models of the DBC and PCB structures. Secondly, in literature the thermal characteristics of the hybrid DBC/PCB structures have not been experimentally verified and are only based on simulation. Thus the purpose of this section is to describe the influence of the PCB on the thermal characteristics and experimentally verify the thermal simulation model.

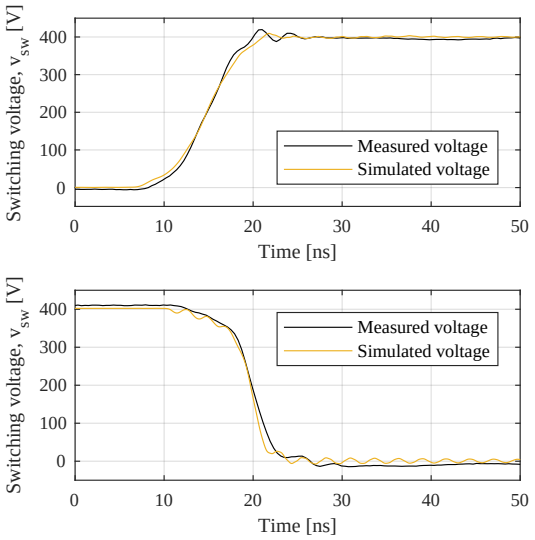


Fig. 4.9: Experimental drain-source voltage and Level 3 simulation during 400 V / 15 A turn-off and turn-on. [Paper D]

4.3.1 Thermal modelling

The methodology of the thermal study is to apply a power loss in one of the devices, and measure the temperature change of the device. Power is dissipated in the junction of the device and flows to the ambient, thus we may define a thermal impedance of the device which dissipates the power as

$$Z_i(t) = \frac{T_i(t) - T_\mathrm{a}}{P_i(t)} \tag{4.3}$$

where Z_i is the thermal impedance of device i, T_i is the temperature of device i, T_a is the ambient temperature and P_i is the power loss in device i. When power is dissipated in one of the devices, there will be a thermal coupling effect, meaning that the other devices on the power module are also experiencing a change in temperature. This is described by the thermal characteristic parameter, Ψ, defined similarly as for the thermal network for the gate driver IC in section 3.2.3, which is given by

$$\Psi_{ij}(t) = \frac{T_i(t) - T_\mathrm{a}}{P_j(t)} \tag{4.4}$$

The thermal characteristic parameter, Ψ_{ij}, is read as the temperature increase of device i, due to the power dissipation in a neighboring device j. It is important to note the difference between the thermal impedance, Z, and the thermal characteristic parameter, Ψ. The thermal impedance, Z can be used only in the

cases where the power flow path is known. In a practical case the exact amount of power flowing between one device to another is not known, and thus it cannot be defined as a thermal impedance, which is why the thermal characteristic parameter Ψ_{ij} is introduced. By applying (4.3) and (4.4) to all four devices in the power module [117]–[119], the temperatures can be calculated from

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix} = \begin{bmatrix} Z_1 & \Psi_{12} & \Psi_{13} & \Psi_{14} \\ \Psi_{21} & Z_2 & \Psi_{23} & \Psi_{24} \\ \Psi_{31} & \Psi_{32} & Z_3 & \Psi_{34} \\ \Psi_{41} & \Psi_{42} & \Psi_{43} & Z_4 \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{bmatrix} + T_{\mathrm{a}} \tag{4.5}$$

The devices are labelled as indicated in Fig. 4.10

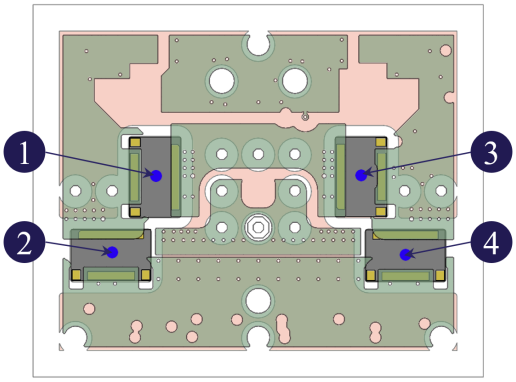


Fig. 4.10: Labelling of device temperature measurement points. [Paper E]

4.3.2 Simulation results

A three dimensional model of the power module is created, based on the software flow diagram presented in Chapter 2. A 3D model was created of the DBC and the GaN devices in Solidworks which has the overall mechanical layout. The 2D layer information of the PCB is imported to ANSYS Electronics Desktop, from which a 3D model is created in the software and later exported as a 3D file. The 3D model of the PCB is then assembled with the other parts using Solidworks. The power module is imported into COMSOL used for the thermal simulation, as shown in Fig. 4.11. The model of the power module requires a relatively fine mesh to also include the details such as thin vias, which is also indicated in the figure.

Device 1 has a power dissipation of 1.8 W (equivalent to 6 A through the 50 mΩ on resistance of the device), and the temperatures are logged. By using (4.3) and (4.4) the thermal characteristics are extracted as the solid line in Fig. 4.12. In steady state the value of Z_1, Ψ_{21}, Ψ_{31} and Ψ_{41} is predicted as

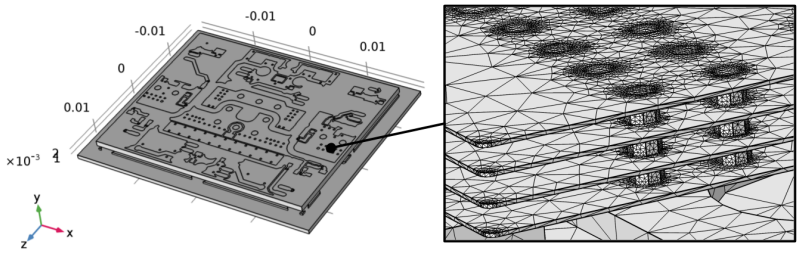


Fig. 4.11: Picture of the mesh quality used for solving the thermal problem. [Paper E]

2.07 K/W, 0.76 K/W, 0.22 K/W and 0.16 K/W, respectively. The simulation model is used to investigate the influence of the PCB.

A new simulation is created where the PCB is disabled in the simulation, meaning that no power flows between devices through the PCB. The results of this simulation is shown in the dashed lines of Fig. 4.12. The steady state value of the thermal impedance of the heated device is increased to 2.33 K/W. This corresponds to an increase of 13 %. For the same power dissipation, the entire power module is heated more when there is no PCB, because the copper layers are not distributing the heat to a greater area of the copper.

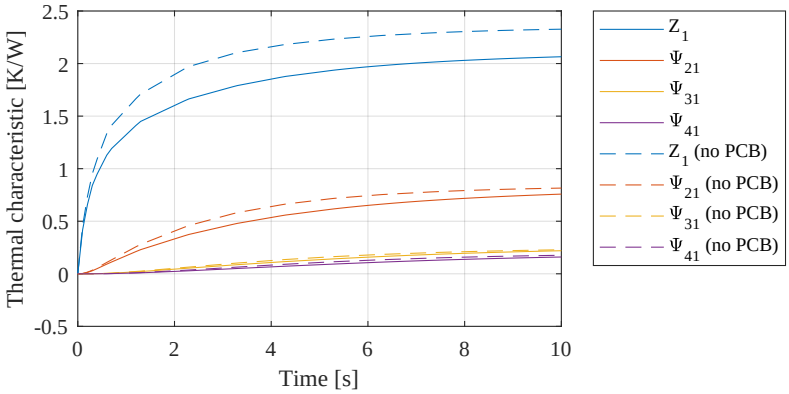


Fig. 4.12: Simulated thermal characteristics with and without the PCB. [Paper E]

4.3.3 Experimental results

An experimental setup is prepared to verify the proposed simulation model. The purpose is to both verify the time constants and the amplitudes of the transient thermal response. A power module is prepared in a housing which has its top milled away. This allows to clamp down the power module to the heat sink, while still having access with optic temperature sensors from Opsens. The

PCB has been manufactured with a small non-filled via on top of each GaN device, thus allowing the temperature sensor a contact point of each device, as shown in Fig. 4.13. The gate driver circuit components are not soldered

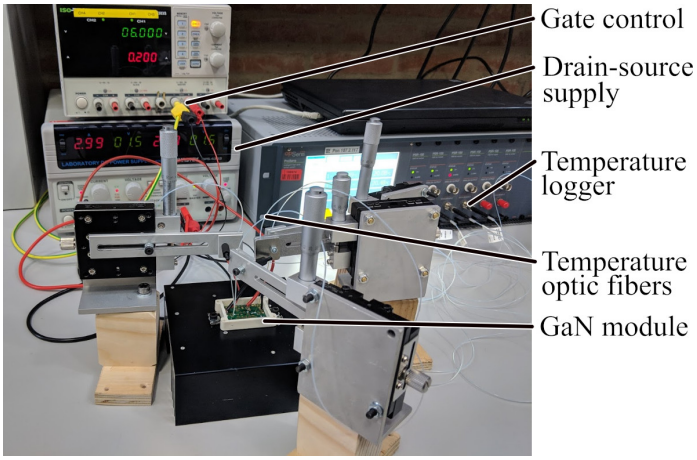


Fig. 4.13: Picture of experimental setup for the thermal test of the GaN power module.

to the PCB for two reasons. The used gate driver bootstrap circuit has limits on the duty cycle and thus should be bypassed to apply the DC power step. Secondly, the thermal model of components on the PCB board is unknown, and thus to ensure a fair comparison to the simulation, the experimental setup is also prepared without any components soldered to the PCB, as this would add thermal mass and could influence the thermal time constants.

A DC power supply in current control mode is connected to the drain-source terminals to supply 6 A, while a second voltage controlled channel is connected to give supply +6 V gate signal. The temperatures are logged for all four devices and (4.3) and (4.4) is applied to the data. The results are shown in Fig. 4.14.

There is a maximum absolute error in temperatures between experiment and simulation of 0.27 °C, which is within the accuracy of the OTG-M280 fiber optic sensors which is ± 0.3 °C [120]. The experiment verifies the magnitude and the time constants of the thermal responses simulated using the finite element method. In conclusion the experimental tests have verified the simulation model. This implies that the results predicted by the simulation related to the thermal contribution from the PCB are considered trustworthy. The PCB contributes with more distribution of the dissipated losses, with results predicting a 13 % increase of the thermal resistance if the PCB is not included.

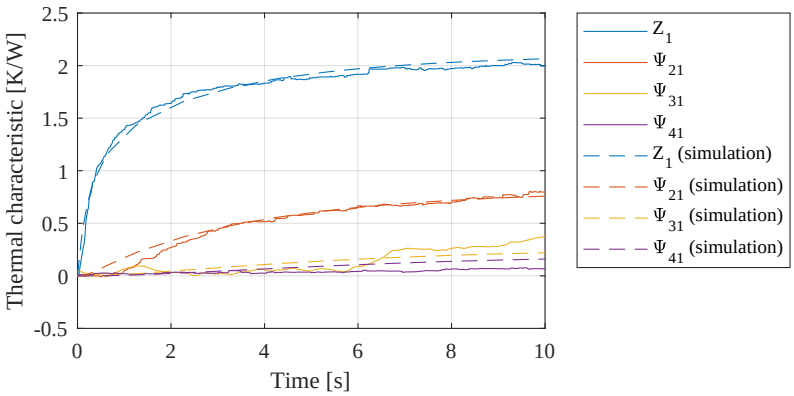


Fig. 4.14: Experimental results during 6 A conduction losses in device 1, with simulated responses for similar conditions in dashed line.

4.4 Benchmarking and discussion

The designed GaN full-bridge prototype is compared with other available commercial full bridge power modules rated at 600-650 V and 15-30 A. The developed GaN prototype is compared to the Semikron SK25GH063 [121] and Infineon IKCM15R60GD [122] Si IGBT full-bridge intelligent power modules (IPM). Shown in Fig. 4.15 is the thermal resistance, on-state voltage drop at 15 A, combined turn on/off losses at 300 V / 15 A and cost for each module in the comparison.

The thermal resistances are similar for the three modules, while the on state voltage is slightly lower for the GaN prototype. The higher on state voltage drop for the Si IGBT IPM modules is mainly due to an initial 0.75-1 V forward voltage, while the GaN is resistive in its on characteristic. The main difference between the GaN prototype and the Si IGBTs is that the switching losses can be reduced by about 75 % to 90 % but comes at an increased cost of 3-4 times. The cost of the GaN eHEMT power semiconductors make up around 60 EUR of the 70 EUR total cost of the GaN module. With an expected global growth in the market of GaN, the unit cost per semiconductor is expected to drop likewise [123], [124]. Power modules based on GaN semiconductors are regarded as a viable choice in future power electronics designs due to their superior switching performance.

4.5 Conclusion

This chapter has introduced a new integrated hybrid DBC/PCB power module structure, enabled by the use of new commercially available GaN eHEMT power

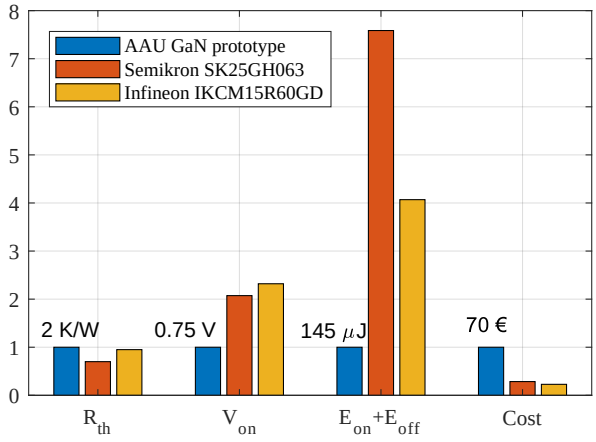


Fig. 4.15: Benchmark between the developed AAU GaN full bridge prototype, Semikron SK25GH063 Si IGBT full-bridge IPM and Infineon IKCM15R60GD Si IGBT full-bridge IPM. They are compared on the thermal resistance, R_{th}, on-state voltage drop V_{on} at 15 A drain-source/collector-emitter current, combined switching energy $E_{\text{on}} + E_{\text{off}}$ at 300 V / 15 A and cost in EUR (lower is better for all parameters). The barchart values are normalized to the value of the GaN prototype.

devices. The power module structure is easier to manufacture compared with other similar hybrid DBC/PCB solutions. A full-bridge prototype is designed in collaboration with Grundfos A/S. A simulation model is presented which includes the extraction of electrical parasitics of the designed PCB board. Three simulations are presented each with a different level of simulation complexity and the influence is compared. Very accurate simulations results are obtained when both mutual coupling of the PCB and the RLC parasitics of each SMD component on the board is included. A power loop inductance of 2.65 nH and a switching speed of 64 V/ns is experimentally demonstrated without significant voltage overshoot. The 3D model of the PCB is used to build an accurate thermal simulation of the power module by following the proposed simulation framework. The thermal simulation model is experimentally verified. The simulation model predicts an increase of 13 % of the thermal resistance if the PCB layers are not included. The PCB layers distribute the generated losses to the other GaN components in the power module, which increases the effective cooling area. The developed GaN prototype offers a reduction in 75 % - 90 % in switching losses when compared with conventional Si IGBT power modules, but comes at an increased cost of 3-4 times.

Chapter 5

Conclusion & future work

To better utilize the benefits of WBG power semiconductors two objectives are defined in Chapter 1 of this thesis as

> To investigate and design packaging prototypes to push the operating range, improve the fast-switching or high voltage switching capabilities of WBG power semiconductors.
>
> To develop and build a digital design framework used for virtual prototyping of new integrated packaging solutions.

The main research contributions of this thesis to the field within simulation and design of power module packaging for WBG semiconductors are summarized as

- This thesis presents a framework for simulation based design for accurate thermo-electric modelling of advanced integrated power modules. The simulation framework is not regarded as a novelty, however a description of simulation tools used is often sparse in published research. This thesis narrows the gap of such framework knowledge.
- The thermal influence of integrating ICs on DBC has been experimentally investigated, with results demonstrating a possible reduction of 45 % in thermal resistance from junction to ambient, if the gate driver IC is placed inside a power module compared to conventional placement on a PCB. This allows WBG semiconductors to be operated without ringing and at much higher frequencies with no requirement of using resonant gate drivers.
- This research presents and demonstrates the worlds first MHz-range operation of a 10 kV SiC MOSFET die. The results indicate the capability of the die to be driven at higher frequencies than previously shown in literature, but more research is required to obtain robust operation.

- A new integrated power module structure using GaN eHEMT power semiconductors with top contacts is proposed. Compared with other integrated PCB/DBC power modules, it significantly reduces the manufacturing complexity while maintaining both good electrical and thermal performance. Experiments demonstrate a 2.65 nH power loop inductance and a switching speed of 64 V/ns with no voltage overshoot. The power module may reduce switching losses in the range of up to 75 - 90 % compared with conventional Si IGBT based intelligent power modules.

- The research contributes with the first thermal simulation of an integrated DBC/PCB power module structure that includes the influence of the PCB board. The results indicate an error of 13 % in the prediction of thermal resistance if PCB layers are not included, which has not been case for the currently published integrated DBC/PCB power modules.

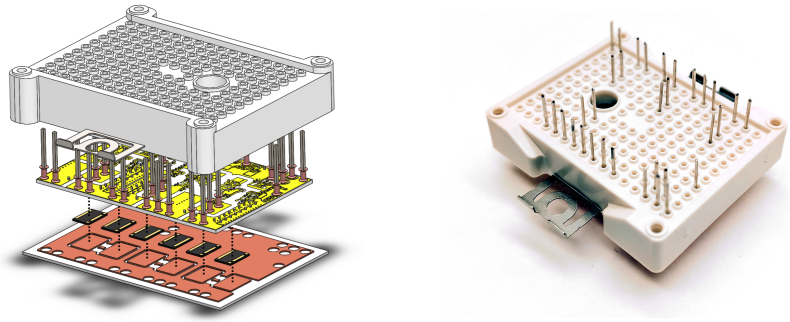
5.1 Future work

The following section highlights several aspects of the presented research which is currently being investigated in more detail or which is planned as future work.

- The developed 10 kV SiC MOSFET half-bridge power module with lower parasitic capacitance is currently undergoing switching tests to map the influence of parasitic capacitance on the switching losses. By detailed voltage and current measurements on two modules that only differ by their parasitic capacitances, it can be effectively mapped out how much losses can be attributed to the parasitic capacitance. The experimental tests are being done in collaboration with Ph.D. student Dipen Narendrabhai Dalal[1]. Following the switching tests, the power modules are to be used in a three-phase medium voltage drive demonstrator.

- For this thesis the electromagnetic finite element simulations and the implementation in SPICE mainly concerned the drain-source and gate-source (output side of the gate-driver circuit) of the power modules. Some issues were encountered, especially during the testing of the medium voltage high frequency integrated power module, which is related to the input side of the gate driver. Future research should focus on expanding the boundary of what is included in the detailed modelling of the circuits, including: input signal integrity to gate drivers, dynamics of linear voltage regulators, decoupling capacitors used for voltage supply. However, one of the main obstacles in this regard is the availability of detailed SPICE

[1]Ph.D. student Dipen Narendrabhai Dalal, Aalborg University working on project titled "Medium Voltage converter based on SiC (MV-BASIC)" - more information available at https://www.et.aau.dk/phd/ongoing-phd-projects/medium-voltage-converter-based-on-sic-mv-basic/



(a) (b)

Fig. 5.1: (a) Exploded 3D view and (b) photograph of manufactured integrated GaN eHEMT three phase power module.

models (or similar) from many IC manufacturers, which is an issue to be addressed.

- The medium voltage high frequency power module had issues with noise on the integrated gate-driver circuit during switching of the 10 kV SiC MOSFET die at increasing voltages. Solutions to mitigate the noise issues should be investigated or alternative packaging solutions should be tested.

- Based on the successful thermal simulations of the integrated GaN eHEMT power module, the next step is to include the physics of thermo-mechanical expansion in the simulation. This is useful to evaluate the thermo-mechanical stress experienced by the module during operation. This may give indications to reliability issues associated with the new packaging structure.

- The GaN full-bridge power module has shown great electric and thermal performance. Due to these results the concept is currently being expanded for a three-phase power module prototype, with the aim of powering a three phase electric drive as a final demonstrator for the technology. This will further highlight the influence of the fast-switching on the filter design and electric drive. A 3D model and a picture of the manufactured three-phase GaN eHEMT power module is shown in Fig. 5.1

Chapter 6

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Part II

Appended papers

Paper A

Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM

Asger Bjørn Jørgensen, Nicklas Christensen, Dipen Narendra Dalal, Simon Dyhr Sønderskov, Szymon Bęczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen

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Asger Bjørn Jørgensen, Nicklas Christensen, Dipen Narendra Dalal, Simon Dyhr Sønderskov, Szymon Bęczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen

Abstract

The benefits of emerging wide-band gap semiconductors can only be utilized if the semiconductor is properly packaged. Capacitive coupling in the package causes electromagnetic interference during high dv/dt switching. This paper investigates the current flowing in the parasitic capacitance between the output node and the grounded heat sink for a custom silicon carbide power module. A circuit model of the capacitive coupling path is presented, using parasitic capacitances extracted from ANSYS Q3D. Simulated values are compared with experimental results. A new iteration of the silicon carbide power module is designed, having reduced capacitive coupling without penalizing other parameters. The new module is tested experimentally, which verifies the reduced capacitive coupling to the heat sink.

Introduction

Emerging wide-band gap semiconductors, such as silicon carbide (SiC) MOSFETs, offer higher breakdown voltage, faster switching speeds and increased operating temperatures, when compared to their silicon counterparts [1], [2]. The capability of a semiconductor to switch fast is influenced by both parasitic inductances and capacitances, introduced by the semiconductor die itself and the package. Fig. A.1a shows parasitic capacitances and main resistances of the semiconductor die. A more detailed model is obtained when considering the parasitic inductances of the package, i.e. copper tracks, terminal pins and bond-wires. Furthermore, direct bonded copper (DBC) planes are only separated from the grounded heat sink by a 0.63 mm aluminium nitride (AlN) substrate layer, causing the Cu-AlN-Cu layers to act as capacitors. Including these parasitic capacitances and inductances, a circuit model of a half-bridge module is shown in Fig. A.1b, in which the semiconductor die parasitics are included in the MOSFET symbols. This model describes the power module during switching transients.

A half-bridge power module with 1st generation 10 kV / 10 A SiC MOSFETs from Wolfspeed is designed and packaged at the Department of Energy Technology, Aalborg University. The module, with baseplate dimensions 104 mm x 59 mm, is shown in Fig. A.2a. Package design for low inductance has

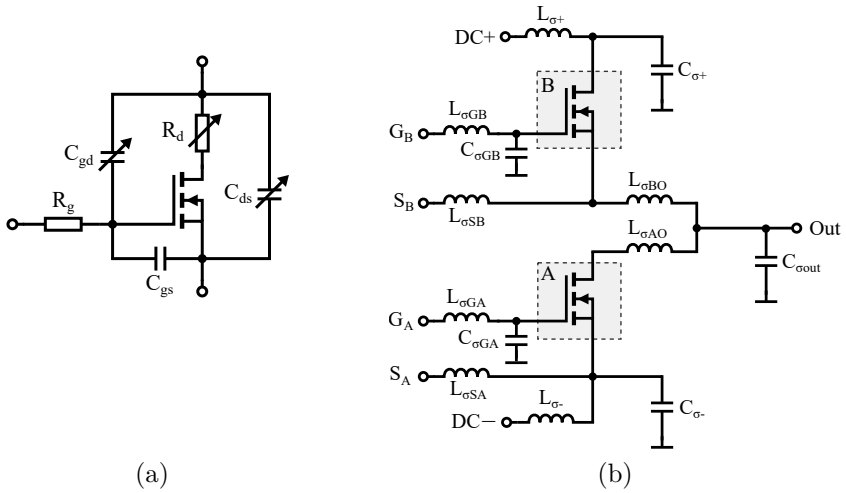

Fig. A.1: (a) Parasitics of the SiC MOSFET die and (b) parasitics added by the packaging.

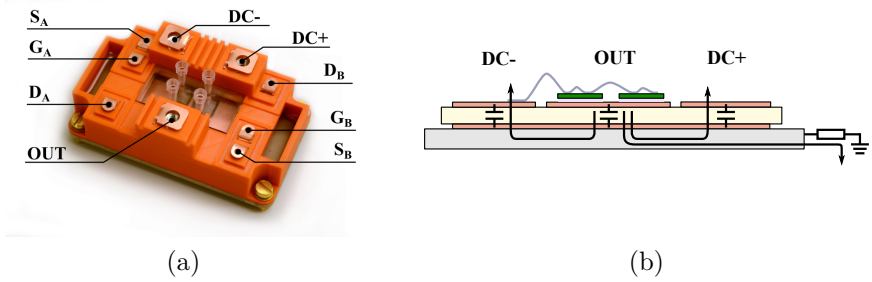

Fig. A.2: (a) Photograph of designed module and (b) principle diagram of capacitive coupling paths.

been studied extensively in literature by the use of Finite Element Method (FEM) software [3]–[7]. During double pulse testing of the module, large current flowing from the output node to the heat sink is observed, as indicated in Fig. A.2b. The high voltage potential and fast switching of the output node, is coupled to the grounded heat sink through parasitic capacitances $C_{\sigma out}$ and $C_{\sigma GB}$. This displacement current does not flow laterally through the copper tracks and bond wires, and thereby bypasses main inductances of the switching circuit model in Fig. A.1b. The currents conduct to both the DC-link and through gate drive circuitry [8], and causes electromagnetic interference (EMI) issues which limits the switching speed of the circuit [9], [10]. O. Kreutzer et. al. [11] suggests the use of a Y-capacitor to suppress this EMI, but in this paper efforts are on mitigating the root cause.

The aim of this paper is to design a power module with low capacitive

coupling between the output node and the heat sink. Circuit diagrams and simulation tools are used and verified to aid the design of a new module. The new power module should be designed without penalizing other parameters. After packaging, the module is tested experimentally to evaluate the effect of the proposed changes.

Design of simulation model and experimental platform

The parasitic capacitances, of the module shown in Fig A.2a, are evaluated in ANSYS Q3D and listed in Table A.1. In order to evaluate the simulation, a double pulse test is used to compare simulated parasitic capacitances and experimental results. In this test the voltage on the heat sink is measured, as a direct measure of the capacitive coupling between top and bottom side DBC planes.

Table A.1: Simulated parasitic capacitances of the SiC power module on 0.63mm ceramic

Parasitic	$C_{\sigma+}$	$C_{\sigma out}$	$C_{\sigma-}$	$C_{\sigma GB}$	$C_{\sigma GA}$
Value	101 pF	149 pF	45 pF	19 pF	22 pF

In addition to the calculated values of the module, contributions from the experimental setup are included. A cooling fan is mounted on the heatsink and the voltage is measured with a high voltage Lecroy PPE probe. The capacitive coupling to the fan is measured as 80 pF using a Keysight E4990A impedance analyzer. The datasheet of the voltage probe states 6 pF of coupling to ground. Thus a total auxiliary contribution of 86 pF is added to the model. When currents flow as in Fig. A.2b, the main parasitic inductances, i.e. copper tracks and bond wires, of Fig. A.1b must be ignored. Neglecting inductances, the simplified model of the system based only on capacitive values evaluated in ANSYS Q3D is shown in Fig. A.3. Currents through capacitances $C_{\sigma GB}$ and

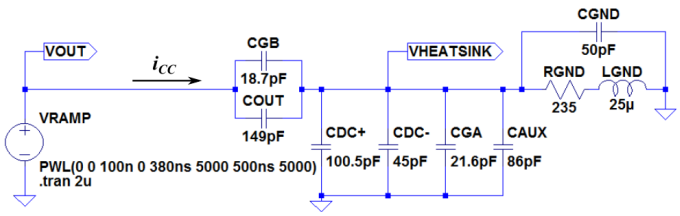

Fig. A.3: LTSpice model to simulate heatsink voltage and current.

$C_{\sigma GA}$ are critical, as they may influence vulnerable gate driver circuitry and control signals. From (A.1), mitigating the coupling current is done by reducing

the capacitive coupling and ensuring slow transients of voltage to the heat sink, but it is not desirable to slow the switching speed of the MOSFETs.

$$i_{CC}(t) = (C_{\sigma GB} + C_{\sigma out}) \cdot \frac{\mathrm{d}(V_{out} - V_{heatsink})}{\mathrm{d}t} \tag{A.1}$$

The heat sink is grounded using a power resistor to provide damping, and is modelled by a resistance $R_{gnd} = 235\ \Omega$, in series with an inductance of $L_{gnd} = 25\ \mu$H and has a parallel parasitic capacitance of $C_{gnd} = 50$ pF. Alternatively, grounding with a short wire, modelled by a series RL-circuit of 0.1 mΩ and 200 nH, could be used. LTSpice simulations of heat sink voltage and combined capacitive coupling current, i_{CC}, for the chosen grounding resistor and the case of undamped short wire is shown in Fig. A.4.

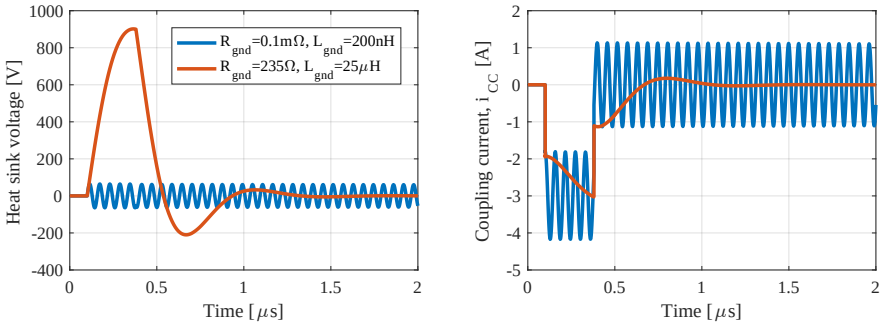

Fig. A.4: LTSpice simulation results of heatsink voltage (left) and current (right) for damped and undamped grounding impedance, during a double pulse test at 5 kV switching in 280 ns (18.2 kV/μs)

The results show that the amplitude of the current flowing through the baseplate is driven by (A.1). This current passes through gate drive and control circuitry, resulting in reduced signal integrity and undesirable noise in grounding planes. The simulation also shows that the higher resistance causes damped transients but increases the amplitude of the heat sink voltage. On the other hand the low resistance reduces heat sink voltage amplitude, but causes undamped ringing which in turn causes current to continuously flow. Since the latter way leads to system instability, the 235 Ω high voltage resistor is chosen for further experiments.

Experimental validation of FEM

The LTSpice model based on capacitances evaluated in ANSYS Q3D is verified using a double pulse test at a DC-link voltage of 5 kV. An experimental test bench was designed to ensure robust operation during high voltage switching [12]. The SiC power modules are powered from custom designed gate driver

supplies [13], due to high coupling capacitance in commercially available medium voltage DC-DC supplies [14]. Voltages of the half-bridge output and heat sink are measured as depicted in Fig. A.5. The LTSpice simulation results are also shown with and without the influence of the auxiliary voltage probe and heat sink fan. There is very good agreement between the experimental results

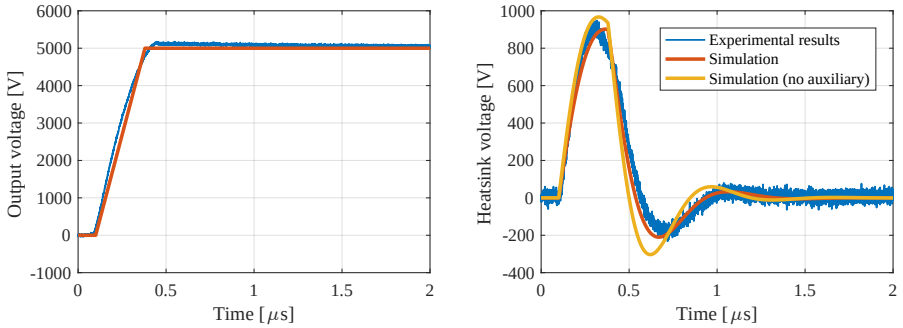

Fig. A.5: Half-bridge output voltage (left) and heat sink voltage (right) during 18.2 kV/μs switching measured experimentally and from LTSpice simulation (with and without influence of auxiliary equipment).

and the LTSpice simulation, which is based on the capacitances obtained in ANSYS Q3D. This result verifies the quantitative accuracy of using ANSYS Q3D in the further design of the power modules. The results also prove the importance of a proper experimental test setup, and that the influence of auxiliary equipment, such as the probe and fan, is taken into consideration.

Developing new design by FEM

The power module design is modified to reduce the parasitic coupling capacitance, without penalizing other parameters excessively. The design is improved by reducing the outer dimensions of the DBC, and by making an overall more compact layout. A total parasitic capacitance of 98 pF is achieved ($C_{\sigma out}$ of 86 pF and $C_{\sigma GB}$ of 12 pF), which is a reduction of 41 % compared to the initial 168 pF. Still a relatively large part of the surface area of the output plane is used to connect to the source terminal S_B of the module. This track was initially kept wide to ensure low parasitic inductance in the gate-source loop. It is desirable to reduce the width of the plane, to reduce the parasitic capacitance, but without increasing the parasitic inductance considerably. The portion of the plane to be removed is marked as the pink area in Fig. A.6. A parametric sweep for the width of the cutout is performed from 0 mm to 7 mm. The parasitic resistance and inductance of three critical paths are monitored. The three paths are: from DC+ to the output terminal, from DC- to the output terminal and the affected

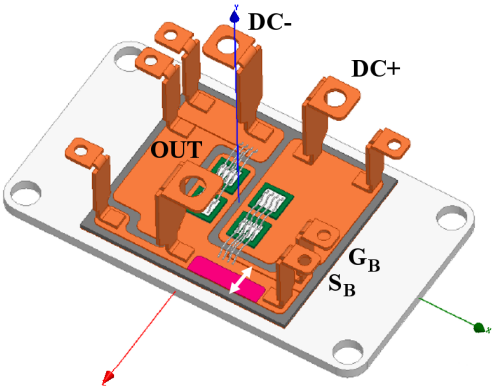

Fig. A.6: ANSYS Q3D model for parametric analysis of reduced Cu track width.

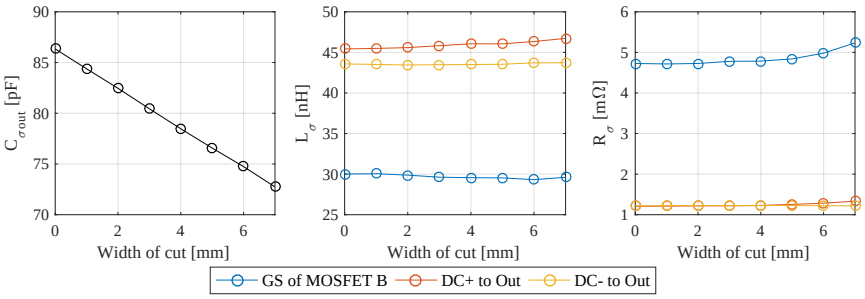

Fig. A.7: $C_{\sigma out}$, L_σ and R_σ as a function of the reduced plane width for three critical paths

gate-source loop of MOSFET B. In this calculation die parameters are excluded i.e. for evaluating the DC+ to output loop the drain and source pads of the MOSFET die are shorted. The results for output capacitance and parasitic inductance and resistance in the three paths considered are shown in Fig. A.7. In ANSYS Q3D low frequency inductances and resistances are evaluated by assuming uniformly distributed current thus neglecting skin effect.

The capacitance is linearly decreasing as the width of the cut is increased, but the parasitic inductance and resistance for all considered current paths are almost constant. Gate-source resistance is mostly affected, but the magnitude is small compared with the gate resistance of the die. At the width of 7 mm to be removed, the remaining track to the source terminal is only 1 mm wide. For manufacturing purposes this is considered the minimum track width for etching of the DBC. At this width the total parasitic capacitive coupling from the output to the heat sink is 85 pF ($C_{\sigma out}$ of 73 pF and $C_{\sigma GB}$ of 12 pF). This is a further reduction of 13 %, without penalizing other parameters. Capacitive couplings from power module planes to the heat sink for the new design are listed in Table A.2. This is the design which is manufactured.

Table A.2: Simulated parasitic capacitances of the new SiC power module on 0.63mm ceramic

Parasitic	$C_{\sigma+}$	$C_{\sigma out}$	$C_{\sigma-}$	$C_{\sigma GB}$	$C_{\sigma GA}$
Value	65 pF	73 pF	32 pF	12 pF	33 pF

In case the design changes proves not to be sufficient to ensure robust operation, modifications to the materials is proposed. The DBC master cards used for the power modules are commercially available with AlN ceramic substrate thickness of 0.63 mm and 1 mm. The increased thickness decreases the capacitive coupling. In an ANSYS Q3D simulation, using a 1 mm substrate layer instead of 0.63 mm reduces the total parasitic capacitance ($C_{\sigma out} + C_{\sigma GB}$) from 85 pF to 57 pF. However, the increased thickness of AlN substrate layer also impacts the thermal resistance. A model of the structure from SiC MOSFET die to heat sink is simulated in COMSOL to evaluate the thermal resistance. FEM is used to account for changing thermal spread angles, caused by the difference in thermal conductivity of each layer [15]. Fig. A.8 shows the temperature distribution throughout the layers at a heat sink temperature of 45 °C, and an average power dissipation level of 55 W per die (estimated from a double pulse test at 5 kV, 5 A). The thermal resistance from junction to heatsink for a thickness of 0.63 mm is evaluated to 0.30 $\frac{\mathrm{K}}{\mathrm{W}}$, and increases to 0.32 $\frac{\mathrm{K}}{\mathrm{W}}$ for a thickness of 1.0 mm ceramic. The penalty of increasing the thickness of the ceramic is only 6 %, due to the relatively high thermal conductivity of 150 $\frac{\mathrm{W}}{\mathrm{m \cdot K}}$ for AlN ceramic [16]. The increased thickness of the ceramic was not implemented, as the main scope is to document the influence of modified DBC layout.

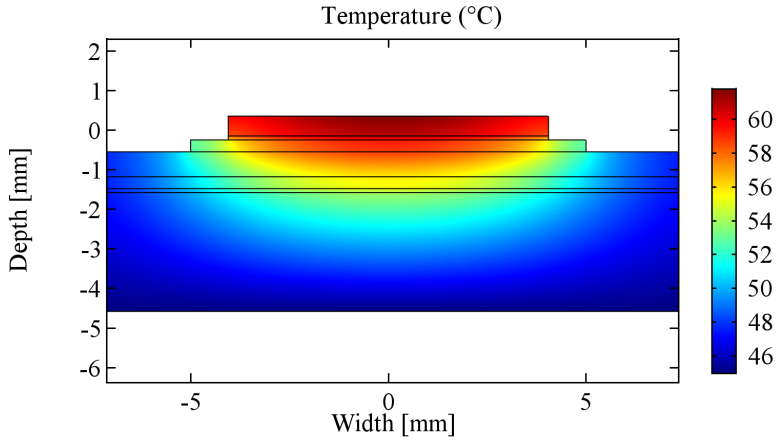

Fig. A.8: Thermal distribution throughout power module layers simulated in COMSOL.

Experimental results

The new improved power module with 0.63mm ceramic thickness was manufactured and packaged, and is shown in Fig. A.9. The power module is populated with 3rd generation Wolfspeed 10 kV / 17 A SiC MOSFET dies. An important improvement in the new generation die is that it has higher gate-source threshold voltage. This change makes it less vulnerable to noise and parasitic turn on. The improved DBC layout and higher robustness of the MOSFET die allows

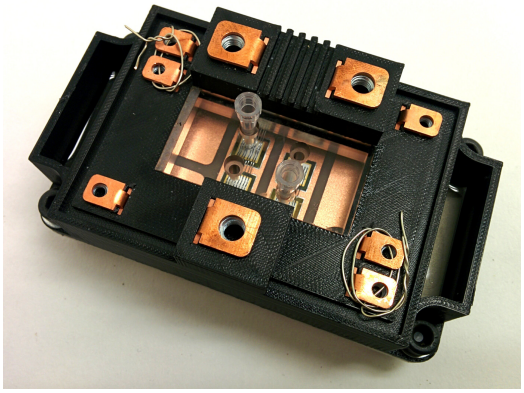

Fig. A.9: Photograph of the new improved power module.

the new test to be done at a switching speed of 21.0 kV/μs. The output voltage and the heat sink voltage during the test are shown in Fig. A.10. As in Fig. A.5 an excellent quantitative agreement between simulation and experiment is observed. The new module is switching 15 % faster, while the amplitude of the heat sink voltage is reduced by 26 %, when compared to the old module in Fig. A.2a.

Conclusion

The high voltage breakdown and fast switching speed of SiC MOSFETs put further demand on low capacitive coupling in power module packaging. A model of parasitic coupling capacitances was evaluated for a SiC MOSFET power module using ANSYS Q3D. A double pulse test verifies the agreement between experimental tests and simulation. The result justifies the use of ANSYS Q3D for further design improvements.

The paper proposes design modifications which reduces the parasitic capacitive coupling. Smaller DBC dimensions and reduced track widths reduces the total output coupling capacitance from 167 pF to 85 pF, which is experimentally verified. A further reduction from 85 pF to 57 pF is proposed by increasing

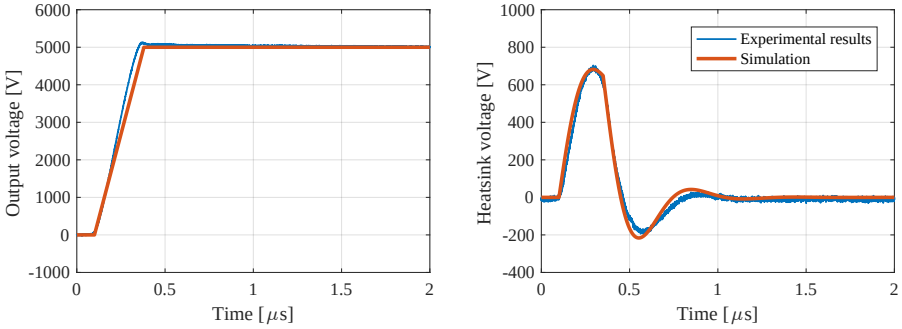

Fig. A.10: Experimentally measured half-bridge output voltage (left) and heat sink voltage (right) during 21.0 kV/μs switching of new module.

ceramic thickness, at the expense of slightly increased thermal resistance. The results also show that coupling between power module and heat sink can be directly observed through measurement of the heat sink voltage.

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Paper B

A SiC MOSFET Power Module With Integrated Gate Drive for 2.5 MHz Class E Resonant Converters

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The layout has been revised.

A SiC MOSFET Power Module With Integrated Gate Drive for 2.5 MHz Class E Resonant Converters

Asger Bjørn Jørgensen, Unnikrishnan Raveendran Nair, Stig Munk-Nielsen and Christian Uhrenfeldt

Abstract

Industrial processes are still relying on high frequency converters based on vacuum tubes. Emerging silicon carbide semiconductor devices have potential to replace vacuum tubes and bring benefits for converters in the high frequency range. At high switching frequencies hard-switched gate drivers can enable high power density design, but suffer from high temperatures and require low inductive design. This paper addresses the two issues through integrated packaging. Integrating the hard-switched gate driver in the power module ensures a low inductive and high thermal conductive package design. The required gate-source loop inductance is calculated and obtained in the design through use of the simulation software ANSYS Q3D Extractor. Two silicon carbide MOSFET power module prototypes are manufactured on a AlN substrate and FR4 PCB, to compare the thermal performance of the gate driver in the two cases. The electrical performance of the final power module is verified at 2.5 MHz in a Class E resonant converter.

B.1 Introduction

High frequency converters used for industrial processes, such as induction and dielectric heating, are still relying on vacuum tubes. Conventional silicon (Si) based power devices cannot operate at the high switching frequencies, high voltages and high powers required for such applications [1]. New wide band gap semiconductor devices, such as silicon carbide (SiC) MOSFETs, provide higher breakdown voltage, higher thermal conductivity and reduced on state resistance when compared with Si. A SiC MOSFET has smaller chip area when compared with a Si chip of similar voltage and current ratings. As a consequence, SiC devices have lower gate charge requirements, which enable higher operating frequencies [2]. Replacing vacuum tubes with new solid state devices, results in both smaller, cheaper and more efficient high frequency converters [3]. However, limited packages are available with SiC devices which utilize these benefits for the high frequency industry applications. Thus, the topic of this paper is on the development of a custom packaged SiC MOSFET power module and uses a 2.5 MHz Class E resonant converter as a test platform.

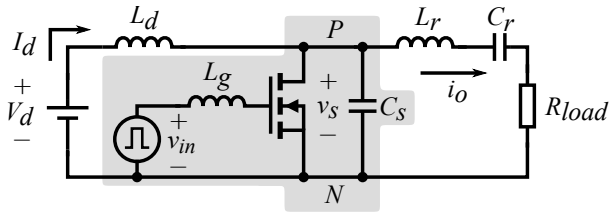

Fig. B.1: Class E resonant converter schematic, with marked components for integration in package.

For switching frequencies in the MHz-range the gate losses of MOSFETs become significant, and resonant gate drivers are often preferred. Compared with conventional hard-switched gate driver integrated circuits (ICs), resonant gate drivers recover some of the gate energy, thereby lowering losses in the gate circuitry. Resonant gate drivers have lower requirements to gate-source loop inductance, as it is included in the resonant loop design [4]. However, resonant gate drivers are more complex to design. More components, i.e. capacitors and inductors, share the losses which makes it easier to cope with the high gate losses [5]. But this comes at the expense of decreased power density [6]. Maintaining the high power density and simplicity of hard-switched gate driver ICs at high frequencies, requires low inductive design and high thermal conductance [7]. Packaging methods such as printed circuit board (PCB) embedded dies [8], [9] or PCBs molded on top of a direct bonded copper (DBC) substrate offer very low inductive design [10]. However, the hard-switched gate driver ICs are still mounted on the low thermally conductive PCB material. A solution is to mount the hard-switched gate driver IC directly on the DBC to dissipate the higher gate losses, but requires bond wires to interconnect the gate driver IC and the die which increase inductance [11], [12]. However, this may be acceptable if the parasitics of the gate-loop are designed properly.

In this paper, a SiC MOSFET power module with integrated hard-switched gate driver IC on DBC is designed for a Class E resonant converter operating at 2.5 MHz. The hard switched gate driver IC is included in the package to more effectively dissipate its losses (see **Figure B.1**). In literature, analysis of existing packaging for fast switching applications, shows the importance in maintaining low inductive design combined with an auxiliary source connection for the gate driver circuit [3], [13]. Additionally, when the switch in the Class E resonant converter turns on/off the current shifts from being conducted through the parallel capacitance, C_s, to the switch, and vice versa. Thus the parallel capacitance, C_s, is also included in the package to ensure low inductance between the two. The gate-source inductance is analysed to ensure fast switching without gate voltage overshoot and ringing. A three dimensional (3D) model of the power module is created and circuit parasitics are extracted using the simulation software ANSYS Q3D Extractor. Two power modules are manufactured to

experimentally evaluate the thermal performance of mounting the gate driver IC on DBC and PCB. The power module design is verified by operation in a Class E resonant converter at 2.5 MHz.

B.2 Design of integrated module

The gate-source inductance must be designed low enough to ensure good transient response [14]. Applying Kirchoffs voltage law on a generic gate-source loop (see **Figure B.2**), including the gate loop inductance L_g, gate resistance R_g and gate-source capacitance C_{gs}, results in

$$v_{in}(t) = L_g \frac{\mathrm{d}i(t)}{\mathrm{d}t} + i(t)R_g + v_{gs}(t) \tag{B.1}$$

By inserting that $i(t) = C_{gs}\frac{\mathrm{d}v_{gs}(t)}{\mathrm{d}t}$, the Laplace transform of (B.1) is written as

$$\frac{V_{gs}(s)}{V_{in}(s)} = \frac{\frac{1}{L_g C_{gs}}}{s^2 + \frac{R_g}{L_g}s + \frac{1}{L_g C_{gs}}} \tag{B.2}$$

This transfer function includes the dynamics from the hard-switched gate driver IC to the gate-source voltage on the SiC MOSFET. To analyze the dynamics of this equation, it is compared to the standard form of a second order system [15], given by

$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{B.3}$$

where ζ is the damping ratio and ω_n the natural frequency. Comparing (B.2) with the standard form in (B.3) an expressing for the inductance in the loop is found as

$$L_g = \frac{C_{gs}R_g^2}{4\zeta^2} \tag{B.4}$$

Here no external gate resistance is used to achieve fast switching speed. A critically damped response $\zeta = 1$ is chosen as a case, and by inserting values of

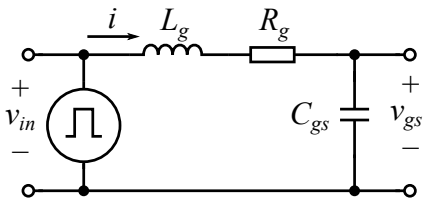

Fig. B.2: Schematic of generic gate-source loop.

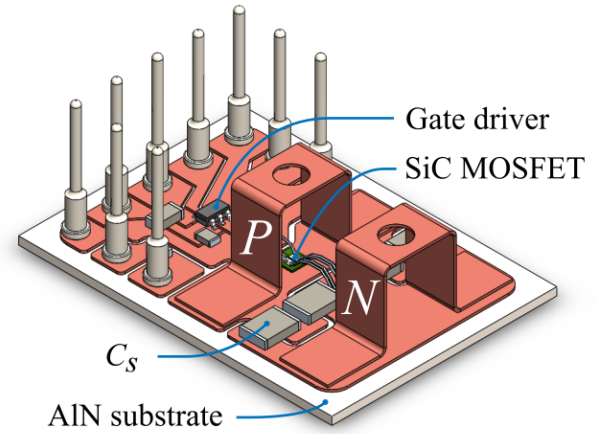

Fig. B.3: 3D model of designed SiC MOSFET power module.

the CPM2-1200-0160B die [16] to (B.4) the inductance is

$$L_g = \frac{521\,\text{pF} \cdot (6.5\,\Omega)^2}{4 \cdot 1^2} = 5.5\,\text{nH} \tag{B.5}$$

A gate loop inductance above the value in (B.5) causes an underdamped gate-source voltage, which results in some overshoot. Any value below results in an overdamped response, meaning no overshoot of gate-source voltage is present.

A SiC MOSFET power module with an integrated gate driver directly on the DBC was designed (see **Figure B.3**). The UCC27531 gate driver from Texas Instruments is used [17], and placed close to the SiC MOSFET. Decoupling capacitors for the +20 V and -5 V supply voltages are also included inside the module. Plate power terminals placed symmetrically around the die ensure low inductance. The capacitance in parallel with the switch is $C_s = 880\,\text{pF}$. The capacitors making up C_s are arranged symmetrically in respect to the drain-source path, to improve the current sharing between the capacitors.

The designed 3D model of the power module is imported into ANSYS Q3D Extractor, to extract the parasitic inductance of three main loops. The three loops are the drain-source, gate-source and die to external capacitors, C_s (see **Figure B.4**).

The inductances are extracted for a frequency of 2.5 MHz, similar to the fundamental component of operation in the Class E resonant converter. To extract the gate-source loop inductance, gate and source pads of the SiC MOSFET model are shorted. In ANSYS Q3D Extractor the loop is simulated as 4.6 nH, which is slightly below the target value calculated in (B.5), required to obtain a critically damped gate-source voltage. To calculate the drain-source loop inductance, drain and source pads of the SiC MOSFET are shorted.

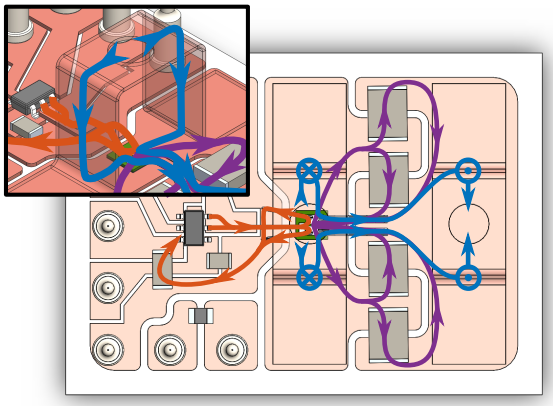

Fig. B.4: Extracted loop inductance of gate-source (red), drain-source (blue) and die to external capacitance (purple). Here $\otimes$ indicates direction inward and $\odot$ outward.

Capacitors are left as open-circuits. The loop is defined from the top surface of power terminal pin P to N (see **Figure B.3**). The drain-source power loop inductance is 6.3 nH. For the inductance between die and external capacitors, initially both drain-source of the MOSFET and terminals of capacitors are modelled as shorts. This results in a loop inductance of 2.1 nH. Current distribution reveals that current crowds at the two inner capacitors closest to the die. Thus, 2.1 nH is considered the minimum inductance for the loop. Due to inductances there might be an instantaneous imbalance in voltage distribution between capacitors. To have equal voltage, they should have equal charge rate, which implies equal current sharing. The maximum inductance path involves the loop of only the two outer capacitors. In order to assess the impact of this loop inductance, a case is simulated where the two inner capacitors are modelled as open-circuits. For this case the loop inductance is simulated as 3.6 nH. The effective loop inductance at 2.5 MHz is within the range 2.1 to 3.6 nH, but is dependent on the inductance between capacitors, their equivalent series resistance and equivalent series inductance. The issue of imbalance is not treated in more detail in this paper.

To manufacture the power modules, the copper layout is etched. A solder stencil with thickness of 125 μm is used to ensure a uniformly distributed solder layer. The SiC MOSFET die, gate driver IC, capacitors and pins are all soldered in a vacuum vapor phase oven. The SiC MOSFET die is wirebonded using 250 μm thick aluminium wire. A single wire is used for the gate pad. A total of four source bond wires are used for the power loop, of which two are chain-bonded and also work as auxiliary source connections for the gate drive circuit (see **Figure B.5**).

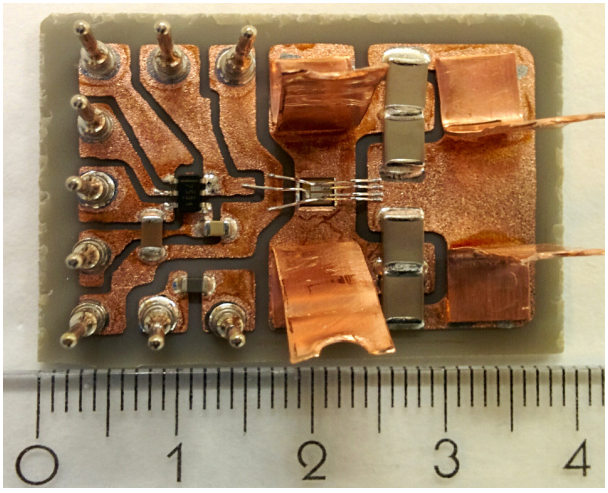

Fig. B.5: Manufactured module on 1 mm AlN DBC.

The thermal benefit of mounting the gate driver on the DBC instead of the conventional placement on a PCB is investigated experimentally. Thus, two power modules were manufactured with the same layout. One was designed on a 1 mm thick AlN DBC substrate with 0.3 mm copper, while the other on a conventional 2-layer PCB of 1.5 mm thick FR4 material and 35 μm copper.

B.3 Experimental tests

The gate driver circuit is tested before the power module is encapsulated in protective gel. This is done to experimentally measure the temperature of the gate driver IC when driving the SiC MOSFET at 2.5 MHz. Temperatures are logged using a FLIR E40 infrared camera. Initially, a calibration test is done to ensure the correct emissivity coefficient is used on the FLIR E40. The calibration test is done in the temperature range from 30 to 110 °C, by placing the gate driver IC on a hotplate. The temperature readings are compared with temperature measurements of the thermocouple on a Fluke 179 and optical temperature sensors OTG-M280 from Opsens. The calibration concludes that an emissivity coefficient of 0.95 results in complying temperature readings in the range tested.

After calibration, the gate driver IC is tested by driving the SiC MOSFET gate at a frequency of 2.5 MHz, between voltage levels -5 V and 20 V. During this test no bias is applied to the drain-source of the SiC MOSFET. The FLIR E40 is configured to automatically detect the point of highest temperature within a region (see **Figure B.6**), and also measures the temperature of the heat sink. The heat sink is coated with black painting to have similar emissivity

coefficient as the gate driver IC. The test is done with no forced convection, thus temperature dissipation from the gate driver IC is mainly through conduction to the heatsink and natural convection from its case surface.

The case top temperature is logged at a frequency of 30 Hz (see **Figure B.7**). At the end of test the maximum case temperatures logged are 69 °C and 120 °C for the gate driver mounted on a DBC and PCB, respectively. This clearly shows a benefit from placing the gate driver IC directly on the DBC in terms of thermal performance.

B.3.1 Estimation of gate driver junction temperature

The UCC27531 gate driver has a maximum allowable junction temperature, $T_{J,max}$, of 150 °C [17]. Only measurements of the top case temperature, T_C, and ambient temperature, T_A are available, thus the actual operating margin is unknown. In the following section an attempt to estimate the junction temperature, T_J, is made. From the datasheet of the UCC27531 gate driver IC [17] its thermal resistances are available as case-to-ambient $R_{CA} = 163.6\frac{\mathrm{K}}{\mathrm{W}}$, junction-to-case $R_{JC} = 14.7\frac{\mathrm{K}}{\mathrm{W}}$[1] and junction-to-board $R_{JB} = 28.3\frac{\mathrm{K}}{\mathrm{W}}$ (see **Figure B.8**).

The thermal resistances are complying with the specifications found in the JESD51 standard, and are given for conditions of only natural convection and when steady state is reached. This is similar conditions as the temperature

[1]Note that this is a mistake. The thermal resistance value used for R_{JC} is instead a thermal characteristic parameter ψ_{JC}. Despite this error, this paper has been kept in its accepted manuscript form. The mistake is corrected in Chapter 3.2.3 of the Extended summary. The reason for keeping the mistake in the appended paper is to maintain consistency between the appended papers and the published versions. IEEE Xplore does not allow changes to the already published conference paper files, as they only deal with the files provided from the conference organizers. Only changes to metadata or abstract are possible, as seen in the support center resources: https://supportcenter.ieee.org/app/answers/detail/a_id/1012/kw/error in pdf

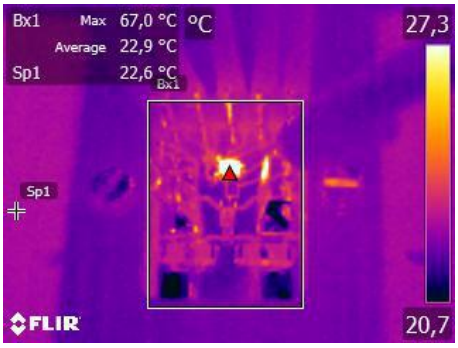

Fig. B.6: Image from FLIR E40 during test.

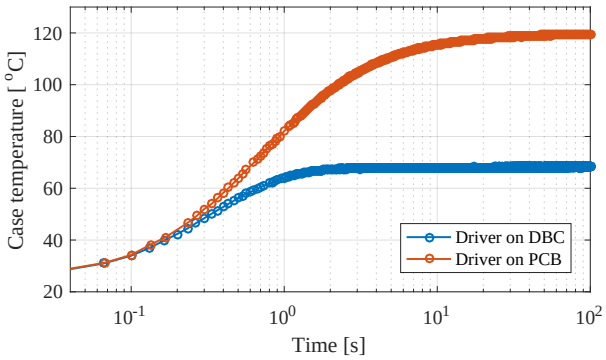

Fig. B.7: Measured top case temperature of gate driver.

measurements presented in this paper, and thus the stated thermal resistances are deemed accurate for estimating the junction temperature.

From the thermal network of the gate driver, it is found that the power dissipation through the top case surface is

$$P_C = \frac{T_C - T_A}{R_{CA}} \tag{B.6}$$

From this information the junction temperature is estimated from

$$T_J = T_C + P_C \cdot R_{JC} \tag{B.7}$$

By using (B.6) and (B.7) on the temperatures obtained in the previous test, the maximum junction temperatures calculated are 72 °C and 129 °C using the DBC and PCB, respectively.

During the test, power is supplied to the gate driver circuit through a GW Instek GPS-4303 power supply. The combined power consumption in the gate circuit is measured as an average value of 1.83 W. It is useful to estimate how

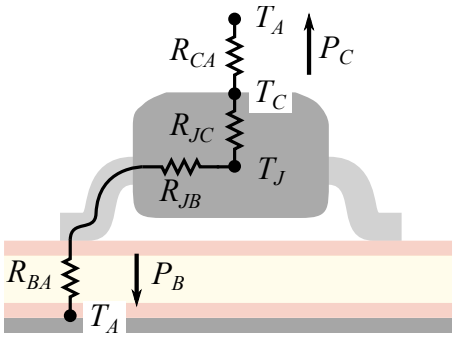

Fig. B.8: Thermal network of the gate driver IC.

much of this power is dissipated in the gate driver IC. Power is dissipated in both the gate driver IC and the gate resistance of the SiC MOSFET, but the distribution between the two is unknown. One approach is to estimate the gate power loss of the CPM2-1200-0160B die by using its available SPICE model [16], and setting up a LTSpice simulation using the parasitics extracted in Section B.2. By doing this, the loss in the SiC MOSFET gate is found to be 0.78 W at 2.5 MHz. Thus the remaining power of 1.05 W is dissipated in the gate driver IC. With this information it is possible to estimate a thermal resistance from junction to ambient, R_{JA}, as

$$R_{JA} = \frac{T_J - T_A}{P_{IC}} \tag{B.8}$$

By employing (B.8) the thermal resistance R_{JA} is found as 46 $\frac{\mathrm{K}}{\mathrm{W}}$ and 98 $\frac{\mathrm{K}}{\mathrm{W}}$ for the gate driver placed on DBC and PCB, respectively. For the conditions tested, the thermal resistance junction-to-ambient of a gate driver IC placed on a PCB is more than two times higher when compared to placement on a 1 mm AlN DBC substrate.

B.3.2 Class E electrical measurement

Before testing the power module in the Class E resonant application, it is encapsulated to withstand the required drain-source voltage bias. This is done by a custom made housing which is mounted and the module is poured with silicone gel, through a hole in the housing (see **Figure B.9**). The power module is placed in a vacuum chamber during curing of the gel, to avoid trapped air bubbles that could cause unwanted corona or partial discharges, due to lower electric field breakdown strength of air compared with silicone gel. The Class E resonant converter setup used for test is based on the findings in [18]. It has an input inductance of $L_d = 25\,\mu\mathrm{H}$, the resonant tank consists of $C_r = 2.08\,\mathrm{nF}$, $L_r = 3.84\,\mu\mathrm{H}$ and the output resistance is $R_{load} = 16.7\,\Omega$. The inductors are wound on powdered iron cores, and the capacitance is achieved by parallel connecting surface mounted NP0 ceramic capacitors. The experiments are evaluated at an input voltage of V_d =150 V. The circuit diagram used for simulation includes the parasitic inductances calculated for each loop (see **Figure B.10**). The SPICE model of the CPM2-1200-0160B SiC MOSFET [16] is imported and the circuit is simulated using LTSpice. The gate-source voltage, v_{gs}, switch voltage, v_s, and output current, i_o, waveforms are measured experimentally and compared with the simulation results (see **Figure B.11**).

The average voltage and input current are measured, resulting in an input power of 461 W. The output power is 406 W, calculated from the root mean square value of the measured output current, i_o, and the output load, R_{load}. The efficiency of the converter is 88 %. The peak switch voltage is 503 V and a sinusoidal output current is observed. There is a very good agreement

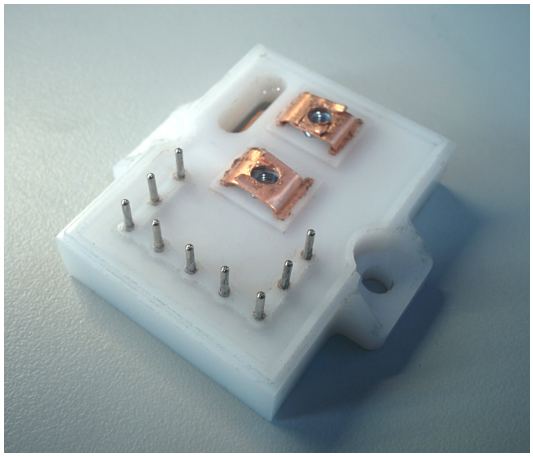

Fig. B.9: Picture of final module after attaching the housing and potting of protective gel.

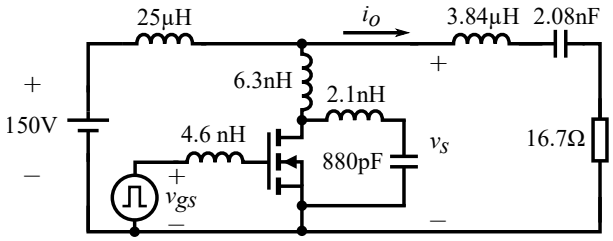

Fig. B.10: Circuit diagram used for simulation.

between the simulation and the experimental results. Due to the low inductive design, neither drain-source voltage, v_s, or the output current, i_o, is disturbed during switching events. The gate-source voltage waveform is undisturbed by the switching, and its response is nearly critically damped. This is the result of achieving proper gate-source loop inductance and by using an auxiliary source connection. This verifies the functionality and operation of the SiC MOSFET power module.

As demonstrated, the gate driver tests show a benefit in terms of thermal performance by integrating the gate driver IC on the DBC of the power module. However, the test was performed with no drain-source bias and no power dissipation from the SiC MOSFET except for its gate losses. For future work, the thermal performance of the combined system will be investigated to see how the gate driver IC is affected by the losses dissipated from the SiC MOSFET during operation. Temperature measurements using the thermistor inside the power module can be used as a metric. Alternatively, by modifying the housing an optical temperature sensor could be used to measure surface temperatures of components inside the power module [19]. Integrating gate driver IC and

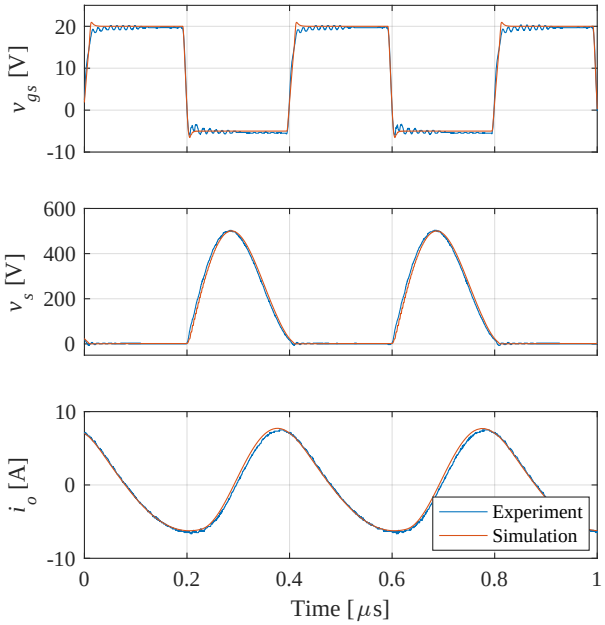

Fig. B.11: Experimental and simulated Class E waveforms, imported to MATLAB for plotting.

ceramic capacitors on DBC changes the thermal stress when compared to conventional placing outside the power module, which could affect the overall reliability. The temperature measurements could be used in a reliability study of the designed power module.

The prototype SiC MOSFET power module shows good electrical performance, which proves the design methodology. Thus in the future the power module concept will be extended to higher voltage and power levels to meet the requirements of the industrial applications. SiC MOSFET dies for 10 and 15 kV are now available [20]–[22], but are yet to be used in the MHz-frequency range which is required for some industrial processes.

B.4 Conclusion

A SiC MOSFET power module with integrated hard-switched gate driver was designed and manufactured. The CPM2-1200-0160B die requires a gate-source inductance of 5.5 nH for a critically damped gate-source voltage when exposed to a step input from the gate driver. The inductive design was attained through the ANSYS Q3D Extractor software. The achieved drain-source loop inductance is 6.3 nH. The inductance loop of MOSFET die and parallel capacitance is

calculated to be in the range 2.1 to 3.6 nH. Substantial lower thermal resistance is achieved by including the gate driver IC on the DBC, when compared to conventional mounting on PCB. The junction-to-ambient thermal resistance was estimated as 46 $\frac{\mathrm{K}}{\mathrm{W}}$ by placing the gate driver IC on the power module DBC, compared with 98 $\frac{\mathrm{K}}{\mathrm{W}}$ when placed on a PCB. This allows hard-switched gate drivers to operate at higher frequency. The performance of the integrated power module was tested through operation in a 2.5 MHz Class-E resonant converter. The gate-source voltage is nearly critically damped and not disturbed by switching, due to the auxiliary source connection. Due to low inductive design switch voltages and output current is unaffected by switching transients. The results show a very good coherence between experiment and simulation. This proves the applicability of the design methodology and software tools used. Due to the successful results, the concept will be extended in the future for new power modules using 10 and 15 kV SiC MOSFETs.

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Paper C

High Frequency Resonant Operation of an Integrated Medium Voltage SiC MOSFET Power Module

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High Frequency Resonant Operation of an Integrated Medium Voltage SiC MOSFET Power Module

Asger Bjørn Jørgensen, Thore Stig Aunsborg, Szymon Bęczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen

Abstract

Industrial processes which use induction and dielectric heating are still relying on resonant converters based on vacuum tubes. New emerging medium voltage silicon carbide semiconductor power devices have a potential to replace vacuum tubes and allow for more efficient and compact converters in the high frequency range. High voltage packages have been proposed in the literature that are suitable for the 10 kV silicon carbide MOSFET*s, and its fast voltage switching capabilities in hard-switched applications have been demonstrated. However, no packaging is presented which allows the high frequency operation of a 10 kV silicon carbide* MOSFET *die. This paper proposes the design of a power module for MHz resonant operation of a 10 kV silicon carbide* MOSFET*. At high switching frequencies the gate losses become substantial, thus the gate driver is included inside the power module package to ensure a low inductive and high thermally conductive design as seen from the gate driver. The inductance of the proposed power module layout structure is evaluated using ANSYS Q3D Extractor. The thermal performance of the integrated gate driver circuitry is experimentally verified. Finally, the resonant operation of a medium voltage silicon carbide* MOSFET *power module is demonstrated experimentally at 1 MHz.*

C.1 Introduction

Resonant converters operating at high voltages and frequencies of hundreds of kHz to tens of MHz, are used in various industrial processes employing induction and dielectric heating. Applications include melting/annealing of metals [1], drying of wood/glue/textiles [2]–[4] and for food processing [5]. The industries require converters operating at hundreds of kHz to tens of MHz at voltages of typically 2-3 kV and are currently using vacuum tubes in their designs. The conventional silicon (Si) power devices are not capable of operating at the high switching frequencies and high voltages that are required for these applications. However, converters based on vacuum tubes suffer from low efficiencies and are bulky in size. In comparison, typical resonant converters realised with solid state devices are smaller, cheaper and reach efficiencies $> 90\%$ [6], [7].

Emerging wide band gap semiconductor devices, such as silicon carbide (SiC) MOSFETs, have increased voltage breakdown strength, higher thermal conductivity and reduced on state resistance when compared with similar Si devices [8]–[10]. As a result the chip area of a SiC MOSFET is smaller when compared with a Si MOSFET device of similar voltage and current ratings. Therefore, SiC devices have reduced gate charge requirements which potentially allows them to be operated at higher frequencies [11], [12]. Resonant converters using SiC devices have already been employed, proving its high efficiency and results in very clean waveforms during zero voltage switching (ZVS) at frequencies of several MHz [13]–[16]. All these converters have been built using SiC MOSFETs with voltage ratings of 1200 V or lower, which is not high enough to replace the vacuum tubes in mentioned applications. Recently, 10 and 15 kV SiC MOSFETs from Wolfspeed have been released [17], [18]. These devices are only available in bare die form, and recent research has been focused on the development of high voltage packaging of such devices. Several research teams have investigated and demonstrated the fast switching capabilities of the 10 kV SiC MOSFETs mainly in hard-switched double-pulse tests [19]–[23], short-circuit characteristics [24]–[26], DC-DC converters [27]–[30] and inverter demonstrators with frequencies up to 40 kHz [31]–[35]. There has not yet been any documented attempts at operating 10-15 kV SiC devices in the MHz-range.

A challenge of operating a high voltage device at high frequency is identified when studying the on resistance of a MOSFET, given by

$$R_{\text{on}} = \frac{4 \cdot V_{\text{br}}^2}{\epsilon \cdot \mu \cdot E_{\text{C}}^3 \cdot A} \tag{C.1}$$

where V_{br} is the breakdown voltage, ϵ is the dielectric constant of the semiconductor, μ is the electron mobility and E_{C} is the critical electric field for breakdown of the semiconductor material and A is the area. Part of the denominator $(\epsilon \cdot \mu \cdot E_{\text{C}}^3)$ is known as the Baliga figure of merit (BFOM) of a semiconductor material [36]. From (C.1) it is seen that increasing the voltage breakdown of a device from its typical ~1 kV to 10 kV, would result in the resistance to increase by 100 times. For Si this would result in a too high on resistance or impractical die area. However, by using the advantageous properties of SiC to yield a higher BFOM, a 10 kV 350 mΩ SiC MOSFET die has been designed by Wolfspeed with an area of 8.1 x 8.1 mm [37]. For high frequency operation, the on resistance should not be reduced by carelessly increasing the die area. Increasing the die area results in a larger input capacitance of the die, which increases the required power to be delivered from the gate driver circuit to charge and discharge the input capacitance of the SiC MOSFET die. The compromise between on resistance and input capacitance is found in the Baliga high frequency figure of merit (BHFFOM) [38], given by

$$\text{BHFFOM} = \frac{1}{R_{\text{on}} \cdot C_{\text{in}}} \tag{C.2}$$

Thus, a careful design of the gate drive circuit is required to effectively deliver the necessary gate power and proper high voltage packaging must be developed to achieve high frequency operation of 10 kV SiC MOSFETs

This paper is the first documented attempt of MHz operation of a 10 kV SiC MOSFET die, as a step in the process of turning vacuum tubes obsolete in some high voltage, high frequency applications. To address the gate driving challenge, this paper contributes with the design of an integrated package of high voltage semiconductor devices and proves the capability of high frequency resonant operation of a 10 kV SiC MOSFET. The power module structure, design and evaluation of its parasitics is presented in Section C.2. In Section C.3 the gate driver circuit itself is tested to ensure that the circuit can deliver the necessary power without overheating at high switching frequencies. The power module is characterized and its performance at high frequencies is experimentally tested in Section C.4. The results are presented and some of the limitations of the power module are discussed. The paper is concluded in Section C.5.

C.2 Power module design

A power module for a ZVS resonant circuit is designed, to test the feasibility of switching a 10 kV SiC MOSFET in the high frequency range. A schematic of components included in the power module is shown in Fig. C.1. The parallel capacitance, C_p, ensures ZVS and this configuration is well-known from single switch resonant topologies such as the Class E, Class Φ_2 and ZVS resonant-switch converters. The parallel capacitance, C_p, should be placed as close to the SiC MOSFET die as possible. This is done to reduce the noise generated when current shifts from being conducted through the SiC MOSFET to parallel capacitance, and vice versa. A hard switched gate driver integrated circuit (IC) is chosen, due to its simplicity and flexibility. To ensure an undisturbed gate-source voltage of the SiC MOSFET a kelvin connection is used. The hard switched gate driver IC should be placed close to the SiC MOSFET to achieve fast switching speed without ringings, as described further in Section C.2.1. Compared with a resonant gate driver, a hard switched gate driver IC has higher power density and allows for easier adjustment of the frequency and duty cycle without changing any components of the circuit [39], [40]. Its disadvantage is higher gate losses as the energy delivered to the gate is not recovered [41]. Operating at high frequencies requires a power module structure which allows both the SiC MOSFET die and the gate driver to dissipate the generated losses. The direct bonded copper (DBC) integrated power module structure, as shown in Fig. C.2, enables both low inductive integrated design and high thermal conductivity and it has demonstrated great performance for lower voltage SiC MOSFETs [15], [16], [42]. A baseplate is used for mechanical stability and allows for mounting the power module onto a heat sink. The DBC is soldered to the

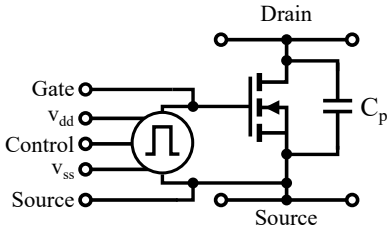

Fig. C.1: Proposed module diagram.

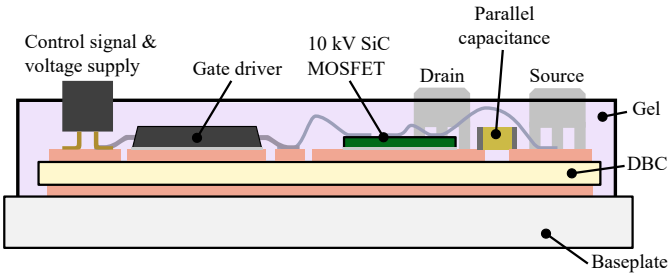

Fig. C.2: Medium voltage SiC MOSFET power module structure.

baseplate, and ensures high voltage insulation capability while still maintaining low thermal resistance. The top side of the DBC is etched and populated with the components. All of the components are enclosed in an insulating silicone gel to allow high voltage operation.

Based on this power module structure, a 10 kV SiC MOSFET power module design is proposed, as shown in Fig. C.3. The power module has both the 10 kV SiC MOSFET die, gate driver and the parallel capacitance soldered directly to the DBC. The ceramic capacitors making up the parallel capacitance, C_p, are of material class NP0 as they effectively maintain capacitance at increasing frequency and voltage bias. In contrast X7R, Y5V and X5R drop typically 10-20 % or more of their specified value, making it hard to maintain a desired capacitance regardless of frequency and voltage bias [43], [44]. The disadvantage of class NP0 is a low capacitance density, meaning that a high voltage capacitor with just a few hundred pF is not easily available in a small form factor. Surface mounted capacitors and a small form factor are requirements for integration of capacitors in the power module. Leaded capacitors introduce higher series inductance and could degrade the ZVS performance. For this paper four ceramic capacitors of 180 pF make up the parallel capacitance C_p, but are only rated for 3000 V. Surface mounted NP0 capacitors of higher voltage have not been available with the required capacitance value. This issue is to be solved for future power modules to further utilize the full 10 kV voltage rating of the SiC MOSFET dies. WACKER Silicone gel with a dielectric strength of 23 kV/mm [45]

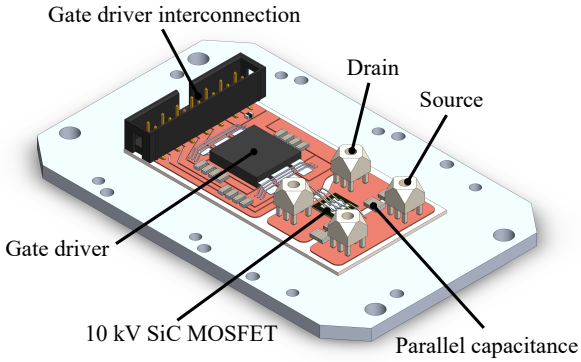

Fig. C.3: 10 kV SiC MOSFET power module design.

is used to ensure safe high voltage operation. The high voltage drain potential has a minimum clearance of 2 mm to all other planes of the power module. The DBC is 0.3 mm copper layer on either side of a 1 mm thick aluminium nitride. Aluminium nitride allows high voltage operation while still maintaining a low thermal resistance, as its thermal conductivity is 150-180 $\frac{\mathrm{W}}{\mathrm{m \cdot K}}$ in comparison to the 24 $\frac{\mathrm{W}}{\mathrm{m \cdot K}}$ of conventional aluminium oxide ceramics [46].

Power terminals from Redcube are directly soldered to DBC for interfacing of drain and source potentials. A pin header socket located on the other side of the power module is used to interface the gate supply voltages, gate driver IC control signal and to allow measurement of the gate-source voltage between gate driver and the 10 kV SiC MOSFET die. The gate driver is a IXRFD630 from IXYS, which is capable of delivering high power. The expected rise and fall time is 5-7 ns [47], and it is rated at a peak output current of 30 A. This is used to ensure fast turn-on and turn-off speed of the 10 kV SiC MOSFET die and allow its operation into the MHz range. The $V_{ds} - I_{ds}$ characteristics of the 10 kV SiC MOSFET die, shown in Fig. C.4, are obtained using a Keysight B1506A power device analyzer. It shows that the gate-source voltage should be maintained above 15 V to prevent saturation effects, which start to occur at currents of 7-8 A. From Fig. C.4 the drain-source on resistance is determined to be 350 mΩ in its linear region. Also using the Keysight B1506A the gate-source threshold voltage is determined to be 4.3 V.

C.2.1 Gate driver design considerations

The layout of the power module is considered to reduce the influence of the unavoidable parasitics. A kelvin connection is employed to reduce influence

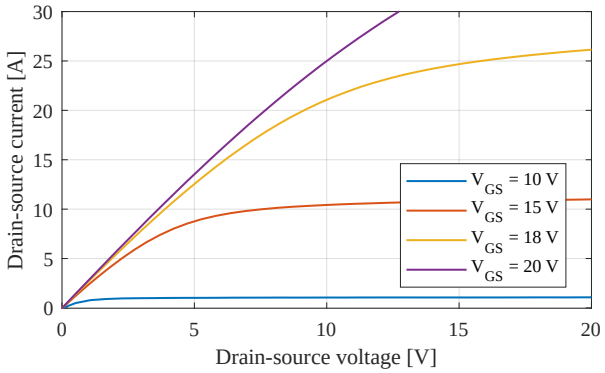

Fig. C.4: Measured V_{ds}-I_{ds} characteristic of the 10 kV SiC MOSFET at different gate-source voltages, V_{GS}.

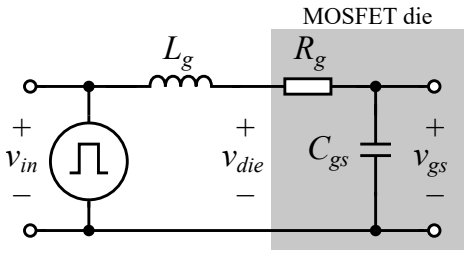

Fig. C.5: Schematic used for gate drive design.

from the power loop on the gate-source voltage. To turn the SiC MOSFET on/off as fast as possible no external gate resistance is inserted, which means that the gate-source loop has limited damping. A too high loop inductance results in an oscillating gate-source voltage which propagates as an undesirable high frequency component on the drain-source voltage [14]. The schematic of the gate driver used to determine its dynamics is shown in Fig. C.5. Modelling the gate driver IC output, v_{in}, as an ideal step input, the dynamic response of gate-source voltage of the SiC MOSFET die, v_{gs}, is determined by [42], [48]

$$L_{\mathrm{g}} = \frac{C_{\mathrm{gs}} R_{\mathrm{g}}^2}{4\zeta^2} \tag{C.3}$$

where L_{g} is the gate-source loop inductance, C_{gs} is the gate-source capacitance of the SiC MOSFET, R_{g} is the gate resistance of the SiC MOSFET and ζ is the damping of the circuit [42].

By selecting a critically damped case ($\zeta = 1$), and using the preliminary datasheet of the 10 kV SiC MOSFET die, the maximum allowable gate-source

loop inductance becomes

$$L_{\mathrm{g}} = \frac{5.8\mathrm{nF} \cdot (3.7\Omega)^2}{4 \cdot 1^2} = 20\mathrm{nH} \tag{C.4}$$

This value or anything below ensures that there will be no overshoot of the gate-source voltage of the SiC MOSFET. Designing a layout with the necessary inductance value is an iterative process where new designs are proposed which are then assessed using ANSYS Q3D Extractor as a design tool, as explained in Section C.2.2.

C.2.2 Evaluation of design in ANSYS Q3D Extractor

The software package ANSYS Q3D Extractor is used to calculate the parasitic inductance of the proposed power module in Fig. C.3. In ANSYS Q3D Extractor source and sink terminals (equivalently to an input and output) are defined on the 3D geometry, and by simulating the electromagnetic fields the inductance between these two terminals is calculated. The parasitics must be solved at a certain frequency. At very low frequencies ANSYS Q3D Extractor assumes there are no inductive effects and current is assumed to flow equally distributed across the conductor volume. At high frequencies the assumption is that inductive effects become pronounced, and due to skin effect the current density is increased at the surface. This paper is mainly concerned with the inductance during the fast switching instances which has components at various high frequencies [49]. Thus the inductance is solved as a surface problem.

The gate-source loop inductance when clamped to the negative voltage, shown in Fig. C.6(a), is calculated as 10 nH. The loop when clamped to positive rail is shown in Fig. C.6(b), and the extracted inductance is 12 nH. Both of these values are below the inductance calculated in (C.3), required for a critically damped response of the gate-source voltage on the SiC MOSFET. Thus, if Kelvin-source connections effectively mitigate the coupling between power and gate loops, limited oscillation is expected to the gate-source voltage. The drain-source power loop is defined from the drain to source terminals, shown in Fig. C.6(c), and the inductance is calculated as 5.5 nH. When the SiC MOSFET turns off the current shifts to the distributed parallel capacitance placed inside the module. Thus, it is very important that this inductance is kept at a minimum. The loop inductance of the path between the SiC MOSFET and the parallel capacitors, as shown in Fig. C.6(d), is calculated as 2.4 nH.

C.3 Performance of gate driver circuit

Before fully operating the power module, the gate driver IC and the gate structure of the 10 kV SiC MOSFET is tested. The purpose of the test is to ensure that the gate driver circuit is capable of delivering the necessary power

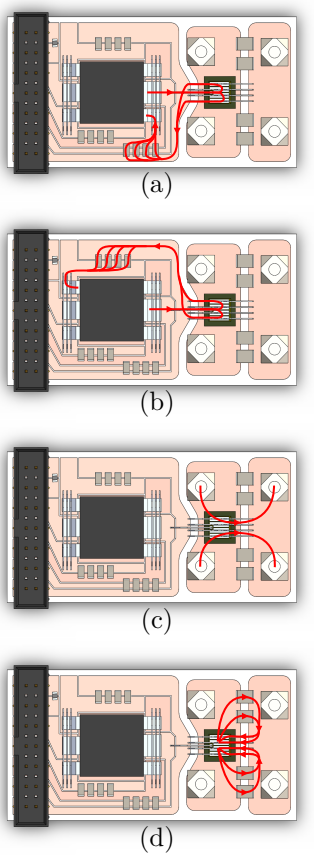

Fig. C.6: (a) gate-source loop when clamped to negative voltage (b) gate-source loop when clamped to positive voltage (c) drain-source power loop (d) current path between SiC MOSFET and parallel capacitance.

without overheating. A diagram of the different layers as seen from the gate driver is shown in Fig. C.7. The gate driver package contains its own DBC to ensure isolation, and bond wires connect the gate driver die to the external leads of the driver. When using this prepackaged gate driver the path from die junction to the heat sink includes a total of: two ceramic layers, four copper layers, three solder interfaces, a baseplate and thermal interface material between baseplate and heat sink. This highlights the necessity to experimentally verify that the gate driver IC is capable of dissipating its power losses when driving the SiC MOSFET at MHz frequencies. Furthermore, the test ensures that the 10 kV SiC MOSFET is capable of being driven at a high frequency. The resistance of the gate structure is relatively high, and it must be ensured that the physical structure of the device can handle the high frequency pulsing of

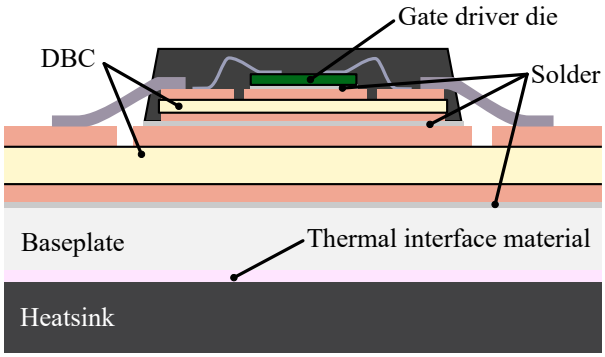

Fig. C.7: Diagram of gate driver thermal structure.

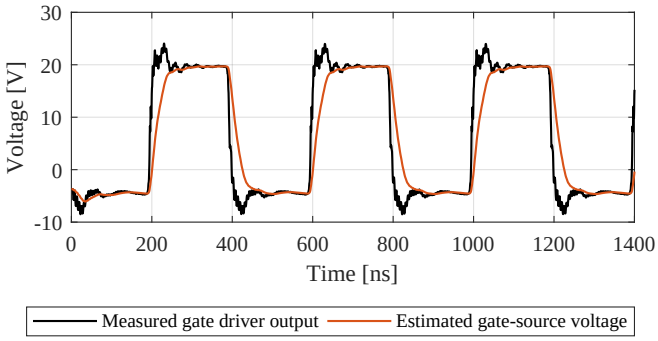

Fig. C.8: Measured gate driver output and estimated gate-source voltage waveform.

power into the gate structure. O. Kreutzer *et al.* [48] demonstrated fusing of the gate-structure of a low voltage SiC MOSFET from excessive current pulsing, in an attempt to increase the switching speed.

The power module is mounted on a heat sink and an input signal of 2.5 MHz is given to the gate driver IC in the power module. The gate driver is supplied with a v_{dd} of +20 V for high output and v_{ss} of -5 V for low output. For the experiment it is not possible to measure the gate-source voltage inside the die, but only the voltage outside denoted v_{die} in Fig. C.5. The measured output voltage from the gate driver is shown in Fig. C.8. There is a spike on the measured output of the gate driver. Using a SPICE simulation the measured v_{die} is used as a voltage source input to the gate-resistance and gate-source capacitance, to estimate the gate-source voltage, v_{gs}, as shown in Fig. C.8. This demonstrates the damped dynamic behavior as designed in Section C.2.1.

The test is performed before the housing is mounted and the silicone gel is applied, which allows measuring surface temperature of the gate driver inside the power module using an thermographic camera. Temperatures of the gate

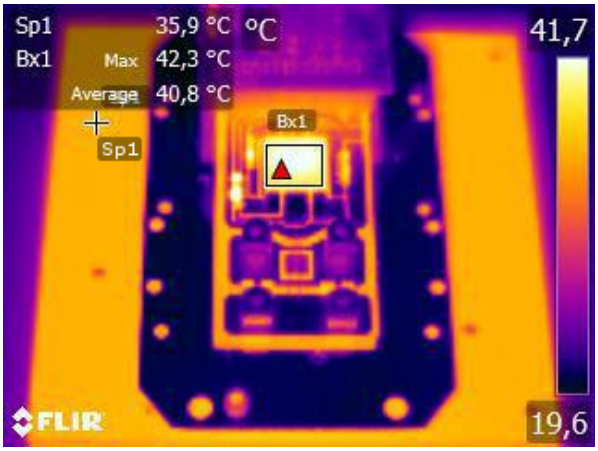

Fig. C.9: Temperatures are logged using a FLIR E40 thermal camera.

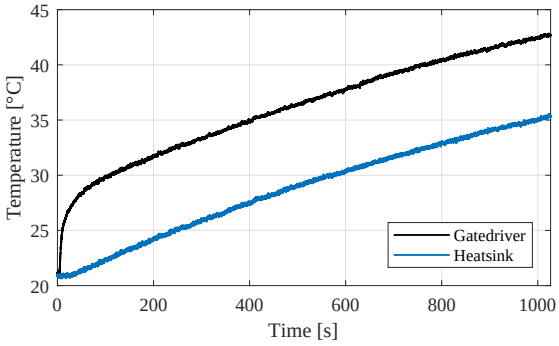

Fig. C.10: Temperatures measured on the gate driver (Bx1.max in Fig. C.9) and the heat sink (Sp1 in Fig. C.9) during experiment.

driver IC and a reference temperature on a heat sink are measured using a FLIR E40 thermographic camera. The thermal image of the FLIR E40 during a test is shown in Fig. C.9, and the surface temperatures are automatically logged at a frequency of 30 Hz during the experiment. Both the gate driver IC and the heat sink are covered in black paint, and an emissivity constant of 0.95 is used. No cooling fans are used to reduce the turbulence of the air around the power module. This is done to obtain conditions which are as close as to when the power module is encapsulated and limited power dissipation is possible through the top surface of the gate driver. Logged temperatures during 2.5 MHz operation of the gate driver are shown in Fig. C.10.

As seen the gate driver temperature quickly increases to a level above the heat sink temperature, which then starts to slowly increase. The absolute temperature difference then becomes constant for the rest of the test, while

the temperature of the heat sink increases. Thus we can evaluate the thermal resistance from the gate driver IC to the heat sink, by

$$R_{\mathrm{gd}}(t) = \frac{T_{\mathrm{gd}}(t) - T_{\mathrm{hs}}(t)}{P_{\mathrm{gd}}} \tag{C.5}$$

where R_{gd} is the thermal resistance from gate driver IC to the heat sink, T_{gd} is the temperature of the gate driver, T_{hs} is the temperature of the heat sink and P_{gd} is the power dissipated in the gate driver IC. The DC power delivered to the gate driver circuit is measured as 17 W. From the LTSpice model of Fig. C.5 the gate driver circuit, including gate resistance, input capacitance and loop inductances is developed. This predicts an energy consumption of 9.8 W in the SiC MOSFET gate resistance, meaning the remaining 7.2 W are assumed to be dissipated in the gate driver. This calculation does not account for the losses that might occur in the equivalent series resistance of the decoupling capacitors in the power module.

For the dataset shown in Fig. C.10, the temperature difference between gate driver, T_{gd} and heat sink T_{hs} reaches a steady state of 7.5 °C after 100 seconds. Taking the value of the temperature difference in steady state and using the power dissipation of 7.2 W in (C.5), results in a thermal resistance from gate driver IC to heat sink, R_{gd}, of 1.04 K/W. The test demonstrates the capability of the 10 kV SiC MOSFET die to be driven at a frequency of minimum 2.5 MHz and that the gate driver can deliver the required power without overheating.

C.4 Experimental results of resonant operation

Following the verification of the gate driver circuit, the final power module is assembled. The housing is milled from a block of transparent acrylic plastic. After mounting of the housing, the power module is encapsulated in protective gel. The final power module is shown in Fig. C.11.

A test setup is assembled to test the performance of the power module during resonant operation in high frequency range. An LC resonance oscillator as shown in Fig. C.12 is used for this purpose.

The current in the inductor, L, is charged during the MOSFET on time by

$$\Delta i_{\mathrm{L}} = \frac{D \cdot \tau_{\mathrm{s}} \cdot V_{\mathrm{d}}}{L} \tag{C.6}$$

where V_d is the DC-link voltage, L is the resonance inductance, D is the duty cycle and τ_s is the switching period. Because of the continuous resonant operation, the inductor current is centered around zero. Thus, geometrically from Fig. C.13, the current which occurs at $t = 0$ is denoted I_0 and is calculated from

$$I_0 = \frac{D \cdot \tau_{\mathrm{s}} \cdot V_{\mathrm{d}}}{2 \cdot L} \tag{C.7}$$

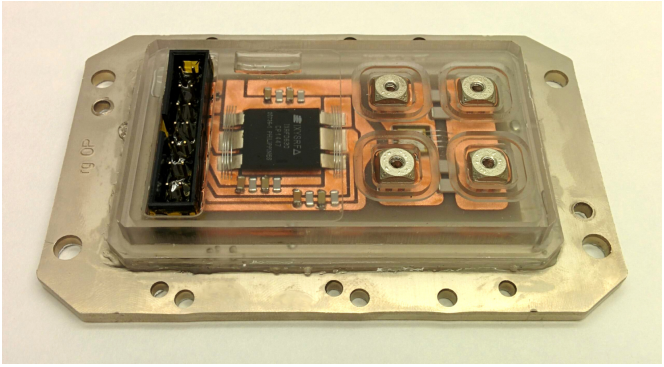

Fig. C.11: Photograph of final power module.

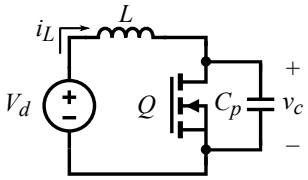

Fig. C.12: *LC* circuit used to demonstrate resonant operation.

At $t = 0$ the switch Q is turned off, and the energy charged in the inductor is released to the parallel drain-source capacitance C_p. The voltage across the capacitor, v_c following $t = 0$ is given by [50]

$$v_{\mathrm{c}} = V_{\mathrm{d}} - V_{\mathrm{d}} \cdot \cos(\omega t) + \sqrt{\frac{L}{C_{\mathrm{p}}}} \cdot I_0 \cdot \sin(\omega t) \tag{C.8}$$

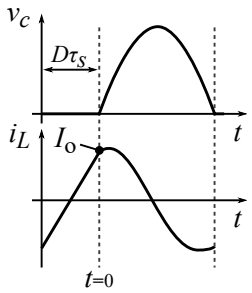

Fig. C.13: Waveforms of *LC* resonant circuit.

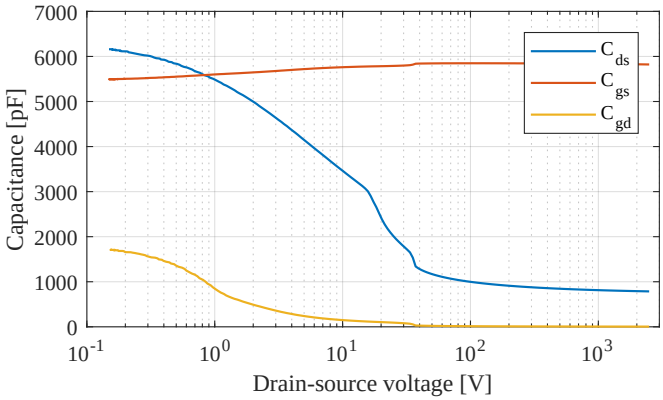

Fig. C.14: Measured drain-source, C_{ds}, gate-source, C_{gs} and gate-drain C_{gd} capacitances of the power module.

To determine the maximum capacitor voltage (C.8) is differentiated

$$\frac{\mathrm{d}v_{\mathrm{c}}}{\mathrm{d}t} = V_{\mathrm{d}} \cdot \omega \cdot \sin(\omega t) + \sqrt{\frac{L}{C_{\mathrm{p}}}} \cdot I_0 \cdot \omega \cdot \cos(\omega t) \tag{C.9}$$

By equating (C.9) to zero and solving for t, its extremes occur at $t = \frac{\pi(2n-1)}{2\omega}$ for $n \in Z$. As the LC circuit is reset at every switching instance, we are mainly concerned with the initial peak, thus $n = 1$. Maximum capacitor voltage is found by inserting $t = \frac{\pi}{2\omega}$ to (C.8) which equals

$$V_{\mathrm{c}} = V_{\mathrm{d}} + \sqrt{\frac{L}{C_{\mathrm{p}}}} \cdot I_0 \tag{C.10}$$

The experimental results shown in this paper are done at an input DC link voltage, V_{d}, of 800 V. The capacitance is $C_{\mathrm{p}} = 890$ pF, as shown in Fig. C.14, which was obtained using a Keysight B1506A power device analyzer.

With the inductance, L, of 25 μH the resonance frequency becomes 1 MHz. Using these values, from (C.7) the build-up current I_0 becomes 5.0 A. Inserting this value to (C.8) the peak drain-source voltage is calculated as 1638 V.

The experimental results are shown in Fig C.15. The drain-source voltage is measured using a high voltage Teledyne Lecroy PPE4kV passive probe, while the gate input voltage is measured using a Teledyne Lecroy ADP305 differential probe. The current is measured using a Teledyne Lecroy CP030 current probe. All probes are connected to a Teledyne Lecroy HDO4024A scope. A Magna XR2000-1.00/380NEG+LXi power supply is used to deliver the voltage, and is connected to a film capacitor bank of 1140 μF, ensuring a stable DC-link voltage up to a rating of 1500 V. To ensure the sinusoidal inductor current, the

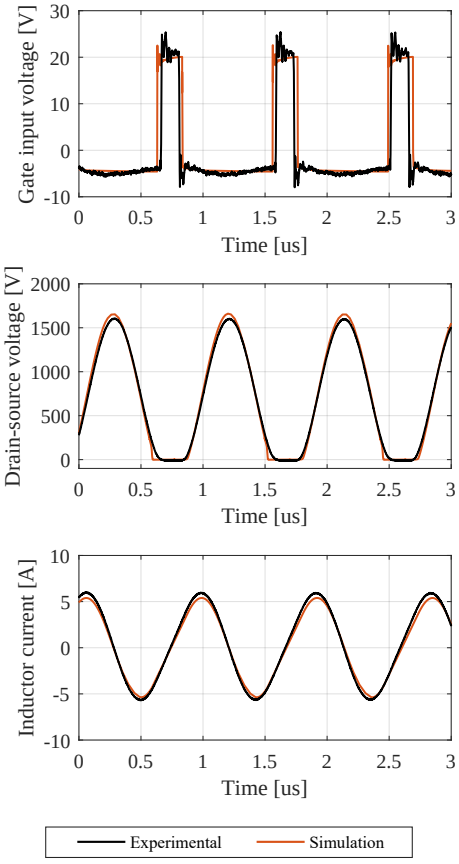

Fig. C.15: Experimental and simulated waveforms during resonance operation of module.

gate driver input signal is timed such that the duty cycle of the SiC MOSFET is $\frac{1}{\pi}$. However, the measured gate driver input signal is slightly below $\frac{1}{\pi}$ to account for non-equal delays during turn-on and turn-off.

The experimental results demonstrate the resonant operation of the medium voltage SiC MOSFET power module at 1 MHz. The measured peak drain-source voltage is 1597 V, which only deviates 2.4 % from the theoretically expected results. There are no higher frequency components of oscillation visible on the drain-source voltage. This indicates both the right damping of the gate-source loop and that the Kelvin connection mitigates coupling between the gate-source and power loop.

A SPICE simulation is made using the *LC* circuit model from Fig. C.12, and adding the parasitic inductances calculation in Section C.2.2. The SiC MOSFET device model is based on the static characteristics of $V_{\mathrm{ds}} - I_{\mathrm{ds}}$ in Fig. C.4 and power module capacitances from Fig. C.14. The SPICE simulation results

are also shown in Fig. C.15 and cohere with the experimental results. Some dynamics of the gate-source signal is not present in the simulation waveform as the gate-driver IC SPICE model is not available from the manufacturer. Nevertheless, the simulation and theoretical calculations verify that in terms of drain-source voltage and inductor current the designed power module produces close to ideal LC oscillator circuit behavior.

During the very first switching of the circuit, the full DC-link voltage is hard switched and results in a high $\mathrm{d}v/\mathrm{d}t$. The high $\mathrm{d}v/\mathrm{d}t$ of the drain copper plane of the DBC is capacitive coupled to the gate driver through the heat sink [51], [52]. The capacitive coupling between the two nodes causes flickering of the gate input signal preventing the circuit from entering its desired LC oscillation. For this reason successful resonance operation was not achieved above an input voltage level, V_d, of 800 V. To solve the root cause for future modules, the parasitic capacitance between the gate driver traces and the heat sink should be reduced. Recently, J. Shin *et al.* [53] proposed such a solution, by removing parts of the bottom-side copper of the DBC to reduce capacitive coupling, but only in places where effective heat transfer is not necessary. Additionally, a bare die gate driver could be used instead of the prepackaged version used for this paper, as this would result in a more compact layout and more flexibility in the routing. This would also reduce the thermal resistance of the gate driver, by removing some of the layers in its thermal path.

In summary, in terms of electromagnetic compatibility the chosen integrated power module structure is disadvantageous, as capacitive coupling to the heat sink links the high $\mathrm{d}v/\mathrm{d}t$ of the SiC MOSFET to the sensitive gate driver circuit. The advantages of the power module structure is its low inductive design and high voltage capability, which are important aspects used to demonstrate the 1 MHz resonant operation of a 10 kV SiC MOSFET.

C.5 Conclusion

The purpose of the paper is to prove the high frequency resonant operation of a 10 kV SiC MOSFET device. An integrated DBC power module structure is chosen, as it allows for low inductive design and allows both the semiconductor die and the gate driver to dissipate its heat effectively. A power module design is proposed, and its layout is evaluated using the simulation software package ANSYS Q3D Extractor. The gate loop inductances are found as 10 nH and 12 nH when clamped to +20 and -5 V voltages, respectively. The drain-source inductance of the module is 5.5 nH, while loop inductance between SiC MOSFET die and parallel capacitance, C_p is 2.4 nH. The gate driver circuit was tested without any drain-source bias, to ensure that both gate driver and SiC MOSFET are capable of operating at high frequencies. A thermographic camera measured temperatures of both gate driver IC and the heat sink, and a thermal resistance

of 1.04 $\frac{K}{W}$ from gate driver to heat sink is calculated. It was demonstrated that the gate driver was capable of driving the SiC MOSFET up to a frequency of minimum 2.5 MHz. A resonant *LC* circuit setup is used to verify the ZVS performance of the designed power module. By using L = 25 μH and a parallel capacitance, C_p = 890 pF, the case of a resonant frequency of 1 MHz is tested. The experimental waveforms show very clean switching at an input voltage of V_d = 800 V, at which a peak voltage of 1.6 kV is measured, and proves the capability of the 10 kV SiC MOSFET to operate at 1 MHz. At increasing DC link voltages the high $\mathrm{d}v/\mathrm{d}t$ causes flickering of the gate driver circuit, which limits tests at higher voltages. The proposed integrated medium voltage SiC MOSFET power module design is advantageous for its low inductive design, high voltage breakdown rating and its power dissipation capability of both SiC MOSFET and gate driver. Due to these properties the ZVS operation at 1 MHz was demonstrated of the 10 kV SiC MOSFET.

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Paper D

A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices

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Abstract

New packaging solutions and power module structures are required to fully utilize the benefits of emerging commercially available wide bandgap semiconductor devices. Conventional packaging solutions for power levels of a few kW are bulky, meaning important gate driver and measurement circuitry is not properly integrated. This paper presents a fast-switching, integrated power module based on gallium nitride enhancement-mode high-electron-mobility transistors, which is easier to manufacture compared with other hybrid structures. The structure of the proposed power module is presented, and the design of its gate driver circuit and board layout structure is discussed. The thermal characteristics of the designed power module are evaluated using COMSOL Multiphysics. ANSYS Q3D Extractor is used to extract the parasitics of the designed power module, and is included in simulation models of various complexity. The simulation model includes the SPICE model of the gallium nitride devices and parasitics of components are included by experimentally characterizing them up to 2 GHz. Finally, the designed power module is tested experimentally, and its switching characteristics cohere with the results of the simulation model. The experimental results show a maximum achieved switching transient of 64 V/ns and verifies the power loop inductance of 2.65 nH.

D.1 Introduction

Power electronics is an ever growing industry, used to handle and treat electrical energy in every aspect from production to consumption. Power electronics are used for all power levels, whether it be in wind turbines, solar panels, industry motor drives, pumps, kitchen appliances or artificial lighting. In many cases the electrical energy is handled by switch mode power supplies, in which the semiconductor die is the core unit. Typically at lower power levels <1 kW, the semiconductor device is directly integrated with other components to form a power supply as a single unit [1]. For higher power levels or systems of higher complexity, the semiconductor devices are often packaged as a power module, which is then just seen as a component of the total power electronic system. In either case, the performance of the semiconductor device is dependent on the interconnection it has with critical components of the circuit such as gate

driver integrated circuits (ICs), capacitors, sensors and other auxiliary circuitry. Furthermore, to ensure reliable and robust operation, it must be ensured that the device is properly cooled, enclosed and interconnected with other peripherals. New wide band gap (WBG) semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), offer potential size, efficiency and performance improvements of power modules used in switch mode power supplies. These materials offer higher breakdown voltage, faster switching speeds, lowered on-resistance and increased operating temperatures, when compared to silicon [2], [3]. The fast switching speed of WBG devices produces high $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ which may induce ringings and electromagnetic interference issues due to parasitic elements in the packaging [4]. Current power module packaging design for power levels in the kilowatt range is still bulky, which causes difficulty in integration and minimization of parasitic elements in both power and gate driver loop simultaneously [5], [6]. To harvest the benefits of WBG devices new designs and integration of parts must be studied and tested.

Silicon power modules with base plates is currently the most dominant design, used in approximately 70 to 80 % of all power modules [7]. A typical sectional view of the conventional power module structure is shown in Fig. D.1(a). At the bottom is the baseplate, which is mounted to a heat sink to ensure low thermal resistance. A direct bonded copper (DBC) is soldered to the baseplate. The DBC is a sandwich structure with copper on either side of ceramic substrate which is an electrically insulating material yet capable of transferring heat efficiently [8]. Encapsulation such as epoxy or silicone gel is used to ensure high electric breakdown strength and protect the semiconductor dies from humidity and contaminants. The entire assembly is enclosed in a plastic housing to mechanically protect the internal structures of the power module. Terminals are mounted on the copper planes, and used to connect the semiconductor with electrical circuits outside the power module. Typically this control circuitry is soldered on a printed circuit board (PCB) and connected outside of the power module. The benefits of this structure is its high voltage blocking capabilities and high power dissipation [9]. The conventional structure is challenged by the emergence of new WBG devices. Due to the terminals and copper planes a parasitic inductance of typically 10-30 nH [10]–[13] limits the utilization of the increased switching speeds of the WBG semiconductors.

A solution is to assemble every part of the switching device into a multilayer PCB, as shown in Fig. D.1(b). In this way the semiconductor die is directly embedded into the PCB, and has copper planes connecting to its peripheral units [14]. This eliminates the use of bond wires. The concept reduces the parasitic inductance in the power loop, reported at 2.8 nH [12]. But it is hard to achieve both good thermal and electrostatic performance simultaneously [15]. An issue is to dissipate the heat, due to the high thermal resistance of the FR4 material. For high power dissipation levels larger copper planes and vias reduce thermal impedance by more effectively conducting the heat to the

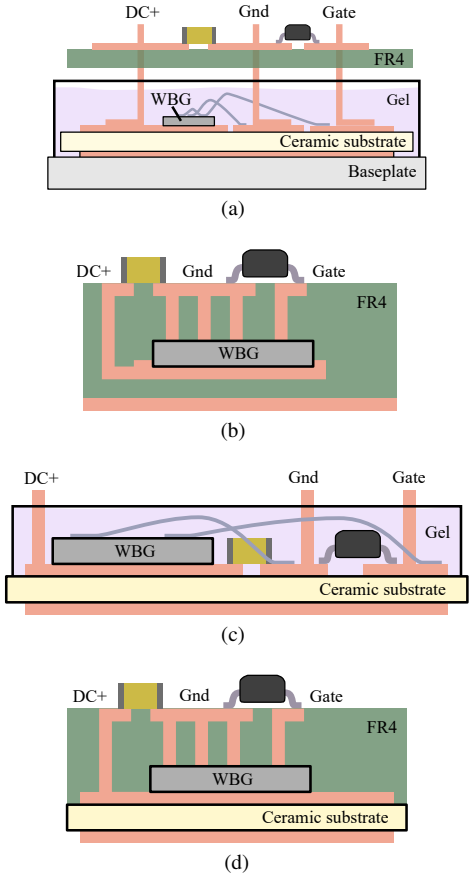

Fig. D.1: Packaging technologies (a) conventional power module structure (b) PCB embedded die technology (c) integrated DBC power module structure (d) PCB/DBC hybrid power module structure.

outer layers of the PCB. To further reduce thermal impedance the FR4 layer is minimized in thickness, which, in turn, causes issues related to high electric field stress. Too high electric field stress cause partial discharges or sparking [16]. Modifications to the geometry allows for some reduction in electric field stress [17], but still restrictions on spacing have to be maintained. In conclusion embedding everything in a PCB enables low parasitic design, but requires strict compromise between thermal and electrostatic performance.

To improve the heat dissipation of the semiconductor device, it is preferred to mount it on a DBC. An idea is to utilize the DBC as much as possible. The most important components such as semiconductor device, gate drivers and capacitors are soldered directly onto the DBC [6]. The structure is depicted in Fig. D.1(c). The power module has good heat dissipation through the ceramic, and high

Table D.1: Comparison of power module structures

	Inductance	Thermal	E-field	Manufacture
(a) Conventional	− −	+ +	+ +	+ +
(b) PCB embedded	+ +	−	−	−
(c) DBC integrated	+	+ +	+ +	+
(d) PCB/DBC	+ +	+ +	+	− −

electrostatic performance is maintained by encapsulating the module in silicone gel. The power loop layout is restricted to a single copper layer and achieves loop inductances of 7-11 nH [18]. This technology does not introduce any new steps in terms of manufacturing when compared to conventional power module. It mainly requires etching of more tracks and soldering of more components. However, as the DBC is limited to only a single layer, it reduces the complexity of circuits which can be incorporated. An attempt to mitigate this issue is to use printed copper thick-film technology on the DBC [13], [19]. This increases the level of integration of the gate driver circuitry, but it is still not as compact as what is achievable using PCB technology.

Power modules using both DBC and PCB technology reduces the issue of poor heat dissipation, while maintaining the low inductive design. A state of the art power loop inductance of 1.5 nH including current measurement is reported [20]. The solution is to mold the PCB directly on top of the DBC, by which no bond wires are used [21]–[23]. A diagram of the structure is shown in Fig. D.1(d). This structure shows very fast switching speeds of both gate and power loops. However, this solution significantly increases the manufacturing complexity, as the PCB molding is done directly on the DBC. A summary of the four packaging structures of Fig. D.1 is given in Table D.1, where positive metrics are given for technologies allowing low inductance, low thermal resistance, high electric field breakdown strength and low manufacturing complexity.

In this paper a power module hybrid structure of DBC and PCB is proposed for use with commercially available lateral GaN enhancement-mode high-electron-mobility transistor (eHEMT), which reduces the manufacturing complexity as only soldering is required for assembly. The structure is used to design a fast-switching integrated GaN eHEMT power module, which focuses on a board layout to simultaneously achieve both fast $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ switching, as described in section D.2. This also requires that the parameters of the gate driver circuit are properly designed. Thermal characteristics of the module are evaluated in section D.3. The switching behavior of the designed power module is simulated prior to testing. Due to the compactness of the designed board, it is difficult to measure and verify the operation. Thus efforts are made to construct

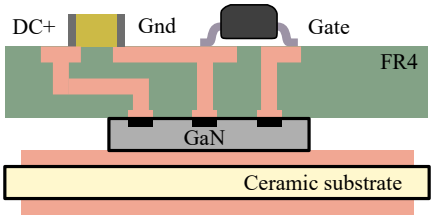

Fig. D.2: Proposed DBC/PCB hybrid power module structure for lateral GaN eHEMT devices.

a simulation model of high accuracy, to get knowledge of voltage/currents internally on the board. A simulation framework is discussed in section D.4, which includes three different levels of simulation complexity and its influence on the resulting waveforms. Finally in section D.5, the power module is built and its switching behavior is experimentally validated and compared with the simulation. The paper is concluded in section D.6.

D.2 Design of integrated GaN power module

New commercially available lateral GaN eHEMT devices have all electrical connections on the top surface, and a solderable bottom surface for heat dissipation [24]. This enables the use of a pre-manufactured PCB to be stacked on top of the GaN device. A power module structure as shown in Fig. D.2 is proposed. This solution offers very low inductance, high power dissipation and low capacitive coupling. The air gap to the DBC, means that traces and planes on the PCB have limited electrical coupling to the DBC and heat sink. A three dimensional model of the stack to be assembled is shown in Fig. D.3. At the bottom is a Al_2O_3 DBC substrate. The GaN eHEMT has an exposed metal backside as a heat sink, but is internally connected to source potential. Thus, a pattern is etched on the DBC to isolate each GaN eHEMT device. Additionally, holes are etched underneath each pin for safety, to avoid shorting of the different press fit pins to DBC. The PCB with all the control and measurement circuitry is soldered on top of the GaN eHEMT. At last, a plastic housing is used to enclose and mechanically protect the power module.

D.2.1 Gate driver

A schematic of the gate driver circuit used for a single half-bridge is shown in Fig. D.4. A bootstrap gate driver configuration is used, due to its simplicity and compactness. Using a bootstrap configuration removes the requirement of isolated power supplies, which can be relatively bulky and adds additional parasitic capacitance between switching output and ground. However, the

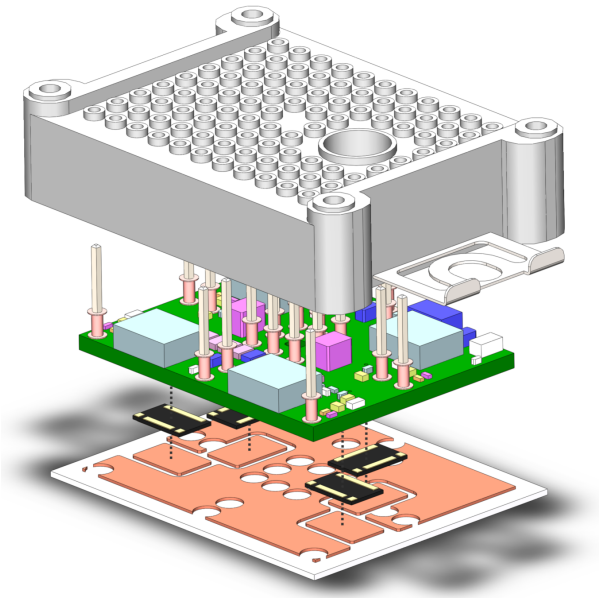

Fig. D.3: Three dimensional rendering of the GaN eHEMT power module stack assembly. DBC dimensions are 36x28 mm.

disadvantage is that there is some limit to the achievable duty cycle range, switching frequency and it requires a start-up procedure to power the high side gate driver circuitry. The ADUM4121 gate driver is used, which provides 5 kV voltage isolation between the input and output side. It has a coupling capacitance of 2 pF between input and output side. It has a 5 V supply on the input side, and is provided with a 6 V supply on the output. Thus the gate-source voltages supplied to the GaN eHEMT are 6 V and 0 V for high and low, respectively. For the high side, a low dropout (LDO) linear regulator is used to stabilize the 6 V supply. The ADUM4121 also has a Miller clamp functionality, but, for the tests shown in this paper, the Miller clamp connection is left unconnected. A 20 nH ferrite bead is inserted in the gate driver path to suppress high frequency ringing originating from the source inductance of the power circuit, and it shifts the resonance frequency of the gate driver loop away from the power loop resonance frequency [25]–[27].

There is a small operation margin of the gate-source voltage of the GaN eHEMT, as its recommended drive voltage is 6 V and maximum limit is 7 V. Thus, the turn-on gate resistance is chosen such that gate-source voltage oscillations are kept low, yet without slowing down the switching speed [21]. The gate-source loop schematic shown in Fig. D.5 is analyzed to obtain such dynamics, including the gate loop inductance L_g, turn-on gate resistance $R_{g,on}$

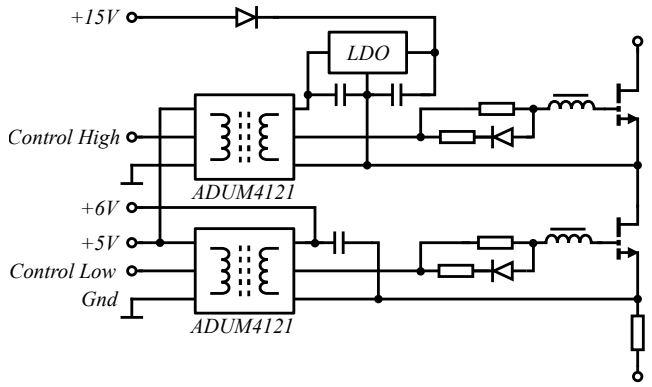

Fig. D.4: Schematic of the gate driver and switching circuit for a single half-bridge.

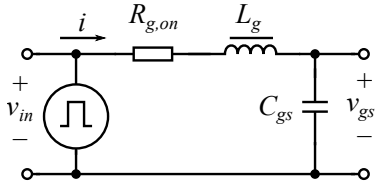

Fig. D.5: Schematic used to analyze the dynamics of the gate-source voltage.

and gate-source capacitance C_{gs}. By applying Kirchhoff's voltage law

$$v_{in}(t) = i(t)R_{g,on} + L_g\frac{\mathrm{d}i(t)}{\mathrm{d}t} + v_{gs}(t) \tag{D.1}$$

The expression $i(t) = C_{gs}\frac{\mathrm{d}v_{gs}(t)}{\mathrm{d}t}$ is inserted, and the Laplace transform of (D.1) becomes

$$\frac{V_{gs}(s)}{V_{in}(s)} = \frac{\frac{1}{L_g C_{gs}}}{s^2 + \frac{R_{g,on}}{L_g}s + \frac{1}{L_g C_{gs}}} \tag{D.2}$$

Equation (D.2) describes the dynamics from the gate driver to the gate-source voltage on the GaN eHEMT. It is compared to the standard form of a second order system [28], given by

$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{D.3}$$

where ζ is the damping ratio and ω_n the natural frequency. By comparing (D.2) to the standard form in (D.3) an expression for the gate turn-on resistance is found as

$$R_{g,on} = 2 \cdot \zeta \cdot \sqrt{\frac{L_g}{C_{gs}}} \tag{D.4}$$

A damping of $\zeta = 0.707$ is chosen to achieve fast rise time, yet limited oscillation of gate-source voltage. Inserting the gate-source capacitance of the GS66508T, and assuming that the gate inductance is dominated by the ferrite bead, the required gate resistance is calculated from (D.5).

$$R_{g,on} = 2 \cdot 0.707 \cdot \sqrt{\frac{20\,\mathrm{nH}}{258\,\mathrm{pF}}} = 12.4\Omega \tag{D.5}$$

The ADUM4121 gate driver and internal gate resistance of the GS66508T GaN device contributes with approximately 1.7-2.7 Ω, and thus the external gate resistor is chosen as 10 Ω. According to the design guidelines for the GS66508T GaN eHEMT [29], the turn-off gate resistance should be 5-10x lower to avoid Miller latch up. Due to the resistance contributions from the ADUM4121 and GS66508T internal gate, external turn-off gate resistance is chosen as 0 Ω. This results in a slight overshoot during turn-off, but as the minimum gate-source voltage is rated at $-10\,\mathrm{V}$, a slight overshoot during turn-off does not pose a threat for safe operation of the module.

D.2.2 Board layout

The board layout is designed to have both low parasitic capacitance and low inductance in the power loop, to push the capability of both high $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$. However, maintaining both low parasitic capacitance and low inductance is often a compromise between the two. For instance, the inductance can be kept small by decreasing the loop area, and use parallel planes on the PCB to cancel the magnetic fields generated. However, parallel planes have a large capacitive coupling, and results in increased common mode current during voltage transients [30]. Likewise, to have low capacitive coupling between planes they should be spaced far apart, but this will increase the loop area and thus increase the inductance. For this board layout, the parasitic capacitance is kept low by ensuring that switching outputs are not overlapping with other planes, as shown in Fig. D.6. Inductance is then kept low by placing the GaN eHEMT devices close to one another, reducing the effective loop area. DC-link capacitors are placed on the top side of the board, directly above the GaN eHEMT devices and multiple vias are used to connect the top and bottom plane.

A current measurement circuit must be integrated for control and safety purposes. For current measurements Hall-effect, Rogowski or similar are often used, but they all require a winding around a current carrying conductor. The inductance introduced by such a solution could compromise the desired fast switching. Instead, it is decided to measure the current through the low GaN eHEMT devices by inserting current shunts resistors in the power loop path. The current shunt resistor array has relatively low insertion inductance compared with other current measurement techniques [31]. The current shunt

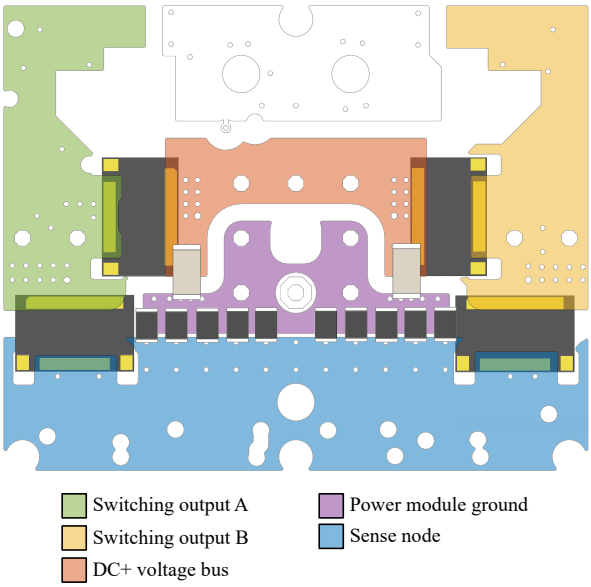

Fig. D.6: PCB layout of main power planes, and positioning of GaN eHEMT devices (bottom side), decoupling capacitors (top side) and current shunt resistors (top side).

layout is based on the design presented in [32], [33]. In total ten current shunt resistors are inserted to minimize the parasitic inductance, which improves measurement bandwidth [34]. The issue of this solution is that the measurement is not isolated, and thus it is influenced by parasitics in the circuit. Thus it is important to accurately model the parasitics of the board, as further studied in Section D.4, to know their influence on the measured shunt resistor voltage. Two half bridges are placed in the same power module, and by symmetrical placement they share both the same current shunt resistors and decoupling capacitors.

D.3 Thermal characteristics

The chosen GaN eHEMT device is a prepackaged device and has a thermal resistance from junction to case, Θ_{jc}, of 0.5 K/W. In comparison the CPM2-1200-0040B SiC MOSFET bare die of similar dimensions has $\Theta_{jc} = 0.38$ K/W [35]. However, the additional 0.12 K/W must be compared to the total thermal resistance from junction to heat sink of the final power module. The thermal performance of the power module is analyzed using a steady state finite element simulation. The 3D model of Fig. D.3 is imported to COMSOL Multiphysics.

The DBC stack has a 0.3 mm thick copper layer with thermal conductivity $k = 380\ \frac{\mathrm{W}}{\mathrm{mK}}$, on either side of 0.63 mm Al_2O_3 ceramic substrate of $k = 25\ \frac{\mathrm{W}}{\mathrm{mK}}$.

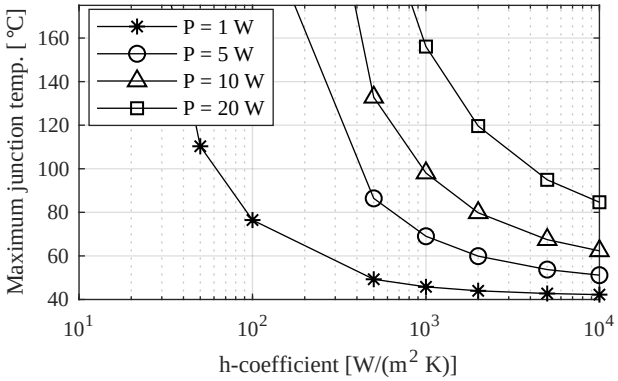

Fig. D.7: Maximum junction temperature for different power inputs and heat transfer coefficient. Exterior temperature is $T_{ext} = 40$ °C.

A thin solder layer of 60 μm thickness having thermal conductivity, $k = 60$ $\frac{\mathrm{W}}{\mathrm{mK}}$, is included to the heat pad of the GaN eHEMT device. The backside of the power module is cooled by the heat flux

$$q = h \cdot (T_{ext} - T) \tag{D.6}$$

where q is the heat flux, h is the heat transfer coefficient and T_{ext} is the exterior temperature. The heat transfer coefficient changes greatly depending on how the power module is cooled. Typically the h-coefficient is up to 100-300 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ for forced convection of air, 500-2000 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ for modules mounted on heat sink and 10000 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ or more for direct water cooling [15], [23], [36]–[38]. Shown in Fig. D.7 is the maximum junction temperature of the power module, when subjected to different power inputs per device and heat transfer coefficients. In all cases the exterior temperature is kept at 40 °C.

A case where each GaN eHEMT device is subjected to a power loss, P of 10 W, the exterior temperature, $T_{ext} = 40$ °C and $h = 1000$ $\frac{\mathrm{W}}{\mathrm{m^2K}}$, is shown in Fig. D.8. The thermal resistances from junction to heat sink, Θ_{jh}, are evaluated as 2.4 $\frac{\mathrm{K}}{\mathrm{W}}$ and 2.1 $\frac{\mathrm{K}}{\mathrm{W}}$ for low and high side, respectively. This is comparable with power modules on similar DBC material, thickness and semiconductor die area [5], [13]. The difference in thermal resistance between high and low side devices is 12 %. Compared to other integrated power modules the difference between devices is found as 18-19 % [15], [23]. It is concluded that the thermal performance, measured in terms of thermal resistance Θ_{jh} and mismatch between devices is within range of similar integrated solutions. Based on the total thermal resistance of the power module, the prepackaged GaN eHEMT device is not regarded as the bottleneck. It is concluded as suitable for use in the power module without modifications to its proposed structure.

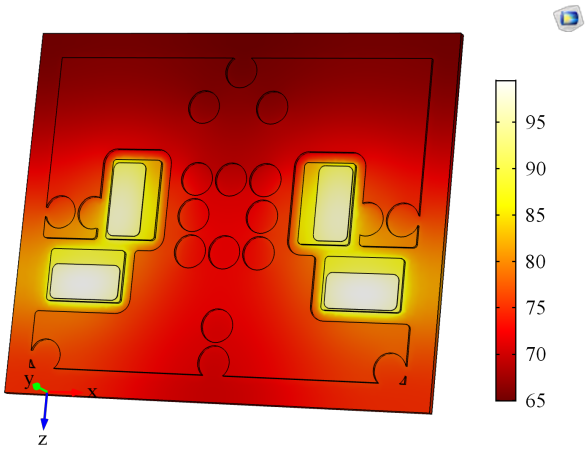

Fig. D.8: Temperature distribution simulated in COMSOL Multiphysics, for conditions P = 10 W per device, $h = 1000\ \frac{\mathrm{W}}{\mathrm{m^2K}}$ and $T_{ext} = 40\ ^{\circ}C$.

D.4 Electrical simulation model

Due to the compactness of the design, there is only a limited amount of measurement points available from the power module: switching output voltages and the current sense measurement. Thus, during development and testing, an accurate simulation model is a necessary tool to gain insight in other nodes of interest, i.e. gate voltages. Secondly, to further improve the design, it is required to know the contribution different board parasitics have on the switching performance and measurements. A simplified schematic of the parasitics and the components of one half-bridge is shown in Fig. D.9. As an example, due to the location of the grounding on the board, and if assuming that trace impedances are mainly inductive, the sense voltage measured is given by

$$v_{sense}(t) = i_1(t) \cdot R_{\mathrm{sense}} + L_{\mathrm{De}} \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} + L_{\mathrm{DC-}} \frac{\mathrm{d}i_2(t)}{\mathrm{d}t} \tag{D.7}$$

where i_1 is the power loop current, i_2 is the circulating current between distributed DC-links, R_{sense} is the resistance of the shunt array and L_{De}, $L_{\mathrm{DC-}}$ are trace self-inductances. When achieving fast switching speed, there is a significant contribution from the parasitic inductances L_{De} and $L_{\mathrm{DC-}}$ and thus their value are important to know, to validate that the experimental measurements are correct.

To extract the board parasitics the ANSYS Q3D Extractor simulation software is used. ANSYS Q3D Extractor uses finite element method and methods of moments to solve electromagnetic field simulations [39]. A three dimensional model of the board is imported to the software, and inputs/outputs of each net are defined. A literature review reveals that different simulation

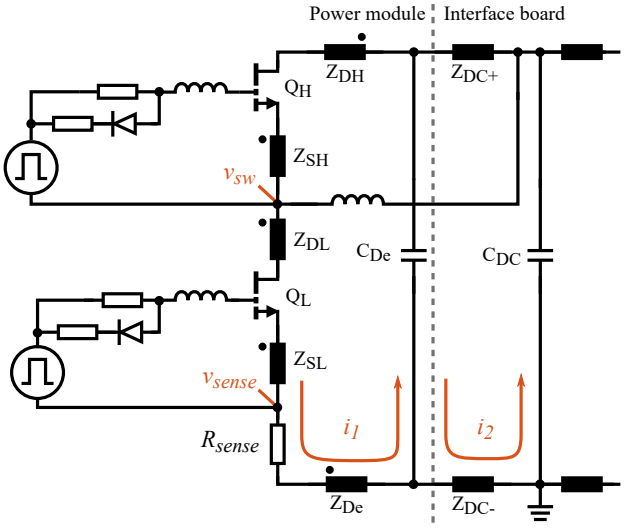

Fig. D.9: Simplified schematic of the simulation model.

Table D.2: Self-inductance of traces

Symbol	Value	Symbol	Value
L_{DH}	0.31 nH	L_{De}	0.23 nH
L_{SH}	0.26 nH	$L_{\mathrm{DC+}}$	1.9 nH
L_{DL}	0.35 nH	$L_{\mathrm{DC-}}$	0.3 nH
L_{SL}	0.86 nH		

approaches are used with the ANSYS Q3D Extractor software, which might result in different accuracy, simulation time and ease of convergence when later implemented in a SPICE solver. In the following section, three different approaches are implemented and the simulation results are compared. The first approach is to replace each impedance of Fig. D.9 with the self-inductance of the trace. The parasitic capacitances are designed to be low for this board, and thus are neglected. The inductances are evaluated using a point-by-point approach, i.e. from the DC-link to the drain of the high device, then from source of high device to drain of low device and so forth [9], [40], [41]. This model is denoted as a Level 1, and self-inductance calculated for each trace is shown in Table D.2. A reported issue of this is that the summation of the inductances becomes large, because when evaluating each inductance individually there are no mutual inductance effects included in the model [42].

Thus, often an approach is used at which the full loop is evaluated [30], [43],

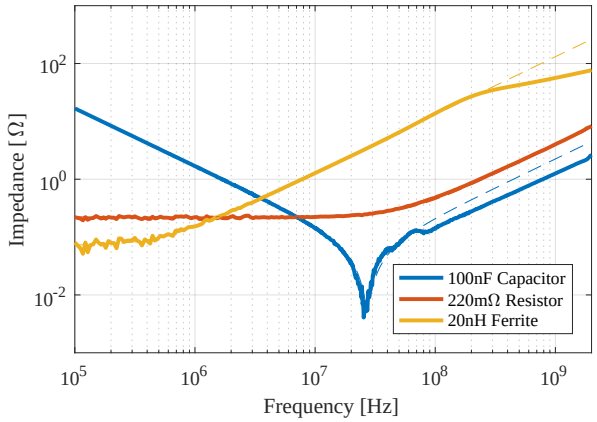

Fig. D.10: Impedance as a function of frequency of main components of the half-bridge circuit (including their simulated models in dashed line).

[44]. In this approach each device is modelled as a conductor, i.e. drain and source of a switch are electrically shorted. The effective inductance of a full loop is calculated, and by this approach the mutual inductance effects are included in the solution. However, to use the extracted inductance in a SPICE simulation it must be placed accordingly in the circuit diagram, and this is difficult when inductances are calculated for the full loop. Thus, an approach considered for this paper, is to use both the self-inductance and mutual-inductance [44]–[46]. From ANSYS Q3D Extractor an RLC matrix is exported, meaning that it models the resistance and self-inductance in each trace, mutual-inductance and parasitic capacitances between nodes. This is denoted as a Level 2 model. It is advantageous during development that electromagnetic fields and couplings are already included in the circuit simulation which reveals effects of conducted and near-field electromagnetic interference issues related to the board-structure.

When exporting the RLC matrix, the parameters must be extracted at a certain frequency. Typically, resistance values are extracted for low frequencies, where skin effect is neglected and current is assumed to flow equally distributed in the conductor volume. This is done to correctly model steady state power loss of the board. The inductance values are extracted for high frequencies, at which the current path shifts to reduce the total loop area, and the inductance value becoming lower. Using this value results in the best approximation of the inductance during fast switching transients.

D.4.1 Measurement of component parasitics

In addition to extraction of parasitics of the board, the influence of the parasitics in the components is also of interest. As board parasitics are small, the relative

Table D.3: Parasitics extracted of SMD components

Model			
Component	R	L	C
100 nF, 1210 capacitor	6 mΩ	257 pH	95.6 nF
220 mΩ, 0805 resistor	224 mΩ	616 pH	-
20 nH, 0603 ferrite bead	71 mΩ	21 nH	-

Table D.4: Complexity in simulation model

	Board parasitics	Component parasitics
Level 1	L w/o coupling	Ideal R, L or C
Level 2	RLC incl. coupling	Ideal R, L or C
Level 3	RLC incl. coupling	Measured RLC

influence of the surface mount device (SMD) packages become larger. Especially the measurement of voltage across the shunt resistors where the influence of the parasitic inductance can be significant. As resistors are conducting the full current and the voltage across them is just a few hundred millivolts, it requires a good estimation of how they are influenced by parasitics. Measuring the parasitic inductance and capacitance of SMD resistors, capacitors and ferrite beads down to just a few nH and pF requires a large frequency range to capture the cutoff/resonance frequency of the component. A Keysight E5016B impedance analyzer is used, which is capable of measuring the components up to 3 GHz. The Keysight 16192A test fixture has a measurement capability up to 2 GHz and is used to mount the SMD components. The impedance spectrum of an 220 mΩ 0805 shunt resistor, 100 nF 1210 DC-link capacitor and the 20 nH ferrite bead in the gate driver is shown in Fig. D.10, which also includes the frequency response of its estimated RLC model. The model used for fitting the response is an idealized RLC series connection. Table D.3 summarizes the parasitics values extracted from the frequency response. The simulation model which includes both RLC board parasitics and RLC of SMD components is denoted as a Level 3 model.

D.4.2 Simulation results

The results are compared for the three different levels of simulation complexity. A summary of what is included in the three simulation models is shown in Table D.4. All simulations use the SPICE model of the GS66508T GaN eHEMT

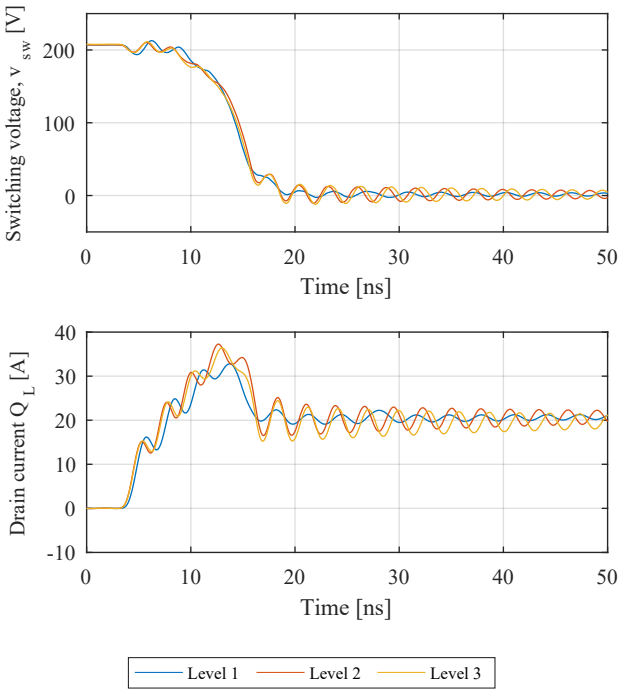

Fig. D.11: Simulated waveforms of switching voltage and drain-source current during turn-on for three different levels of simulation complexity.

device, and are all solved using the recommended solver settings provided by GaNSystems [47]. The SPICE model used includes a drain-source stray inductance of 0.4 nH originating from the packaging of the device and its temperature is set at 25 °C.

A double pulse test is simulated. The DC-link voltage is 200 V and current is ramped up in a 10 μH load inductor for 1 μs, to achieve a load current of 20 A. Transients of turn on and turn off are investigated, as shown in Fig. D.11 and D.12, respectively.

The voltage rise time is defined as the time from 10 % to 90 % of DC-link voltage, and vice versa for voltage fall time. By this definition, both the fall and rise time is 6 ns, equivalent to 27 V/ns. These switching speeds are the same for all three simulation cases. Following turn-on and turn-off oscillations in both voltage and current are visible, due to the resonance frequency of the power loop, shown as i_1 in Fig. D.9. The resonance frequency is given by

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{D.8}$$

For the Level 1 model, the power loop inductance is calculated as the sum of inductances in the power loop, i_1 in Fig. D.9, combined with the 0.4

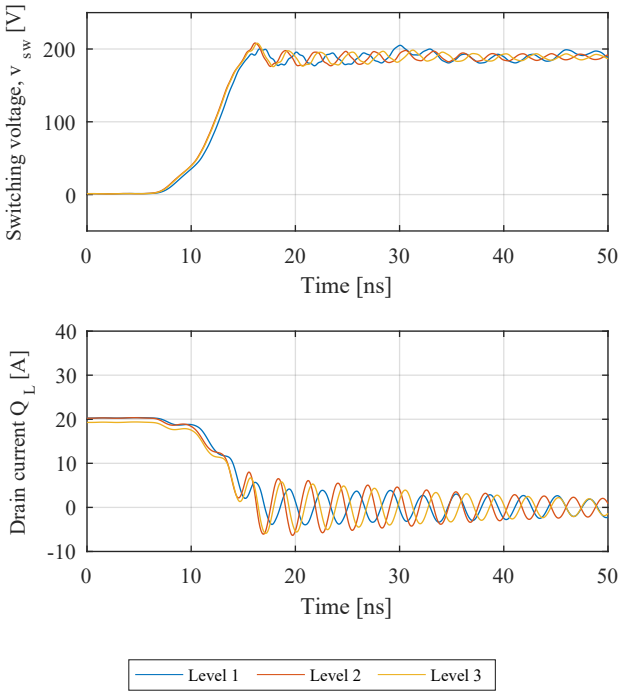

Fig. D.12: Simulated waveforms of switching voltage and drain-source current during turn-off for three different levels of simulation complexity.

nH contribution from the packaging of the two GaN devices. The resonance frequency for the Level 1 model is calculated by reading the time period of oscillations in Fig. D.11 and D.12. The output capacitance of the GaN eHEMT device is estimated for the given test condition by rearranging (D.8).

$$C = \frac{1}{(2 \cdot \pi \cdot 325\text{MHz})^2 \cdot 2.8\text{nH}} = 85\text{pF} \tag{D.9}$$

From the simulation result the resonance frequency is slightly higher for the Level 2 and 3 models. However, because they include mutual inductance coupling terms the effective loop inductance is cumbersome to calculate. Instead, the effective loop inductance for Level 2 and 3 models are calculated by reading the resonance frequency from the simulation results and equals 358 MHz and 338 MHz, respectively. By rearranging (D.8) the effective inductance for the Level 3 model is calculated as

$$L_{L3} = \frac{1}{(2\pi \cdot 338\text{MHz})^2 \cdot 85\text{pF}} = 2.6\text{nH} \tag{D.10}$$

Thus, the effective inductance is 8 % higher for Level 1 which only includes self-inductance, compared with Level 3 case where mutual inductance coupling

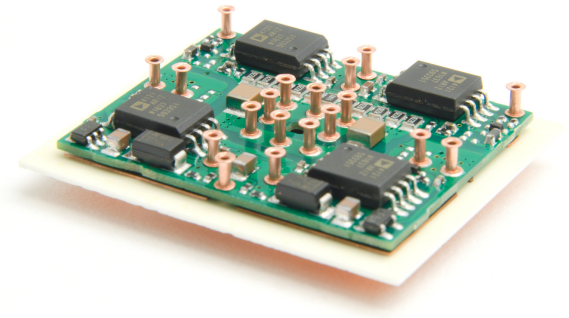

Fig. D.13: Photograph of power module after soldering.

and component parasitics are included. The slightly higher inductance values of the Level 1 model, means it could be more susceptible to false and oscillatory turn on during simulation, due to increased ringing of the gate-source loop [25], [48]. However, this cannot be concluded because the coupling of the RLC matrix introduce new complexity that have not yet been studied in literature. The three models differ in terms of time required to generate the simulated turn on/off waveforms, which are simulated for a total of 5 μs. The real time required in LTSpice XVII is 5.5s, 7.4s and 11.3s for the Level 1, Level 2 and Level 3 model, respectively. Thus the total simulation time is about 2 times longer for the increased complexity.

D.5 Experimental results

The power module is built for experimental tests on a 0.63 mm thick Al_2O_3 DBC and is etched with the designed pattern. All components are soldered to the PCB board in a multi-vacuum vapor phase oven. Following this step, the PCB board including the GaN eHEMT devices are soldered to the DBC, as shown in Fig. D.13. At last the pressfit pins are inserted in the sockets and the plastic housing is mounted. For the experimental tests the power module is connected to a test board, as shown in Fig. D.14. The test board interfaces the auxiliary voltages and control signals for the gate drivers. It includes the main DC power supply and switching output terminals for each half-bridge. BNC connectors are used to measure the voltage switching outputs and the current shunt signal. The voltage switching waveforms are measured using 500 MHz LeCroy PP018-1 probes on a Lecroy HDO6104A oscilloscope. All cables of probes, auxiliary power supply and main power supply are equipped with common mode choke cores.

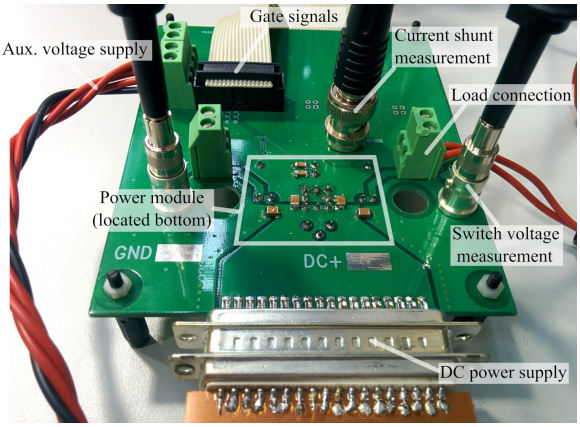

Fig. D.14: Test board interfacing auxiliary voltage supply, gate control signals and BNC connector points for measurements of switching voltage and current shunt. The power module is located below the test board.

D.5.1 Switching behavior

The experimental waveforms are compared with the level 3 simulation model during turn-off and turn-on as shown in Fig. D.15. The voltage switching waveforms show very good coherence with the simulation model. The experimental results shows that the GaN eHEMT devices for both voltage fall and rise time switch in 6 ns for the tested 200 V / 20 A condition, equivalent to a voltage transient of 27 V/ns. The resonance frequency of the experimental results is read as 335 MHz. Assuming that the loop capacitance is the same as observed from the simulation model in Section D.4, it indicates that the effective power loop inductance is 2.65 nH.

To further verify the simulation model, the operating conditions are modified to 400 V / 15 A, as shown in Fig. D.16. The simulation model is the same, except for a change in the DC bus voltage and gate-timing to achieve the right current value. At 400 V / 15 A the voltage fall and rise times are 5 ns and 8 ns, respectively. This corresponds to voltage transients during turn-on and turn-off of 64 V/ns and 40 V/ns.

In addition to verifying the switching voltage, it is also ensured that the shunt resistor array delivers accurate current measurements for control purposes, preferably without additional measurements and computational expensive compensations. The measured sense voltage is divided by 22 mΩ (now called measured sense signal). As an additional verification the current through the inductor is measured using a Teledyne LeCroy CP030 current probe, as a reference which is not affected by the high frequency ringing. The measured sense current, the measured inductor load current and the simulated sense current are shown in Fig. D.17. The results highlight that due to damping

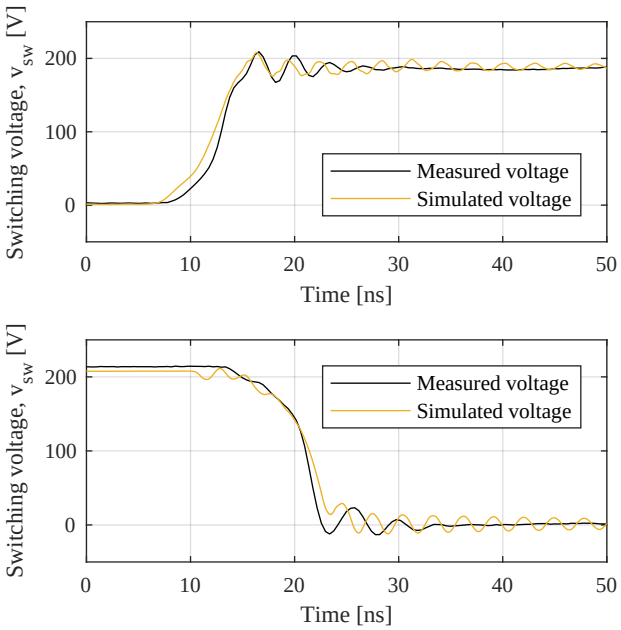

Fig. D.15: Comparison of experimental and level 3 simulated waveforms of switch voltage during turn-off and turn-on at 200 V / 20 A.

in the circuit, the influence of inductive terms shown (D.7) are decayed after 1 μs, at which an accurate current measurement can be sampled. The initial high frequency oscillations are due to the power loop, indicated as i_1 in Fig. D.9. The lower frequency ringing is due to ringing of the decoupling and main DC-link capacitors. As the GaN eHEMTs are switching, power is delivered from the decoupling capacitors, C_{De}, inside the power module and their voltage drop. Current i_2, as denoted in Fig. D.9, conducts to charge the decoupling capacitors. When the two voltages are equal, current is still loaded in inductances, and thus charges the decoupling capacitors slightly above their initial 200 V. This causes an oscillating current, which experimentally is measured at a frequency of 8.8 MHz. This oscillation is correctly predicted by the simulation model. In general, the oscillations of the simulated response are less damped than the experimental results. This can be explained by the choice of using the DC resistance values in the exported RLC matrix from ANSYS Q3D Extractor. To solve this a frequency dependent resistance model should be implemented, such that the resistance is higher for increasing frequency due to the skin effect. However, in terms of the switching speed of both turn-on and turn-off voltage as well as its frequency and amplitude of oscillation this has minor impact. In conclusion the use of ANSYS Q3D Extractor provides a very good simulation result of the switching voltage transient.

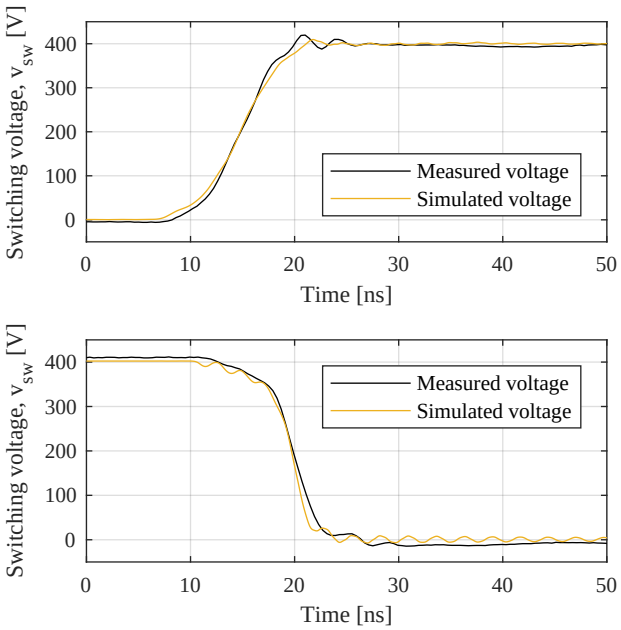

Fig. D.16: Comparison of experimental and level 3 simulated waveforms of switch voltage during turn-off and turn-on at 400 V / 15 A.

D.6 Conclusion

A hybrid PCB/DBC structure is proposed, designed for fast-switching and high power dissipation. In contrast to other hybrid methods, the proposed structure does not require embedding of dies and molding of PCBs on top of a DBC. The DBC, PCB and semiconductors are available from suppliers and only requires vapor phase soldering to assemble the stack, which decreases the manufacturing complexity.

A finite element simulation is used to assess the thermal characteristics of the power module, and the thermal resistance from junction to heat sink is evaluated as 2.4 K/W. ANSYS Q3D Extractor is used to extract the parasitics of the board, which are implemented in a SPICE solver. Three levels of simulation complexity were investigated. A level 1 simulation model only including self inductance, a level 2 model with a coupled RLC matrix and a level 3 which is also combined with SMD component parasitics, by using an impedance analyzer up to 2 GHz. The level 1 simulation case estimates 8 % higher loop inductance, when compared to the level 3 model. The experimental results verified the simulation model for the main switching voltage waveforms, and shows a turn-on and turn-off speed of both 6 ns during switching at 200 V / 20 A. By analyzing the resonance frequency, it is concluded that the achieved

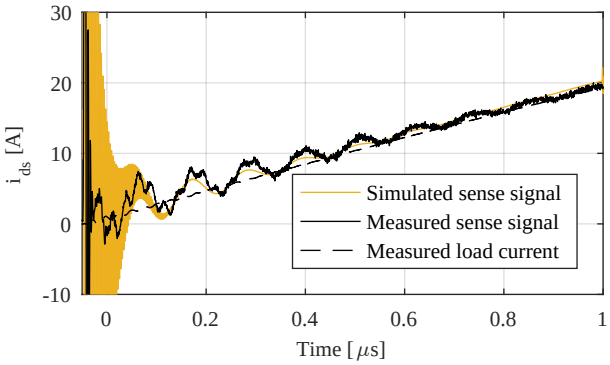

Fig. D.17: Measured load current of inductor, measured sense current and level 3 simulated sense current.

power loop inductance is 2.65 nH including current measurement circuitry. The level 3 simulation model provides the best approximation of the inductance seen from the experimental results, but takes two times longer to simulate when compared to level 1. The power module is tested at 400 V / 15 A, at which voltage fall and rise times of 5 ns and 8 ns are achieved, respectively. This equals a maximum $\mathrm{d}v/\mathrm{d}t$ of 64 V/ns. The measured switching voltage waveform of the GaN eHEMT integrated power module shows low overshoot and ringing, which proves the proposed module structure and its accompanying board layout. Compared with other integrated power module structures, the proposed hybrid DBC/PCB power module structure performs well in terms of thermal performance, has very low commutation loop inductance and is relatively easy to manufacture.

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Paper E

Thermal characteristics and simulation of an integrated GaN eHEMT power module

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Szymon Beczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen

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Thermal characteristics and simulation of an integrated GaN eHEMT power module

Asger Bjørn Jørgensen, Tzu-Hsuan Cheng, Douglas Hopkins, Szymon Beczkowski, Christian Uhrenfeldt and Stig Munk-Nielsen

Abstract

Compact power module structures are emerging to achieve fast switching of wide bandgap semiconductors. The thermal characteristics of a new integrated GaN power module are obtained experimentally. A simulation workflow to extract the thermal characteristics of integrated module structures using finite element method software is presented and verified.

Introduction

New power module and packaging solutions are being developed to better utilize the benefits of new commercially available wide bandgap (WBG) semiconductor devices, based on silicon carbide and gallium nitride. Compared to silicon one of the main benefits offered by the new WBG devices are faster switching speeds, resulting in lower switching losses and higher power densities. The full potential of WBG is difficult to achieve using conventional packaging structures. Typically, semiconductor devices are soldered to a direct bonded copper (DBC) and packaged as a standalone component. External leads of the component are then soldered to a printed circuit board (PCB) for interconnection with crucial elements such as DC-link capacitors and gate driver circuits. This typically results in power loop and gate driver loop inductances in the range of 10-30 nH. Recent developments in power module packaging is to integrate the semiconductor device with both the DBC and PCB, such as the structure shown in Fig. E.1 [1]. Using such hybrid DBC/PCB approaches enable parasitic inductances as low as 1.1-2.7 nH [2]–[4], while the thermal performance is maintained at a level similar to conventional power modules.

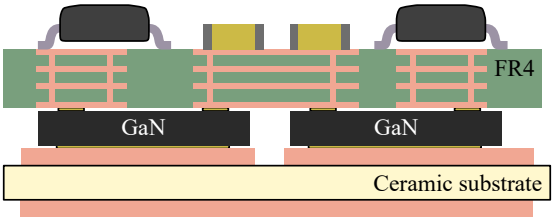

Fig. E.1: Structure of integrated GaN eHEMT power module.

However, the literature presenting thermal analysis of the integrated DBC/PCB hybrid power modules is done without the modelling of the PCB and its copper layers/traces [3]–[5]. This could suggest that simulation of the total power module structure including the PCB is cumbersome or that the thermal impact of the PCB is insignificant and therefore can be rightfully left out. Secondly, no literature has experimentally verified the thermal performance of the new integrated DBC/PCB power module structures.

In this paper, the thermal characteristics are experimentally demonstrated of an integrated DBC/PCB power module based on GS66508T GaN eHEMT devices, as shown in Fig. E.2. Additionally, this paper presents a software framework to build up a model of the DBC/PCB power module which includes the influence of the PCB on the thermal performance.

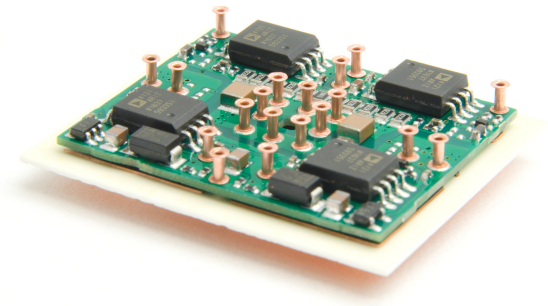

Fig. E.2: Picture of integrated GaN eHEMT power module.

Methodology

The methodology to obtain the thermal characteristics of the power module is the same for both the simulation and the experiment. The approach, as described in [6], is to apply a step input of power to one of the devices in the power module and measure the device temperatures as a function of time. This gives information about the thermal impedance of the device and its thermal coupling to other devices. The procedure is then repeated once per device. The thermal impedance from a device to ambient based on its power dissipation is calculated

$$Z_i(t) = \frac{T_i(t) - T_a}{P_i(t)} \tag{E.1}$$

where Z_i is the thermal impedance of device i, T_i is the temperature of device i, T_a is the ambient temperature and P_i is the power dissipation of device i. To model the thermal coupling between devices in the power module, the thermal

characteristic parameter, Ψ, is defined as

$$\Psi_{ij}(t) = \frac{T_i(t) - T_a}{P_j(t)} \tag{E.2}$$

where T_i is the temperature of device i and P_j the power dissipation of device j. Thus, the thermal characteristic parameter Ψ_{ij} describes the temperature increase of a device i due to the power dissipation of one of its neighbor devices j. While the definition of Ψ and Z looks similar and they share the same unit, it is important to note the distinction. The use of Ψ is of more value in a practical case, as power flow distribution in different paths throughout the power module is difficult to measure, but the temperature and power dissipation in devices is known. When combining the thermal impedance of a device in (E.1) and the temperature gained from neighboring devices in (E.2), the temperature of all devices in the power module can be calculated from

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix} = \begin{bmatrix} Z_1 & \Psi_{12} & \Psi_{13} & \Psi_{14} \\ \Psi_{21} & Z_2 & \Psi_{23} & \Psi_{24} \\ \Psi_{31} & \Psi_{32} & Z_3 & \Psi_{34} \\ \Psi_{41} & \Psi_{42} & \Psi_{43} & Z_4 \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{bmatrix} + T_a \tag{E.3}$$

The designed PCB board of the power module in Fig. E.2, has floating non-filled vias directly on top of each GS66508T GaN eHEMT device, which allows for fiber optic temperature sensors of diameter 0.28 mm to measure the device temperatures [7]. The devices and their measurement points are labelled as shown in Fig. E.3.

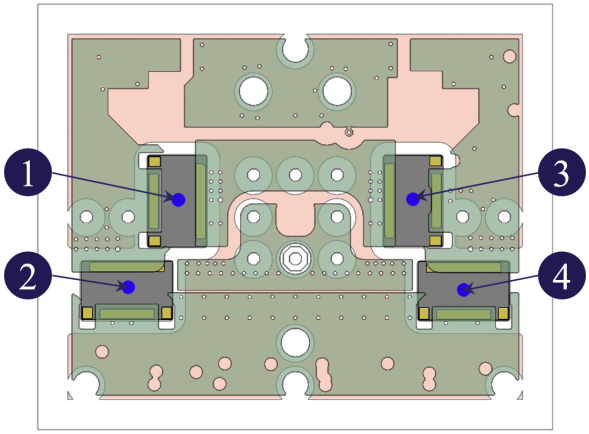

Fig. E.3: Labelling of devices and measurement points.

Experimental results

An experimental test setup is constructed, as shown in Fig. E.4. A DC power supply is connected to the drain-source of the device under test and a positive gate signal is given. Temperatures are logged using OTG-M280 fiber optic temperature sensors from Opsens.

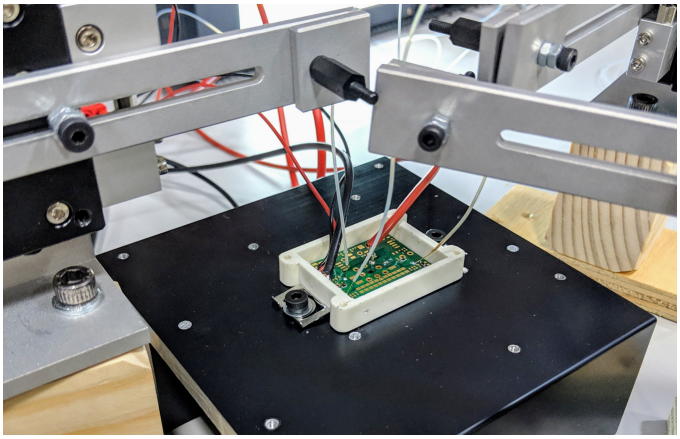

Fig. E.4: Picture of the experimental setup.

A current of 6 A is conducted through the GaN eHEMT device. For an on-state resistance of 50 mΩ this equals 1.8 W in power dissipation. Temperatures of all four devices in the power module are measured, and (E.1) and (E.2) is applied to the data. The thermal characteristics obtained are shown in Fig. E.5. The steady state thermal impedance from device to ambient is 2.07 K/W for the device under self-heating. The results show that device 1 is thermally coupled to device 2, 3 and 4 by 0.84 K/W, 0.37 K/W and 0.09 K/W, respectively.

Thermal modelling using finite element method software

The following section describes the finite element method simulation of the designed integrated GaN eHEMT power module. To get a three dimensional model of the PCB the board files are imported into ANSYS Siwave, which allows conversion of the two dimensional layer information into a three dimensional model. Solidworks is then used to assemble the three dimensional models of the GaN Systems GS66508T devices, the DBC and the PCB including its copper planes and vias. The full power module model is imported to the finite element method software COMSOL, as shown in Fig. E.6. A relatively fine mesh is used because of the thin vias and features of the PCB board. A thin resistive layer

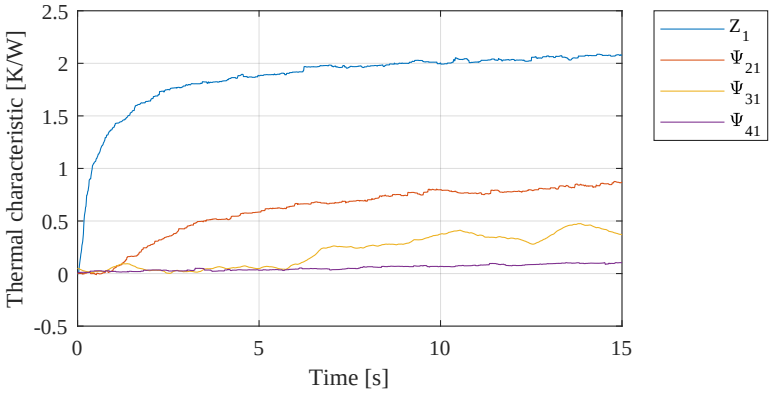

Fig. E.5: Experimental thermal response of the integrated GaN eHEMT power module.

boundary is added to the contacts of the GaN Systems GS66508T to model its junction to case thermal resistance of 5 K/W to its top electrical contacts and 0.5 K/W to the bottom heat pad. The material properties used in the transient simulation model are listed in Table E.1.

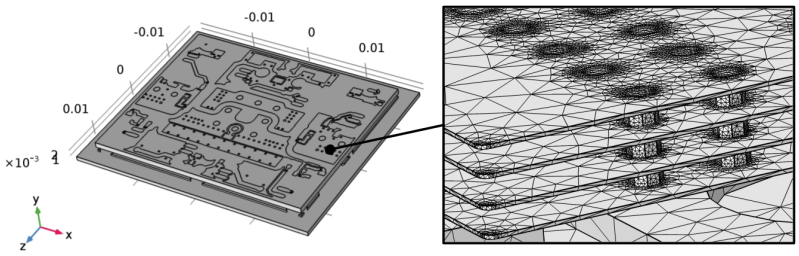

Fig. E.6: 3D model of the power module in COMSOL and close-up of the mesh around via array.

A power dissipation of 1.8 W is applied to device 1 and temperatures of all four devices are logged. The boundary condition on the DBC backside facing the heatsink is modelled as

$$q = h \cdot \Delta T \tag{E.4}$$

where q is the heat flux, h is the heat transfer coefficient and ΔT is the temperature difference between the solid surface and surrounding environment. One of the main unknowns of the simulation is the h-coefficient. For a power module connected to a heat sink it may vary from approximately 500 to 3000 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ [3], [8], [9] depending on parameters such as the thermal interface material used, heatsink coolant, the applied pressure and surface roughness etc. For this paper the h-coefficient is chosen as 1800 $\frac{\mathrm{W}}{\mathrm{m^2K}}$, based on achieving

Table E.1: Material properties used in the simulation model.

Material	**Conductivity** $\left[\frac{\mathrm{W}}{\mathrm{m\cdot K}}\right]$	**Heat capacity** $\left[\frac{\mathrm{J}}{\mathrm{kg\cdot K}}\right]$	**Density** $\left[\frac{\mathrm{kg}}{\mathrm{m^3}}\right]$
Cu	400	385	8960
Al_2O_3	24	765	3970
FR4	0.3	1369	1900

the same temperature for device 1 in steady state for both simulation and experiment. By applying (E.1) and (E.2) the transient thermal characteristics of the integrated power module are extracted as shown in Fig. E.7.

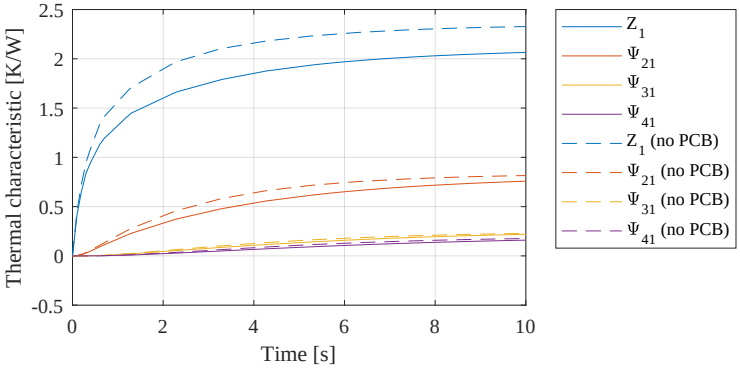

Fig. E.7: Simulated thermal response of the integrated GaN eHEMT power module.

The simulation model predicts a Z_1, Ψ_{21}, Ψ_{31} and Ψ_{41} of 2.07 K/W, 0.76 K/W, 0.22 K/W and 0.16 K/W, respectively. For the power dissipation of 1.8 W, the absolute errors between experiment and simulation of devices 2, 3 and 4 temperatures are 0.14 °C, 0.27 °C and 0.12 °C. The OTG-M280 fiber optic temperature sensors have an accuracy of ± 0.3 °C [7]. Thus the simulation result is within bounds the expected error from the experiment. As the finite element method simulation is verified with the experimental results, it allows for the investigation of how much influence the PCB has on the thermal performance. The dashed lines of Fig. E.7 show the thermal characteristics of the power module when the PCB is not included in the simulation. The thermal impedance of the heated device is increased to a steady state value of 2.33 K/W, and a slight increase of Ψ is experienced by the other devices in the module. Compared relatively to the temperature of device 1 the remaining devices are less thermally coupled, but their absolute temperature is increased. Thus without the PCB the entire power module is heated more for the same power dissipation. The copper layers of the PCB distributes the generated heat to other devices and thus utilizes more area of the top side copper. In

conclusion, the PCB enables double sided cooling of the GaN eHEMT devices and without the influence of the PCB the thermal impedance of the self-heated device under test increases by 13 %. Failure to model the copper layers of the PCB may result in a wrong prediction of device temperatures.

Conclusion

New integrated and low inductive power module structures are being developed to better utilize the benefits of new WBG semiconductors. However, current literature presenting the thermal capabilities of the integrated power module structures all lack the modelling of the PCB and the thermal characteristics are not experimentally verified. A new integrated hybrid DBC/PCB full-bridge power module using GaN eHEMT devices is tested experimentally. The steady state thermal impedance from a device to ambient is 2.07 K/W for the device under self-heating. A three dimensional model of the PCB is obtained by exporting the board from ANSYS Siwave. Solidworks is used to assemble the models of GaN devices, PCB and DBC, and the finite element method software COMSOL is used for thermal simulation. The finite element method simulation is verified by matching it with the experimental results. The simulation predicts an increase of the thermal impedance by 13 %, if the PCB board is not included in the thermal simulation of the GaN eHEMT device. While the FR4 PCB board material has low thermal conductivity, the copper layers of the PCB facilitates additional heat distribution. Disregarding the influence of the PCB board may result in a significant error in predicting the temperature of devices in integrated DBC/PCB hybrid power modules.

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