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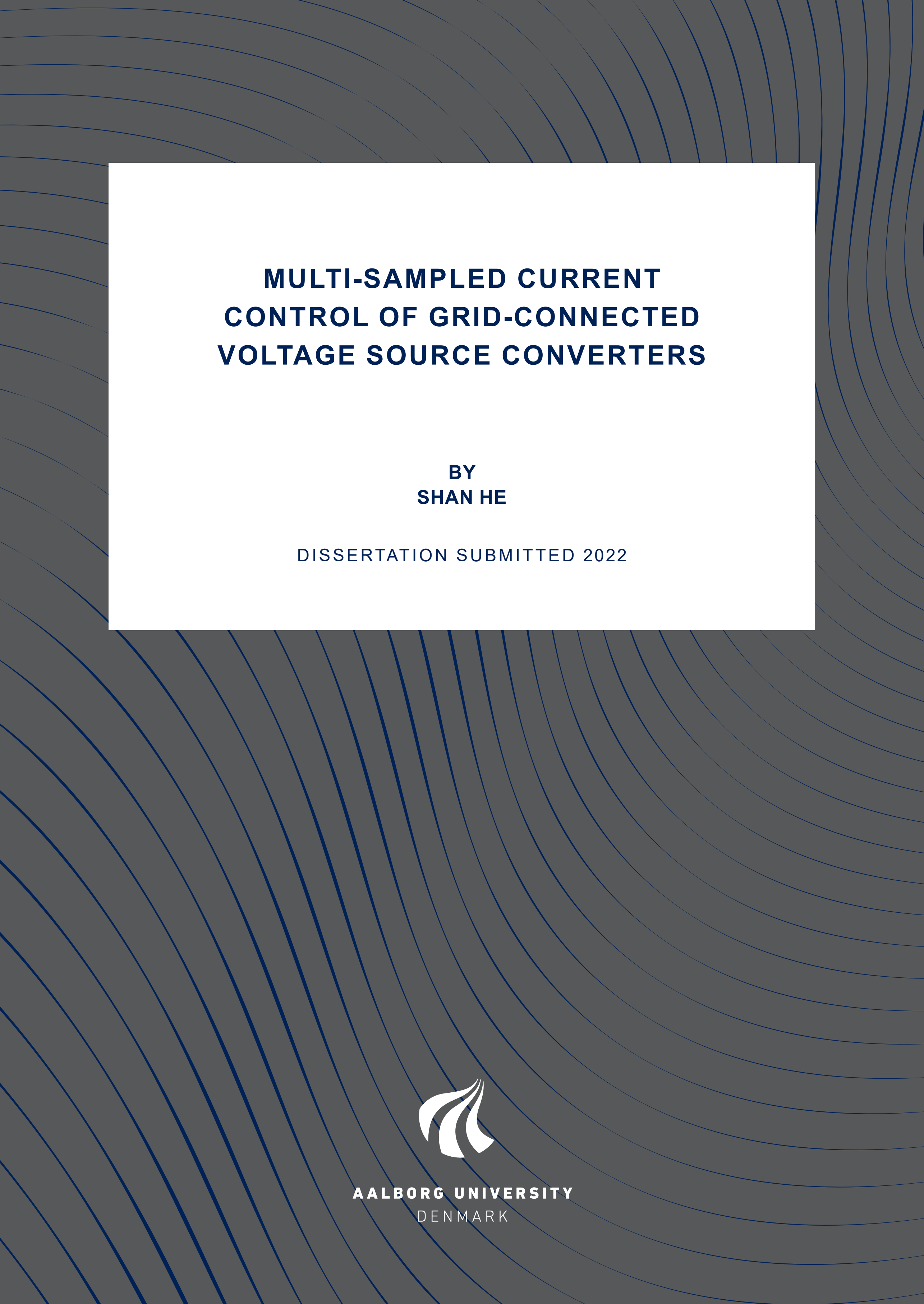

MULTI-SAMPLED CURRENT CONTROL OF GRID-CONNECTED VOLTAGE SOURCE CONVERTERS

BY
SHAN HE

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AALBORG UNIVERSITY
DENMARK

MULTI-SAMPLED CURRENT CONTROL OF GRID-CONNECTED VOLTAGE SOURCE CONVERTERS

by

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CURRICULUM VITAE

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ENGLISH SUMMARY

Grid-connected voltage source converter (VSC) is the key interface between the renewable energy sources and the power grid, and pulse width modulation (PWM) based digital control has been the most commonly used method due to its flexibility, adaptability, and robustness. Especially, the sampling frequency is usually set to one or two times larger than the switching frequency to acquire the average value of voltage/current in VSCs, which are so-called single-sampling or double-sampling control. As the performance/price ratio of microprocessors increased in the past years, multi-sampling control gradually attracts attention where the sampling rate is higher than two. When using multi-sampling, in addition to the average voltage/current value, the switching ripple can also be sampled, which is the key distinction from regular sampling. Hence, how to fully employ the potential benefits from multi-sampling to achieve robust control of grid-connected converters is of interest.

First, a control delay is introduced in the PWM process of the VSCs, which will limit the control bandwidth design and even the stabilization of the VSCs. Multi-sampling PWM can effectively reduce the control delay, however, the internal mechanism of multi-sampling PWM is still not fully investigated. Second, with the large-scale integration of renewable energy sources, the grid admittance varies in a wide range, which may threaten the harmonic stability of the VSC-grid system. Because the control delay is critical to the stability, how to apply the multi-sampling PWM to further enhance the stability is worth to be investigated. Third, to get the most out of multi-sampling technology, the multi-sampled switching ripple can be used to estimate some additional states and parameters in the controlled VSCs. Hence, multi-sampling-based condition monitoring is of interest to be studied.

To cope with the aforementioned issues, this Ph.D. project first graphically analyzes the connection between the multi-sampling PWM and the double-sampling PWM, based on which, the grid-side current will be distorted by the aliased low-order harmonics and the multi-sampled switching ripple is the main reason. Then, the related anti-aliasing filters are proposed to remove the sampled switching ripple while the introduced phase lag is low. Further, how to select the sampling rate for the single-phase H-bridge VSCs and the three-phase interleaved VSCs is discussed.

As an extension of the admittance shaping, the passivity-based control is a promising solution to tackle the instability challenges in the VSC-grid system. Specifically, if the VSC output admittance is passive, the stable operation can be secured regardless of the grid admittance. Based on multi-sampling with anti-aliasing filters, the related passivity-based damping strategies are proposed considering inverter-side current control or grid-side current control. To further optimize the control delay, a multi-sampling-based real-time-update current control is proposed where the anti-aliasing filters are not required.

By utilizing the multi-sampled current data, a grid voltage estimator is proposed, which can help to reduce the cost of voltage sensors and also work as a backup under

a voltage sensor fault. To address the transients during start-up, a soft start-up method is proposed where the VSC is controlled as a boost converter. On the other hand, based on the multi-sampled voltage data, a grid impedance estimator is proposed for a three-phase interleaved VSC under an inductive grid.

The findings of this Ph.D. thesis have improved the application of multi-sampling technology on grid-connected VSCs.

DANSK RESUME

Grid-connected voltage source converter (VSC) er nøglegrænsefladen mellem de vedvarende energikilder og elnettet, og pulsbreddemodulation (PWM) baseret digital kontrol har været den mest almindeligt anvendte metode på grund af dens fleksibilitet, tilpasningsevne og robusthed. Specielt er samplingsfrekvensen normalt indstillet til en eller to gange større end omskiftningsfrekvensen for at opnå den gennemsnitlige værdi af spænding/strøm i VSC'er, som er såkaldt single-sampling eller double-sampling kontrol. Efterhånden som mikroprocessorernes ydeevne/pris-forhold steg i de seneste år, tiltrækker multi-sampling-kontrol gradvist opmærksomhed, hvor samplingsraten er højere end to. Ved brug af multi-sampling kan ud over den gennemsnitlige spænding/strømværdi også samples switching ripple, hvilket er den vigtigste forskel fra almindelig sampling. Derfor er det interessant, hvordan man fuldt ud udnytter de potentielle fordele ved multi-sampling for at opnå robust kontrol af nettilsluttede konvertere.

Først introduceres en kontrolforsinkelse i VSC'ernes PWM-proces, som vil begrænse kontrolbåndbreddedesignet og endda stabiliseringen af VSC'erne. Multi-sampling PWM kan effektivt reducere kontrolforsinkelsen, men den interne mekanisme for multi-sampling PWM er stadig ikke fuldt ud undersøgt. For det andet, med den omfattende integration af vedvarende energikilder, varierer netadgang i et bredt område, hvilket kan true den harmoniske stabilitet af VSC-netsystemet. Fordi kontrolforsinkelsen er kritisk for stabiliteten, er det værd at undersøge, hvordan man anvender multi-sampling PWM for yderligere at forbedre stabiliteten. For det tredje, for at få mest muligt ud af multi-sampling-teknologien, kan den multi-samplede switching ripple bruges til at estimere nogle yderligere tilstande og parametre i de kontrollerede VSC'er. Derfor er multi-sampling-baseret tilstandsovervågning af interesse at blive undersøgt.

For at klare de førnævnte problemstillinger har denne ph.d. Projektet analyserer først grafisk forbindelsen mellem multi-sampling-PWM og dobbelt-sampling-PWM, baseret på hvilken grid-side-strømmen vil blive forvrænget af de aliaserede lavordens harmoniske, og den multi-samplede switching ripple er hovedårsagen. Derefter foreslås de relaterede anti-aliasing-filtre for at fjerne den samplede switch-rippel, mens den indførte faseforsinkelse er lav. Yderligere diskuteres, hvordan man vælger prøvetagningshastigheden for de enkeltfasede H-bro VSC'er og de trefasede interleaved VSC'er.

Som en forlængelse af adgangsudformningen er den passivitetsbaserede kontrol en lovende løsning til at tackle ustabilitetsudfordringerne i VSC-netsystemet. Specifikt, hvis VSC-udgangsadmittansen er passiv, kan den stabile drift sikres uanset netadmittansen. Baseret på multi-sampling med anti-aliasing-filtre foreslås de relaterede passivitetsbaserede dæmpningsstrategier under hensyntagen til strømstyring på invertersiden eller strømstyring på netsiden. For yderligere at optimere kontrolforsinkelsen foreslås en multi-sampling-baseret real-time-opdatering af strømstyring, hvor anti-aliasing-filtre ikke er påkrævet.

Ved at udnytte de multi-samplede strømdata foreslås en netspændingsestimator, som kan hjælpe med at reducere omkostningerne til spændingssensorer og også fungere som backup under en spændingssensorfejl. For at imødegå transienterne under opstart foreslås en blød opstartsmetode, hvor VSC'en styres som en boost-konverter. På den anden side, baseret på de multi-samplede spændingsdata, foreslås en netimpedansestimator for en trefaset interleaved VSC under et induktivt net.

Resultaterne af denne ph.d. afhandling har forbedret anvendelsen af multi-sampling teknologi på nettilsluttede VSC'er.

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Aalborg University, April, 2022

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PART I. REPORT

CHAPTER 1. INTRODUCTION

1.1. BACKGROUND

Electric power system is being modernized with the help of power electronics, which can transform voltages and currents from one level and shape to another [1]. Voltage-source converters (VSCs), as an interface between the AC system and the DC system (see Fig. 1.1), are widely used in renewable energy generation [2], battery energy storage [3], high-voltage direct current (HVDC) transmission [4], transportation electrification [5], and low-voltage distribution network [6], etc. Depending on the power demand, the VSC topologies vary. Three-phase two-level VSC is the most commonly used converter, but the allowed output power is limited by the current rating and the voltage rating of the power semiconductors. Multi-level VSCs are mainly used in the medium-voltage and high-voltage level power conversions [7], such as three-level neutral point clamped VSCs, modular multi-level converters, interleaved parallel VSCs, etc.

In terms of the hardware level of VSCs, raising efficiency and power density are always the primary demands to save energy costs and reduce emissions. These two requirements can be achieved in several ways, e.g., by reducing switching losses in power semiconductors, magnetic integration, and advanced thermal management from layout of printed circuit boards to case enclosure [8-9]. In light of the critical applications and harsh operation environments, reliable operation of VSCs is of necessity to ensure long lifetime and low maintenance cost [10]. In addition, the fast protection of semiconductors should be secured in terms of over-current and over-voltage faults.

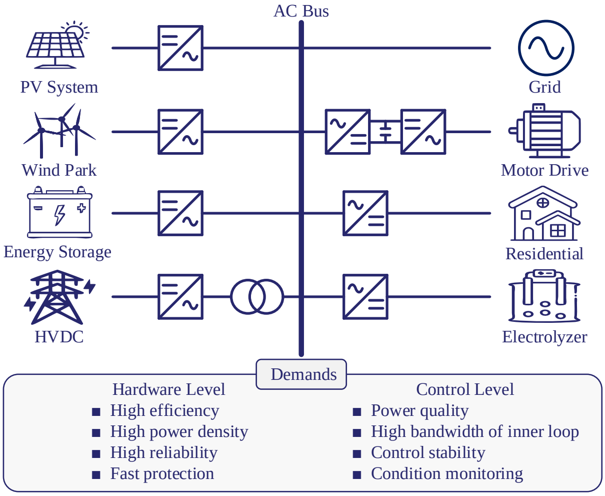

AC Bus
PV System
Grid
Wind Park
Motor Drive
Energy Storage
Residential
HVDC
Electrolyzer
Demands
Hardware Level
■ High efficiency
■ High power density
■ High reliability
■ Fast protection
Control Level
■ Power quality
■ High bandwidth of inner loop
■ Control stability
■ Condition monitoring

Fig. 1.1. Applications and demands of VSCs in power system.

In terms of the control level of VSCs, power quality should be normally guaranteed at a satisfactory level when connected to the grid/load [11]. For instance, a total harmonic distortion for the controlled current should be lower than 5%, which can be achieved through the harmonic suppression control or the hard passive filtering [12]. In addition, the VSCs are usually equipped with multiple control loops with different dynamics, and the high bandwidth of the inner control loop is preferred. On the other hand, the dynamics of the outer loops are usually low to decouple the controller design, which, however, leads to frequency coupling with both the load and grid. Consequently, the VSC system may be unstable with wide-band oscillations, based on which, the accurate modeling and careful controller design are emphasized [13]. To further save the cost and enhance the reliability, advanced condition monitoring may be applied such as motor speed estimation, grid voltage estimation, grid impedance estimation, and fault diagnosis [14-16].

Increasing the integration of renewables has been regarded as a critical pathway to de-carbonize the power system [17-19]. As a bridge between the renewables and the power grid, grid-connected VSCs are of importance to fulfill the above demands. To achieve efficient and reliable power conversion, three basic control loops including the alternating current controller (ACC), dc-link voltage controller (DVC), and phase-locked loop (PLL) are required. Fig. 1.2 shows a typical control structure of a three-phase VSC, where U_g is the grid voltage, U_{pcc} is the point of common coupling (PCC) voltage, U_c is the filter capacitor voltage, U_{dc}^* is the dc-link reference voltage, i_{inv} is the inverter-side current, L_1 is the converter-side filter inductance, L_2 is the grid-side filter inductance, C is the filter capacitance, Z_g represents a grid impedance, respectively. The dq-frame proportional-integral (PI) current control is adopted, where the dc-link voltage U_{dc} is controlled to generate the d-axis current reference i_{invd}^* . PLL is used for the grid synchronization, where the PCC voltage or the filter capacitor voltage is measured to obtain the phase angle θ, which is then used with *abc*/*dq* transformations. The outputs of PI current controllers go through a *dq*/*abc* transformation, generating the modulation signal. The voltage pulse pattern is produced through a pulse width modulation (PWM) process.

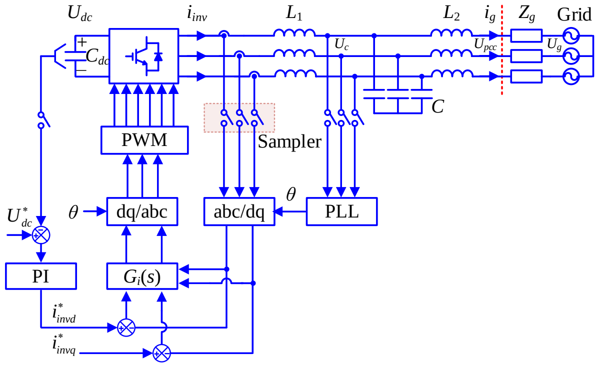


Fig. 1.2. Typical control structure of a three-phase VSC. Source: [J1].

For the controller design, a fast dynamic response is required for ACC, and the bandwidth of ACC is usually set to 1/5 to 1/10 of the switching frequency [20]. In addition, the bandwidth of outer loops such as DVC and PLL should be set to a low value to decouple the dynamics with ACC [21]. Nevertheless, the control delay is inevitable in the PWM process, which limits the bandwidth design of ACC. On the other hand, the passive grid admittance tends to vary in a wide range with the increasing proportion of renewable energy sources, which poses a significant challenge to VSC-grid interactions [22]. Even though the ACC is designed internally stable, the system may still be unstable due to the control delay. According to the impedance-based stability criterion, the VSC control system can be represented as a current source $i_s(s)$ with an output admittance $Y_o(s)$ in parallel (see Fig. 1.3). First, the current source $i_s(s)$ should be stable. Second, the ratio of output admittance to grid admittance should meet the Nyquist criterion. While the first condition can be easily guaranteed through the bandwidth design of ACC, the second is difficult to achieve. Due to the control delay, the phase difference at the intersection point between $Y_o(s)$ and $1/Z_g(s)$ can be easily over 180°, then the VSC-grid system will be not stable [23].

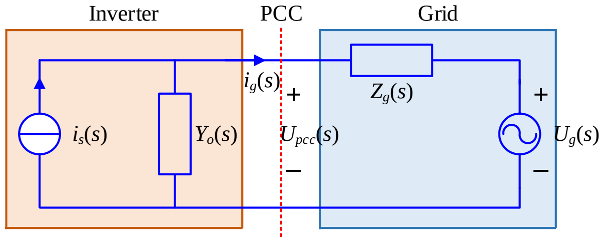
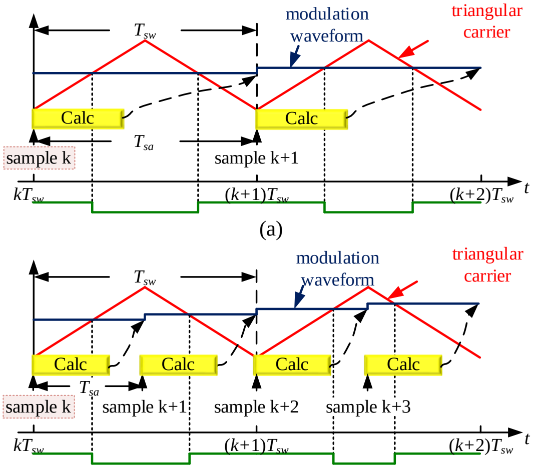

Inverter
PCC
Grid
$i_g(s)$
$Z_g(s)$
+
+
$i_s(s)$
$Y_o(s)$
$U_{pcc}(s)$
$U_g(s)$
−
−

Fig. 1.3. Representation of VSC-grid system.


T_{sw}
modulation waveform
triangular carrier
Calc
Calc
T_{sa}
sample k
sample k+1
kT_{sw}
$(k+1)T_{sw}$
$(k+2)T_{sw}$
t
T_{sw}
modulation waveform
triangular carrier
Calc
Calc
Calc
Calc
T_{sa}
sample k
sample k+1
sample k+2
sample k+3
kT_{sw}
$(k+1)T_{sw}$
$(k+2)T_{sw}$
t

(a)

(b)

Fig. 1.4. Regular PWM in digital control. (a) Single-sampling, (b) Double-sampling. Source: [J2].

Hence, the control delay is crucial in the bandwidth of ACC and the VSC-grid interactive stability. Moreover, the control delay is determined by the sampling methods. For the digital control of VSC, single-sampling and double-sampling PWM are the most used sampling methods. As shown in Fig. 1.4, the sampling period T_{sa} is the same as or half of the switching period T_{sw}. The main advantage of single-sampling and double-sampling is that the average value of current and voltage can be directly obtained without using the anti-aliasing filters [24]. Yet, the control delays for both of sampling methods are $1.5T_{sw}$ and $\frac{1.5T_{sw}}{2}$, which are far away from the critical delay $0.25T_{sw}$ according to passivity-based theory [25]. In order to compensate the control delay, a series of digital filters are proposed but their performance in the high-frequency range is restricted [26].

In the past decades, the cost of high-performance microprocessors has significantly decreased, which promotes the utilization of multi-sampling PWM in reducing the control delay [27]. Fig. 1.5 illustrates the diagram of multi-sampling PWM, where the sampling and the calculation are implemented more than twice. Especially, if the sampling rate is infinite, multi-sampling control will become the analog control [28]. Moreover, the control delay inversely relates to the multi-sampling rate, which can help to overcome the bandwidth limit of the ACC design and to enhance the stability considering the effect of grid impedance [29]. In addition, the linear controllers can be easily transplanted, and only the sampling frequency needs to be increased.

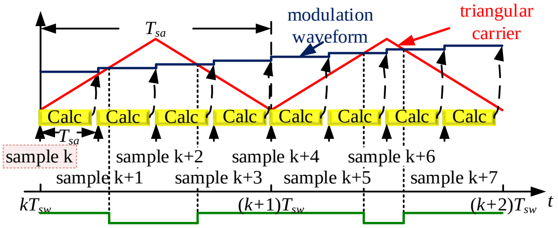


Fig. 1.5. Multi-sampling PWM. Source: [J2].

Yet, compared with single-sampling and double-sampling PWM, the switching harmonics (SHs) are introduced besides the average value. Although several digital methods are proposed in the prior art to deal with the multi-sampled SHs, their effect on the control is still not clear [30]. Further, the duty cycle is updated more than twice during one switching period, but an effective voltage pulse can only be produced by two duty cycles. Hence, the internal mechanism of multi-sampling PWM should be further investigated.

In light of the considerable control delay in single-sampling PWM and double-sampling PWM, several passivity-based current control methods are proposed in the prior art. The main principle is to shape the output admittance of VSC to be passive using active damping, then the VSC system can be always stable regardless of grid admittance [31]. However, the current multi-sampling PWM-based control methods mainly focus on the bandwidth improvement of ACC, and how to utilize the multi-sampling PWM with less control delay to further enhance the passivity is still not widely discussed. Moreover, the design of the passivity-based damping terms should be based on the internal mechanism of multi-sampling PWM.

Besides the bandwidth improvement of ACC and the VSC-grid interactive stability enhancement, the multi-sampled switching ripple can be further used to estimate additional states and parameters in VSCs. Consequently, more information can be acquired to unleash more possibilities for better control performance. However, the current applications of multi-sampling-based estimation mainly focus on the motor drives [32], and few works discuss the grid-connected VSCs.

1.1.1. MULTI-SAMPLING PWM

The control delay T_d for single-sampling and double-sampling PWM is $1.5T_{sa}$, which contains a one-step computation delay and a half-step zero-order-hold delay [33-34]. Note that the expression of control delay for multi-sampling PWM is $\frac{1.5T_{sw}}{N}$ (N is the sampling rate), which can be regarded as an extension of regular sampling PWM [28]. However, the control delay derivation is based on DC-DC converters [35]. For the two-level three-phase VSCs, the internal mechanism of delay reduction remains unclear. Moreover, the effect of the sampled SHs on the control system is still not thoroughly discussed, which makes it difficult to design the related sampled SHs suppression methods.

The four-sampling PWM is recommended in the control of single-phase VSCs [36]. It can be seen in Fig. 1.6 that the apparent switching frequency is twice as large as the carrier frequency with unipolar modulation. Hence, the average current can be sampled at the intersection points and the peak/valley of the carrier. Fig. 1.7 gives a comparison when using different sampling rates. Herein, the carrier frequency is set as 2 kHz, and the apparent switching frequency is 4 kHz. When the sampling rate is larger than four such as sixteen, the SHs around multiple switching frequencies are introduced. More generally, the noise-free sampling rate can be set to $4M$ for the cascaded H-bridge VSCs with M cells [37].

It seems that multi-sampling technology is more suitable for multi-level VSCs, and the SHs will not be sampled by setting a proper sampling rate. However, the ability of multi-sampling PWM to control delay reduction will be constrained. Moreover, interleaved VSCs are another kind of commonly used multi-level VSCs, where the switching cells are connected in parallel instead of in series like the cascaded H-bridge VSCs [38]. Unfortunately, the multi-sampling PWM is still not widely applied in interleaved VSCs. Therefore, the selection of multi-sampling rate for multi-level VSCs is of importance to be further studied, and the prerequisite is that the multi-sampling PWM in two-level three-phase VSCs should be fully understood.

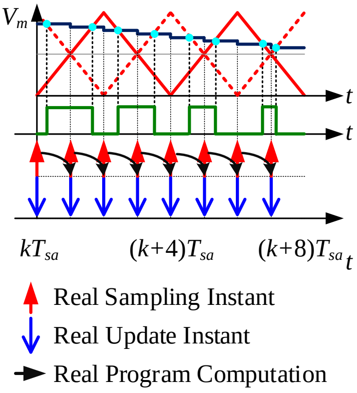
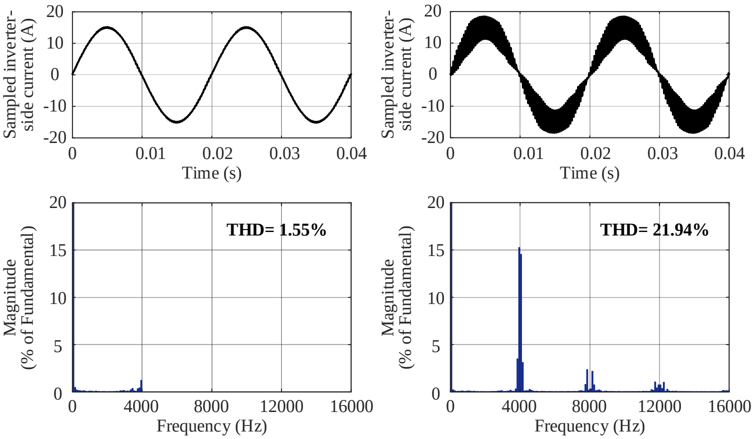


Fig. 1.6. Four-sampling PWM for a single-phase VSC (Blue: modulation signal, Red: carrier). Source: [J1].



(a) (b)

Fig. 1.7. Sampled inverter-side current for a single-phase VSC (f_{sw}=2 kHz). (a) Four-sampling (f_{sa}=8 kHz), (b) Sixteen-sampling (f_{sa}=32 kHz). Source: [J3].

1.1.2. PASSIVITY BASED CURRENT CONTROL

As an extension of the admittance shaping, the passivity-based current control is a promising solution to tackle the VSC-grid interactive instability challenges. Similar to the impedance-based criterion, the first condition to achieve passivity is that the ACC should be stable. The second condition is stricter, i.e., the output admittance should be passive for all frequencies. Specifically, the phase characteristic of VSC output admittance $Y_o(s)$ in Fig. 1.3 will be within $[-90^\circ, 90^\circ]$, which is the same as resistors, inductors, capacitors, or a combination. Consequently, the phase difference can be always below 180° at the intersection point between the VSC output admittance and the grid admittance, and the system stable operation can be secured regardless of the grid admittance [31]. The first condition can be easily guaranteed by setting the bandwidth of ACC. However, the second condition is hard to achieve due to the control delay, and the passivity goal is compromised to Nyquist frequency.

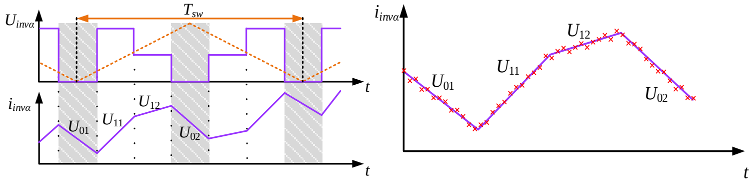
LCL filters are commonly used in grid-connected VSCs to reduce the volume of the required inductors and improve the power quality, which, however, leads to the quite different non-dissipative regions according to the current sampling position. When the control target is converter-side current, the non-dissipative region for the VSC output admittance is between the critical frequency ($\frac{1}{4T_d}$) and the Nyquist frequency. Hence, control delay compensation can help to shrink the non-dissipative region and enhance the passivity [25]. Another passivity enhancement route is to add extra damping terms such as filter capacitor current damping, filter capacitor voltage damping, PCC voltage damping, etc [39].

When the control target is grid-side current, the non-dissipative region for the VSC output admittance is between the anti-resonant frequency ($\frac{1}{2\pi}\sqrt{\frac{1}{L_1 C}}$) and critical frequency ($\frac{1}{4T_d}$) [40]. In contrast with the converter-side current control, the passivity is threatened by control delay reduction, and the extra damping terms are mandatory. Similar to the converter-side current control, several passivity-based current control methods using filter capacitor current damping, filter capacitor voltage damping, and PCC voltage damping have been proposed in [41-44], but only the regular sampling PWM is considered.

The current applications of multi-sampling PWM mainly focus on the bandwidth and the internal stability improvement, and the discussion of VSC-grid interactive stability is rare. Hence, how to utilize multi-sampling PWM with reduced control delay to update the previous passivity-based control methods and further enhance the stability robustness needs to be further explored.

1.1.3. CONDITION MONITORING

The multi-sampling technology not only reduces the control delay, but also additional states and parameters can be predicted using multi-sampled data. Up till now, there are two applications in VSCs including current slope estimation and grid impedance estimation. Fig. 1.8 shows a three-phase PWM, and the current slope can be estimated by utilizing the sampled current data during the active vectors (U_{11} and U_{12}) or the zero vectors (U_{01} and U_{02}) [45-46]. Based on the estimated current slope, several states and parameters in the field of motor drives can be further estimated such as motor speed, motor inductance open-circuit fault detection, and dead-time compensation [47-50].



(a) (b)

Fig. 1.8. Voltage vectors and currents for a three-phase PWM. (a) $U_{inv\alpha}$ and $i_{inv\alpha}$ within a switching period, (b) Estimated current slope. Source: [J4].

As discussed before, the grid impedance plays a key role in the VSC-grid interactive stability. Besides the passivity-based control, grid impedance estimation is also a promising candidate. Then the control parameters can be adjusted online to shape the output admittance and maintain the stable operation of VSCs. By using the four-sampled current and voltage, as shown in Fig. 1.9, the grid impedance is estimated for a two-level three-phase VSC [51]. Similarly, by only using the four-sampled PCC voltage, the grid impedance estimation is achieved for a single-phase VSC [52]. Considering the prior art of multi-sampling-based estimation, there are still a lot of possibilities to estimate more parameters and states and to achieve a better control performance, especially for the grid-connected VSCs.

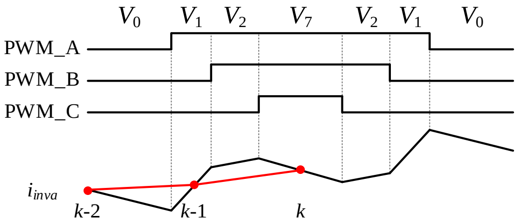


Fig. 1.9. Measurement instants for grid impedance estimation. Source: [J1].

1.2. PROJECT OBJECTIVES AND LIMITATIONS

1.2.1. PROJECT OBJECTIVES

The overall goal of this project is to exploit the multi-sampling technology in grid-connected VSCs. The main hypothesis is summarized as follows:

- **Can multi-sampling technique improve the robustness of grid-connected VSCs?**

Guided by this hypothesis, the following research questions are pursued:

- Q1: What is the internal mechanism of multi-sampling PWM in VSCs?
- Q2: How to enhance the passivity for VSCs using multi-sampling PWM?
- Q3: How to utilize multi-sampling for condition monitoring in VSCs?

Aiming to address the abovementioned research questions, three research objectives are listed as follows:

- O1: Reveal the internal mechanism of multi-sampling PWM for two-level and multi-level VSCs

The effect of different anti-aliasing filters on the sampled SHs and control performance needs to be investigated. Moreover, the control delay reduction for multi-sampling PWM in VSCs needs to be identified, based on which, the detailed implementation in the two-level and multi-level VSCs will be discussed as well.

- O2: Develop multi-sampling control strategies to enhance the passivity of the current control of VSCs

The passivity characteristic for the single/double-sampled ACC of VSCs will be investigated first. Based on the reduced control delay, the multi-sampling control strategies will be developed to further enhance the passivity when sampling the VSC-side current or the grid-side current, respectively. In addition, the robustness to the filter parameter fluctuations will be researched as well.

- O3: Estimate more states and parameters in VSCs using the multi-sampled current/voltage switching ripple

Based on the equivalent circuit of VSCs, the utilization of multi-sampled switching ripple will be investigated to estimate the crucial states and parameters such as grid voltage estimation, grid impedance estimation, fault diagnosis, passive filter parameters estimation, etc.

1.2.2. PROJECT LIMITATIONS

This Ph.D. project has the following limitations:

- The analysis of multi-sampling PWM is based on the voltage-balance equivalence, which still lacks strict mathematic deduction. Moreover, the non-linear phenomenon in the multi-sampling PWM such as vertical crossing and multiple switching are ignored.
- In the passivity-based current control, the side band effect close to the switching frequency is ignored in the PWM model. Additionally, the effect of outer loops on the stability in the low-frequency range is ignored.
- For the grid-voltage estimation, the effect of sampling noise on the estimation accuracy is not considered. Also, the stability robustness to the VSC-side inductor saturation and grid impedance variation is not considered.
- In the experimental validation, the VSC is connected to a grid emulator instead of the real power grid. In addition, the dc-side is not connected to a real solar panel or a wind turbine. Hence, the feasibility and reliability of the proposed control methods in this Ph.D. project require more field tests.

1.3. THESIS OUTLINE

This Ph.D. project's outcomes are documented in the form of a paper-based Ph.D. thesis, containing a ***Report*** and a collection of the ***Selected Publications*** throughout the entire study. The thesis structure is shown in Fig. 1.10 to illustrate how to connect the content in the ***Report*** to the ***Selected Publications***.

There are eight chapters in the ***Report***. The research background and motivation of the Ph.D. project are introduced in ***Chapter 1***. ***Chapter 2*** analyzes the mechanism of multi-sampling PWM and aliasing, and an improved repetitive filter is proposed to suppress the aliasing having a small phase lag. To enhance the passivity of ACC, a damping strategy controlling converter-side current is proposed in ***Chapter 3***, and the robustness against the filter parameter deviation is also discussed. In addition, the proposed method is extended to the single-phase VSCs. Similarly, a passivity-based damping strategy controlling grid-side current is proposed in ***Chapter 4***, where the robustness to the filter parameter deviation and the transient performance during start-up are enhanced. To further reduce the control delay, an enhanced real-time-update current control method is developed in ***Chapter 5***, and the dissipation below Nyquist switching frequency can be achieved only using single-loop converter-side current control. ***Chapter 6*** focuses on the multi-sampled current control of three-phase interleaved VSCs, and the sampling rate selection and the control parameter design are discussed. Moreover, based on the multi-sampled PCC voltage, the grid impedance is estimated under a pure inductive grid. ***Chapter 7*** proposes a grid voltage estimator while using multi-sampled current control, based on which, the sensor cost might be saved and the voltage sensor fault can be prevented. Finally, ***Chapter 8*** concludes this Ph.D. project and suggests future trends.

1.4. LIST OF PUBLICATIONS

The outcomes of during Ph.D. study have been submitted/published in the form of journal papers and conference papers, as indicated below. Parts of these publications are used in the Ph.D. dissertation (***Report***), which are also listed in Fig. 1.10.

Journal Papers:

[J1] **S. He**, D. Zhou, X. Wang, Z. Zhao, and F. Blaabjerg, "A review of multi-sampling techniques in power electronics applications," *IEEE Trans. Power Electron., early access,* 2022.

[J2] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Aliasing suppression of multi-sampled current controlled LCL-filtered inverters," *IEEE Trans. Journal Emerg. Sel. Topics Power Electron*., vol. 10, no. 2, pp. 2411-2423, April 2022.

[J3] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Passivity based multi-sampled current control of LCL-filtered grid-connected inverters," *IEEE Trans. Power Electron.*, 2022 (Second-round revision).

[J4] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Line voltage sensorless control of grid-connected inverters using multisampling," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4792-4803, April 2022.

Conference Papers:

[C1] **S. He**, Z. Yang, D. Zhou, X. Wang, F. Blaabjerg, and Rik De Doncker, "Robust passivity enhancement for LCL-filtered grid-following inverters with multi-sampled grid-side current control", in *Proc. IEEE ECCE*, 2022 (Accepted).

[C2] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Switching harmonics suppression of single-loop multi-sampling control of grid-connected inverter", in *Proc. IEEE IECON*, pp. 3259-3264, 2020.

[C3] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Enhanced real-time-update current control for grid-following inverters," in *Proc. IEEE PEDG.*, 2022 (Accepted).

[C4] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Multisampling control of two-cell interleaved three-phase grid-connected converters", in *Proc. IEEE APEC*, pp. 590-594, 2021.

[C5] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Multisampling based grid impedance estimation for two-cell interleaved three-phase inverters", in *Proc. IEEE ECCE*, pp. 1432-1437, 2021.

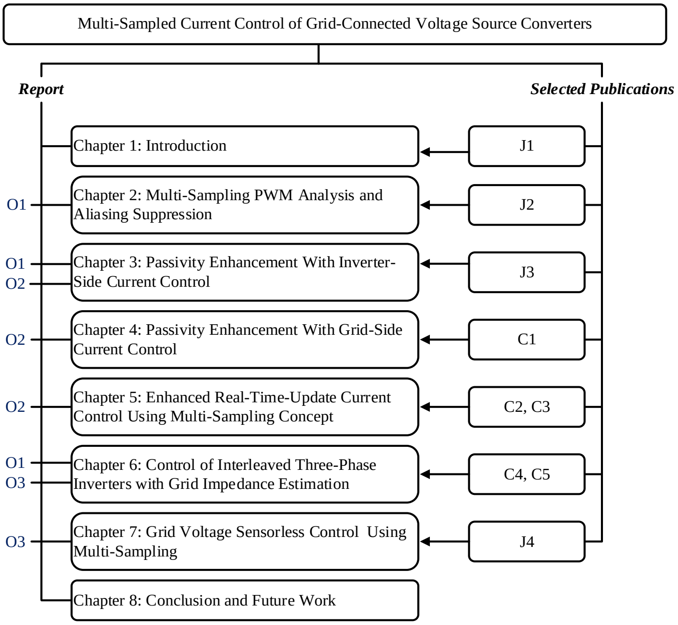

Multi-Sampled Current Control of Grid-Connected Voltage Source Converters
Report
Selected Publications
Chapter 1: Introduction
J1
O1
Chapter 2: Multi-Sampling PWM Analysis and Aliasing Suppression
J2
O1
O2
Chapter 3: Passivity Enhancement With Inverter-Side Current Control
J3
O2
Chapter 4: Passivity Enhancement With Grid-Side Current Control
C1
O2
Chapter 5: Enhanced Real-Time-Update Current Control Using Multi-Sampling Concept
C2, C3
O1
O3
Chapter 6: Control of Interleaved Three-Phase Inverters with Grid Impedance Estimation
C4, C5
O3
Chapter 7: Grid Voltage Sensorless Control Using Multi-Sampling
J4
Chapter 8: Conclusion and Future Work

Fig. 1.10. Thesis structure with related topics and research outcomes for each chapter; where "O" denotes objective, while "J" and "C" refer to a journal or conference publication, respectively.

Other publications not included in the Ph.D. thesis:

[OP1] **S. He**, X. Sui, Z. Liu, M. Kang, D. Zhou and F. Blaabjerg, "Torque ripple minimization of a five-phase induction motor under open-phase faults using symmetrical components," *IEEE Access*, vol. 8, pp. 114675-114691, June 2020.

[OP2] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Overview of multisampling techniques in power electronics converters", in *Proc. IEEE IECON*, pp. 1922-1927, 2019.

[OP3] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Switching harmonics suppression of single-loop multi-sampling control of grid-connected inverter", in *Proc. IEEE IECON*, pp. 3259-3264, 2020.

[OP4] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Grid voltage sensorless control of three-phase LCL grid-connected inverters using multisampled current", in *Proc. IEEE ECCE Asia*, pp. 2002-2006, 2020.

[OP5] **S. He**, Y. Pan, D. Zhou, X. Wang, and F. Blaabjerg, "Current harmonic analysis of multisampled LCL type grid-connected inverter", in *Proc. IEEE ECCE*, pp. 4329-4335, 2020.

[OP6] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Multisampling control of LCL-type grid connected inverter with an improved repetitive filter", in *Proc. IEEE ECCE*, pp. 4336-4341, 2020.

[OP7] **S. He**, Z. Yang, D. Zhou, X. Wang, F. Blaabjerg, and Rik De Doncker, "Low-frequency stability enhancement for LCL-Type grid-following inverters with multi-sampled current control", in *Proc. IEEE ECCE*, 2022 (Accepted).

[OP8] **S. He**, X. Sui, and F. Blaabjerg, "Comparative study of different fault-tolerant control strategies for a five-phase concentrated-full-pitch winding induction motor," in *Proc. IEEE ECCE Europe*, pp. P.1-P.10, 2019.

[OP9] **S. He**, X. Sui, D. Zhou and F. Blaabjerg, "Torque ripple minimization of seven-phase induction motor under more-than-two-phase fault," in *Proc. IEEE ICEM*, pp. 2222-2228, 2020.

[OP10] **S. He**, X. Sui, D. Zhou, and F. Blaabjerg, "Zero torque ripple operation of seven-phase concentrated-full-pitch winding induction motor under open circuit faults," in *Proc. IEEE ISIE*, pp. 380-385, 2020.

[OP11] **S. He**, X. Sui, D. Zhou, and F. Blaabjerg, "Torque ripple suppression of a five-phase induction motor under single-phase open", in *Proc. IEEE ECCE Asia*, 2020.

[OP12] Z. Liu.; P. Zhang, **S. He**, J. Huang, "A review of modeling and diagnostic techniques for eccentricity fault in electric machines," *Energies*, vol. 14, no. 6, pp. 4296, July 2021.

[OP13] Z. Li, F. Zhao, X. Wang, **S. He**, S.-M. Nielsen, "Multi-sampling with real-time update PWM for time-delay minimization of FPGA-based voltage controlled converters," in *Proc. IEEE APEC*, 2022. (Accepted).

CHAPTER 2. MULTI-SAMPLING PWM ANALYSIS AND ALIASING SUPPRESSION

2.1. BACKGROUND

In the implementation of multi-sampling PWM, the effect of sampled SHs on the control is still not fully discussed, and the internal mechanism of multi-sampling PWM is also not clear. Prior-art studies mainly focused on the multi-sampled SHs suppression and four strategies have been proposed as follows.

First, by using the first-order hold sampler, the modulation signal has more continuity but the small-signal model needs further analysis [53-54]. Second, the saw-tooth carrier is added to the feedback loop to counteract the switching noise, however, the triangle carrier is more general in DC-AC converters and the compensation method cannot be utilized directly [55-56]. Third, the grid-side current and the filter capacitor voltage are preferred since they contain less switching noise [57-58]. Fourth, Moving average filter (MAF) can effectively suppress the sampled SHs, but the introduced phase lag is large [59-61]. The phase lag for the simplified repetitive filter (SRF) is low, but only the odd-order SHs can be filtered out [30].

In this chapter, the multi-sampling PWM is transformed into a double-sampling PWM based on the voltage-second equivalence. Then, the Nyquist frequency for multi-sampling PWM is the same as the Nyquist frequency of double-sampling control. Then, the aliasing in the grid-side currents can be explained as the non-average value of current is sampled for the control. To suppress the aliasing, as shown in Fig. 2.1, an improved repetitive filter (IRF) is presented to suppress the sampled SHs while the phase lag is low.

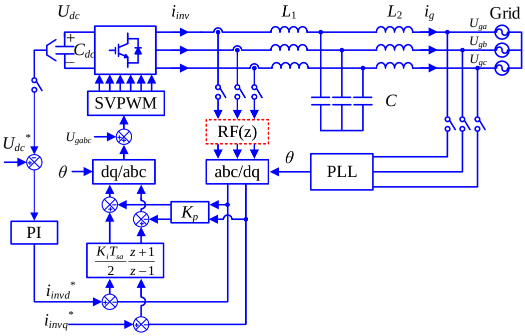
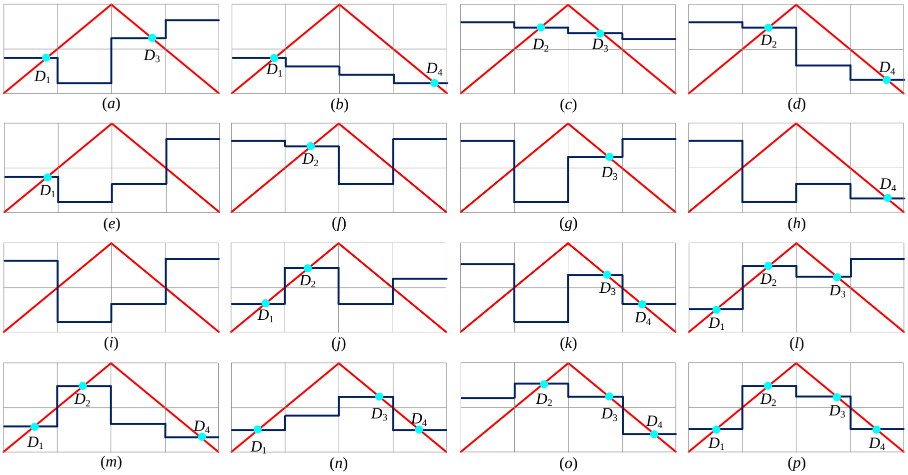


Fig. 2.1. Single-loop multi-sampling control with inverter-side current feedback (RF: repetitive filter). Source: [J2].

2.2. ALIASING ANALYSIS FOR MULTI-SAMPLING PWM

2.2.1. FOUR-SAMPLING PWM

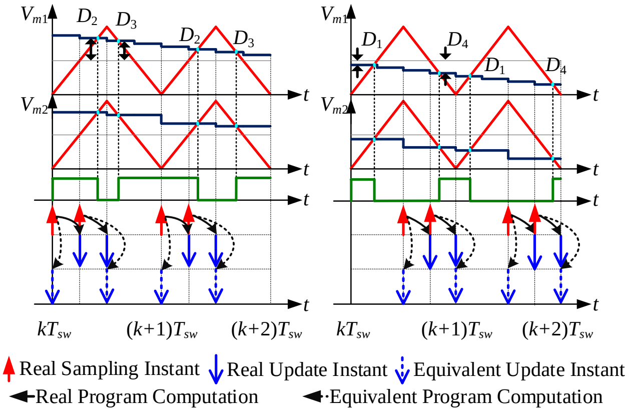
The analysis begins with the most basic multi-sampling PWM, i.e., four-sampling PWM, as seen in Fig. 2.2. According to the probability theory, there are 2^4 possible intersection cases, and the amplitude of the duty cycle determines the intersection position. Fig. 2.2(*l*)-(*p*) shows one non-linear phenomenon called multi-intersection, where the power semiconductor is triggered more than two times during one switching period and the switching loss will increase. One solution is to restrict the slew rate of the reference to be lower than the carrier [62-63], the ‘‘self-lock’’ logic from the microprocessor can be also utilized to prevent multi-switching [64]. Fig. 2.2(*e*)-(*i*) shows the vertical crossing phenomenon, and only one duty cycle or no duty cycles can produce the effective voltage pulse. When the vertical crossing happens, the PWM is forced to output pull-up and pull-down [64]. Similarly, the cases in Fig. 2.2(*j*)-(*k*) can be also ignored because they are a combination of multi-switching and vertical crossing. In addition, the cases in Fig. 2.2(*a*) and (*d*) should be disregarded since they only occur when the modulation wave crosses 0.5.



(*a*) (*b*) (*c*) (*d*)
(*e*) (*f*) (*g*) (*h*)
(*i*) (*j*) (*k*) (*l*)
(*m*) (*n*) (*o*) (*p*)

Fig. 2.2. Intersection analysis for four-sampling PWM (Blue: modulation signal, Red: carrier). Source: [J2].

Consequently, we mainly consider the cases in Fig. 2.2(b) and (c), where the modulation signal is positive or negative, respectively. Considering the positive half cycle in Fig. 2.3(a), the effective duty cycles are D_2 and D_3. According to the voltage-second equivalence, the computation delay is zero for D_2 and the computational delay for D_3 is $0.25T_{sw}$.[75]. Hence, the average computational delay during one switching period is $(0.25+0)/2=0.125T_{sw}$. Combined with the double-sampling PWM delay $0.25T_{sw}$, the total control delay is in line with $1.5T_{sw}/N$ [5], which verifies the feasibility of the equivalence method. Further, since the non-average value of current is sampled for the calculation of D_3, the aliasing will be introduced in the grid-side current [68-69]. The analysis in the negative half cycle is similar, which is not further discussed herein.



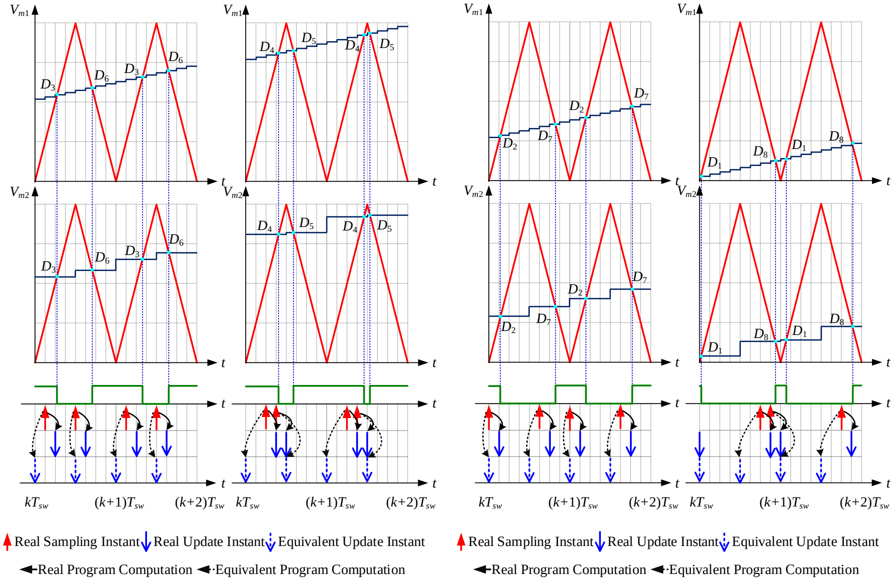
(a) (b)

Fig. 2.3. The mechanism analysis for four-sampling PWM. (a) Positive half cycle of modulation signal, (b) Negative half cycle of modulation signal. Source: [J2].

2.2.2. EIGHT-SAMPLING PWM

Four duty cycle ranges are determined based on the geometric relationship between the modulation signal and the carrier, i.e., (0, 0.25), (0.25, 0.5), (0.5, 0.75), (0.75, 1). Then there are 4^8 intersection cases, only four cases are considered in order to simplify the analysis, as given in Fig. 2.4. When the amplitude of the modulation signal is from 0.5 to 0.75 (see Fig. 2.4(a)), D_3 and D_6 are the effective duty cycles. Based on the voltage-second equivalence, the computation delay for D_3 is $-0.125T_{sw}$ which functions as a phase-leading, and the computation delay for duty cycle D_6 is zero. Combined with the double-sampling PWM delay $0.25T_{sw}$, the total control delay is again in line with $1.5T_{sw}/N$ [5]. Moreover, the aliasing also exists since the non-average value is used for the calculation of effective duty cycles. The same conclusion can be obtained for the other three cases in Fig. 2.4.

To summarize, multi-sampling PWM is essentially a double-sampling PWM, and the equivalent Nyquist frequency is the same as the switching frequency. Especially, the computation delay for the effective duty cycles can be optimized to zero even a minus value, thereby the total control delay can be effectively reduced. Note that the sampled non-average value will introduce low-order aliased harmonics, and filtering the sampled SHs can help to suppress the aliasing.


V_{m1}
V_{m2}
D_3
D_6
D_4
D_5
D_2
D_7
D_1
D_8
t
kT_{sw}
$(k+1)T_{sw}$
$(k+2)T_{sw}$
Real Sampling Instant
Real Update Instant
Equivalent Update Instant
Real Program Computation
Equivalent Program Computation

(a) (b)

Fig. 2.4. The mechanism analysis for eight-sampling PWM. (a) Positive half cycle of modulation signal, (b) Negative half cycle of modulation signal (Blue: modulation signal, Red: carrier). Source: [J2].

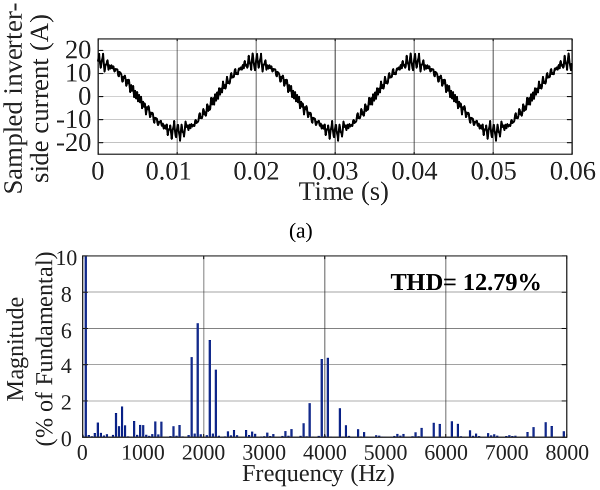
2.3. IMPROVED REPETITIVE FILTER

Fig. 2.1 shows a diagram of single-loop current control. When using multi-sampled current control, the bandwidth can be higher than the regular sampling, but the overshoot will be large when using a PI controller. Hence, the pseudo-derivative-feedback (PDF) controller is selected to suppress the overshoot and improve the dynamics at the same time [65-66]. The parameters for the used three-phase inverter are shown in Table 2.1. It can be seen from Fig. 2.5 that the high-frequency SHs in the eight-sampled inverter-side current (rated value) are located around odd-order and even-order switching frequencies. An SRF is used to filter the sampled SHs [30] which is given as

$$SRF(z) = \frac{1}{2}(1 + z^{-N/2}) \tag{2.1}$$

It can be seen from Fig. 2.6 and Fig. 2.7 that SRF for eight-sampling is only effective around odd-order switching frequencies. On the other hand, the RF in the multi-sampling control of the DC-DC converter is shown in (2.2), but it can only remove the sampled SHs at the integer switching frequency (see Fig. 2.6) [30].

$$RF(z) = \frac{(1+0.25)(1-(z^{-N}-\frac{1}{N}\sum_{n=1}^{N} z^{-n}))}{1-(z^{-N}-\frac{1}{N}\sum_{n=1}^{N} z^{-n})+0.25} \tag{2.2}$$



(a)

(b)

Fig. 2.5. The eight-sampled inverter-side current without anti-aliasing filters. (a) Sampled inverter-side current waveform, (b) Current spectrum. Source: [J2].

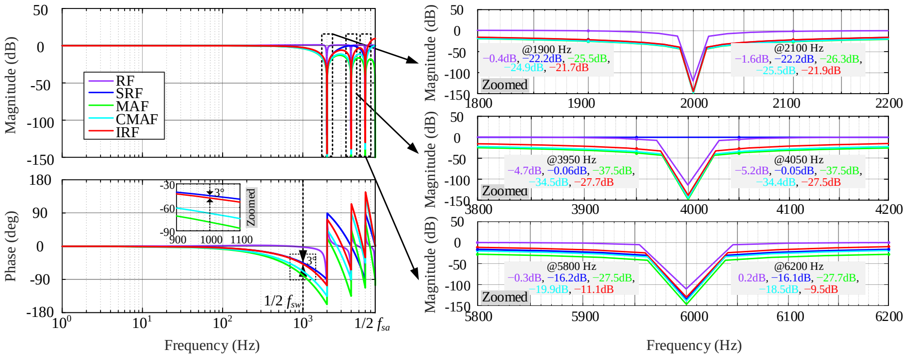
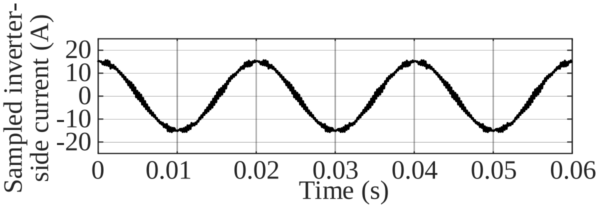
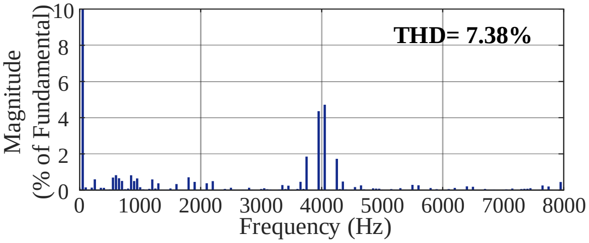


Fig. 2.6. The bode diagram of the repetitive filters using eight-sampling (RF: repetitive filter, SRF: simplified repetitive filter, MAF: moving average filter, CMAF: compromised moving averaging filter, IRF: improved repetitive filter). Source: [J2].



(a)



(b)

Fig. 2.7. The eight-sampled inverter-side current with a simplified repetitive filter. (a) Sampled inverter-side current waveform, (b) Current spectrum. Source: [J2].

MAF can effectively remove the sampled SHs (see (2.3)), but an extra $T_{sw}/2$ delay is introduced [61]. To obtain a good filtering ability and a low delay, a compromised moving average filter (CMAF) is proposed. Compared with MAF, CMAF reduces the window width from T_{sw} to $T_{sw}/2$, as given in (2.4). Then a linear delay compensation block in [67] is used to further optimize the delay, i.e., improved repetitive filter (IRF), as given in (2.5) [67].

$$MAF(z)=\frac{1}{N}\sum_{k=0}^{N-1}z^{-k} \tag{2.3}$$

$$CMAF(z)=\frac{2}{N}(1+z^{-2}+z^{-4}+\cdots z^{-(N-2)}) \tag{2.4}$$

$$IRF(z)=\frac{2}{N}(1+z^{-2}+z^{-4}+...z^{-(N-2)})\times(3\log_2 N-7-(3\log_2 N-8)z^{-1}) \tag{2.5}$$

When using eight-sampling PWM, the IRF is given as

$$IRF(z)_{N=8}=\frac{1}{4}(1+z^{-2}+z^{-4}+z^{-6})(2-z^{-1}) \tag{2.6}$$

It can be observed from Fig. 2.8 that not all the SHs can be suppressed when using IRF, but also the introduced phase lag is similar with SRF according to Fig. 2.6. The model of the single-loop current control is presented in Fig. 2.9, and the open-loop transfer function of the inner current loop is given in (2.7)-(2.10).

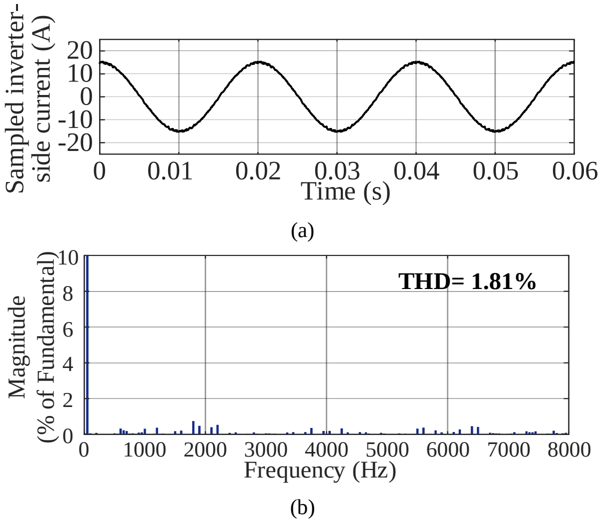
$$T_{oin}(s)=K_p IRF(s)G_d(s)G_{i1v}(s) \tag{2.7}$$

$$G_{i1v}(s)=\frac{L_2Cs^2+1}{L_1L_2Cs^3+(L_1+L_2)s} \tag{2.8}$$

$$IRF(s)=\frac{1-e^{-8sT_{sa}}}{1-e^{-2sT_{sa}}}(\frac{1}{2}-\frac{1}{4}e^{-sT_{sa}}) \tag{2.9}$$

$$G_d(s)=e^{-1.5sT_{sa}} \tag{2.10}$$

The bode diagram using double-sampling and eight-sampling is given in Fig. 2.10. When the bandwidth is set to 100 Hz using double-sampling, the phase margin (PM) is only 12.8° (PM_1). When using eight-sampling, the bandwidth can be set to 200 Hz and the PMs using SRF and IRF are 36.2° (PM_2) and 34.6° (PM_3). Therefore, a high-bandwidth multi-sampled ACC can be achieved with the proposed IRF, and the aliasing is suppressed at the same time.



(a)

(b)

Fig. 2.8. The eight-sampled inverter-side current with an improved repetitive filter. (a) Sampled inverter-side current waveform, (b) Current spectrum. Source: [J2].

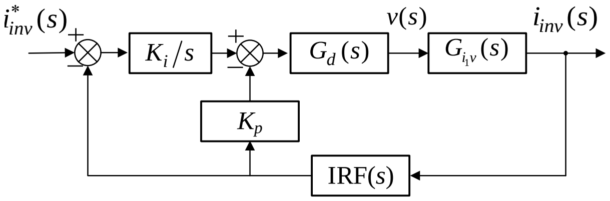


Fig. 2.9. Model of the single-loop inverter-side current control using multi-sampling. Source: [J2].

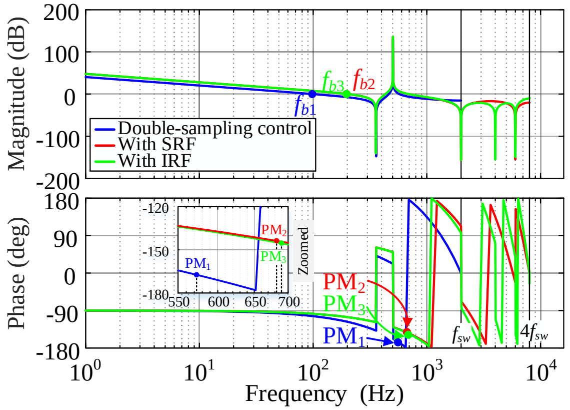


Fig. 2.10. Bode diagram of the inner loop using double-sampling and eight-sampling (SRF: simplified repetitive filter, IRF: improved repetitive filter). Source: [J2].

TABLE 2.1. Main parameters of a grid-connected VSC. Source: [J2].

Symbol	Description	Value	Symbol	Description	Value
U_{grms}	Grid voltage	220 V	P_o	Output power	7 kW
L_1	Inverter-side inductance	5 mH	L_2	Grid-side inductance	5 mH
C	Filter capacitance	40 μF	C_{dc}	DC-link capacitance	297 μF
f_r	Resonance frequency	503 Hz	U_{dc}	DC-link voltage	600 V
f_{sw}	Switching frequency	2 kHz	T_f	DC-link filter time constant	1 ms
K_{p8}	Proportional gain (N=2)	15.6	K_{i8}	Integral gain (N=2)	5050
K_{p2}	Proportional gain (N=8)	6.6	K_{i2}	Integral gain (N=8)	600
K_{pdc}	Proportional gain	0.03	K_{idc}	Integral gain	0.4

2.4. CASE STUDIES

To validate the proposed method, experiments are implemented in a VSC system from Imperix, as shown in Fig. 2.11. The power rack includes eight half-bridge PEB-8024 modules, which can be assembled flexibly to achieve various types of converters. Herein, a three-phase two-level VSC is used, and the B-Box RCP is a rapid prototyping controller system with programmable DSP and FPGA. The current THD is measured through the Newtons-4th PPA5530 power analyzer. The experimental parameters for the setup can be seen in Table 2.1.

It can be seen from Fig. 2.12 that the grid-side current THD is 1.01% when using double-sampling, but the dynamic performance is slow due to the considerable control delay. Although the eight-sampling control can achieve a faster dynamic performance (see Fig. 2.13), the grid-side current is distorted due to the aliasing. As shown in Fig. 2.14, SRF can partly remove the sampled SHs and the aliasing still exists. Fig. 2.15 illustrates that all the SHs are removed when using the proposed IRF, thereby the current THD is 1.10% which is close to the double-sampling control.

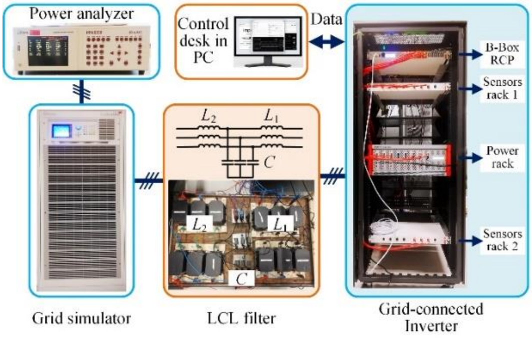
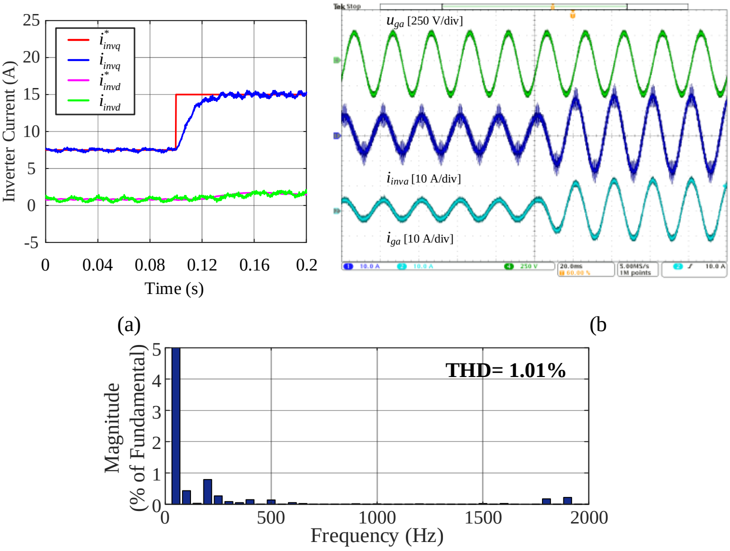


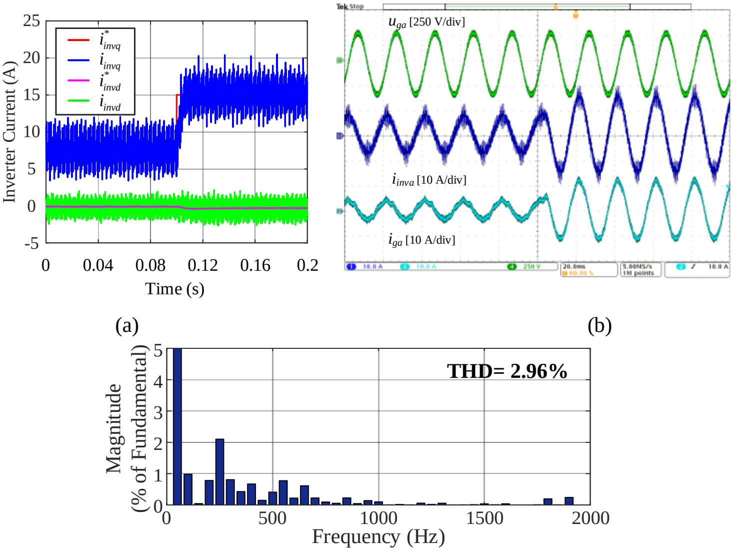
Fig. 2.11. Three-phase grid-connected VSC prototype. Source: [J2].



(a) (b

(c)

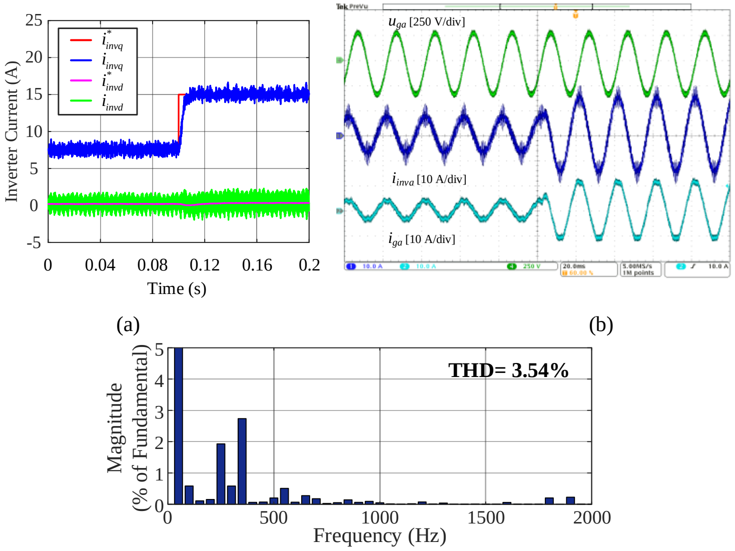
Fig. 2.12. Experimental results when using double-sampling control. (a) Step response, (b) Analogue inverter-side and grid-side current, (c) THD of analog grid-side current. Source: [J2].



(a) (b)

(c)

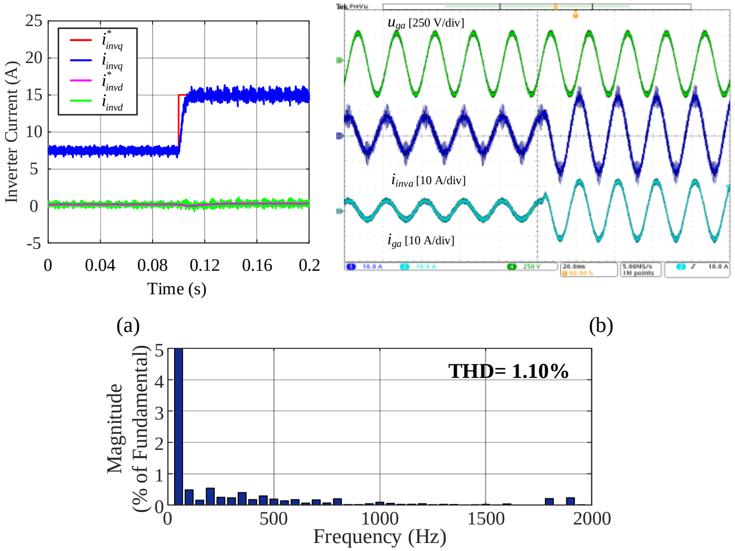
Fig. 2.13. Experimental results when using eight-sampling control without anti-aliasing filters. (a) Step response, (b) Analogue inverter-side and grid-side current, (c) THD of analog grid-side current. Source: [J2].



(a) (b)

(c)

Fig. 2.14. Experimental results when using eight-sampling control with a simplified repetitive filter. (a) Step response, (b) Analogue inverter-side and grid-side current, (c) THD of analog grid-side current. Source: [J2].



(a) (b)

(c)

Fig. 2.15. Experimental results when using eight-sampling control with an improved repetitive filter. (a) Step response, (b) Analogue inverter-side and grid-side current, (c) THD of analog grid-side current. Source: [J2].

2.5. SUMMARY

This chapter reveals the internal mechanism of multi-sampling PWM for grid-connected VSCs, and the multi-sampling PWM is essentially a double-sampling PWM. Moreover, the sampled non-average value, i.e., sampled SHs, can cause low-order aliasing. To suppress the aliasing, an improved repetitive filter is proposed to filter the sampled SHs with a low phase lag. Finally, a high-bandwidth ACC without aliasing is achieved through multi-sampling.

Related publications:
[J2] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, "Aliasing suppression of multi-sampled current controlled LCL-filtered inverters," *IEEE Trans. Journal Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 2411-2423, April 2022.

CHAPTER 3. PASSIVITY ENHANCEMENT WITH INVERTER-SIDE CURRENT CONTROL

3.1. BACKGROUND

With the large-scale integration of renewables, the grid admittance varies in a wide range, which threatens the inverter-grid interactive stability [13]. As an extension of the admittance shaping, the passivity-based control is a promising solution to tackle the instability challenges. Specifically, the output admittance should be passive below Nyquist frequency, and the stable operation can be secured regardless of the grid admittance [25].

Inverter-side current control is a cost-effective scenario since the inverter-side current sensors can also be used for over-current protection. To achieve dissipation, capacitor current damping is commonly used [40]. Yet, if the capacitor current is estimated through a digital derivative, the phase-frequency characteristic around the switching frequency will not be accurate which weakens the damping performance [70]. An analog circuit-based high-pass filter can be used to mimic the ideal derivative, but the cost as well as implementation complexity are increased [31]. Another passivity enhancement route is control delay compensation. Various terms are inserted in parallel with the ACC, such as high pass filter [71], biquad filter [72], and a predictive term [73], but their compensation performance in the high-frequency range is limited. Besides, to address the transient current during start-up and grid faults, the grid voltage feedforward should be reserved, which is often ignored due to stability considerations [71-72, 74]. Because of the phase lag from the anti-aliasing filter, there is still a non-dissipative region even though using single-loop multi-sampled inverter-side current control, and the extra active damping is required [75].

On the other hand, for a single-phase VSC, the four-sampling control is usually recommended since no SHs are introduced [36-37]. Consequently, using a higher sampling rate with an anti-aliasing filter seems unnecessary due to the extra phase lag. Actually, the four-sampling control can be regarded as a double-sampling control from the point of view of the apparent switching frequency. Then the dissipative region is the same as the regular sampling control, and the benefits of multi-sampling PWM in reducing control delay are not fully utilized.

To extend the dissipative region for a multi-sampling controlled three-phase inverter, a filter capacitor voltage feedforward scheme is proposed. Further, the issues related to the capacitor current sensor cost and start-up transients are solved at the same time. Then the proposed method is extended to a single-phase VSC, and the dissipative region is lifted to the apparent switching frequency.

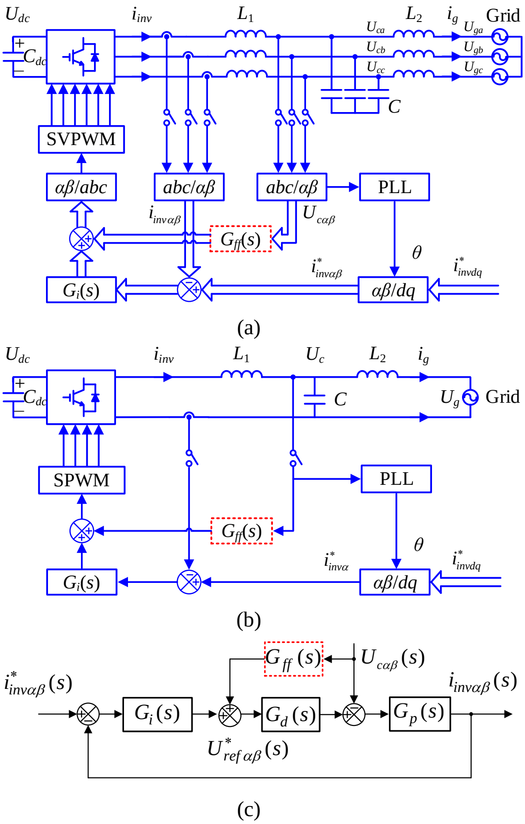

U_{dc}
C_{dc}
i_{inv}
L_1
L_2
i_g
Grid
U_{ca}
U_{cb}
U_{cc}
U_{ga}
U_{gb}
U_{gc}
C
SVPWM
$\alpha\beta/abc$
$abc/\alpha\beta$
$abc/\alpha\beta$
PLL
$i_{inv\alpha\beta}$
$U_{c\alpha\beta}$
$G_{ff}(s)$
θ
$i^*_{inv\alpha\beta}$
i^*_{invdq}
$G_i(s)$
$\alpha\beta/dq$
(a)
U_{dc}
C_{dc}
i_{inv}
L_1
U_c
L_2
i_g
C
U_g
Grid
SPWM
PLL
$G_{ff}(s)$
θ
$i^*_{inv\alpha}$
i^*_{invdq}
$G_i(s)$
$\alpha\beta/dq$
(b)
$i^*_{inv\alpha\beta}(s)$
$G_i(s)$
$G_{ff}(s)$
$U_{c\alpha\beta}(s)$
$G_d(s)$
$G_p(s)$
$i_{inv\alpha\beta}(s)$
$U^*_{ref\alpha\beta}(s)$
(c)

Fig. 3.1. Current control diagram of a single/three-phase grid-connected VSC. (a) Three-phase control diagram, (b) Single-phase control diagram, (c) General current control model. Source: [J3].

3.2. PASSIVITY ANALYSIS OF CURRENT CONTROLLERS

A. System Model

Fig. 3.1(a-b) shows a single-loop control diagram for a three/single-phase inverter, and the model in the static frame is given in Fig. 3.1(c). i^*_{invdq} and $i^*_{inv\alpha\beta}$ are current references in the *dq*- and *αβ*-frame, respectively. Regarding C and L_2 as the grid admittance, only the inverter-side inductance needs to be considered and the plant model $G_p(s)$ is

$$G_p(s) = \frac{1}{sL_1} \tag{3.1}$$

$G_d(s)$ is the control delay as given in (3.2).

$$G_d(s) = e^{-sT_d} \tag{3.2}$$

$G_i(s)$ is the proportional-resonant (PR) controller which is

$$G_i(s) = K_p + K_r \omega_{rc} \frac{s\cos\varphi_g - \omega_g \sin\varphi_g}{s^2 + \omega_{rc} s + \omega_g^2} \tag{3.3}$$

where ω_g, ω_{rc}, φ_g, K_p and K_r are the fundamental angle frequency, the cut-off angle frequency of the resonant controller, the compensation angle of the resonant controller, the proportional gain, and the resonant gain, respectively. Based on Fig. 3.1(c), the output inverter-side current in the static frame is

$$i_{inv}(s) = G_{cl}(s) i_{inv}^*(s) - Y_o(s) U_c(s) \tag{3.4}$$

where $G_{cl}(s)$ is the closed-loop transfer function between the reference current and the feedback current. $Y_o(s)$ is the output admittance with the current controller.

$$G_{cl}(s) = \frac{G_d(s)G_i(s)G_p(s)}{1 + G_d(s)G_i(s)G_p(s)} \tag{3.5}$$

$$Y_o(s) = \frac{G_p(s)}{1 + G_d(s)G_i(s)G_p(s)} \tag{3.6}$$

Based on the passivity criterion, two constraints should be secured. First, the ACC in (3.5) should be stable. For a given PM φ_m, the maximum bandwidth r_b is given in (3.7), which is the ratio between the crossover angle frequency ω_c and the switching angle frequency ω_{sw} [76].

$$r_b = \frac{\omega_c}{\omega_{sw}} = \frac{0.5\pi - \varphi_m}{T_d \omega_{sw}} = \frac{0.5\pi - \varphi_m}{2\pi h} \tag{3.7}$$

where the control delay $T_d = hT_{sw}$, If φ_m is set to 0.25π and r_b is set from 0.1 to 0.2, the allowed maximum T_d should be in the interval of $[0.625T_{sw}, 1.25T_{sw}]$. For the single-sampling and double-sampling PWM, as shown in Fig. 1.4, T_d is equal to $1.5T_{sw}$ or $0.75T_{sw}$, respectively. Hence, the r_b using double-sampling PWM can be 1/6 when φ_m is 0.25π, which means that the inner stability in (3.5) can be easily secured.

Second, $Y_o(s)$ should be passive below Nyquist frequency. As the control delay mainly impacts the high-frequency passivity, the resonant controller can be temporarily ignored. Then the real part of output admittance is given as

$$\mathrm{Re}\{Y_o(j\omega)\} \approx \frac{K_p \cos(\omega T_d)}{(K_p \cos(\omega T_d))^2 + (\omega L_1 - K_p \sin(\omega T_d))^2} \tag{3.8}$$

According to (3.8), the dissipative region is given as

$$f_{dissipative} = (0, \frac{1}{4T_d}) \tag{3.9}$$

Then the dissipative region for single-sampling and double-sampling PWM is $(0, \frac{1}{6} f_{sw})$ and $(0, \frac{1}{3} f_{sw})$, respectively. It can be seen that only if the control delay is smaller than $0.25T_{sw}$, and the dissipation can be achieved below the switching frequency. Hence, the regular sampling PWM cannot satisfy the dissipation requirement if using single-loop control.

B. Multi-sampled current controller for three-phase VSCs

Based on (3.9), when the sampling rate is greater or equal to six, the dissipation goal can be met. However, as discussed in Chapter 2, the IRF should be used to suppress the aliasing and an extra phase lag is introduced. When using a high sampling rate, e.g., N=50, the high-frequency noise can be amplified by the linear compensator in IRF, as shown in Fig. 3.2. Herein, a modified repetitive filter (MRF) is proposed in (3.10) based on the compensator in [77-78].

$$MRF(s)=\underbrace{\frac{2}{N}\frac{1-e^{-NsT_{sa}}}{1-e^{-2sT_{sa}}}}_{\text{CMAF}}\underbrace{\frac{1-r^{N}}{1-r^{2}}\frac{1-r^{2}e^{-2sT_{sa}}}{1-r^{N}e^{-NsT_{sa}}}}_{\text{Delay compensator}} \approx e^{-0.25sT_{sw}} \tag{3.10}$$

where r is set between 0 to 1. Increasing r can reduce the introduced phase lag but the noise suppression performance in the high-frequency range will be weak. The MRF delay is similar to the SRF [70] and the IRF [75], i.e., $0.25T_{sw}$. Consequently, the current control diagram is shown in Fig. 3.3, and the total loop delay is

$$T_{d\_MS\_MRF}=\underbrace{\frac{1.5}{N}T_{sw}}_{\text{computation delay + PWM delay}}+\underbrace{0.25T_{sw}}_{\text{MRF delay}}=\frac{6+N}{4N}T_{sw} \tag{3.11}$$

Similarly, substituting (3.11) into (3.10), the dissipative region using multi-sampling PWM with MRF is given as

$$f_{dissipative\_MS\_MRF}=(0,\frac{N}{6+N}) \tag{3.12}$$

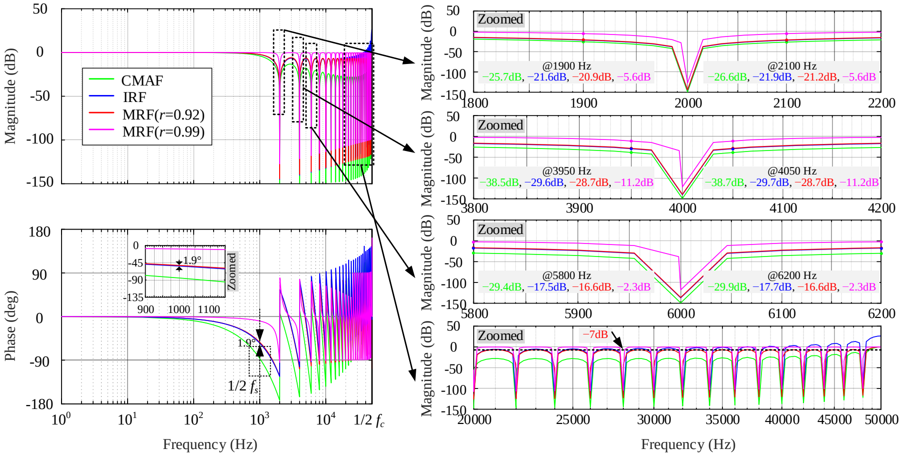


Fig. 3.2. Bode diagram of repetitive filters with a high sampling rate (CMAF: compromised moving average filter, IRF: improved repetitive filter, MRF: modified repetitive filter). Source: [J4].

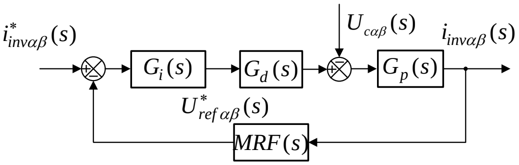


Fig. 3.3. Single-loop control diagram using multi-sampling (MRF: modified repetitive filter). Source: [J3].

The comparison of $Re\{Y_o(j\omega)\}$ using different sampling rates is given in Fig. 3.4. Table 3.1 gives the main parameters of the three-phase VSC. With the increase of sampling rate N, the non-dissipative region can be further reduced. When N is infinite, the total loop delay is equal to $0.25T_{sw}$ and the dissipation can be achieved. However, due to the limited computation ability of digital processors, multi-sampled single-loop control cannot meet the passivity goal, and extra damping is required.

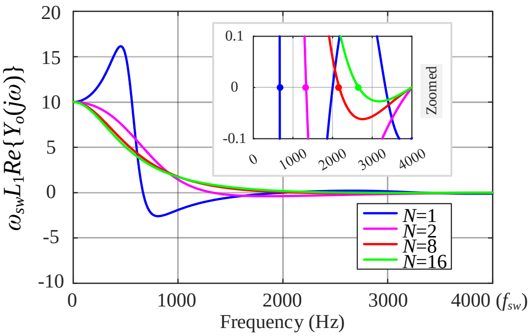


Fig. 3.4. Real part of VSC output admittance for a single-loop current controller using regular sampling (N=1, 2), eight-sampling (N=8), and sixteen-sampling (N=16). Source: [J3].

TABLE 3.1. Main parameters of a three-phase grid-connected VSC. Source:[J3].

Symbol	Description	Value	Symbol	Description	Value
P_o	Output power	7 kW	U_{grms}	Grid voltage	220 V
U_{dc}	DC-link voltage	700 V	C_{dc}	DC-link capacitance	297 μF
L_1	Inverter-side inductance	4 mH	L_2	Grid-side inductance	2 mH
C	Filter capacitance	3 μF	f_{sw}	Switching frequency	4 kHz
f_r	Resonance frequency	2516 Hz	f_{sa8}	Sampling frequency	32 kHz
f_{sa16}	Sampling frequency	64 kHz	r_8	Attenuation factor (N=8)	0.6
r_{16}	Attenuation factor (N=16)	0.8	δ_{p8}	Proportional feedforward gain (N=8)	0.9
δ_{d8}	Derivative feedforward gain (N=8)	2.4e-5	δ_{p16}	Proportional feedforward gain (N=16)	0.9
K_p	Proportional gain	20	K_r	Resonant gain	1000

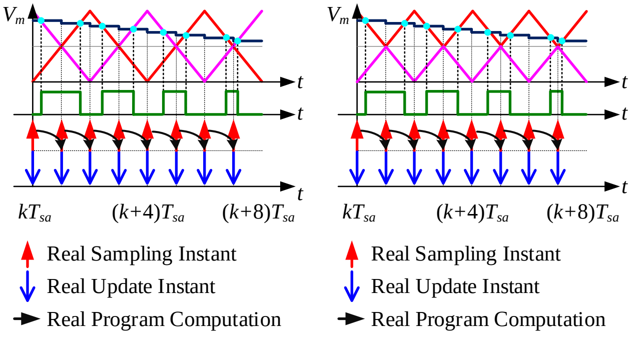
C. Multi-sampled current controller for single-phase VSCs

Four-sampling PWM is preferred for single-phase VSCs in the prior art [36], as shown in Fig. 3.5. If considering the apparent switching frequency as the base value, the four-sampling control can be regarded as a double-sampling control (see Fig. 3.5(b)), which is the reason why no SHs are introduced in the four-sampled current. Hence the dissipative region should be re-evaluated and the Nyquist frequency is the apparent switching frequency f_{ap_sw}. As shown in (3.13), the four-sampling control delay is equal to $0.75T_{ap\_sw}$.

$$\begin{aligned} T_{d\_4S} &= \underbrace{\frac{T_{sw}}{4}}_{\text{Computation Delay}} + \underbrace{\frac{T_{sw}}{8}}_{\text{PWM Delay}} = \frac{1.5T_{sw}}{4} \\ &= \underbrace{\frac{T_{ap\_sw}}{2}}_{\text{Computation Delay}} + \underbrace{\frac{T_{ap\_sw}}{4}}_{\text{PWM Delay}} = \frac{1.5T_{ap\_sw}}{2} \end{aligned} \tag{3.13}$$

Substituting (3.13) into (3.9), the dissipative region using four-sampling PWM is

$$f_{dissipative\_4S} = (0, \frac{1}{3} f_{ap\_sw}) \tag{3.14}$$



(a) (b)

Fig. 3.5. Four-sampling PWM for a single-phase VSC. (a) Seen from a preset switching frequency perspective, (b) Seen from an apparent switching frequency perspective. Source: [J3].

Table 3.2 gives the parameters of a single-phase VSCs. The preset switching frequency is 2 kHz, and the apparent switching frequency is 4 kHz. Hence, the LCL filter parameters for the single-phase inverter can be designed as same as the three-phase VSC where the rated power decreased to 1/3. According to (3.14), the non-dissipative region using four-sampling is large, as shown in Fig. 3.6. Again, only using four-sampled single-loop control cannot achieve the dissipation goal, and an extra damping term is required as same as the three-phase system. It is worth noting that the sign of $Re\{Y_o(j\omega)\}$ for the conventional single-sampling and double-sampling change more than once, which is because the Nyquist frequency is $0.5f_{sw}$ and f_{sw}, respectively. The sign of $Re\{Y_o(j\omega)\}$ for four-sampling control only changes once as the Nyquist frequency is $2f_{sw}$ [24].

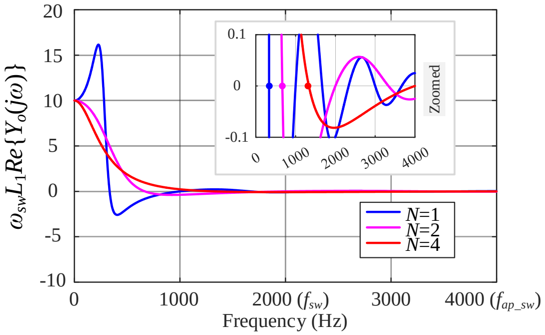


Fig. 3.6. Real part of VSC output admittance for a single-loop inverter-side current controller using regular sampling (*N*=1, 2) and four-sampling (*N*=4) for a single-phase inverter. Source: [J3].

TABLE 3.2. Main parameters of a single-phase grid-connected VSC. Source:[J3].

Symbol	Description	Value	Symbol	Description	Value
P_o	Output power	2.3 kW	U_{grms}	Grid voltage	220 V
U_{dc}	DC-link voltage	360 V	C_{dc}	DC-link capacitance	198 μF
L_1	Inverter-side inductance	4 mH	L_2	Grid-side inductance	2 mH
C	Filter capacitance	3 μF	f_{sw}	Switching frequency	2 kHz
f_r	Resonance frequency	2516 Hz	f_{sa16}	Sampling frequency	32 kHz
f_{sa32}	Sampling frequency	64 kHz	r_{16}	Attenuation factor (*N*=16)	0.6
r_{32}	Attenuation factor (*N*=32)	0.8	δ_{p16}	Proportional feedforward gain (*N*=16)	0.9
δ_{d16}	Derivative feedforward gain (*N*=16)	2.4e-5	δ_{p32}	Proportional feedforward coefficient (*N*=32)	0.9
K_p	Proportional gain	20	K_r	Resonant gain	1000

On the other hand, it is reported that the control delay can be reduced by using a single-phase cascaded H-bridge VSC with an optimum sampling rate [32]. As discussed in Section 1.1.1, if considering the apparent switching frequency as the base value, it is still a double-sampling control. Comparing (3.16) with (3.14), the passivity cannot be enhanced by increasing the number of cascaded cells, and the focus should go back to the passivity enhancement of a single cell.

$$\begin{aligned} T_{d\_CHB} &= \underbrace{\frac{T_{sw}}{4M}}_{\text{Computation Delay}} + \underbrace{\frac{T_{sw}}{8M}}_{\text{PWM Delay}} = \frac{1.5T_{sw}}{4M} \\ &= \underbrace{\frac{T_{ap\_sw}}{2}}_{\text{Computation Delay}} + \underbrace{\frac{T_{ap\_sw}}{4}}_{\text{PWM Delay}} = \frac{1.5T_{ap\_sw}}{2} \end{aligned} \tag{3.15}$$

$$f_{dissipative\_CHB} = (0, \frac{1}{3} f_{ap\_sw}) \tag{3.16}$$

3.3. PASSIVITY ENHANCEMENT

A. General analysis using capacitor voltage proportional-derivative feedforward

Capacitor voltage feedforward is a cost-saving way to extend the dissipative region of voltage source inverters, as shown in Fig. 3.1(c). The proportional (P) feedforward and derivative (D) feedforward terms are the most commonly used damping methods, their effects on the passivity in terms of control delay are first evaluated. The feedforward function is given as

$$G_{ff}(s) = \delta_p + \delta_d s \tag{3.17}$$

where δ_p and δ_d are the P feedforward coefficient and D feedforward coefficient, respectively. Ignoring the resonant controller, the output admittance is given as

$$Y_o(s) \approx \frac{1 - e^{-sT_d}\delta_p - e^{-sT_d}\delta_d s}{sL_1 + K_p e^{-sT_d}} \tag{3.18}$$

By substituting '$s=j\omega$' into (3.18), $Re\{Y_o(j\omega)\}$ is given as

$$\begin{aligned}\operatorname{Re}\{Y_o(j\omega)\} \approx\ & \frac{\overbrace{K_p\cos(\omega T_d)}^{\text{Single-loop control}}\overbrace{-\delta_p K_p + \delta_p \omega L_1 \sin(\omega T_d)}^{\text{Proportional feedforward}}}{(K_p\cos(\omega T_d))^2 + (\omega L_1 - K_p\sin(\omega T_d))^2} \\ & - \frac{\overbrace{-\delta_d \omega^2 L_1 \cos(\omega T_d)}^{\text{Derivative feedforward}}}{(K_p\cos(\omega T_d))^2 + (\omega L_1 - K_p\sin(\omega T_d))^2}\end{aligned} \tag{3.19}$$

If only considering the P feedforward, the sign of $Re\{Y_o(j\omega)\}$ is determined by $\delta_p \omega L_1 \sin(\omega T_d)$ instead of $K_p \cos(\omega T_d)$ [40], and the dissipative region is

$$f_{dissipative} = (0, \frac{1}{2T_d}) \tag{3.20}$$

According to (3.20), the passivity can be achieved only if the control delay is lower than $0.5T_{sw}$. Recalling (3.9), the allowed maximum delay for dissipation increases twice, which can easily be met using multi-sampling. It can be seen from Fig. 3.7 that when the control delay is equal to $0.5T_{sw}$, the sign of $Re\{Y_o(j\omega)\}$ around the switching frequency is negative, which can be removed when the control delay is small enough, e.g., $0.35T_{sw}$. In addition, the P coefficient should be lower than one since the R controller will affect the stability in the low-frequency range. On the other hand, if only using D feedforward, the dissipation can be achieved by changing the sign of $Re\{Y_o(j\omega)\}$ at the critical frequency $\frac{1}{4T_d}$ [74]. The D coefficient is given as

$$\delta_d = \frac{4{T_d}^2 K_p}{\pi^2 L_1} \tag{3.21}$$

Moreover, the ideal derivative does not exist in the practical implementation [70], and a digital derivative is given as

$$dev(s) = \frac{1.8}{T_{sa}} \frac{1-e^{-sT_{sa}}}{1+0.8e^{-sT_{sa}}} \tag{3.22}$$

As shown in Fig. 3.8, the stability around the critical frequency is weak which is easily affected by the resonant controller [31]. In addition, the non-dissipative region around the switching frequency appears again and the control delay should be lower than $0.5T_{sw}$.

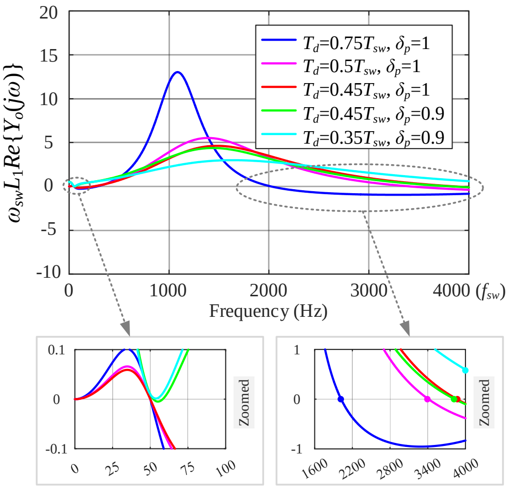


Fig. 3.7. Real part of VSC output admittance with proportional feedforward and different control delays. Source: [J3].

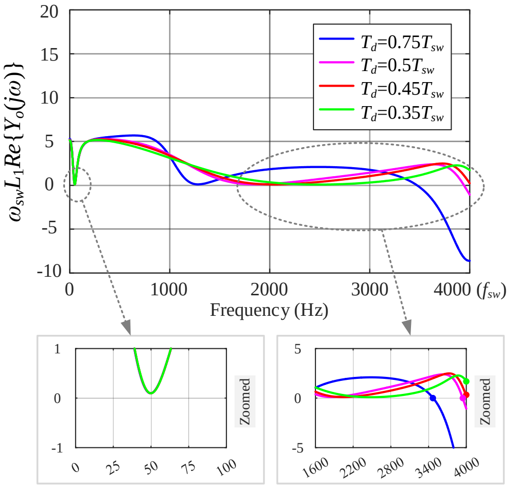


Fig. 3.8. Real part of VSC output admittance with derivative feedforward and different control delays. Source: [J3].

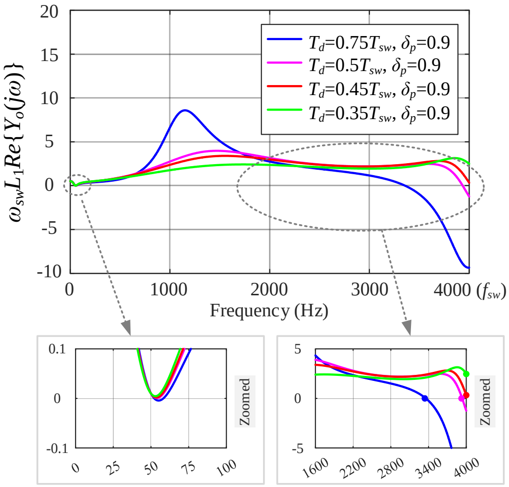


Fig. 3.9. Real part of VSC output admittance with proportional-derivative feedforward and different control delays. Source: [J3].

If combining the P feedforward and D feedforward, the stability around the critical frequency can be enhanced. In addition, when the control delay is lower than 0.5T_{sw}, the stability around the switching frequency can also be enhanced (see Fig. 3.7 and Fig. 3.9 when the delay is 0.45T_{sw}). To summarize the prior analysis, if the multi-sampled loop delay is small enough, based on Fig. 3.7, the first choice is to use the P feedforward to achieve dissipation since the derivative may amplify the noise. If the P feedforward cannot meet the goal, based on Fig. 3.9, then adding the derivative part but the loop delay should be lower than 0.5T_{sw}.

B. Multi-sampled current control of three-phase VSCs

Fig. 3.10 shows the multi-sampled current control diagram with the capacitor voltage feedforward. Especially, besides the MRF used in the inverter-side current feedback path, the MRF should also be inserted in the feedforward path to remove the sampled SHs. The feedforward function is given in (3.23).

$$G_{ff}(s) = \delta_p MRF(s) + \delta_d dev(s) MRF(s) \tag{3.23}$$

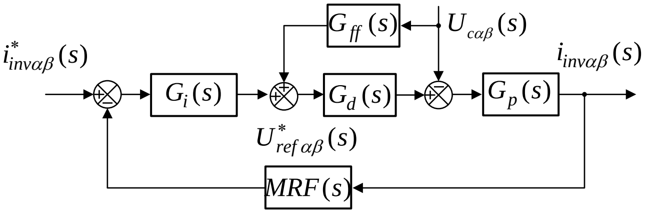


Fig. 3.10. Multi-sampled inverter-side current control diagram with filter capacitor voltage feedforward (MRF: modified repetitive filter). Source: [J3].

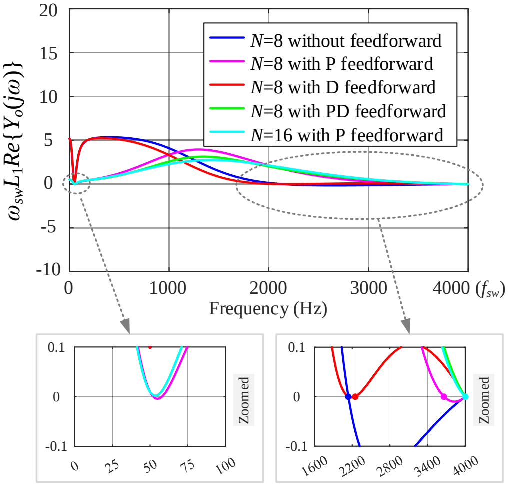


Fig. 3.11. Real part of VSC output admittance with and without filter capacitor voltage feedforward based on different sampling rates for three-phase inverters. Source: [J3].

It can be seen from Fig. 3.11 that *N*=8 with P feedforward cannot achieve passivity around the switching frequency. That is because the delay compensator in (3.10) cannot make the loop delay small enough. *N*=8 with PD feedforward can achieve passivity in the whole frequency range. If the sampling rate is further increased to sixteen, only using P feedforward can achieve dissipation. Hence, using *N*=8 with PD feedforward or *N*=16 with P feedforward can achieve the dissipation, where the stability around the critical frequency is enhanced compared with *N*=8 with D feedforward. Fig. 3.12 shows a comparison of $Re\{Y_o(j\omega)\}$ with the proposed method by considering ±20% variations of L_1. It can be seen that the passivity can still be achieved and the proposed method performs robustly against filter inductance variations.

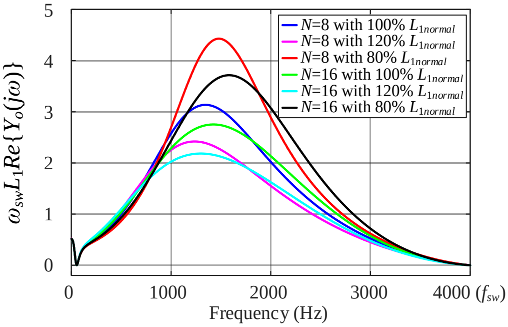


Fig. 3.12. Robustness analysis of proposed method against ±20% inverter-side inductance variation (*N*=8 with PD feedforward or *N*=16 with P feedforward). Source: [J3].

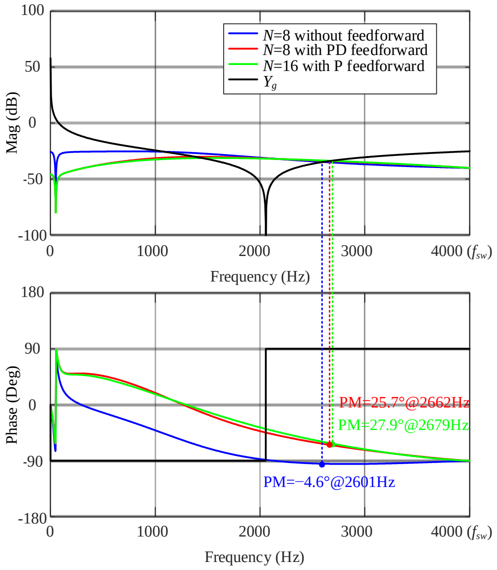


Fig. 3.13. Output admittance for a multi-sampled three-phase VSC with and without the filter capacitor voltage feedforward. Source: [J3].

In terms of parameter design, K_p can be determined based on the given PM or bandwidth. When using eight-sampling, the δ_d is first deduced to achieve the dissipation. Then δ_p is set to 0.85-0.9, and tune K_r until the non-dissipative region in the low-frequency range is removed. When using sixteen-sampling, only δ_p and K_r need to be tuned. Considering the admittance-based stability analysis, the filter capacitance and grid-side inductance can be regarded as the grid admittance, i.e., $Y_g(s)=sC+1/sL_2$. As shown in Fig. 3.13, the grid admittance intersects the inverter output admittance in its negative-real-part region for N=8 without feedforward, which leads to a -4.6° PM. Hence, the system will be unstable. Nevertheless, the system can still be stabilized using the proposed method N=8 with PD feedforward or N=16 with P feedforward, and the PMs for both proposed methods are similar.

C. Multi-sampling control of single-phase VSCs

To extend the dissipative region to f_{ap_sw}, the proposed method in the three-phase inverters can be extended to the single-phase inverters by doubling the sampling rate. Specifically, the sampling frequency is set to $8f_{ap\_sw}$, i.e., $16f_{sw}$. Then the MRF in (3.11) is used to suppress the switching ripple in the sampled voltage and current, where the sampling rate N is still set to eight. When the sampling frequency is set to $16f_{ap\_sw}$, i.e., $32f_{sw}$, and r is set to 0.8. More generally, for the cascaded H-bridge inverter with M cells, the sampling frequency can be set to $8f_{ap\_sw}$ or $16f_{ap\_sw}$, i.e., $16Mf_{sw}$ or $32Mf_{sw}$. In addition, r should be tuned accordingly to satisfy the filtering ability around the switching frequencies. To illustrate the relationship between the multi-sampled current-controlled single-phase inverters and three-phase inverters, the Nyquist frequencies for both of them are set to be the same (4 kHz), as shown in Table

3.1 and Table 3.2. In addition, the LCL filter parameters and controller parameters are also the same. The only difference is that the sampling rate of the single-phase inverter is two times larger than the three-phase inverter. The control diagram is the same as that of the three-phase inverter in Fig. 3.10.

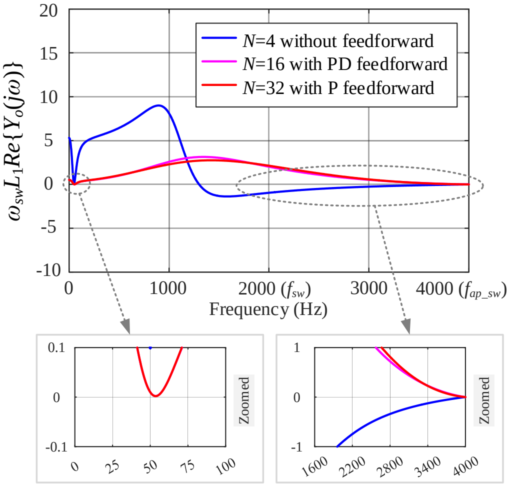


Fig. 3.14. Real part of output admittance for four-sampling control, sixteen-sampling control with proportional-derivative feedforward, and thirty two-sampling control with proportional voltage feedforward. Source: [J3].

It can be observed from Fig. 3.14 that N=4 without feedforward has a large non-dissipative region as the four-sampling control is a kind of double control based on the apparent switching frequency. On the other hand, N=16 with PD feedforward in the single-phase system is equal to N=8 with PD feedforward in the three-phase system, hence the dissipation is achieved below the apparent switching frequency for the single-phase VSC. Similarly, N=32 with P feedforward in the single-phase system is equal to N=16 with P feedforward in the three-phase system, and the dissipation goal up to apparent switching frequency can also be achieved.

Considering ±20% deviation of the inverter-side inductance, as shown in Fig. 3.15, the passivity can still be achieved with the proposed method. Fig. 3.16 plots the output admittance of multi-sampled current controllers for a single-phase inverter. It can be seen that the PM for the four-sampling control is negative, which leads to the system being unstable. Nevertheless, the system can still be stabilized using the proposed method N=16 with PD feedforward or N=32 with P feedforward, and the PMs for both proposed methods are similar.

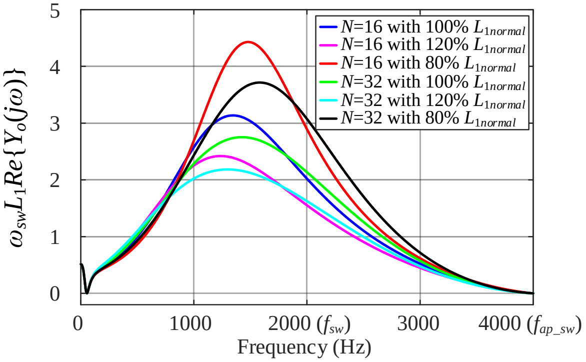


Fig. 3.15. Robustness analysis of proposed method against ±20% inverter-side inductance variation (N=16 with PD feedforward or N=32 with P feedforward). Source: [J3].

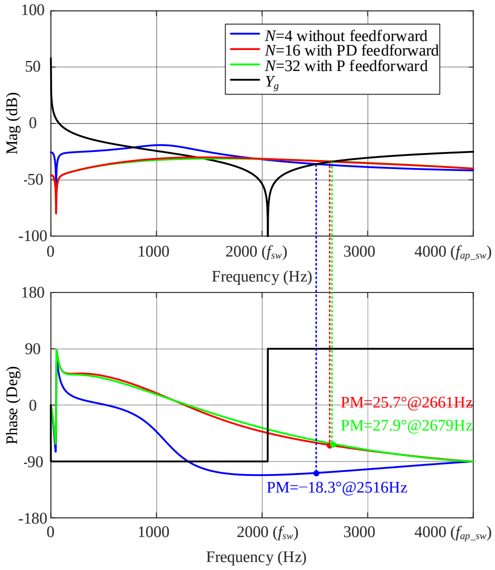


Fig. 3.16. Output admittance for a multi-sampled single-phase HB inverter with and without the filter capacitor voltage feedforward. Source: [J3].

3.4. CASE STUDIES

To validate the proposed method, experiments are implemented in a VSC system from Imperix, as shown in Fig. 3.17. Herein, a three-phase two-level VSC and a single-phase H-bridge VSC are used, and the parameters for the experiments are shown in Table 3.1 and Table 3.2.

A. Three-phase VSC

The experimental result using N=8 without feedforward for the down-scaled three-phase inverter is shown in Fig. 3.18. The inverter starts at 40 ms, and the reference current is set to zero in order to address the transient current during start-up. Then the reference current steps up to 15 A (rated current), the system becomes unstable and the protection is triggered, which is in line with the theoretical analysis in Fig. 3.14. When using N=8 with PD feedforward, the system stability is secured as well as the start-up transients are suppressed, as shown in Fig. 3.19. Since the result using N=16 with P feedforward is very similar to the result in Fig. 3.19, it is not presented in this section.

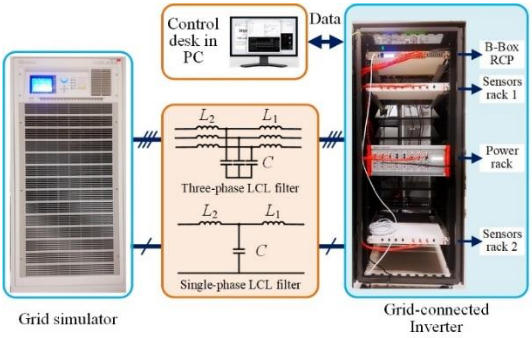
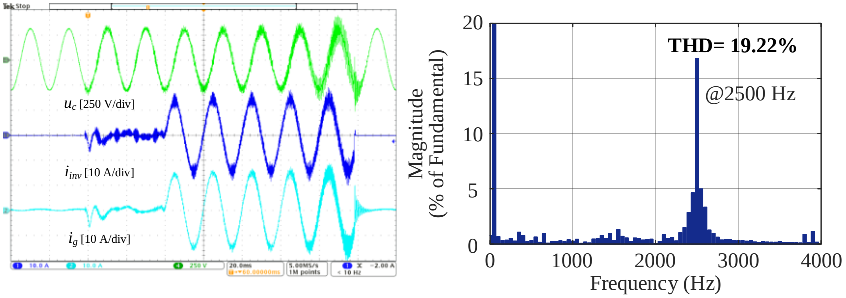
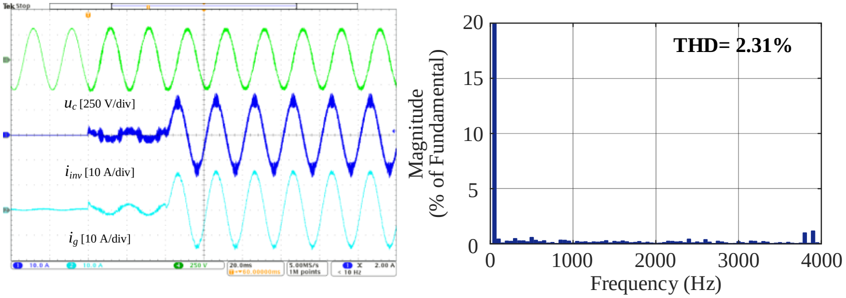

Control desk in PC
Data
B-Box RCP
Sensors rack 1
Power rack
Sensors rack 2
L_2
L_1
C
Three-phase LCL filter
L_2
L_1
C
Single-phase LCL filter
Grid simulator
Grid-connected Inverter

Fig. 3.17. Single/three-phase grid-connected VSC prototype. Source: [J3].



(a) (b)

Fig. 3.18. Experimental results for a three-phase VSC using N=8 without feedforward. (a) Inverter-side current and grid-side current, (b) Grid-side current harmonic spectrum. Source: [J3].

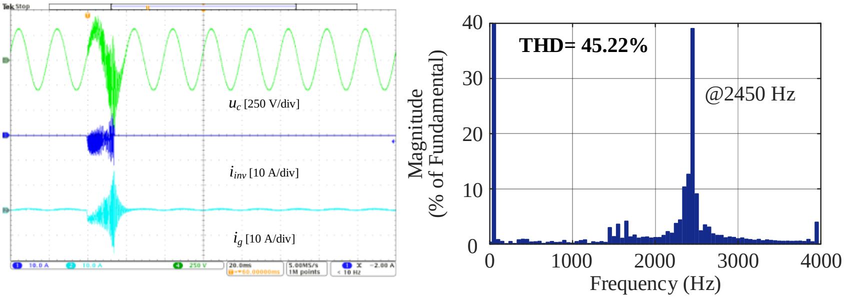


(a) (b)

Fig. 3.19. Experimental results for a three-phase VSC using N=8 with proportional-derivative feedforward. (a) Inverter-side current and grid-side current, (b) Grid-side current harmonic spectrum. Source: [J3].

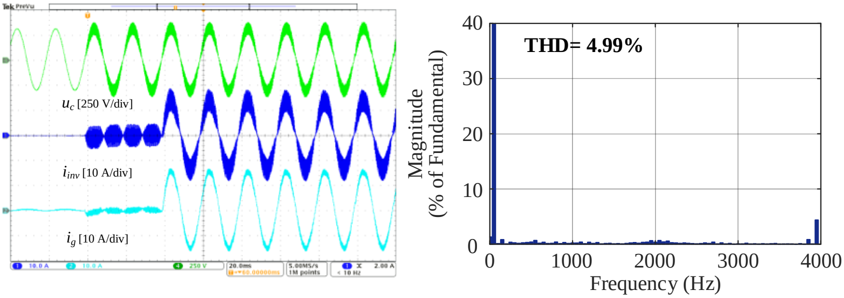
B. Single-phase VSC

The experimental result using *N*=4 without feedforward on the down-scaled single-phase VSC is shown in Fig. 3.20. The inverter starts at 40 ms, and the reference current is set to zero to address the transient current during the start-up. Then the reference current steps up to 15 A (rated current), the system becomes unstable and the protection is triggered, which is in line with the analysis in Fig. 3.16. When using *N*=16 with PD feedforward, the system stability is secured as well as the start-up transients are suppressed, as shown in Fig. 3.21. Since the result using the *N*=32 with P feedforward is very similar to the result in Fig. 3.21, it is not presented in this section.



(a) (b)

Fig. 3.20. Experimental results for a single-phase VSC using *N*=4 without feedforward. (a) Inverter-side current and grid-side current, (b) Grid-side current harmonic spectrum. Source: [J3].



(a) (b)

Fig. 3.21. Experimental results for a single-phase VSC using *N*=16 with proportional-derivative feedforward. (a) Inverter-side current and grid-side current, (b) Grid-side current harmonic spectrum. Source: [J3].

3.5. SUMMARY

This chapter first investigates the passivity of single-loop multi-sampling control for VSCs with inverter-side current feedback. Due to the phase lag from the anti-aliasing filter in the feedback path, there is always a non-dissipative region, which threatens the stable operation. To resolve this challenge, a filter capacitor voltage feedforward scheme is proposed in this chapter. For the three-phase VSCs, eight-sampling with proportional-derivative feedforward or sixteen-sampling with proportional feedforward can achieve the dissipation below switching frequency. Then, the proposed method is extended to a single-phase VSC by doubling the sampling rate. Finally, experimental results validate the proposed method.

Related publications:
[J3] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, “Passivity based multi-sampled current control of LCL-filtered grid-connected inverters,” *IEEE Trans. Power Electron.*, 2022 (Second-round revision).
[J4] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, “Line voltage sensorless control of grid-connected inverters using multisampling,” *IEEE Trans. Power Electron*., vol. 37, no. 4, pp. 4792-4803, April 2022.

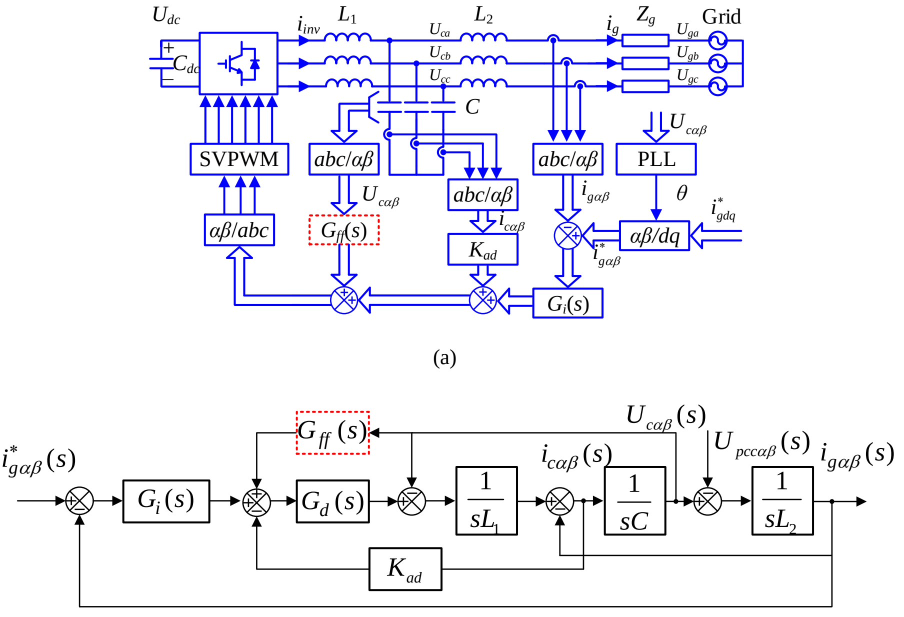
CHAPTER 4. PASSIVITY ENHANCEMENT WITH GRID-SIDE CURRENT CONTROL

4.1. BACKGROUND

Besides the discussed inverter-side current control in Chapter 3, grid-side current control is also widely used in the grid-connected inverters. Especially under a distorted grid, the filter capacitor current still needs to be estimated when using inverter-side current control, otherwise, the filter capacitor will provide a path for the grid harmonics [79-80]. As a result, inverter-side and grid-side current sensors are required for the overcurrent protection and the current regulation, but the capacitor current can be calculated for active damping control.

In terms of single-loop grid-side current control, the non-dissipative region is located in the interval between the anti-resonant frequency ($\frac{1}{2\pi}\sqrt{\frac{1}{L_1C}}$) and critical frequency ($\frac{1}{4T_d}$) [40-41]. In order to achieve the whole frequency range dissipation up to the switching frequency, various methods have been studied in the previous work. A negated Euler derivative term is inserted in parallel with the proportional resonant controller [71], however, the anti-resonant frequency should be restrained to a specific range. Moreover, as the grid voltage feedforward is abandoned due to stability issues, not only the transients during the start-up and grid faults cannot be addressed properly [81], but also the advantage of grid background harmonic suppression is lost [82]. Capacitor current active damping (CCAD) is another effective method to remove the non-dissipative region, and the optimum damping coefficient is derived based on a general admittance model [40]. To overcome the negative effect of filter parameter fluctuation on the dissipation around the critical frequency, the damping coefficient is replaced with a digital filter but the anti-resonance frequency is restrained [42]. Only using the capacitor voltage feedforward (CVF) can also achieve dissipation [41], but the design of the inverter-side inductance and filter capacitance is again restricted. Combining the CCAD and the PCC voltage feedforward, the phase margin around the critical frequency is further improved, but the design process is more complicated [44].

Therefore, the first challenge for the passivity design is that the anti-resonance frequency is restrained within a specific range. The second challenge is that the grid voltage feedforward is often overlooked due to the stability consideration, which deteriorates the transient performance during the start-up or under a voltage sag. To solve these issues, a multi-sampling control scheme is proposed in this chapter, which combines the CCAD and CVF. Compared to the conventional double-sampling control, both the transient performance and the robustness against the filter parameter deviation are enhanced. Case studies validate the effectiveness of the proposed method.


U_{dc}
C_{dc}
i_{inv}
L_1
L_2
U_{ca}
U_{cb}
U_{cc}
i_g
Z_g
U_{ga}
U_{gb}
U_{gc}
Grid
C
$U_{c\alpha\beta}$
SVPWM
$abc/\alpha\beta$
$abc/\alpha\beta$
$abc/\alpha\beta$
PLL
$U_{c\alpha\beta}$
$i_{g\alpha\beta}$
θ
i^*_{gdq}
$\alpha\beta/abc$
$G_{ff}(s)$
$i_{c\alpha\beta}$
K_{ad}
$i^*_{g\alpha\beta}$
$\alpha\beta/dq$
$G_i(s)$
$i^*_{g\alpha\beta}(s)$
$G_i(s)$
$G_{ff}(s)$
$G_d(s)$
$\frac{1}{sL_1}$
$i_{c\alpha\beta}(s)$
$\frac{1}{sC}$
$U_{c\alpha\beta}(s)$
$U_{pcc\alpha\beta}(s)$
$\frac{1}{sL_2}$
$i_{g\alpha\beta}(s)$
K_{ad}

(a)

(b)

Fig. 4.1. Diagram of a three-phase VSC with grid-side current feedback. (a) Three-phase control diagram, (b) Mathematic model. Source: [C1].

4.2. PASSIVITY ANALYSIS OF CURRENT CONTROLLER

The control diagram of a three-phase grid-connected inverter with the grid-side current control is depicted in Fig. 4.1(a), where $i_{c\alpha\beta}$ is the capacitor current, K_{ad} is CCAD coefficient, $G_{ff}(s)$ is the capacitor voltage feedforward function, i^*_{gdq} and $i^*_{g\alpha\beta}$ are current references in the dq- and $\alpha\beta$-frame, respectively. $G_i(s)$ is the proportional-resonant (PR) controller, which is the same as given in (3.3). Fig. 4.1(b) illustrates the mathematic model in a static frame, and the grid-side current depends on both the current reference and the PCC voltage, as given in (4.1).

$$i_g(s) = G_{cl}(s) i_g^*(s) - Y_o(s) U_{pcc} \tag{4.1}$$

$$G_{cl}(s)=\frac{G_i(s)G_d(s)}{s^3L_1L_2C\underbrace{+s^2L_2CK_{ad}G_d(s)}_{\text{CCAD}}+s(L_1+L_2)+G_i(s)G_d(s)} \tag{4.2}$$

$$Y_o(s)=\frac{s^2L_1C\overbrace{+sG_d(s)K_{ad}C}^{\text{CCAD}}+1}{s^3L_1L_2C\underbrace{+s^2L_2CK_{ad}G_d(s)}_{\text{CCAD}}+s(L_1+L_2)+G_i(s)G_d(s)} \tag{4.3}$$

Since the stability of the closed-loop transfer function is similar to the inverter-side current control in Chapter 3, the PR parameters can be deduced based on the general admittance model in [90]. Hence, the PR parameters are the same in Chapter 3. Ignoring *R* controller, the real part of the VSC output admittance *Re*{$Y_o(j\omega)$} is

$$\begin{gathered}\mathrm{Re}\{Y_o(j\omega)\}\approx\frac{\overbrace{(1-L_1C\omega^2)K_p\cos(\omega T_d)}^{\text{Single-loop control}}\overbrace{+K_{ad}\omega^2L_1C\cos(\omega T_d)}^{\text{CCAD}}}{A^2+B^2}\\ \begin{cases}A=-\omega^2K_{ad}L_2C\cos(\omega T_d)+K_p\cos(\omega T_d)\\ B=\omega^3L_1L_2C-\omega^2K_{ad}L_2C\sin(\omega T_d)-\omega(L_1+L_2)+K_p\sin(\omega T_d)\end{cases}\end{gathered} \tag{4.4}$$

According to (4.4), the dissipative region for single-loop control is

$$f_{dissipative}=\left(\frac{1}{4T_d},\frac{1}{2\pi}\sqrt{\frac{1}{L_1C}}\right)\text{ or }\left(\frac{1}{2\pi}\sqrt{\frac{1}{L_1C}},\frac{1}{4T_d}\right) \tag{4.5}$$

The comparison of *Re*{$Y_o(j\omega)$} for single-loop control is given in Fig. 4.2, where double-sampling, eight-sampling, and sixteen-sampling techniques are considered. The MRF in Chapter 3 is considered when using multi-sampled current control, and the total control delay is specialized in (3. 12). Table 4.1 shows the parameters of the used three-phase grid-connected VSC. It can be seen that the non-dissipative region expands with the increase of the sampling frequency, and extra damping is required. By changing the sign of *Re*{$Y_o(j\omega)$} at the critical frequency, the CCAD damping coefficient K_{ad} is

$$K_{ad}=K_p-\frac{4T_d^2K_p}{\pi^2L_1C} \tag{4.6}$$

Note that the MRF is also required in the capacitor current feedback path to remove the sampled SHs [84]. As shown in Fig. 4.3(a), *Re*{$Y_o(j\omega_{cri})$} is zero at the critical frequency when using CCAD, and the dissipation up to the switching frequency is achieved. However, the stability around the critical frequency is weak, which can easily be affected by the parameter deviation of L_1 and C (see Fig. 4.3(b)). Moreover, the advantage of multi-sampling PWM is not fully exploited, because the dissipation of the inverter output admittance is not enhanced if only using a multi-sampled CCAD. Therefore, besides the CCAD, an extra damping term is still required.

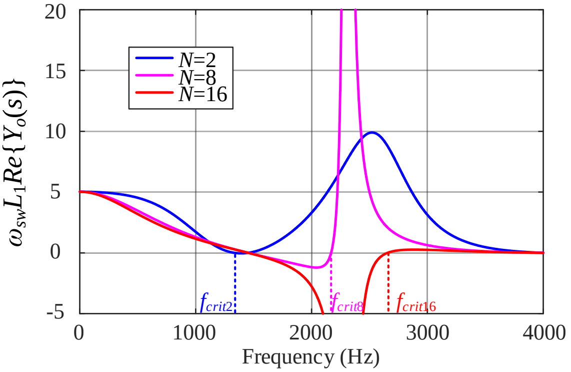


Fig. 4.2. Passivity of $Y_o(s)$ for a single-loop grid-side current controller using double-sampling (N=2), eight-sampling (N=8), and sixteen-sampling (N=16) for three-phase inverters. Source: [C1].

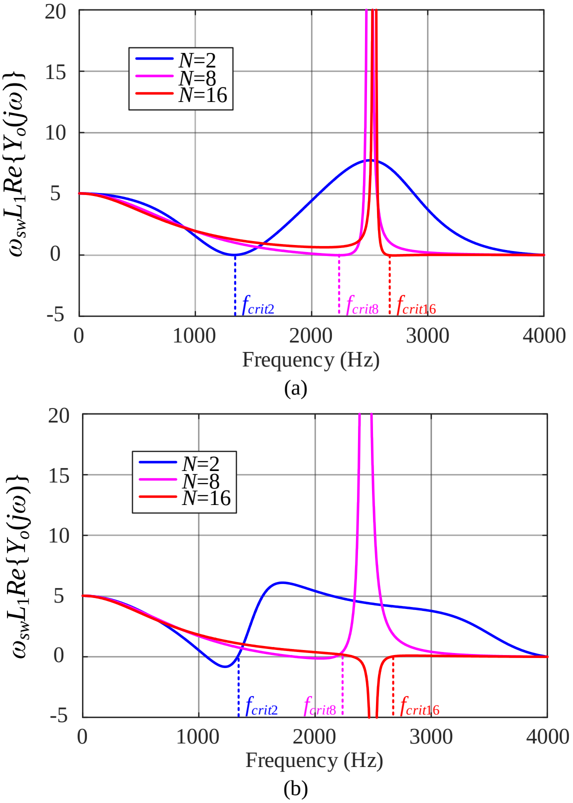


Fig. 4.3. Passivity of $Y_o(s)$ with capacitor current active damping using double-sampling (N=2), eight-sampling (N=8), and sixteen-sampling (N=16) for three-phase inverters. (a) With nominal values of L_1 and C, (b) With +20% unit deviation of L_1 and C. Source: [C1].

TABLE 4.1. Main parameters of a three-phase grid-connected VSC. Source: [C1].

Symbol	Description	Value	Symbol	Description	Value
P_o	Output power	7 kW	U_{grms}	Grid voltage	220 V
U_{dc}	DC-link voltage	700 V	L_1	Inverter-side inductance	4 mH
L_2	Grid-side inductance	2 mH	C	Filter capacitance	3 μF
f_{sw}	Switching frequency	4 kHz	N	Sampling rate	2/8/16
K_p	Proportional coefficient	20	K_r	Resonant coefficient	1000
K_{ad2}	Damping coefficient	-3.7	δ_{p2}	Proportional feedforward coefficient	0.9
K_{ad2}	Damping coefficient	11.9	δ_{p8}	Proportional feedforward coefficient	0.9
K_{ad2}	Damping coefficient	15	δ_{p16}	Proportional feedforward coefficient	0.9
r_8	Attenuation factor	0.6	r_{16}	Attenuation factor	0.8

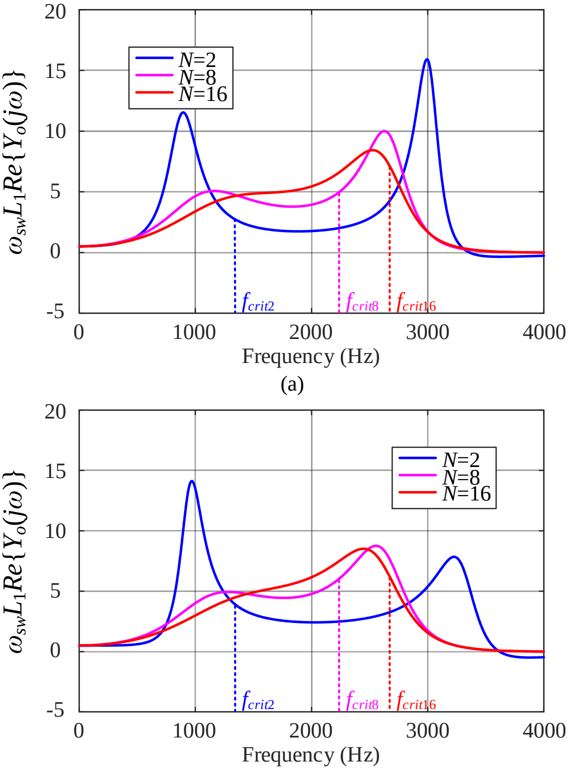
4.3. PASSIVITY ENHANCEMENT

To enhance the robustness against the filter parameter fluctuation and the transient performance, a CVF term is further added based on the CCAD. The inverter output admittance considering both CCAD and CVF is given in (4.7), and $Re\{Y_o(j\omega)\}$ is given in (4.8).

$$Y_o(s)=\frac{s^2L_1C\overbrace{+sG_d(s)K_{ad}C}^{\text{CCAD}}+\overbrace{1-\delta_pG_d(s)}^{\text{CVF}}}{s^3L_1L_2C\underbrace{+s^2L_2CK_{ad}G_d(s)}_{\text{CCAD}}+s(L_1+L_2)\underbrace{-sL_2\delta_pG_d(s)}_{\text{CVF}}+G_c(s)G_d(s)} \tag{4.7}$$

$$\begin{gathered}\mathrm{Re}\{Y_o(j\omega)\}\approx\frac{\overbrace{(1-L_1C\omega^2)K_p\cos(\omega T_d)}^{\text{Single-loop control}}\overbrace{+K_{ad}\omega^2L_1C\cos(\omega T_d)}^{\text{CCAD}}\overbrace{-\delta_pK_p+\delta_p\omega L_1\sin(\omega T_d)}^{\text{CVF}}}{A^2+B^2}\\ \begin{cases}A=-\omega^2K_{ad}L_2C\cos(\omega T_d)+K_p\cos(\omega T_d)-\omega\delta_pL_2\sin(\omega T_d)\\ B=\omega^3L_1L_2C-\omega^2K_{ad}L_2C\sin(\omega T_d)-\omega(L_1+L_2)+K_p\sin(\omega T_d)+\omega\delta_pL_2\cos(\omega T_d)\end{cases}\end{gathered} \tag{4.8}$$

To study the dissipation at the critical frequency, $Re\{Y_o(j\omega_{crit})\}$ is obtained as given in (4.9), where ω_c is the current control bandwidth. The critical frequency ω_{crit} is $0.33\omega_{sw}$ for the double-sampling control based on (3.10), which shifts towards a higher frequency with an increased sampling rate. Since ω_c is usually chosen between $0.1\omega_{sw}$ to $0.2\omega_{sw}$, $Re\{Y_o(j\omega_{crit})\}$ can always remain positive. Hence, the dissipation around the critical frequency can be enhanced with the CVF (see Fig. 4.4(a)). Moreover, as shown in Fig. 4.4(b), the inverter output admittance can still behave dissipative around the critical frequency, considering even a 20% filter parameter deviation.



(a)

(b)

Fig. 4.4. Passivity of $Y_o(s)$ with CCAD and CVF using double-sampling (N=2), eight-sampling (N=8), and sixteen-sampling (N=16) for three-phase inverters. (a) With nominal values of L_1 and C, (b) With +20% unit deviation of L_1 and C. Source: [C1].

$$\text{Re}\{Y_o(j\omega_{crit})\} \approx \frac{-\delta_p\omega_c L_1 + \delta_p\omega_{crit}L_1}{A^2+B^2} > 0 \tag{4.9}$$

However, a non-dissipative region still exists in the higher frequency range with the double-sampling control (see Fig. 4.4). Taking the switching frequency point as an example, the dissipation of $Y_o(s)$ presents a negative value, as explained in (4.10). Due to the reduced time delay, the dissipative range can be extended up to the switching frequency using eight-sampling. As shown in (4.11), when T_d is $0.5T_{sw}$, $Re\{Y_o(j\omega_{sw})\}$ is always larger than zero because the CVF coefficient is smaller than 1 (δ_p=0.9 in this chapter). If the CVF coefficient is set to 1, the low-frequency dissipation will be affected, which has been explained in Fig. 3.7. With the proposed multi-sampling control method combining both the CCAD and the CVF, the passivity robustness can be enhanced at the critical frequency, and the passivity range can be extended up to the switching frequency simultaneously.

$$\text{Re}\{Y_o(j\omega_{sw})\}_{T_d=0.75T_{sw}} \approx \frac{-\delta_p\omega_c L_1 - \delta_p\omega_{sw}L_1}{A^2+B^2} \tag{4.10}$$

$$\mathrm{Re}\{Y_o(j\omega_{sw})\}_{T_d=0.5T_{sw}} \approx \frac{3K_p-\delta_p K_p}{A^2+B^2} \tag{4.11}$$

4.4. CASE STUDIES

To validate the proposed method, two cases with different grid parameters are studied through simulations. The Bode plot of the inverter output admittance is depicted in Fig. 4.5, considering L_g=8 mH and +20% unit deviation. The PM is negative with the double-sampling CCAD according to Fig. 4.5, which results in resonances around the critical frequency as illustrated in Fig. 4.6(a). Moreover, there is a high inrush current during the start-up. After implementing the CVF, high-frequency resonances disappear when using double-sampling and eight-sampling (see Fig. 4.6(b)-(c)). Besides, the start-up transient is well addressed.

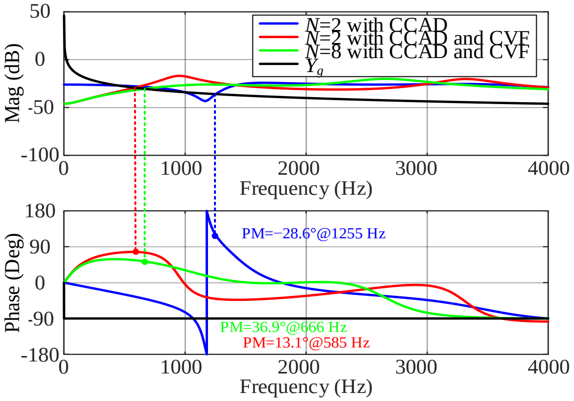
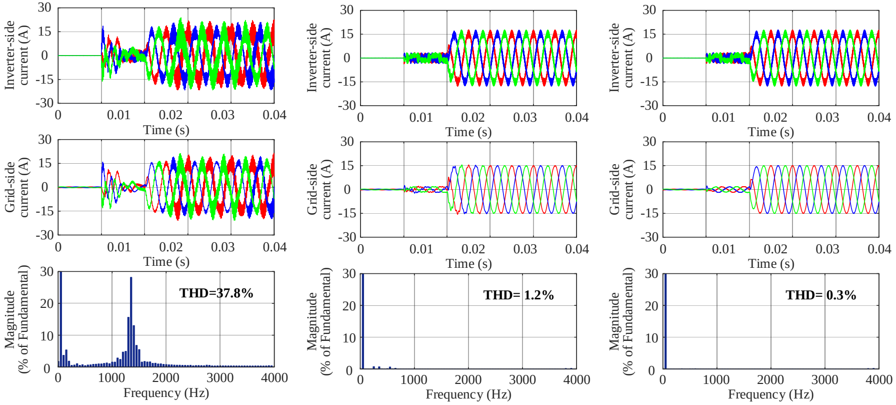


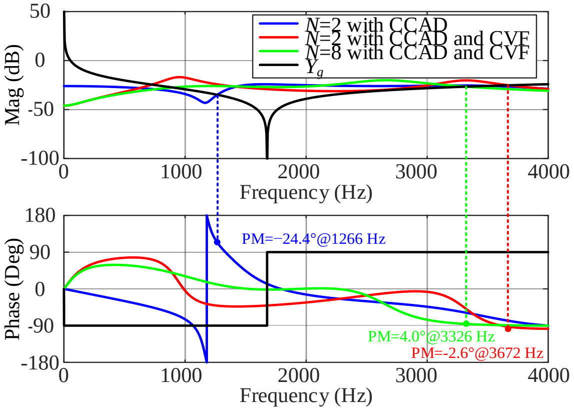
Fig. 4.5. Bode plot of inverter output admittance with +20% unit deviation of L_1 and C when L_g=8 mH. (CCAD: capacitor current active damping, CVF: capacitor voltage feedforward) Source: [C1].



(a) (b) (c)

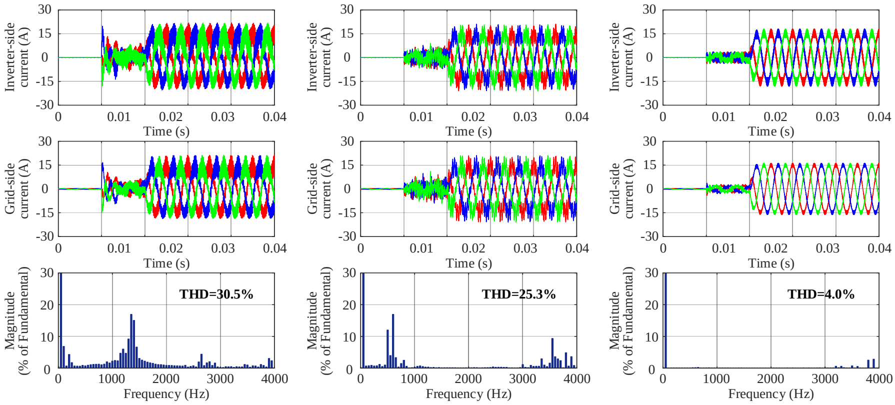
Fig. 4.6. Simulation results under +20% deviation of L_1 and C when L_g=8 mH. (a) N=2 with CCAD, (b) N=2 with CCAD and CVF, (c) N=8 with CCAD and CVF. (CCAD: capacitor current active damping, CVF: capacitor voltage feedforward) Source: [C1].

For L_g=3 mH, C_g=3 μF, and +20% unit deviation, as shown in Fig. 4.7, the PM for the double-sampling CCAD is negative, and the resonance around the critical frequency still exists (see Fig. 4.8(a)). Moreover, the system is not stable even when using double-sampling CCAD and CVF (see Fig. 4.8(b)), which is consistent with the analysis in Fig. 4.7. It can be seen from Fig. 4.8(c) that the system only can remain stable with the eight-sampled CCAD and CVF due to the reduced control delay from multi-sampling PWM.



(b)

Fig. 4.7. Bode plot of inverter output admittance with +20% unit deviation of L_1 and C when L_g=3 mH and C_g=3 μF. (CCAD: capacitor current active damping, CVF: capacitor voltage feedforward) Source: [C1].



(a) (b) (c)

Fig. 4.8. Simulation results under +20% deviation of L_1 and C when L_g=3 mH and C_g=3 μF. (a) N=2 with CCAD, (b) N=2 with CCAD and CVF, (c) N=8 with CCAD and CVF. (CCAD: capacitor current active damping, CVF: capacitor voltage feedforward) Source: [C1].

4.5. SUMMARY

This chapter has investigated the robustness of the CCAD against filter parameter deviations for *LCL*-filtered VSCs. The stability near the critical frequency becomes vulnerable if the filter parameter discrepancy is considered. To tackle this challenge, a control method is proposed by combining an additional CVF. However, a non-dissipative region is inevitable in the high-frequency area with the double-sampling control. By further utilizing the multi-sampling control, the passivity can be enhanced up to the switching frequency, so that the wideband resonances can be eliminated. With the proposed multi-sampling control scheme, wideband passivity can be robustly designed against variations of the filter and grid parameters. The transient performance is also improved. The effectiveness of the proposed method is validated through the simulation.

Related publications:

[C1] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, and Rik De Doncker, “Robust passivity enhancement for LCL-filtered grid-following inverters with multi-sampled grid-side current control”, in *Proc. IEEE ECCE*, 2022 (Under review).

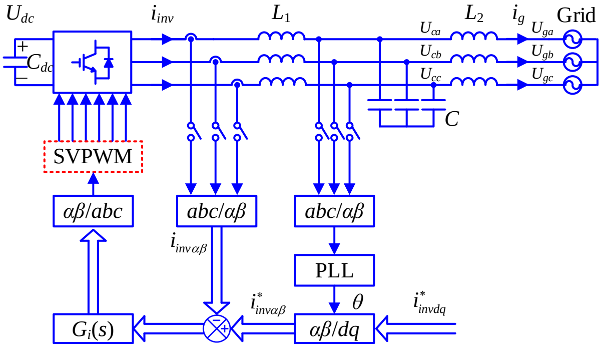
CHAPTER 5. ENHANCED REAL-TIME-UPDATE CURRENT CONTROL USING MULTI-SAMPLING CONCEPT

5.1. BACKGROUND

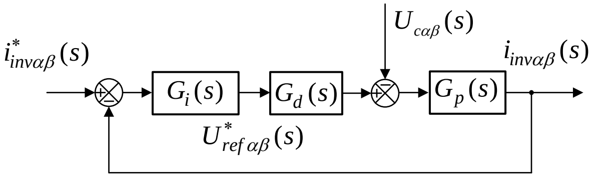
As discussed in Chapter 3, when using the multi-sampled current control with an anti-aliasing filter, the total loop delay is $(0.25+\frac{1.5}{N})T_{sw}$ [75]. As a result, the extreme control delay can only be $0.25T_{sw}$ even though the sampling rate N is infinite. However, the critical control delay should be $0.25T_{sw}$ according to the passivity theory [25]. Hence extra active damping is required for the single-loop multi-sampled inverter-side current control, which makes the control system more complicated.

On the other hand, real-time sampling can also help to reduce the control delay. but low-order aliasing will appear since the non-average current is sampled for the control [68]. Real-time-update PWM only uses the average value, and the control delay can be optimized to $0.25T_{sw}$ only if the code processing time is short enough [83]. However, in practical applications, the code processing time may be long, which may bring extra control delay and threaten the stability of the VSC-grid system.

In order to tackle the above challenges, the existing real-time-update PWM methods are evaluated, and a control delay analysis is given based on the voltage-second balance principle [84]. Then an enhanced real-time-update (ERTU) PWM using the multi-sampling concept is proposed in this chapter. As a result, the control delay can always be kept to be $0.25T_{sw}$, and the burden on the code processing time is released as well. Finally, the proposed method is verified through the simulation.



(a)



(b)

Fig. 5.1. Single-loop control diagram of a three-phase VSC using inverter-side current feedback. (a) Diagram of single-loop control, (b) Mathematic model. Source: [C2].

5.2. CONVENTIONAL REAL-TIME-UPDATE PWM

Fig. 5.1(a) shows a single-loop control diagram for a three-phase VSC using inverter-side current feedback. Fig. 5.1(b) illustrates the mathematic model in the static frame. The critical control delay for the dissipation of inverter output admittance is $0.25T_{sw}$, based on this optimization goal, the control delays for the conventional real-time-update PWM methods are evaluated one by one.

Real-time-update PWM methods using single-sampling include the single-valley-sampling real-time-update (SVSRTU) PWM and single-peak-sampling real-time-update (SPSRTU) PWM. Specifically, the average value of current at the peak/valley of the carrier is used for the control, and the calculated duty cycle is loaded in real-time [85]. Fig. 5.2(a) shows the diagram of SVS PWM, based on the voltage-second equivalence, the equivalent update instant is the same as the sampling instant. Then the computation delay is $0T_{sw}$, and only the single-sampling PWM delay $0.5T_{sw}$ is remained, as shown in (5.1). However, when the duty cycle is low, as shown in Fig. 5.2(b), the computation delay increases from 0 to $0.5T_{sw}$, and the control delay increases from $0.5T_{sw}$ to T_{sw}. Based on the geometric principle, the critical duty cycle is given in (5.2), which is determined by the code processing time T_{cp}.

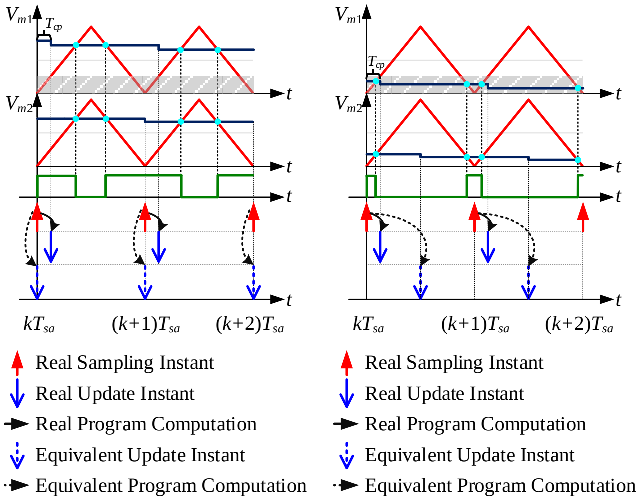
$$\begin{cases} T_{d\_SVSRTU} = \underset{\text{computation delay}}{0} + \underset{\text{PWM delay}}{0.5T_{sw}} = 0.5T_{sw} \quad d \geq d_{cri} \\ T_{d\_SVSRTU} = \underset{\text{computation delay}}{0.5T_{sw}} + \underset{\text{PWM delay}}{0.5T_{sw}} = T_{sw} \quad d < d_{cri} \end{cases} \tag{5.1}$$

$$d_{cri} = \frac{2T_{cp}}{T_{sw}} \tag{5.2}$$

Substituting (5.1) to (3.9), the dissipative region is given as

$$\begin{cases} f_{dissipative\_SVSRTU} = (0, \frac{1}{2} f_{sw}) \quad d \geq d_{cri} \\ f_{dissipative\_SVSRTU} = (0, \frac{1}{4} f_{sw}) \quad d < d_{cri} \end{cases} \tag{5.3}$$

It can be seen from (5.3) that the dissipative region is shrunk when the duty cycle is lower than the critical value.


V_{m1}
T_{cp}
V_{m2}
t
kT_{sa}
$(k+1)T_{sa}$
$(k+2)T_{sa}$
Real Sampling Instant
Real Update Instant
Real Program Computation
Equivalent Update Instant
Equivalent Program Computation

(a) (b)

Fig. 5.2. Single-valley-sampling real-time-upate PWM. (a) Without duty cycle limitation, (b) With duty cycle limitation. Source: [J1].

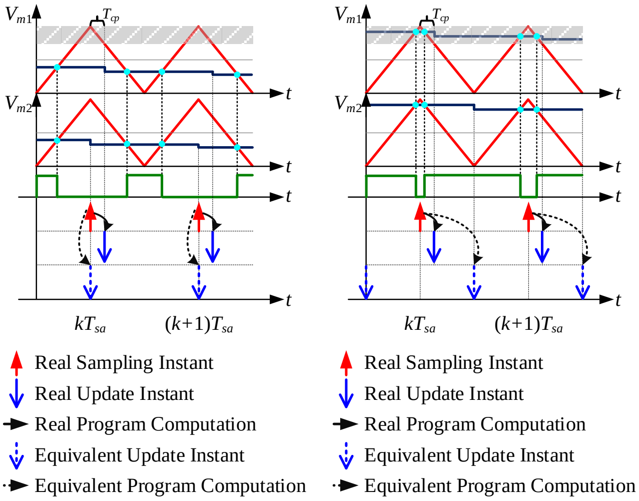
Compared with the SVSRTU PWM, the sampling instant is located at the peak of the carrier for the SPSRTU PWM. As shown in Fig. 5.3, the critical duty cycle is

$$d_{cri} = 1 - \frac{2T_{cp}}{T_{sw}} \tag{5.4}$$

For the SPSRTU PWM, when the duty cycle is smaller than the critical value, only the single-sampling PWM delay $0.5T_{sw}$ remains (see (5.5)). When the duty cycle is larger than the critical value, the computation delay increases from 0 to $0.5T_{sw}$, and the control delay increases from $0.5T_{sw}$ to T_{sw}. The dissipative region for SPSRTU PWM is given in (5.6). Moreover, for the single-sampling real-time-update PWM, the performance on the control delay reduction can still not meet the passivity requirement even though the duty cycle is not limited.

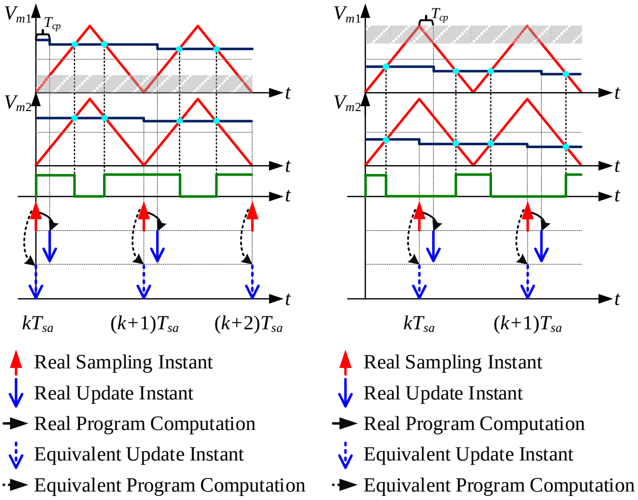
$$\begin{cases} T_{d\_SPSRTU} = \underbrace{0}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} = 0.5T_{sw} & d \le d_{cri} \\ T_{d\_SPSRTU} = \underbrace{0.5T_{sw}}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} = T_{sw} & d > d_{cri} \end{cases} \tag{5.5}$$

$$\begin{cases} f_{dissipative\_SPSRTU} = (0, \frac{1}{2} f_{sw}) & d \le d_{cri} \\ f_{dissipative\_SPSRTU} = (0, \frac{1}{4} f_{sw}) & d > d_{cri} \end{cases} \tag{5.6}$$


V_{m1}
T_{cp}
V_{m2}
t
kT_{sa}
$(k+1)T_{sa}$
Real Sampling Instant
Real Update Instant
Real Program Computation
Equivalent Update Instant
Equivalent Program Computation

(a) (b)

Fig. 5.3. Single-peak-sampling real-time-update PWM. (a) Without the duty cycle limitation, (b) With the duty cycle limitation. Source: [J1].


V_{m1}
T_{cp}
V_{m2}
t
kT_{sa}
$(k+1)T_{sa}$
$(k+2)T_{sa}$
Real Sampling Instant
Real Update Instant
Real Program Computation
Equivalent Update Instant
Equivalent Program Computation

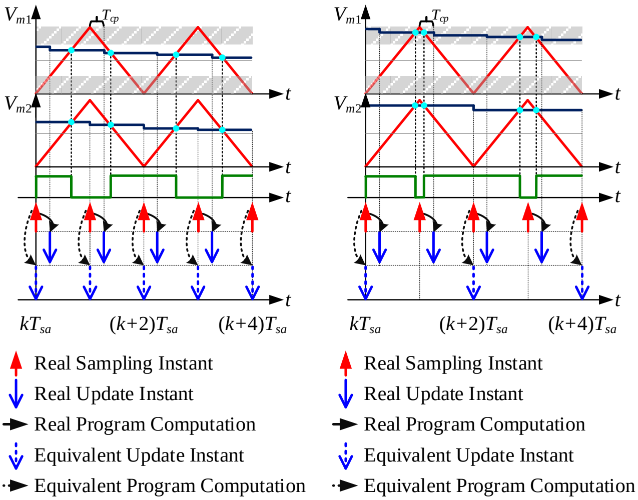
(a) (b)

Fig. 5.4. Real-time-update PWM without duty cycle limitation. (a) Positive half cycle of modulation signal, (b) Negative half cycle of modulation signal. Source: [J1].

Combining SVSRTU PWM and SPSRTU PWM, the control delay can be always maintained as $0.5T_{sw}$ (see (5.7)), i.e., without duty cycle limitation (WDCL) PWM [86]. It can be seen in Fig. 5.4 that the shaded areas are same in the positive half cycle and negative half cycle of modulation signal. Moreover, the sampling instants will switch between the peak and valley of carrier according to the amplitude of duty cycle. As a result, the dissipation for WDCL PWM can be optimized to $0.5f_{sw}$, as given in (5.7). and the dissipative region is given in (5.8). Note that WDCL PWM cannot strictly be regarded as a single-sampling PWM but as a kind of double-sampling PWM, because the sampling instant is switched between the peak and the valley of the carrier. Further, by substituting d_{cri}=0.5 into (5.4), the maximum allowed computation time for WDCL PWM is also acceptable $0.25T_{sw}$.

$$T_{d\_WDRL} = \underset{\text{computation delay}}{0} + \underset{\text{PWM delay}}{0.5T_{sw}} = 0.5T_{sw} \tag{5.7}$$

$$f_{dissipative\_WDRL} = (0, \frac{1}{2} f_{sw}) \tag{5.8}$$


V_{m1}
T_{cp}
t
V_{m2}
t
t
t
kT_{sa}
$(k+2)T_{sa}$
$(k+4)T_{sa}$
Real Sampling Instant
Real Update Instant
Real Program Computation
Equivalent Update Instant
Equivalent Program Computation
V_{m1}
T_{cp}
t
V_{m2}
t
t
t
kT_{sa}
$(k+2)T_{sa}$
$(k+4)T_{sa}$
Real Sampling Instant
Real Update Instant
Real Program Computation
Equivalent Update Instant
Equivalent Program Computation

(a) (b)

Fig. 5.5. Double-sampling real-time update PWM. (a) Without the duty cycle limitation, (b) With the duty cycle limitation. Source: [C3].

Double-sampling real-time-update PWM (DSRTU) can be applied as well [83, 88]. Similar to the single-sampling real-time-update PWM, the control delay is equal to the PWM delay when the duty cycle is smaller than the critical value, as shown in Fig. 5.5(a). However, when the duty cycle is larger than the critical value (see Fig. 5.5(b)), DSRTU is the same as the single-sampling real-time-update PWM without duty cycle limitation. As a result, the dissipation still cannot be achieved based on the control delay in (5.9) and the dissipative region in (5.10). Compared with WDCL PWM, DSRTU PWM can optimize the control delay to the critical delay $0.25T_{sw}$ when the code process time is short enough. For example, if $T_{cp} \leq 0.005T_{sw}$, the duty cycle can be in the interval of (0.01, 0.99). In addition, when the duty cycle is limited, the control delay can be the same as WDCL PWM. In addition, the maximum allowed computation time decreases from $0.25T_{sw}$ to $0.125T_{sw}$. To summarize, although DSRTU PWM can be a potential candidate to achieve the dissipation below the

Nyquist frequency, the requirement for the computation speed of microprocessors is high. Once the duty cycle is limited, the dissipation in the high-frequency range will be jeopardized.

$$\begin{cases} T_{d\_DSRTU} = \underset{\text{computation delay}}{0} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} = 0.25T_{sw} & \frac{2T_{cp}}{T_{sw}} \le d \le 1-\frac{2T_{cp}}{T_{sw}} \\ T_{d\_DSRTU} = \underset{\text{computation delay}}{0} + \underset{\text{PWM delay}}{0.5T_{sw}} = 0.5T_{sw} & others \end{cases} \tag{5.9}$$

$$\begin{cases} f_{dissipative\_DSRTU} = (0,\ f_{sw}) & \frac{2T_{cp}}{T_{sw}} \le d \le 1-\frac{2T_{cp}}{T_{sw}} \\ f_{dissipative\_DSRTU} = (0, \frac{1}{2} f_{sw}) & others \end{cases} \tag{5.10}$$

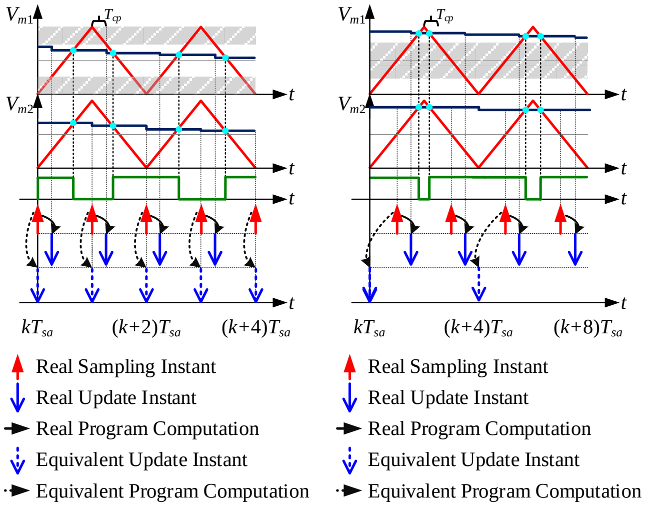
5.3. ENHANCED REAL-TIME-UPDATE CURRENT CONTROL

In order to remove the duty cycle limitation of the DS PWM, an ERTU PWM using the multi-sampling concept is proposed in this chapter. As shown in Fig. 5.6(a), the sampling instants are the same as the DSRTU PWM when the duty cycle is lower than the critical value. On the other hand, when the duty cycle is larger than the critical value, the sampling instants are moved to the middle points of the carrier. As shown in Fig. 5.6(b), the computation delay is -0.25T_{sw} which achieves a phase-leading function. Note that the PWM delay is the same as the single-sampling PWM delay, and the total control delay is $-0.25T_{sw}+0.5T_{sw}=0.25T_{sw}$, which is given in (5.11). Moreover, the negative computation delay concept is inspired by the conventional four-sampling in Fig. 2.3, which can also be regarded as a four-sampling PWM due to the number of used current samples. Consequently, the dissipation can be achieved using single-loop control, as given in (5.12).

$$\begin{cases} T_{d\_ERTU\_PWM} = \underset{\text{computation delay}}{0} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} = 0.25T_{sw} & \frac{2T_{cp}}{T_{sw}} \le d \le 1-\frac{2T_{cp}}{T_{sw}} \\ T_{d\_ERTU\_PWM} = \underset{\text{computation delay}}{-0.25} + \underset{\text{PWM delay}}{0.5T_{sw}} = 0.25T_{sw} & others \end{cases} \tag{5.11}$$

$$f_{dissipative\_ERTU} = (0,\ f_{sw}) \tag{5.12}$$

On the other hand, the sampling instants are switched to the middle points of the carrier when the duty cycle is larger than the critical value, and the non-average current is used for the control. But the introduced low-order aliasing is minimum compared with the case where the sampling instant is shifted to other points. Moreover, when the code processing time is shorter, the duration time using the currents at the middle points of the carrier within one fundamental period will be shorter, i.e., the shaded area in Fig. 5.6(a). Consequently, the aliasing effect caused by the middle points sampling will be weakened. Based on (5.11), if $T_{cp}=0.25T_{sw}$, ERTU PWM changes back to WDCL PWM. If $T_{cp}=0.125T_{sw}$, the shaded area and the unshaded area in Fig. 5.6(a) are the same. Therefore, T_{cp} is recommended to $0.0625T_{sw}$ for ERTU PWM, the shaded area occupies 1/4 and the maximum allowed computation time is the same with sixteen-sampling.



(a) (b)

Fig. 5.6. Enhanced real-time-update PWM with double-sampling. (a) Sampling at Peak/valley point of carrier, (b) Sampling at middle point of carrier. Source: [C3].

TABLE 5.1. Comparison between real-time-update PWM and multi-sampling PWM. Source: [C3] and [J1].

PWM methods / Index	SVSRTU (see Fig. 5.2)	SPSRTU (see Fig. 5.3)	WDCL (see Fig. 5.4)	DSRTU (see Fig. 5.5)	MS with an anti-aliasing filter (see Fig. 2.3)	ERTU (see Fig. 5.6)
Control delay	$\frac{1}{2}T_{sw}$	$\frac{1}{2}T_{sw}$	$\frac{1}{2}T_{sw}$	$\frac{1}{4}T_{sw}$	$(\frac{1.5}{N}+\frac{1}{4})T_{sw}$	$\frac{1}{4}T_{sw}$
Dissipative region	$(0, \frac{1}{2}f_{sw})$	$(0, \frac{1}{2}f_{sw})$	$(0, \frac{1}{2}f_{sw})$	$(0, f_{sw})$	$(0, \frac{N}{6+N}f_{sw})$	$(0, f_{sw})$
Aliasing	No	No	No	No	No	Small
Duty cycle limitation	Yes	Yes	No	Yes	No	No
Maximum allowed computation time	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{8}T_{sw}$	$\frac{1}{N}T_{sw}$	$\frac{1}{16}T_{sw}$

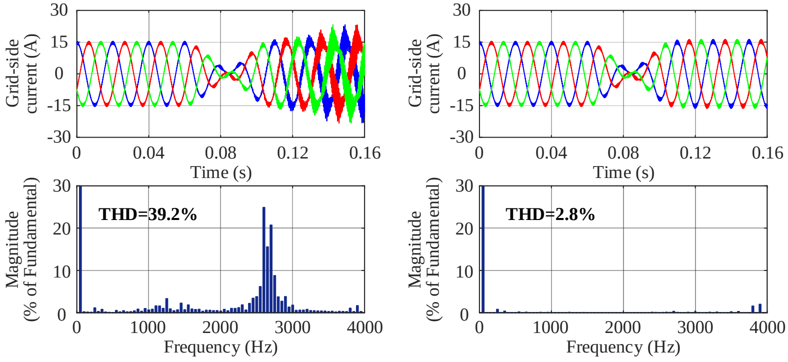
SVS: Single-valley-sampling real-time-update, SPS: Single-peak-sampling real-time-update, WDCL: Without the duty cycle limitation, DS: Double-sampling real-time-update, MS: Multi-sampling, ERTU: Enhanced real-time-update.

Then the proposed ERTU PWM can not only optimize the control delay to the critical value and achieve the dissipation up the Nyquist frequency, but has also the same computation burden with sixteen-sampling. In addition, ERTU PWM has a constant control delay, which simplifies the system modeling compared with the piecewise control delay in DSRTU PWM. To further clarify the advantage of ERTU PWM, a comparison among various PWM methods is given in Table 5.1, and their priority is given as follows.

1) If $T_{cp} \leq 0.005T_{sw}$, select DSRTU PWM where $T_d = 0.25T_{sw}$ and $d \in (0.01, 0.99)$;
2) If $0.005T_{sw} < T_{cp} \leq T_{sw}/16$, select ERTU PWM where $T_d = 0.25T_{sw}$ and $d \in (0, 1)$;
3) If $T_{sw}/16 < T_{cp} < T_{sw}/6$, select MS PWM with an anti-aliasing filter where $0.25T_{sw} < T_d < 0.5T_{sw}$ and $d \in (0, 1)$;
4) If $T_{sw}/6 \leq T_{cp} \leq 0.25T_{sw}$, select WDCL PWM where $T_d = 0.5T_{sw}$ and $d \in (0, 1)$.

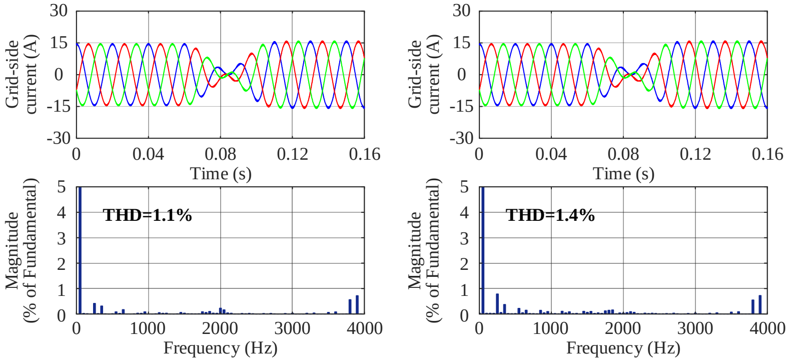
5.4. CASE STUDIES

To investigate the validity of the proposed method, two cases with different filter capacitances are studied through simulations. Table 5.2 gives the parameter of the used three-phase grid-connected inverter. i_{invq}^{*} changes from 15 A to -15A in order to simulate the duty cycle limitation. For Case 1 with C=3 μF and f_r=2517 Hz, as shown in Fig. 5.7, the system is not stable with DS real-time-update PWM because the resonance frequency is located in the non-dissipative region in (5.10). ERTU PWM can make the system stable instead, which is consistent with the theoretical analysis in Section 5.3. For Case 2 with C=6 μF and f_r=1779 Hz, as shown in Fig. 5.8, the system can be stable for DS real-time-update PWM and ERTU PWM, and the grid-side current quality is similar.



(a) (b)

Fig. 5.7. Simulation results of Case 1 (C=3 μF and f_r=2517 Hz). (a) Double-sampling real-time-update PWM, (b) Enhanced real-time-update PWM. Source: [C3].



(a) (b)

Fig. 5.8. Simulation results of Case 2 (C=6 μF and f_r=1779 Hz). (a) Double-sampling real-time-update PWM, (b) Enhanced real-time-update PWM. Source: [C3].

TABLE 5.2. Main parameters of a three-phase grid-connected VSC. Source: [C3].

Symbol	Description	Value	Symbol	Description	Value
P_o	Output power	7 kW	U_{grms}	Grid voltage	220 V
U_{dc}	DC-link voltage	700 V	L_1	Inverter-side inductance	4 mH
L_2	Grid-side inductance	2 mH	C	Filter capacitance	3/6 μF (Case 1/Case 2)
f_{sw}	Switching frequency	4 kHz	T_{cp}	Computation time	T_{sw} /16
K_p	Proportional coefficient	20	K_r	Integral coefficient	1000

5.5. SUMMARY

This chapter investigates the duty cycle limitation phenomenon when using real-time-update PWM. It is revealed that the control delay will increase when the duty cycle is larger than the critical value, which jeopardizes high-frequency dissipation. In order to optimize the control delay to the critical value ($0.25T_{sw}$), an enhanced real-time-update PWM is proposed by switching the sampling instants when the duty cycle is limited. Consequently, the control delay can always be kept to the critical value and the dissipation is achieved up to the Nyquist frequency. Finally, the proposed method is validated through simulations.

Related publications:
[J1] **S. He**, D. Zhou, X. Wang, Z. Zhao, and F. Blaabjerg, “A review of multi-sampling techniques in power electronics applications,” *IEEE Trans. Power Electron., early access,* 2022.
[C2] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, “Switching harmonics suppression of single-loop multi-sampling control of grid-connected inverter”, in *Proc. IEEE IECON,* pp. 3259-3264, 2020.
[C3] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, “Enhanced real-time-update current control for grid-following inverters,” in *Proc. IEEE PEDG.*, 2022 (Accepted).

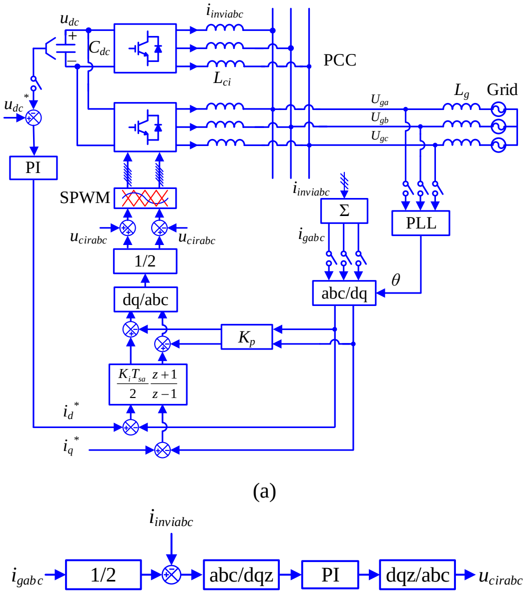
CHAPTER 6. CONTROL OF INTERLEAVED THREE-PHASE INVERTERS WITH GRID IMPEDANCE ESTIMATION

6.1. BACKGROUND

In light of the rise in the power level of renewable generation, interleaved three-phase grid-connected VSC is a competitive candidate where multiple modules are connected in parallel (see Fig. 6.1). Further, a set of benefits are harvested such as increased capacity, current sharing of switching devices, and the reduced output current ripple [88]. There are two current control loops including the main current control loop and the circulating current control loop. One typical control method is to control every VSC module separately, but the system stability may be jeopardized since the two control loops are coupled [89]. Fig. 6.1 presents a decoupled current control strategy, where the power sharing can be achieved by controlling the PCC currents, and the inverter-side currents are used to suppress the circulating current [90]. Nevertheless, only the regular single/double-sampling is used in the control, and the bandwidth and the system stability will be weakened by the control delay.

Under a weak grid having a low short circuit ratio, the stability in the low-frequency range is mainly challenged by PLL, dc-link voltage controller, and alternating voltage controller, and the control delay only affects the stability in the high-frequency range. Besides adding the virtual damping, grid impedance estimation is also an alternative solution to enhance the low-frequency stability [91-92]. Active estimation methods mainly rely on the disturbance injection to the inverter, and the effect on the control of the inverter should be further researched [93-95]. By only utilizing the sampled current/voltage information, the grid impedance can be also estimated through passive estimation methods [96-97]. Unfortunately, the robustness analysis and the parameter design are often complicated.

This chapter proposes a multi-sampling control strategy for a two-cell interleaved three-phase VSC. The sampling rate selection and the controller design for the PCC current regulation and the circulating current suppression are discussed. In addition, the grid impedance is estimated based on the four-sampled PCC voltage under an inductive grid, and the effect of sampled noise is also considered. Finally, the effectiveness of the findings is verified through the experiments.


u_{dc}
C_{dc}
$i_{inviabc}$
L_{ci}
PCC
L_g
Grid
U_{ga}
U_{gb}
U_{gc}
u_{dc}^*
PI
SPWM
u_{cirabc}
u_{cirabc}
1/2
dq/abc
K_p
$\frac{K_i T_{sa}}{2} \frac{z+1}{z-1}$
i_d^*
i_q^*
$i_{inviabc}$
Σ
i_{gabc}
abc/dq
PLL
θ
$i_{inviabc}$
i_{gabc}
1/2
abc/dqz
PI
dqz/abc
u_{cirabc}

(a)

(b)

Fig. 6.1. Current control diagram of an interleaved two-cell three-phase VSC. (a) PCC current control loop, (b) Circulating current control loop. Source: [C4].

6.2. SAMPLING RATE SELECTION

Due to the interleaved modulation, the apparent switching frequency seen from the PCC can increase with the number of the paralleled cells as given in (6.1).

$$f_{ap\_sw} = Nf_{sw} \tag{6.1}$$

Where f_{ap_sw}, N, and f_{sw} is the apparent switching frequency, the number of interleaved cells, and the switching frequency for every cell, respectively. Hence, the maximum sampling frequency without noise can be set as twice larger than the apparent switching frequency, i.e., the equivalent double-sampling in Chapter 3, and the expression is given in (6.2).

$$f_{sa} = 2 f_{ap\_sw} \tag{6.2}$$

According to Fig. 6.2, the average value of current can be obtained using four-sampling, which is the same as the single-phase VSC. However, the average output voltages for two modules are affected by the update rate, thereby causing the current unbalance among paralleled modules. For instance, in the positive half cycle, the average output voltages for two modules are different when using the four-sampling four-update PWM, which are given in (6.3).

$$\begin{cases} i_{inv1}(k+4)-i_{inv1}(k)=L_{c1}(d_2+d_3)\dfrac{u_{dc}}{2} \\ i_{inv2}(k+4)-i_{inv2}(k)=L_{c2}(d_1+d_4)\dfrac{u_{dc}}{2} \end{cases} \tag{6.3}$$

where i_{inv1}~i_{inv2} and L_{c1}~L_{c2} are the inverter-side currents and the filter inductance for every single cell, d_1~d_4 are the four-updated duty cycles. It can be seen that the average output voltages for two VSC modules are different, and the low-frequency circulating current will be introduced [98-100]. If using four-sampling double-update PWM, the average output voltage for two modules are same, as given in (6.4). As a result, the low-frequency circulating current is removed if the parallel two modules are the same, which simplifies the circulating current control. Hence, the four-sampling double-update PWM is selected for the control of two-cell interleaved inverters.

$$\begin{cases} i_{inv1}(k+4)-i_{inv1}(k)=L_{c1}(d_1+d_3)\dfrac{u_{dc}}{2} \\ i_{inv2}(k+4)-i_{inv2}(k)=L_{c2}(d_1+d_3)\dfrac{u_{dc}}{2} \end{cases} \tag{6.4}$$

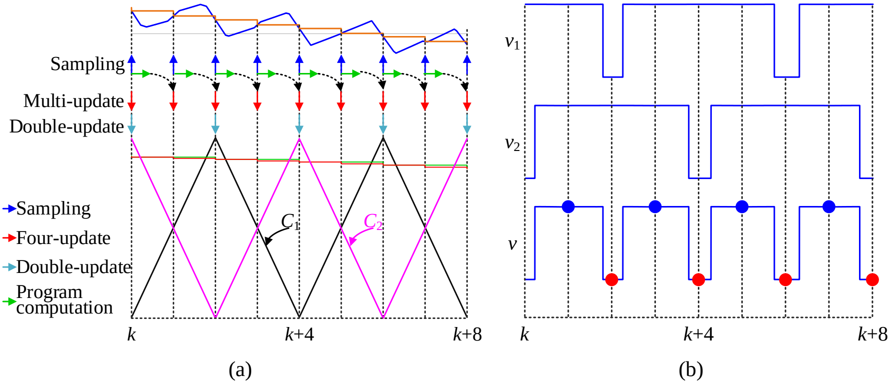


Fig. 6.2. PWM process and sampling rate selection for two-cell interleaved three-phase VSCs. (a) Sampling and modulation, (b) Pulse pattern. Source: [C4].

6.3. CONTROLLER DESIGN

Fig. 6.1 shows the overall control diagram of the two-cell interleaved three-phase inverter, where the inverter-side sensors for every module are used for the overcurrent protection and circulating current control. The PCC current is calculated from the sum of the inverter-side currents. The mathematic model of the main current control loop is shown in Fig. 6.3, the open-loop transfer function of the inner loop is given in (6.5) and the plant model is given in (6.6). As four-sampling double-update PWM is the same as the double-sampling PWM with the sampling instant shift, hence the computation delay reduces from $0.5T_{sw}$ to $0.25T_{sw}$. Combined with the double-sampling PWM delay 0.25Tsw, the total control delay is $0.25T_{sw}+0.25T_{sw}=0.5T_{sw}$, as shown in (6.7).

$$T_{oin} = \frac{K_p}{2} G_d(s) G_{igv}(s) \tag{6.5}$$

$$G_{igv}(s) = \frac{L_{c1} + L_{c2}}{s L_{c1} L_{c2}} \tag{6.6}$$

$$G_d(s) = e^{-0.5 s T_{sw}} \tag{6.7}$$

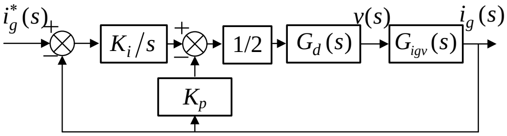


Fig. 6.3. Model of PCC current control loop. Source: [C4].

Table 6.1 gives the main parameters of the used interleaved inverter. Given the 45° phase margin (PM), the bandwidth can be designed to 500 Hz with the proposed four-sampling double-update control method. As shown in Fig. 6.4, the double-sampling control can only achieve a bandwidth of 333 Hz since the control delay is larger ($T_d = 0.5T_{sw} + 0.25T_{sw} = 0.75T_{sw}$). Hence, the proposed control method can achieve a lower control delay and a higher control bandwidth, thereby the dynamic performance can be enhanced.

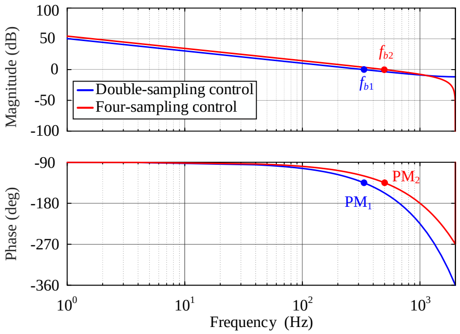


Fig. 6.4. Bode diagram of the inner loop of PCC current control loop. Source: [C4].

As the inverter-side current for every module is sampled for the circulating current suppression, the SHs are introduced when using four-sampling. A RF should be inserted in the feedback path [30], as shown in Fig. 6.5. The open-loop transfer function for the circulating current control loop is shown in (6.8), and the expression for the RF is shown in (6.10).

$$T_{ocir} = 2K_{pc} RF(s) G_d(s) G_{icirv}(s) \tag{6.8}$$

$$G_{icirv}(s) = \frac{1}{s(L_{c1} + L_{c2})} \tag{6.9}$$

$$RF(s) = 0.5(1 + e^{-0.5 s T_{sw}}) \tag{6.10}$$

Because a $0.25T_{sw}$ delay is introduced from RF, the total loop delay using four-sampling double-update control is $0.5T_{sw}+0.25T_{sw}=0.75T_{sw}$ which is the same as the double-sampling control. As a result, both control methods can achieve the same bandwidth (333 Hz) and the phase margin (45°), as shown in Fig. 6.6. It can be concluded that double-sampling is recommended in the circulating current control loop since the SHs are not introduced and the control implementation is simpler.

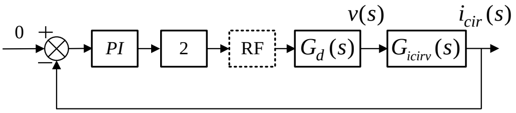


Fig. 6.5. Model of the circulating current control loop. Source: [C4].

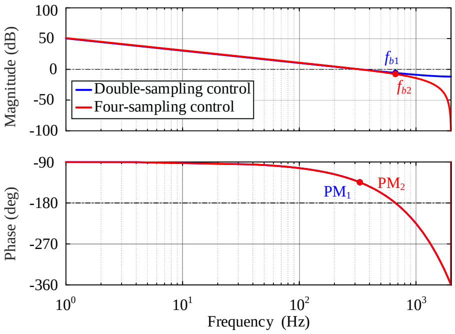


Fig. 6.6. Bode diagram of circulating current control loop. Source: [C4].

TABLE 6.1. Main parameters of an interleaved three-phase two-cell grid-connected VSC. Source: [C4].

Symbol	Description	Value	Symbol	Description	Value
U_{dc}	DC-link voltage	200 V	U_g	Grid voltage	90 V
P_o	Output power	3 kW	L_c	Converter-side inductance	2 mH
f_{sa}	Sampling frequency	4/8 kHz	f_{sw}	Switching frequency	2 kHz
C_{dc}	DC-link capacitance	594 µF	T_{dead}	Dead time	3 µs
K_{p2}	Proportional gain	4.1	K_{i2}	Integral gain	2000
K_{p4}	Proportional gain	6.6	K_{i4}	Integral gain	5000
K_{pc2}	Proportional gain	4.1	K_{ic2}	Integral gain	500
K_{pc4}	Proportional gain	4.1	K_{ic4}	Integral gain	500

6.4. GRID IMPEDANCE ESTIMATION

Fig. 6.7 shows the single-phase equivalent circuit of a two-cell interleaved inverter, where L_g is the grid impedance. As discussed in Section 6.3, the average value of PCC currents can be obtained using four-sampling. However, the four-sampled PCC voltage within one switching period is still not utilized besides the grid synchronization. Herein, a simple grid impedance method under an inductive grid is proposed based on the sampled PCC voltage at different instants.

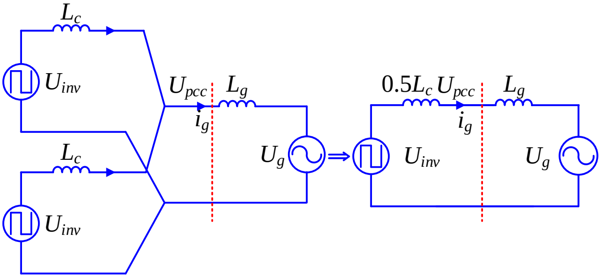


Fig. 6.7. Equivalent circuit for a two-cell interleaved VSC. Source: [C5].

Based on Fig. 6.7, the PCC voltage and the grid-side current are given in (6.11) and (6.12).

$$U_{pcc} = sL_g i_g + U_g \tag{6.11}$$

$$i_g = \frac{U_{inv} - U_g}{s(L_{ceq} + L_g)} \tag{6.12}$$

Substituting (6.12) into (6.11), the variable i_g is removed and the PCC voltage is re-written as in (6.13).

$$U_{pcc} = \frac{L_{ceq}}{L_{ceq} + L_g} U_g + \frac{L_g}{L_c + L_g} U_{inv} \tag{6.13}$$

Further, considering the inverter output voltage difference at peak/valley and the intersection points of the carriers, the PCC voltage is given in (6.14) and (6.15), respectively.

$$U_{pccpeak/valley} = \frac{L_{ceq}}{L_{ceq} + L_g} U_{gpeak/valley} \tag{6.14}$$

$$U_{pcc\,\mathrm{int}\,er} = \frac{L_{ceq}}{L_{ceq} + L_g} U_{g\,\mathrm{int}\,er} + \frac{L_g}{L_{ceq} + L_g} U_{inv\,\mathrm{int}\,er} \tag{6.15}$$

Using the sampled PCC voltage bias $U_{pcc\,\mathrm{int}\,er} - U_{pccpeak/valley}$, the expression of grid impedance can be deduced in (6.16). Since the sampled grid voltage bias $U_{g\,\mathrm{int}\,er} - U_{gpeak/valley}$ is small, the grid impedance can be simplified as (6.17).

$$\begin{aligned} L_g &= L_{ceq}\frac{U_{pcc\,inter}-U_{pccpeak/valley}}{U_{inv\,inter}-(U_{pcc\,inter}-U_{pccpeak/valley})} \\ &\quad -\underbrace{L_{ceq}\frac{U_{g\,inter}-U_{gpeak/valley}}{U_{inv\,inter}-(U_{pcc\,inter}-U_{pccpeak/valley})}}_{\text{Sampeld grid voltage bias}} \end{aligned} \tag{6.16}$$

$$L_{gest} = L_{ceq}\frac{U_{pcc\,inter}-U_{pccpeak/valley}}{U_{inv\,inter}-(U_{pcc\,inter}-U_{pccpeak/valley})} \tag{6.17}$$

Further, besides the sampled PCC voltage, only the inverter output voltage at the intersection point of the phase-shifted carriers is required for the grid impedance estimation. The expression of the inverter output voltage is given in (6.18), where *x* represents phase *a*, phase *b*, phase *c*, *y* is the VSC module number.

$$U_{inv\,inter\,x} = \frac{u_{dc}}{4}\sum_{y=1}^{2}\left(sign(m_{xy})-\sum_{x=a}^{c} sign(m_{xy})\right) \tag{6.18}$$

Comparing (6.16) and (6.17), the sampled grid voltage bias is the main reason for the grid impedance estimation error. It can be seen from Fig. 6.8 that the estimation error is minimum at the peak point of the grid voltage. Further, the same conclusion can be obtained from the analytic deduction in (6.19) and (6.20).

$$U_{g\,inter}-U_{gpeak/valley} = V\sin(\omega_g t+\omega_g T_{sa})-V\sin(\omega_g t) \tag{6.19}$$

$$U_{g\,inter}-U_{gpeak/valley}\Big|_{\theta=90^\circ/270^\circ} = \pm V\left(\cos(\omega_g T_{sa})-1\right)\approx 0 \tag{6.20}$$

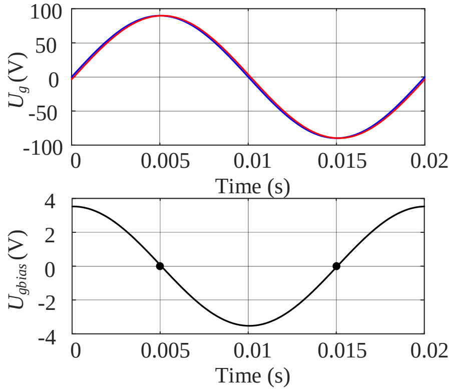


Fig. 6.8. Sampled grid voltage bias analysis. Source: [C5].

Hence, by only using the sampled PCC voltage at the specific phase angle, the grid impedance estimation error can be compensated. Based on the PLL, the specific grid phase angle for phases *a*-*c* is 90°/270°, 30°/210°, and 330°/150°. Fig. 6.9 shows the predicted inverter output voltage at the intersection point of the carriers. It can be observed that the inverter output voltage has six sections where the duration time is the same. To overcome the effect of noise, a moving average calculation is used around the specific angle [52]. For instance, the angle range for phase *a* can be [75°, 105°] and [255°, 285°]. As a result, the grid impedance estimation error can be removed after using the PLL-based moving average calculation, as shown in Fig. 6.10(b)-(c).

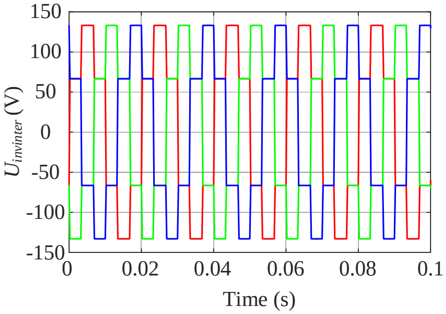


Fig. 6.9. Predicted VSC output voltage at the intersection point of the interleaved carriers. Source: [C5].

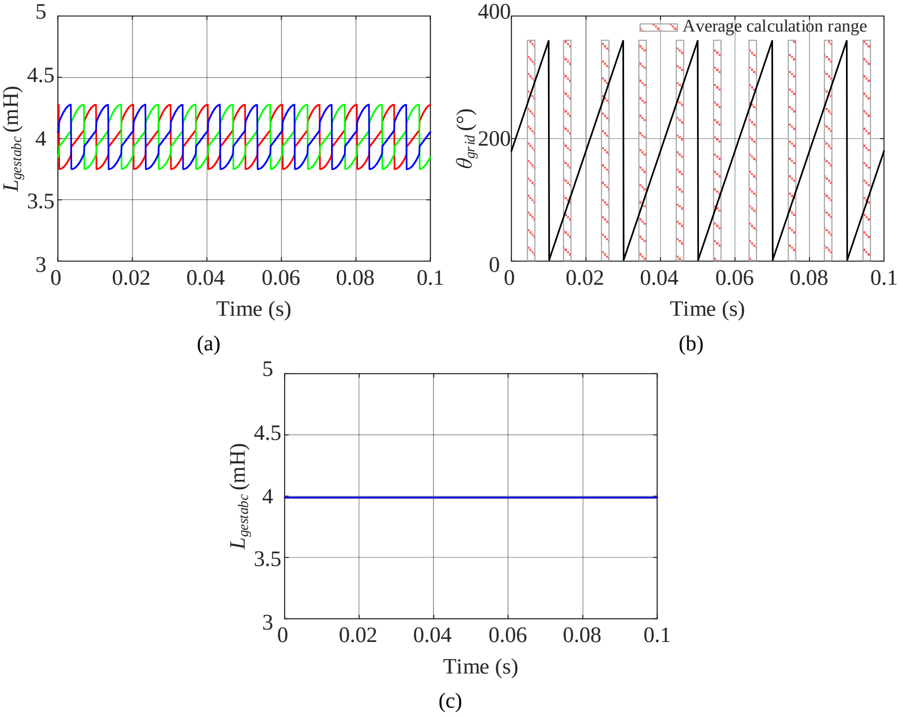


Fig. 6.10. Grid impedance estimation results. (a) Estimated grid impedance without compensation, (b) Grid phase angle, (c) Estimated grid impedance with compensation. Source: [C5].

6.5. CASE STUDIES

To validate the proposed method, experiments are implemented in a VSC system from Imperix, as shown in Fig.6.11. Herein, a two-cell interleaved VSC is used, and the experimental parameters are given in Table 6.1.

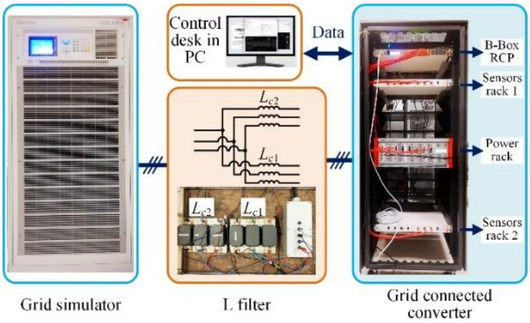
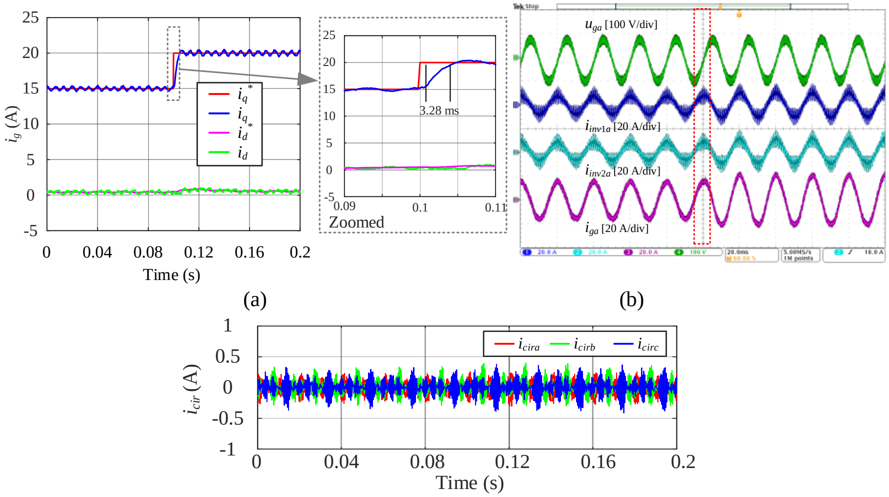

Control desk in PC
Data
B-Box RCP
Sensors rack 1
Power rack
Sensors rack 2
L_{c2}
L_{c1}
Grid simulator
L filter
Grid connected converter

Fig. 6.11. Two-cell three-phase interleaved VSC prototype. Source: [C4].



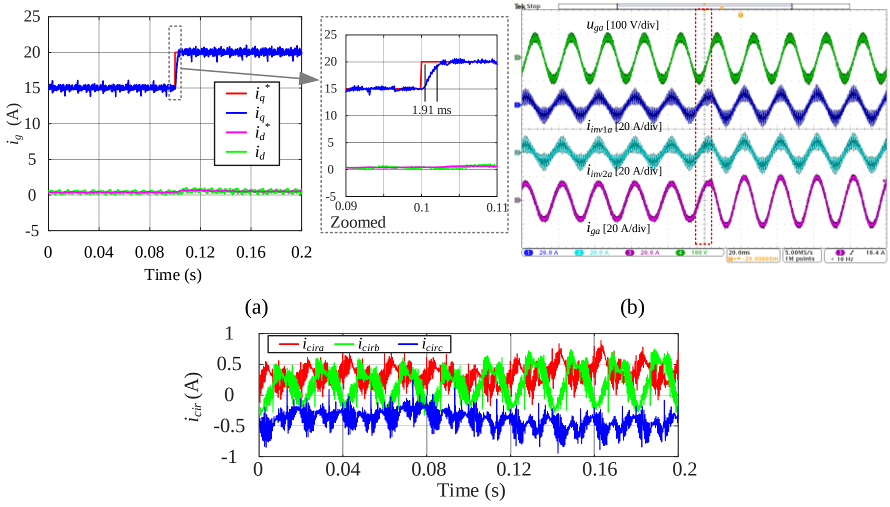
(a) (b)

(c)

Fig. 6.12. Experimental results when using double-sampling double-update control with circulating current suppression. (a) Step response, (b) converter-side currents and PCC currents, (c) Low frequency circulating currents. Source: [C4].

Fig. 6.12 and Fig. 6.13 show the test results for the double- and four-sampling control. Similar noises are observed in the *d*- and *q*-axis for both control methods. In addition, the dynamic performance of the four-sampling control is better. However, as the average output voltages for two VSC modules are not balanced, there is a large circulating current for the four-sampling four-update control where the circulating current control is not used.

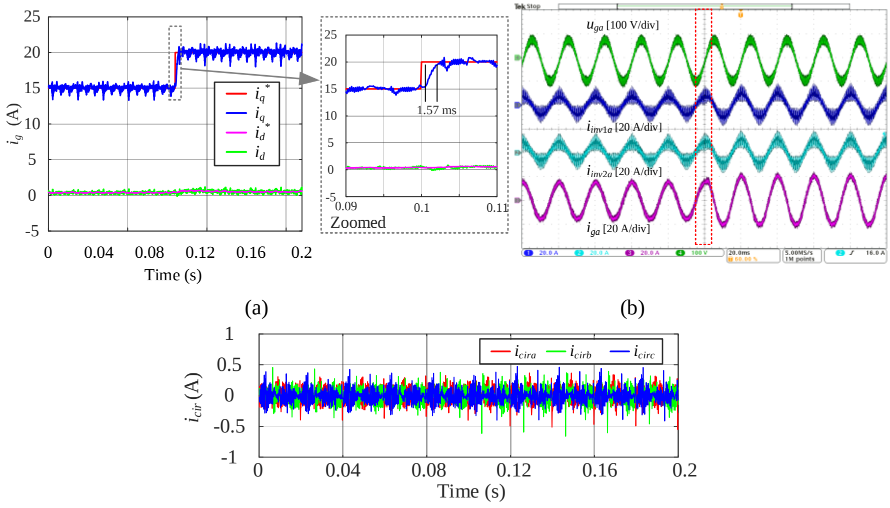
Fig. 6.14 shows that the average voltages for two VSC modules are same, thereby the circulating current is suppressed. In addition, in comparison with the double-sampling double-update control (see Fig. 6.12), this controller performs better in terms of dynamic response.



(a) (b)

(c)

Fig. 6.13. Experimental results when using four-sampling four-update control without circulating current suppression. (a) Step response, (b) Converter-side currents and PCC currents, (c) Low frequency circulating currents. Source: [C4].

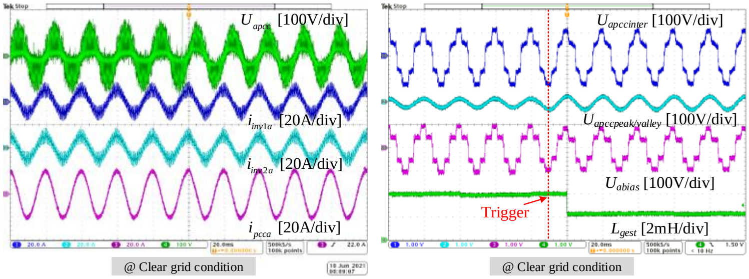


(a) (b)

(c)

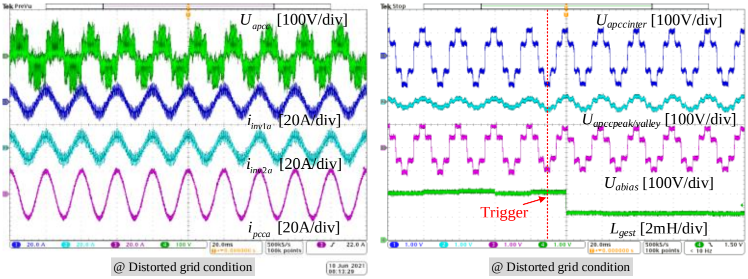
Fig. 6.14. Experimental results when using four-sampling double-update control with circulating current suppression. (a) Step response, (b) Converter-side currents and PCC currents, (c) Low frequency circulating currents. Source: [C4].

Based on four-sampling double-update control, grid impedance estimation can be achieved in the same two-cell three-phase interleaved VSC. Fig. 6.15 (b) indicates that the sampled PCC voltage bias has the same shape as the inverter output voltage, which further supports the theoretical analysis. Additionally, when the grid impedance is manually switched (by operating relay) from 4 mH to 2 mH, the estimator can quickly follow the real value within 10 ms. At the same time, it is found that the influence of sampling noise on the grid impedance estimator is significantly reduced. Under a distorted grid condition, as shown in Fig. 6.16, the grid impedance can also be estimated with the proposed method.



(a) (b)

Fig. 6.15. Grid impedance estimation results under a clear grid condition. (a) Inverter-side current and grid-side current, (b) Sampled PCC voltage and estimated grid impedance. Source: [C5].



(a) (b)

Fig. 6.16. Grid impedance estimation results under a distorted grid condition (10% 5th and 7th grid harmonics). (a) Inverter-side current and grid-side current, (b) Sampled PCC voltage and estimated grid impedance. Source: [C5].

6.6. SUMMARY

A multi-sampled current control strategy for two-cell interleaved three-phase VSCs is presented in this chapter. The average value of PCC can be obtained using four-sampling. Besides, the duty cycle updating rates considering circulating currents are investigated. In comparison with the double-sampling control strategy, the proposed method helps to enhance the bandwidth and dynamic performance. In addition, a grid impedance estimation method utilizing the PCC voltage bias at different sampling instants is proposed. At the same time, a PLL-based moving average calculation is further proposed to remove the effect of noise on the grid impedance estimator Finally, the findings are verified through experiments.

Related publications:
[C4] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, “Multisampling control of two-cell interleaved three-phase grid-connected converters”, in *Proc. IEEE APEC*, pp. 1432-1437, 2021.
[C5] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, “Multisampling based grid impedance estimation for two-cell interleaved three-phase inverters”, in *Proc. IEEE ECCE*, pp. 1432-1437, 2021.

CHAPTER 7. GRID VOLTAGE SENSORLESS CONTROL USING MULTI-SAMPLING

7.1. BACKGROUND

So far, the project discusses the utilization of multi-sampling techniques to enhance the performance of current controllers. Furthermore, by utilizing the multi-sampled data, more controllability can be brought. One typical example is the current derivative estimation, which is widely used in motor drives [101-102], but few works are reported in grid-connected VSCs.

To ensure the reliable operation of LCL-filtered VSCs, grid voltage estimation is preferred to prevent voltage sensor failure and also to save the cost to some extent [103]. The conventional grid voltage estimation methods can be summarized as direct calculation, virtual flux-based, and observer-based methods. The direct way to estimate the grid voltage is by subtracting the voltage drop across the inverter-side inductor from the inverter output voltage [104]. Despite its simplicity, this method can be easily affected by noise due to the derivative operator. The virtual flux concept offers an alternative to derivative operators, but its estimation accuracy is affected by grid harmonics [105-106]. Many observer-based methods are designed based on the grid-side current [107-109], hence the number of current sensors is not reduced considering over-current protection.

Start-up transient is another significant challenge for grid voltage sensorless control. One possible solution is to estimate the initial grid phase angle by injecting a zero voltage vector [110-111]. However, this approach faces a risk of over-current since the injection time is open-loop controlled. Another possible solution is to estimate the grid voltage using grid-side current measurements before the start-up [107]. Nevertheless, this approach is not suitable for applications where the current sensor in the grid-side is omitted.

To address the aforementioned concerns, a multi-sampling-based grid voltage estimator is proposed, which can accurately estimate the grid voltage only using the inverter-side currents. At the same time, a soft start-up method is proposed by controlling the inverter as a boost converter. Finally, the findings are verified through the experiments.

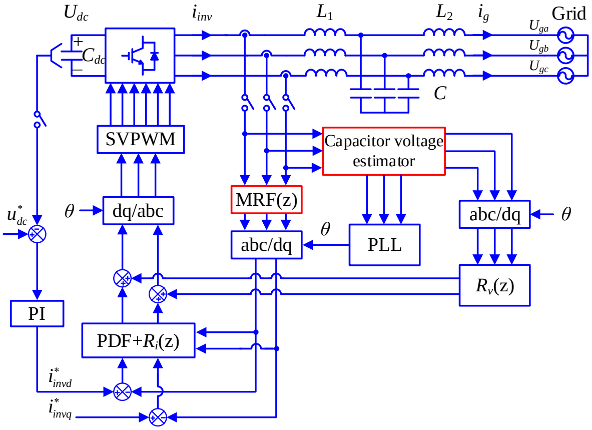

U_{dc}
C_{dc}
i_{inv}
L_1
L_2
i_g
Grid
U_{ga}
U_{gb}
U_{gc}
C
SVPWM
Capacitor voltage estimator
MRF(z)
dq/abc
abc/dq
PLL
abc/dq
R_v(z)
θ
u^*_{dc}
PI
PDF+R_i(z)
i^*_{invd}
i^*_{invq}

Fig. 7.1. Diagram of proposed grid voltage sensorless control for three-phase VSCs (MRF: modified repetitive filter, PDF: pseudo-derivative-feedback). Source: [J4].

7.2. GRID VOLTAGE ESTIMATION

Fig. 7.1 shows the diagram of the proposed grid voltage sensorless control. Similar to Chapter 3, the MRF is used to suppress the sampled SHs. In addition, the filter capacitor voltage is estimated using the sampled current switching ripple, which is then used for the grid synchronization. Further, a PDF controller is used for the fundamental current regulation, and the resonant controllers ($R_i(z)$ and $R_v(z)$) are used for the grid-side current harmonics suppression. As the main focus of this section is grid voltage estimation, the current controller design will be given in Section 7.3. As discussed in Chapter 1, the VSC output voltage is zero during the zero voltage vectors. Hence, according to Fig. 7.2, the idea is to estimate the filter capacitor voltage through the inverter-side current derivative, as given in (7.1). Suppose the inverter-side current changes as a first-order function (see (7.2)), the current derivative a_1 and the intercept a_0 can be estimated using linear regression [45-46], which is given in (7.3).

$$U_c = -L_1 \frac{di_{inv}}{dt} \tag{7.1}$$

$$i(t) = a_1 t + a_0 \tag{7.2}$$

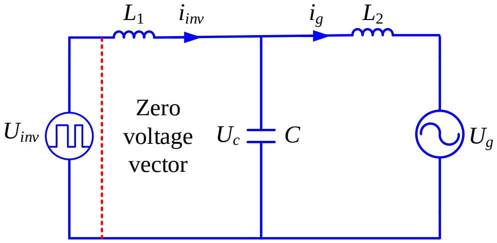

L_1
i_{inv}
i_g
L_2
U_{inv}
Zero voltage vector
U_c
C
U_g

Fig. 7.2. Single-phase equivalent circuit for a three-phase VSC. Source: [J4].

$$\begin{cases} a_1 = \dfrac{\overline{it} - \bar{i}\bar{t}}{\overline{t^2} - \bar{t}^2} = \dfrac{\dfrac{1}{n}\sum\limits_{k=1}^{n} i(t_k)t_k - \dfrac{1}{n^2}\sum\limits_{k=1}^{n} i(t_k)\sum\limits_{k=1}^{n} t_k}{\dfrac{1}{n}\sum\limits_{k=1}^{n} t_k^2 - \dfrac{1}{n^2}(\sum\limits_{k=1}^{n} t_k)^2} \\ a_0 = \bar{i} - a_1\bar{t} = \dfrac{1}{n}\sum\limits_{k=1}^{n} i(t_k) - a_1\dfrac{1}{n}\sum\limits_{k=1}^{n} t_k \end{cases} \tag{7.3}$$

The proposed filter capacitor voltage estimation flowchart is given in Fig. 7.3. Since the current derivative is related to the average values $\overline{it}$, $\bar{i}$, $\bar{t}$, and $\overline{t^2}$, twelve state variables x_1-x_{12} are used to calculate the related products iteratively. Note that the multi-sampling rate affects the dataset of the sampled current, and further affects the filter capacitor voltage estimation accuracy. The minimum dataset should include two samples to achieve the linear regression in (7.3). In this chapter, the fifty-sampling is used, and the maximum allowed output duty cycle and the minimum allowed output duty cycle is 0.96 and 0.04, respectively (see Fig. 7.4).

Yet, if the duty cycle is out of the allowed range, the last current derivative is used and an estimation error is introduced. In light of practical implementation, the update instant of the filter capacitor estimator is fixed at the peak/valley of the carrier, as shown in Fig. 7.5. As a result, the estimated filter capacitor voltage is the same as the double-sampled value, and a half switching period delay is introduced compared with the real value. Hence the output grid phase should be compensated as given in (7.4).

$$\theta_{est} = \theta_{PLL} + 2\pi f_{PLL} \frac{T_{sw}}{2} \tag{7.4}$$

where θ_{est} is the estimated grid phase angle, θ_{PLL} and f_{PLL} are the uncompensated grid phase angle and the estimated grid frequency.

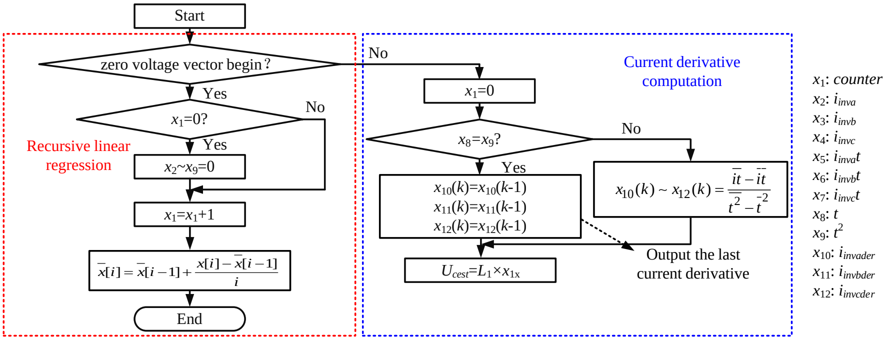

Start
zero voltage vector begin ?
Yes
No
x_1=0?
No
Yes
Recursive linear regression
x_2~x_9=0
x_1=x_1+1
$\bar{x}[i] = \bar{x}[i-1] + \frac{x[i] - \bar{x}[i-1]}{i}$
End
Current derivative computation
x_1=0
x_8=x_9?
No
Yes
$x_{10}(k)$=$x_{10}(k$-1)
$x_{11}(k)$=$x_{11}(k$-1)
$x_{12}(k)$=$x_{12}(k$-1)
$x_{10}(k) \sim x_{12}(k) = \frac{\overline{it} - \bar{i}\bar{t}}{\overline{t^2} - \bar{t}^2}$
Output the last current derivative
U_{cest}=L_1×x_{1x}
x_1: counter
x_2: i_{inva}
x_3: i_{invb}
x_4: i_{invc}
x_5: $i_{inva}t$
x_6: $i_{invb}t$
x_7: $i_{invc}t$
x_8: t
x_9: t^2
x_{10}: $i_{invader}$
x_{11}: $i_{invbder}$
x_{12}: $i_{invcder}$

Fig. 7.3. Proposed filter capacitor voltage estimation flowchart. Source: [J4].

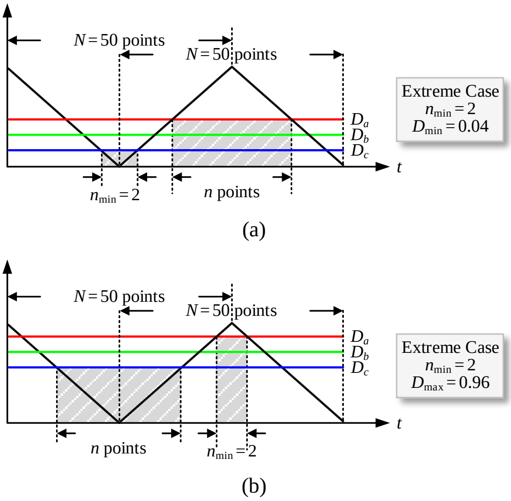

N = 50 points
N = 50 points
Extreme Case
$n_{min} = 2$
$D_{min} = 0.04$
D_a
D_b
D_c
t
$n_{min} = 2$
n points
(a)
N = 50 points
N = 50 points
D_a
D_b
D_c
Extreme Case
$n_{min} = 2$
$D_{max} = 0.96$
t
n points
$n_{min} = 2$
(b)

Fig. 7.4. Duty cycle limitation for the dataset used for linear regression. (a) Minimum duty cycle, (b) Maximum duty cycle. Source: [J4].

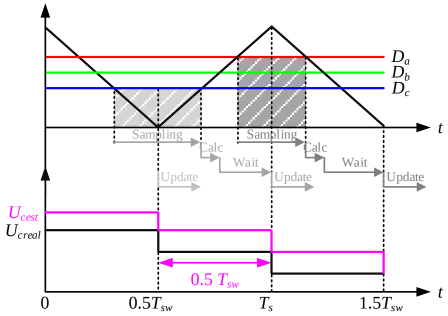
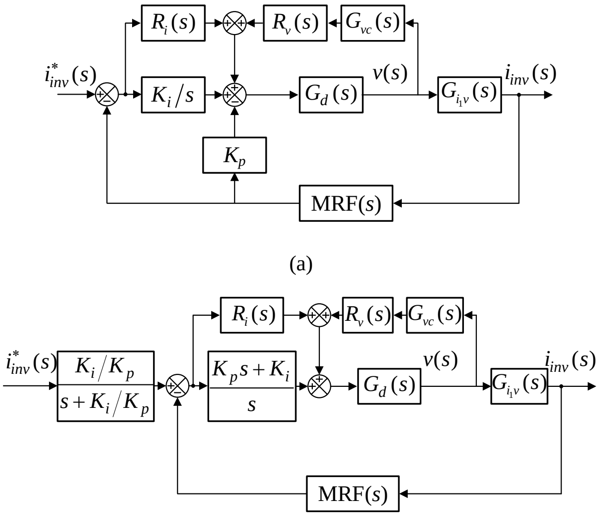

D_a
D_b
D_c
t
Sampling
Calc
Wait
Update
Sampling
Calc
Wait
Update
Update
U_{cest}
U_{creal}
0.5 T_{sw}
t
0
0.5T_{sw}
T_s
1.5T_{sw}

Fig. 7.5. Update scheme of filter capacitor voltage estimator. Source: [J4].

7.3. CONTROLLER DESIGN

The block diagram of the proposed grid voltage sensorless controller is shown in Fig. 7.6. The PI controller is replaced by the PDF controller for the fundamental current regulation. Through the equivalent transformation, the PDF controller is equivalent to a PI controller with an extra low-pass filter [66]. This is why the overshoot can be suppressed in the current control with a high bandwidth, and the time constant K_p/K_i determines the introduced delay from the equivalent low-pass filter. $G_{i1v}(s)$ and G_{vc}(s) represent the transfer function from the U_{inv} to the i_{inv} and U_c, respectively.



(a)

(b)

Fig. 7.6. Model of the current control loop. (a) PDF controller-based control diagram, (b) Equivalent PI controller-based control diagram. Source: [J4].

The resonant controller $R_i(s)$ is inserted in parallel with the PDF controller to suppress the effect of grid harmonics, but the grid-side current distortion still exists because the control target is still the inverter-side current [79]. If the filter capacitor current can be estimated using a derivative operator, and the harmonics in the grid-side current will be fully controlled through another resonant controller $R_v(s)$ as given in (7.5). Based on Fig. 7.6(b). the open-loop transfer function is given in (7.6).

$$R_v(s) = CR_i(s)\underbrace{\frac{1.8}{T_{sa}}\frac{1-e^{-sT_{sa}}}{1+0.8e^{-sT_{sa}}}}_{\text{Digital derivative}} \tag{7.5}$$

$$T_o(s) = (K_p + R_i(s))\frac{G_{i1v}(s)MRF(s)G_d(s)}{1-R_v(s)G_{vc}(s)G_d(s)} \tag{7.6}$$

Table 7.1 shows the used parameters of the three-phase VSC. The bandwidth of the ACC is set as 1/8 of the switching frequency. It can be seen from Fig. 7.7 that similar PMs can be achieved when using IRF and MRF, which are 47.2° and 48.5°, respectively. Moreover, as discussed in Chapter 3, the high-frequency noise can be suppressed by MRF when using a very high sampling rate such as 50.

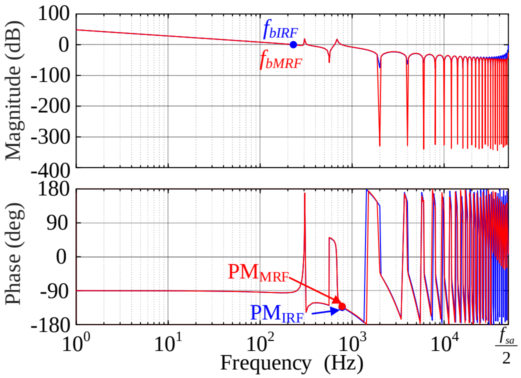


Fig. 7.7. Bode diagram of the current control loop with IRF and MRF (IRF: improved repetitive filter, MRF: modified repetitive filter). Source: [J4].

TABLE 7.1. Main parameters of a grid-connected three-phase VSC. Source: [J4]

Symbol	Description	Value	Symbol	Description	Value
P_o	Output power	7 kW	U_{grms}	Grid voltage	220 V
L_1	Inverter-side inductance	8 mH	C	Filter capacitance	20 μF
L_2	Grid-side inductance	4 mH	C_{dc}	DC-link capacitance	297 μF
f_r	Resonance frequency	689 Hz	U_{dc}	DC-link voltage	600 V
f_{sw}	Switching frequency	2 kHz	f_{sa}	Sampling frequency	100 kHz
K_p	Proportional gain	20.5	K_i	Integral gain	8000
K_{pdc}	Proportional gain	0.03	K_{idc}	Integral gain	0.4
K_{ppre}	Proportional gain	0.1	K_{ipre}	Integral gain	4.5
$K_{pfastpll}$	Proportional gain	933	$K_{ifastpll}$	Integral gain	15550
$K_{pslowpll}$	Proportional gain	41.67	$K_{islowpll}$	Integral gain	723.38

7.4. SOFT START-UP

Two conditions should be satisfied to suppress the start-up transients. The first condition is that the grid voltage should be known in advance, as shown in (7.7). The second condition is that the dc-link voltage should be charged to the reference value otherwise the duty cycle will be saturated.

$$L_1 \frac{di_{inv}}{dt} = U_{inv0} \sin(\omega_1 t + \varphi_{inv0}) - U_{c0} \sin(\omega_1 t + \varphi_{g0}) \tag{7.7}$$

where φ_{inv0} and φ_{g0} are the initial angles, U_{inv0} and U_{c0} are the initial amplitudes for the inverter output voltage and the filter capacitor voltage, respectively. Hence, Traditional zero voltage vector injection is an effective method, where the filter capacitor voltage can be estimated through the multi-sampled current data during the interval of injection. However, the dc-link voltage is not closed-loop controlled which may cause over-current. It can be seen from Fig. 7.8(a) that only the lower three arms are in operation during the injection, and all the arms are locked when stopping the injection. As a result, the output characteristic of the inverter is equivalent to a boost converter [112], as seen in Fig. 7.8(b). The input voltage of the boost converter U_{in} is $\sqrt{3}U_c$, and R_{dis} is used to discharge the dc-link capacitor when the inverter stops operation.

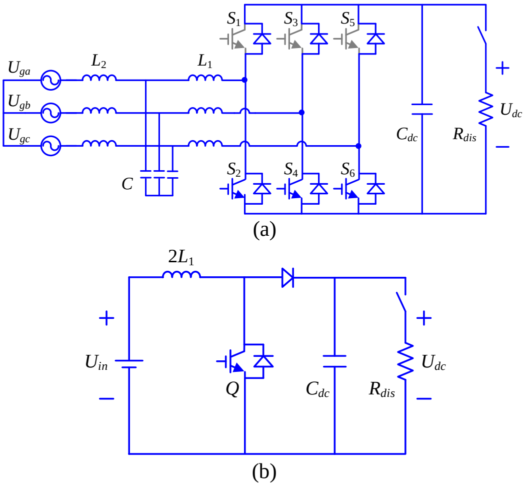


Fig. 7.8. Topology deviation when injecting zero voltage vectors. (a) Three-phase VSC with locked three upper arms, (b) Equivalent boost converter. Source: [J4].

Then, an improved zero voltage vector injection method is proposed where the dc-link voltage is closed-loop controlled, which is presented in Fig. 7.9. In terms of parameter design, the equivalent boost converter will conduct discontinuously as the discharging resistance R_{dis} is larger than the critical load [113], as given in (7.8).

$$R_{dis} > \underbrace{\frac{4L_1}{D_{on}(1-D_{on})^2 T_{sw}}}_{\text{Critical load}} \tag{7.8}$$

where D_{on} is the duty cycle in the steady-state, which is given in (7.9).

$$D_{on} = \sqrt{\frac{4L_1(U_{dc}^{*2} - U_{dc}^{*}U_{in})}{T_{sw}R_{dis}U_{in}^2}} \tag{7.9}$$

Based on Fig. 7.4, at least two current samples should be acquired within one switching period, and the boundary duty cycle can be deduced as given in (7.10).

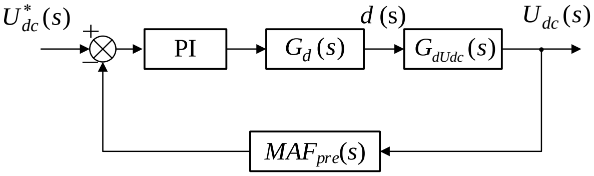


Fig. 7.9. Block diagram of pre-charging control. Source: [J4].

$$D_{on} > \frac{2}{N} \tag{7.10}$$

Based on (7.9) and (7.10), the maximum discharging resistor is

$$R_{dis} < \frac{N^2 L_1 (U_{dc}^{*2} - U_{dc}^* U_{in})}{T_{sw} U_{in}^2} \tag{7.11}$$

When using fifty-sampled current control, the maximum resistance can be 15.6 kΩ according to Table 7.1, hereby a 5 kΩ resistance is used. A high control bandwidth of the equivalent boost converter is not required as it is only used for the pre-charging, the window width of the anti-aliasing filter $MAF_{pre}(s)$ is set to 100 to fully remove the sampled switching noises.

$$MAF_{pre}(s) = \frac{1}{100} \frac{1 - e^{-100 s T_{sa}}}{1 - e^{-s T_{sa}}} \tag{7.12}$$

$G_{dU_{dc}}(s)$ is the plant model of the equivalent boost converter which is given as

$$G_{dU_{dc}}(s) = \frac{2U_{dc}^*}{D_{on}(R_{dis} C_{dc} s + 2)} \tag{7.13}$$

Then the open-loop transfer function is given in (7.14), and the bode diagram is presented in Fig. 7.10 where the bandwidth is 200 Hz and the PM is 53°.

$$T_{ov} = PI(s) G_d(s) G_{dU_{dc}}(s) MAF_{pre}(s) \tag{7.14}$$

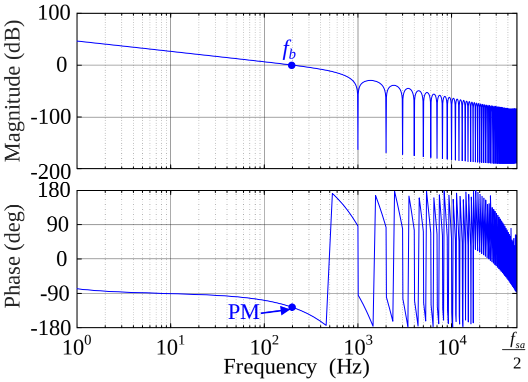


Fig. 7.10. Bode diagram of dc-link voltage controller during pre-charging. Source: [J4].

During the zero voltage vector injection, the filter capacitor voltage can be estimated, thereby the grid phase angle can be obtained through the PLL. Note that a slow PLL is usually recommended in the grid-connected VSCs due to the stability issue under a weak grid. But a fast PLL can be used in order to save time for the start-up, this is because the grid phase angle is not required in the equivalent boost converter. After the grid phase angle is known, the fast PLL is replaced by the slow PLL preparing the start-up of the three-phase VSC. The switching mechanism of fast and slow PLL is shown in Fig. 7.11, and the control parameters can be seen in Table 7.1.

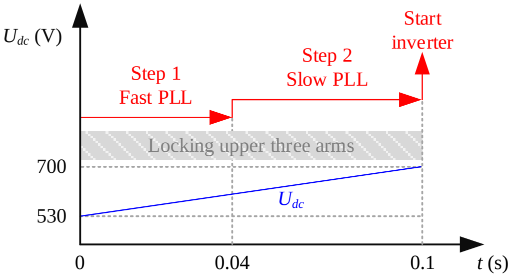


Fig. 7.11. Switching mechanism of fast and slow PLL during start-up process. Source: [J4].

7.5. CASE STUDIES

To validate the proposed method, experiments are implemented in a VSC system from Imperix, as shown in Fig. 7.12. Herein, a three-phase VSC is used, and Table 7.1 shows the experimental parameters for the setup.

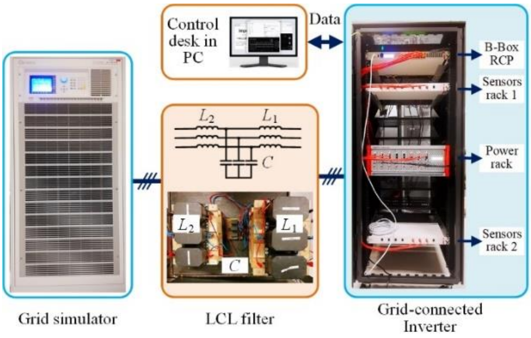
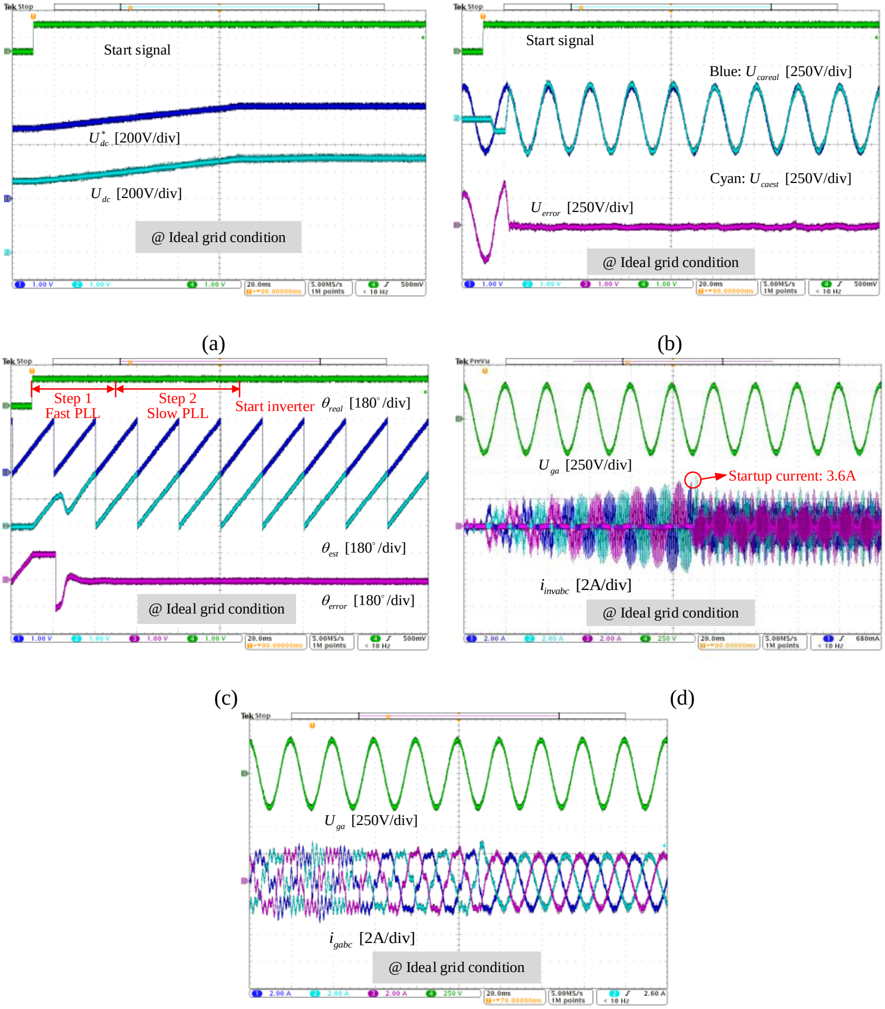


Fig. 7.12. Three-phase grid-connected VSC prototype. Source: [J4].

A. Start-up transient suppression

Fig. 7.13 shows the start-up process when the grid is ideal. At the moment of start-up, i.e., the startup signal changes from 0 to 1, the fast PLL is executed first, which takes 40 ms to track the phase angle of the ideal grid (see Fig. 7.13(c)). Then the execution is smoothly transited to the slow PLL until 100 ms after the start signal is given, the DC voltage is pre-charged to 700 V, and the inverter is started at the same time (see Fig. 7.13(a)). Because the knowledge of the grid information can be obtained beforehand when i_{invq}^{*} is set to 0 A, the starting current can be guaranteed small, i.e., 3.6A in this start-up experiment (see Fig. 7.13(d)). In addition, the steady-state current on the inverter side is 2.8A (see Fig. 7.13(e)), indicating that this method helps suppress the start-up transient. Note that the filter voltage estimation error is large in the first 10 ms after the start-up signal is enabled, this is because the size of the dataset is not enough (see Fig. 7.13(b)). Similarly, the transient current can be also suppressed under a distorted grid condition (see Fig. 7.14).



(a) (b)

(c) (d)

(e)

Fig. 7.13. Experimental results for start-up under an ideal grid condition. (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents. Source: [J4].

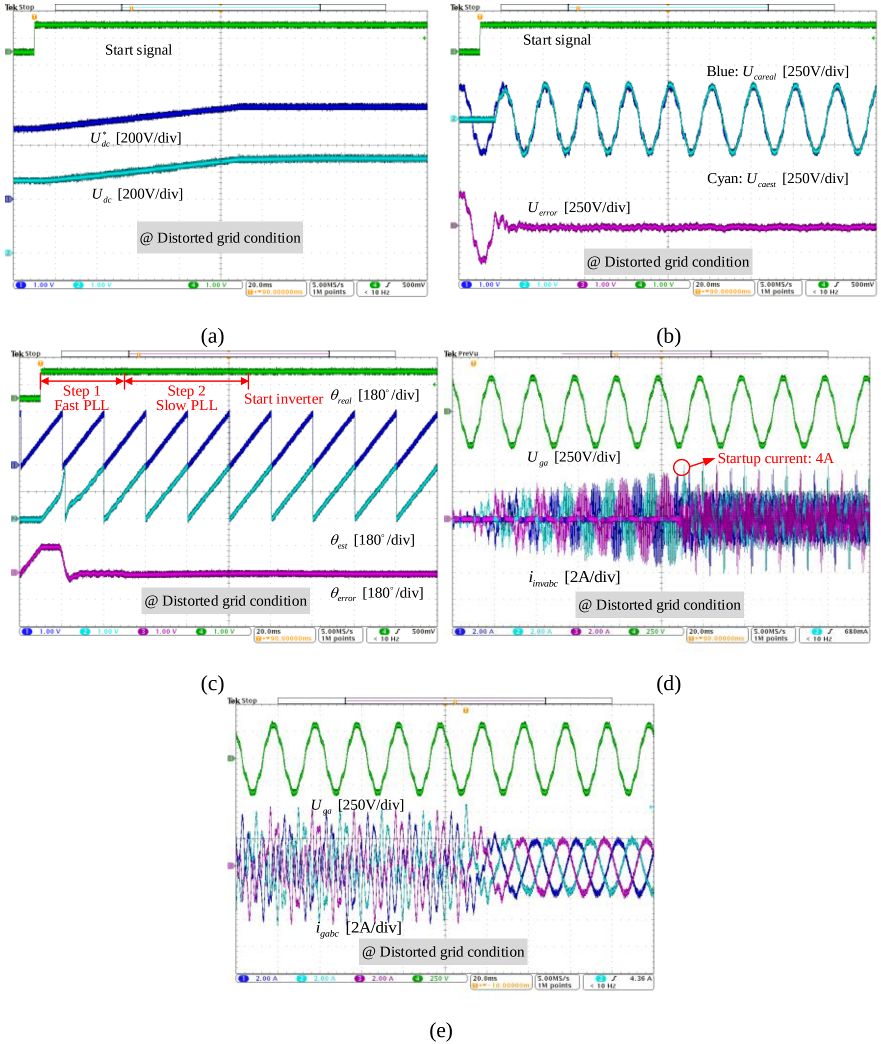
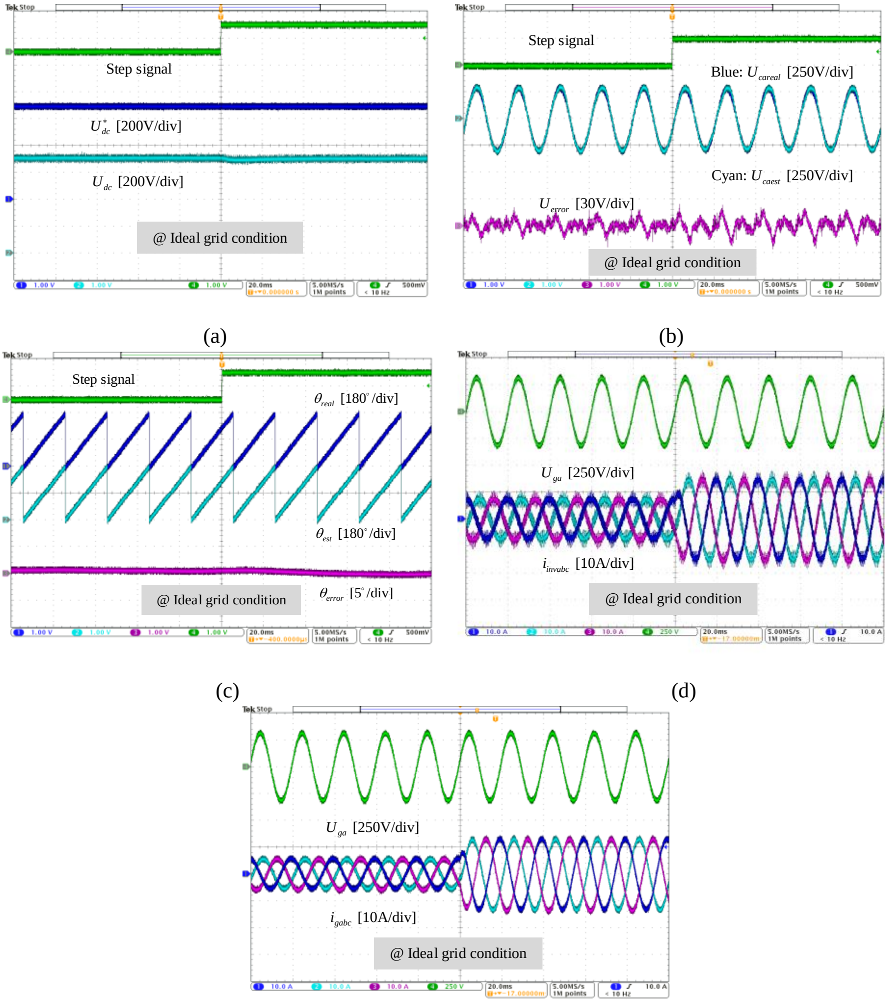


Fig. 7.14. Experimental results for start-up under a distorted grid condition (10% 5th and 7th harmonics). (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents. Source: [J4].

B. Reference current step-change performance

When i_{invq}^{*} changes from 7.5 A to 15 A, the estimation error is below 30 V and 5° for the filter capacitor voltage and the grid phase angle (see Fig. 7.15(b-c)). After the reference current steps to 15 A, there is an increase in the filter capacitor voltage estimation error, as shown in Fig. 7.15(b), this is because the inverter-side inductor is saturated to some extent.



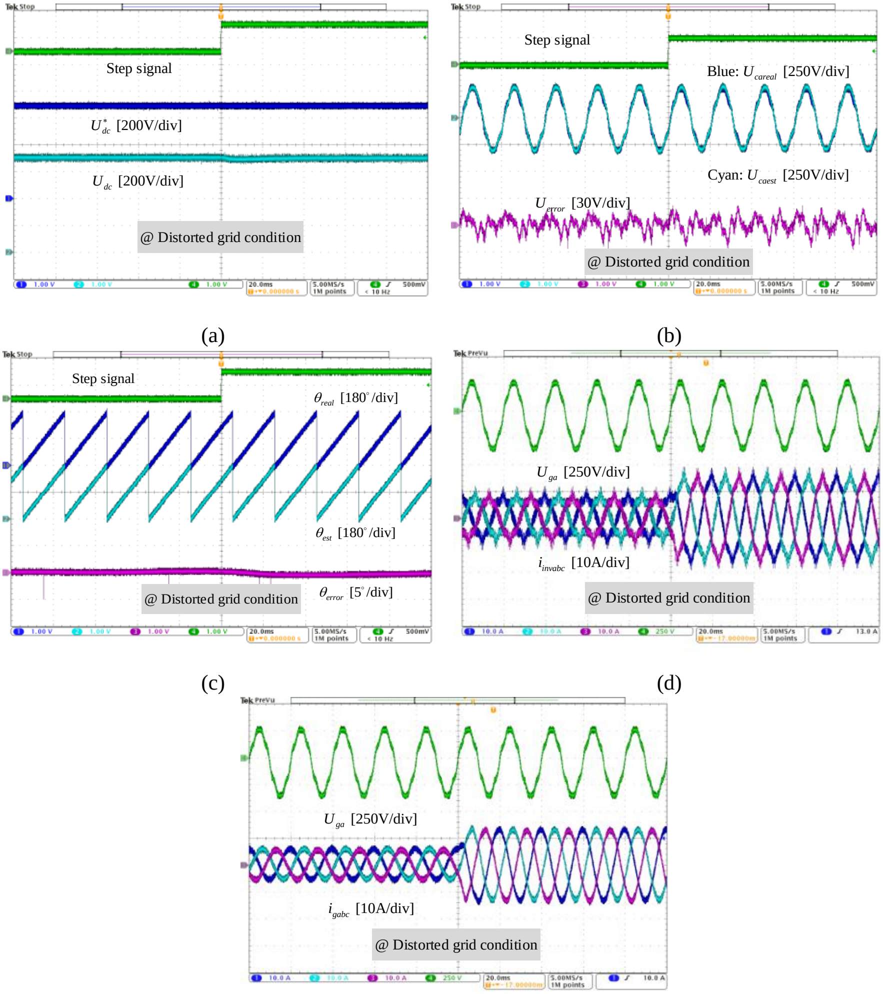
(a) (b)

(c) (d)

(e)

Fig. 7.15. Reference current step-change performance under an ideal grid condition. (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents. Source: [J4].

The saturation of the inverter inductor also slightly increases the filter capacitor voltage estimation error when the grid is distorted (see Fig. 7.16(b)). In addition, the suppression of harmonic current effectively improves the current quality on the grid side (see Fig. 7.16(d-e)). In summary, the proposed estimator is effective in steady-state as well as in transient-state.



(a) (b)

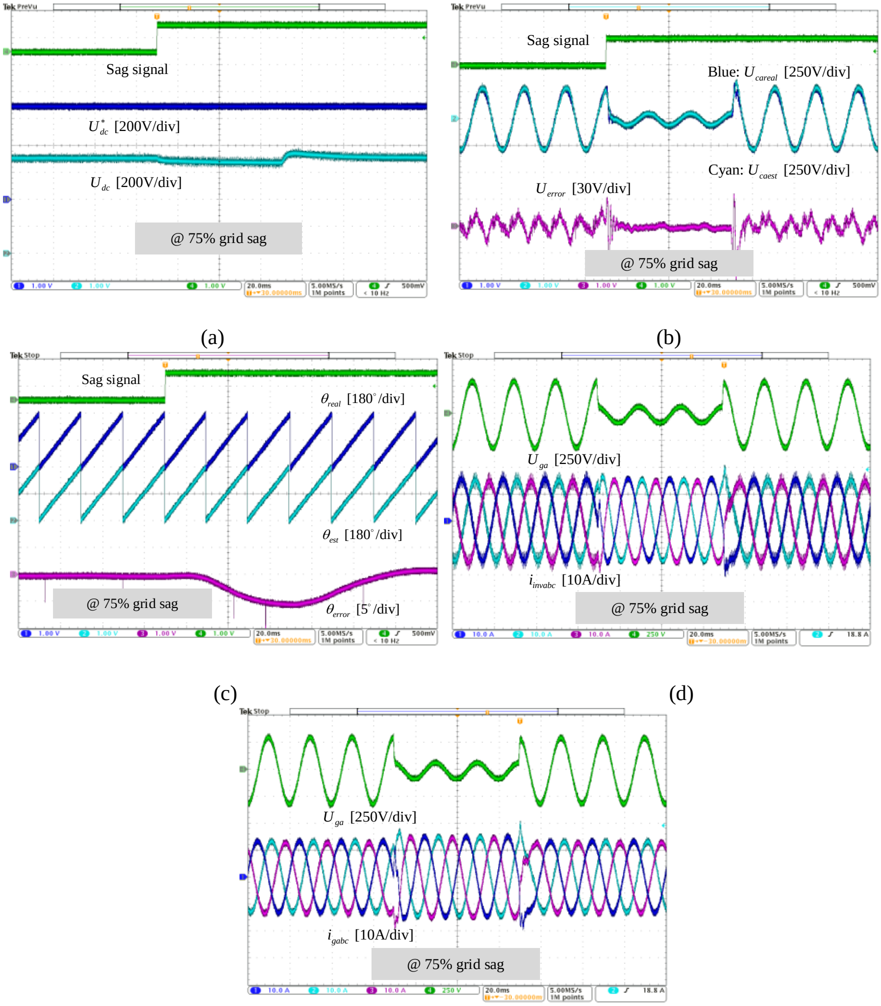
(c) (d)

(e)

Fig. 7.16. Reference current step-change performance under a distorted grid condition (10% 5th and 7th harmonics). (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents. Source: [J4].

C. Performance under a symmetrical grid voltage sag

Take a 75% grid voltage sag as an example, the results in Fig. 7.17 (b-c) show that the method effectively tracks the real value. By comparing 7.16 (b) and 7.17 (b), the voltage estimation error in the fault condition is smaller than that in the normal condition. This is because more data is collected during the zero voltage vector. In addition, because the bandwidth of the PLL is low, the maximum grid phase angle estimation error in transients can be 6.5°.



(a) (b)

(c) (d)

(e)

Fig. 7.17. Experimental results under a 75% grid voltage sag. (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents. Source: [J4].

7.6. SUMMARY

This chapter presents a control method without grid voltage sensors for three-phase VSCs. By multi-sampling the inverter-side currents, the control delay reduction and the bandwidth improvement can be harvested for the control system. In addition, the inverter-side current derivative during zero voltage vectors can be obtained thereby estimating the filter capacitor voltage. By locking the upper arms, the three-phase

VSC is controlled as a boost converter, and the grid voltage can be estimated in advance. Consequently, the start-up transient currents for the grid voltage sensorless control are suppressed. Finally, the findings are verified through the experiments.

Related publications:
[J4] **S. He**, D. Zhou, X. Wang, and F. Blaabjerg, “Line voltage sensorless control of grid-connected inverters using multisampling,” *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4792-4803, April 2022.

CHAPTER 8. CONCLUSION AND FUTURE WORK

This chapter begins with a summary of the work, then the main contributions are highlighted. Finally, the outlook is given in the end.

8.1. SUMMARY

This Ph.D. project mainly focuses on improving the robustness of grid-connected VSCs using multi-sampling techniques. In Chapter 1, the challenge issues about the application of multi-sampling in VSCs are discussed. Then three research objectives are proposed, i.e., the internal mechanism investigation of multi-sampling PWM, passivity enhancement of current controllers, and the condition monitoring using multi-sampled data.

To understand the mechanism of multi-sampling PWM in reducing control delay, a graphical analyzing method based on the voltage-second equivalence is proposed in Chapter 2. It is revealed that the multi-sampling PWM can be converted to a double-sampling PWM sampling the non-average value. Then a low-phase-lag anti-aliasing filter is proposed to filter the sampled SHs and suppress the aliasing, which can help to overcome the bandwidth limits of current controllers without compromising the grid current quality.

As discussed in Chapter 2, the bandwidth and the stability can be improved when using single-loop multi-sampled inverter-side current control. However, the dissipation of current controllers below Nyquist frequency still cannot be achieved due to the phase lag from the anti-aliasing filter. Then a passivity-based current control strategy with capacitor voltage feedforward is proposed in Chapter 3, and the extension to the single-phase inverter VSCs is also discussed. Further, a similar damping strategy with grid-side current control is proposed in Chapter 4, where the dissipation below the Nyquist frequency, the robustness to parameter deviation, as well as the transient performance are enhanced. When adding an anti-aliasing filter, the extreme value of control delay is one-quarter of the switching period when the sampling frequency is infinite. By switching the sampling instant, an enhanced real-time-update PWM is proposed in Chapter 5, and the dissipation below Nyquist frequency can be achieved only using single-loop inverter-side current control.

Besides the three-phase two-level VSC and the single-phase VSC, the three-phase interleaved VSC is also commonly used in renewable generation. Due to the circulating current among the parallel cells, the multi-sampled current control methods in Chapter 3 to Chapter 5 cannot be duplicated directly. Hence, a constrained multi-sampled current control strategy is proposed in Chapter 6, where the sampling rate selection in the PCC current regulation and the circulating current suppression are discussed. In addition, based on the multi-sampled PCC voltage data, a grid impedance estimator is proposed, which can help to enhance the stability under a weak grid. In Chapter 7, based on the multi-sampled current data, a grid voltage estimator is proposed, which saves the cost of the transducers and enhances the reliability in the case of the voltage sensor fault. Moreover, a soft start-up method is proposed by controlling the inverter as a boost converter, and the grid information can be estimated beforehand.

8.2. MAIN CONTRIBUTIONS

In light of the aforementioned findings, the main contributions can be highlighted as follows:

Analysis and implementation of multi-sampling PWM

- Based on the voltage-second balance equivalence, the multi-sampling control delay is analyzed, and the effect of multi-sampled SHs is presented.
- Two anti-aliasing filters, i.e., IRF and MRF are proposed to suppress the aliasing with a low-phase lag.
- The implementations of multi-sampling PWM in two types of multi-level VSCs are discussed, i.e., single-phase H-bridge VSC and three-phase interleaved VSC.

Passivity enhancement using multi-sampling PWM

- A passivity-based damping strategy with capacitor voltage feedforward is proposed for the inverter-side current control.
- A passivity-based damping strategy with capacitor voltage feedforward and capacitor current feedback is proposed for the grid-side current control.
- An enhanced real-time-update PWM is proposed, and the control delay is optimized to $0.25T_{sw}$ with a low computation burden (critical value for passivity).

Condition monitoring using multi-sampled data

- A grid impedance estimation method is proposed for the two-cell three-phase interleaved VSC based on the multi-sampled PCC voltage.
- A grid voltage estimator is proposed for a three-phase two-level VSC based on the multi-sampled inverter-side current. Moreover, a soft start-up method is proposed and the grid information can be estimated beforehand.

8.3. OUTLOOK

The entire work conducted in this Ph.D. project demonstrates a big potential of using multi-sampling in power electronics applications, and more advantages of using multi-sampling can be explored in the future at least from the following four aspects:

- In this project, the stability in the high-frequency range is enhanced by using multi-sampling PWM. The effect of control delay on the low-frequency stability is little, which is determined by the outer loops. To improve the stability in all frequency ranges, it is worth exploring more comprehensive damping strategies using multi-sampling.

- Grid-forming VSCs play a key role in the power electronics-dominated power system. Future research should consider how to use multi-sampling PWM to enhance the small-signal stability with less control delay. The application of multi-sampling PWM on transient stability enhancement is also an interesting topic.
- The multi-sampling PWM is only investigated in two-level three-phase VSC, single-phase H-bridge VSC, and the three-phase interleaved VSC. There are still many other efficient VSCs, and how to apply the multi-sampling PWM in these converters is worth being researched.
- As the multi-sampling can provide a large dataset, how to further mine the information to enhance the control performance of power electronics is of interest. A combination with artificial intelligence can be a potential application in the future.

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PART II. PAPERS

JOURNAL PAPER I

[J1] A Review of Multi-Sampling Techniques in Power Electronics Applications

S. He, D. Zhou, X. Wang, Z. Zhao, and F. Blaabjerg

The paper has been published in
IEEE Trans. Power Electron, early access, 2022.
DOI:10.1109/TPEL.2022.3169662.

JOURNAL PAPER II

[J2] Aliasing Suppression of Multi-Sampled Current Controlled LCL-Filtered Inverters

S. He, D. Zhou, X. Wang, and F. Blaabjerg

The paper has been published in
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JOURNAL PAPER III

[J3] Passivity Based Multi-Sampled Current Control of LCL-Filtered Grid-Connected Inverters

S. He, D. Zhou, X. Wang, and F. Blaabjerg

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JOURNAL PAPER IV

[J4] Line Voltage Sensorless Control of Grid-Connected Inverters Using Multisampling

S. He, D. Zhou, X. Wang, and F. Blaabjerg

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CONFERENCE PAPER I

[C1] Robust Passivity Enhancement for LCL-Filtered Grid-Following Inverters with Multi-Sampled Grid-Side Current Control

S. He, Z. Yang, D. Zhou, X. Wang, F. Blaabjerg, and R. De Doncker

The paper has been accepted by IEEE ECCE 2022.

CONFERENCE PAPER II

[C2] Switching harmonics suppression of single-loop multi-sampling control of grid-connected inverter

S. He, D. Zhou, X. Wang, and F. Blaabjerg

The paper has been published in
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CONFERENCE PAPER III

[C3] Enhanced Real-Time-Update Current Control Using Multi-Sampling Concept

S. He, D. Zhou, X. Wang, and F. Blaabjerg

The paper has been accepted by IEEE PEDG 2022.

CONFERENCE PAPER IV

[C4] Multisampling control of two-cell interleaved three-phase grid-connected converters

S. He, D. Zhou, X. Wang, and F. Blaabjerg

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CONFERENCE PAPER V

[C5] Multisampling based grid impedance estimation for two-cell interleaved three-phase inverters

S. He, D. Zhou, X. Wang, and F. Blaabjerg

The paper has been published in
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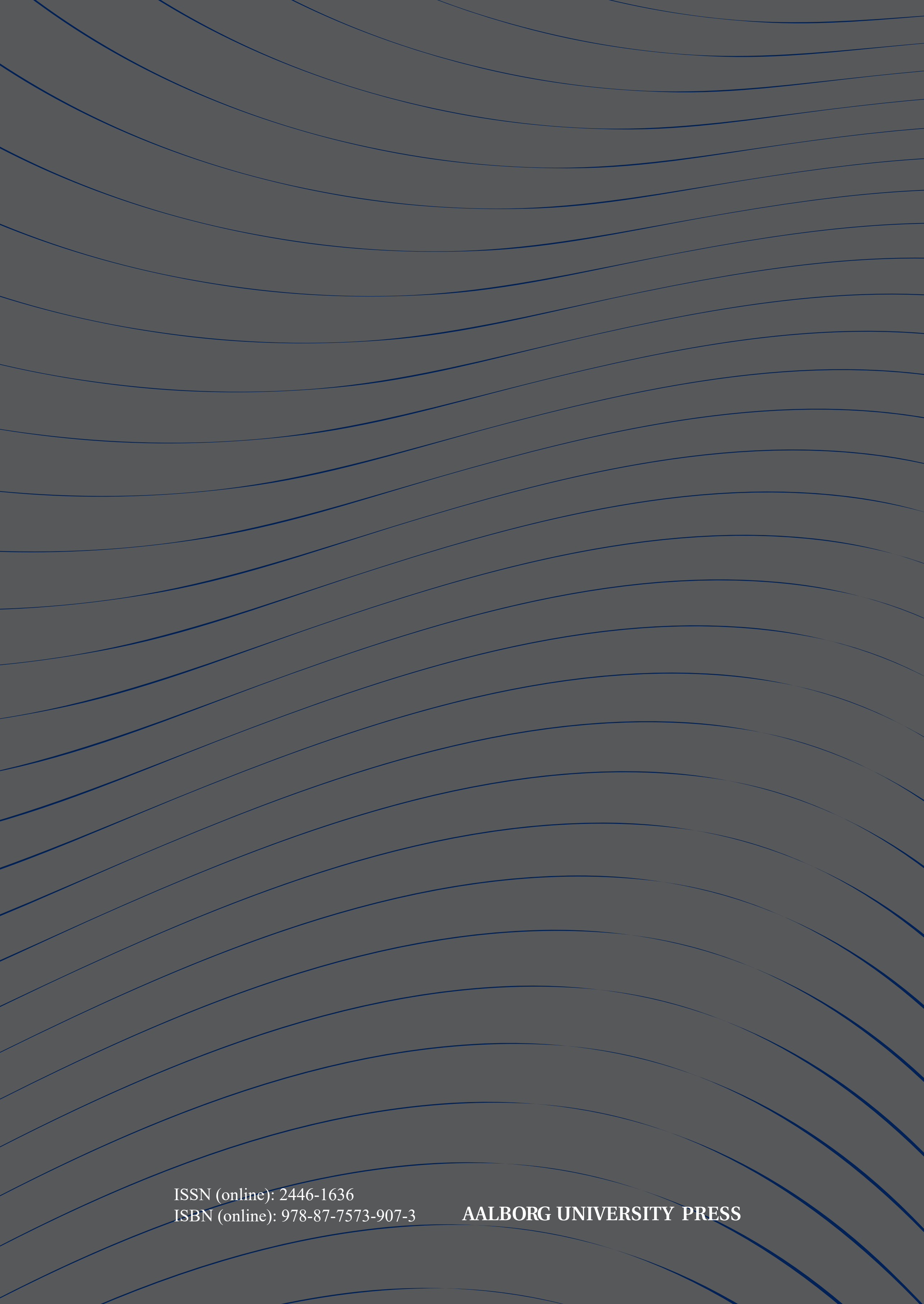

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