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Song, Chaochao

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BY
CHAOCHAO SONG

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Efficient and Reliable Control of Multi-Level Dual-Active-Bridge Converters

Ph.D. Dissertation

Chaochao Song

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PhD supervisor: Prof. Frede Blaabjerg
Aalborg University

Assistant PhD supervisors: Assistant Prof. Ariya Sangwongwanich
Aalborg University

Prof. Yongheng Yang
Zhejiang University, China

PhD committee: Associate Professor Szymon Bęczkowski
Aalborg University, Denmark

Associate Professor Sergio Busquets-Monge
Universitat Politècnica de Catalunya (UPC), Spain

Dr. Thiwanka Wijekoon
Huawei Technologies – Nuremberg Research Centre, Germany

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Abstract

Medium-voltage DC (MVDC) networks have been drawing increasing attention in various power supply systems since they can achieve high efficiency, flexibility and reliability. DC-DC converters with high step-up ratio and high voltage-blocking capability to be employed to the MVDC systems are key devices. The two-three (2/3)-level dual-active-bridge (DAB) converter with a neutral-point-clamped (NPC) structure is a promising solution. However, most of the previous study for DAB converters is based on traditional two-level DAB instead of multi-level DAB converters. Due to different topologies, some research on the two-level DAB converter is not possible to be used in the multi-level DAB converters. In addition, some new issues are introduced with the NPC bridge, e.g., capacitor voltage imbalance. Therefore, this project was proposed to enhance reliability and efficiency of the 2/3-level DAB through exploring several control strategies. To do so, the main challenges should be addressed.

Firstly, to enhance the converter efficiency by control strategies, optimum combinations of the control variables, i.e., phase-shift and duty-cycle ratios, should be obtained based on certain optimization objective, e.g., peak or root-mean-square (RMS) transformer currents. Compared to numerical solutions, analytical solutions are preferred for automatically regulating the control variables online, especially when the operating parameters (e.g., the transferred power and DC-link voltages) vary in wide ranges. However, with the increased number of the control variables in multi-level DAB converters, the difficulty for obtaining the analytical solutions increases, and the previous methods for the two-level DAB may fail to address the optimization problem.

Secondly, to suppress capacitor voltage imbalance and the corresponding negative effects, e.g., increased voltage stress on certain power switches, some voltage balancing methods were developed. However, these previous voltage balancing methods rely on the transformer current polarity, which is challenging to be identified with various operating conditions or parameters. In addition, current and power fluctuations will occur along with the changed transformer terminal voltage, which will result in overshoot current, and may activate the protection system during the voltage balancing.

Moreover, open-circuit-fault (OCF) issues have not been fully discussed in multi-level DAB converters. The previous OCF diagnosis methods, which were proposed based on two-level DAB converter, fail to identify the specific faulty switch due to the increased number of switches. In addition, some traditional fault-tolerant control strategies can be used to suppress the current overshoots and DC bias caused by the OCF. Nevertheless, the three-level NPC bridge provides more current conduction paths, and thus, it has more potential for enhancing the post-fault performance, e.g., extending the transferred power range, which should be utilized in the fault-tolerant methods.

To address these challenges, this Ph.D. project proposes several control strategies to enhance the converter efficiency and reliability. To obtain a generic optimal control strategy for improving the efficiency, a minimum-current-stress control strategy with analytical solutions is put forward. In order to simplify the complexity for calculating the analytical solutions, the numerical solutions are first analyzed to determine certain operating modes where the optimal solutions appear. Then, the analytical solutions are obtained by the Karush-Kuhn-Tucker (KKT) conditions. Accordingly, a simplified closed-loop control system is developed to achieve online regulation of the control variables along with the operating conditions.

Two control methods for capacitor voltage balancing are developed to address the above two issues during the voltage balancing, i.e., current fluctuations and model-based feature. For the conditions where the transformer current can be easily determined, e.g., soft-switching operation, the complementary-switching-state (CSS) method is suitably applied to improve the dynamics. During this method, the switching states that cannot assist the voltage balancing are replaced by their CSSs. By doing so, required charges to the neutral point are able to increase without voltage change after the CSS method is enabled. Thus, the transferred power and current fluctuations can be effectively suppressed. On the other hand, for the conditions where the current polarity is challenging to be determined when the operating conditions/parameters change in a wide range, a fixed-switching-state (FSS) method can be applied, where two additional switching states are utilized to achieve the model-free feature for the voltage balancing control, and thus, the current polarity is not needed to be determined.

Furthermore, to locate the faulty switch, a fault diagnosis method by applying the midpoint voltages as the diagnostic signals is proposed, where the specific faulty switch is determined based on the average post-fault midpoint voltages and the duty cycles after waveform transition. Subsequently, a complementary-switch-blocking (CSB) method is applied to the fault-tolerant control to suppress the current overshoots and DC bias resulting from the OCFs. In addition, compared to the traditional fault-tolerant method, the post-fault transferred power range can be extended under the CSB control method.

Resumé

Mellemspændings-DC elektriske net (MVDC) har tiltrukket sig mere og mere opmærksomhed i forskellige energiforsyningssystemer på grund af fordele som høj effektivitet, pålidelighed og fleksibilitet. DC-DC-konvertere (omformere) til denne mellemspænding er nøgle-komponenter og oftest kræves der et højt spændingsløft imellem indgang og udgang. Her er specielt omformeren med navnet dual-active-bridge (DAB) DC-DC-konverter med en transformer og med et neutralt spændingspunkt (NPC) en lovende løsning, som giver tre spændings-trin og kan håndtere det omtalte mellemspændingsniveau. Studier indenfor DAB-omformere er dog hovedsageligt baseret på traditionelle DAB-konvertere, som kun har to spændings-niveauer. På grund af de forskellige transistor-kredse der anvendes, kan nogle af de metoder der er brugbare i to-niveau DAB-konverteren ikke anvendelig på DAB-konvertere med flere spændingstrin. Derudover introduceres der nogle nye problemer med NPC-punktet, f.eks. spændingsubalance ved kondensatorerne. Derfor omhandler dette ph.d. projekt det at forbedre effektiviteten og pålideligheden af en DAB-konverter med to spændings-trin på den ene side og tre spændingstrin på den anden side (2/3-niveau) ved brug af nye kontrolstrategier.

For at forbedre effektiviteten af en 2/3-niveau DAB-konverter kan optimale kombinationer af eksisterende styrevariabler, dvs. faseforskydningsvinkler og arbejds-frekvens, opnås baseret på bestemte mål for en optimering, f.eks. den maximale strøm eller effektiv-værdien af strømmen. Sammenlignet med numeriske løsninger foretrækkes analytiske løsninger som kan bruges til en online regulering af styrevariablerne, som er i samspil med den overførte effekt eller DC-spændingerne over kondensatorerne. Dette er især ønskværdig når driftsbetingelserne/parametrene ændres i bredere arbejds-områder. Men med det øgede antal kontrolvariable til styringen af multi-level DAB-konverteren, opstår der vanskeligheder i at opnå analytiske løsninger, hvorfor tidligere foreslåede metoder for to-niveau DAB-konvertere ikke kan løse det ønskede optimeringsproblem.

Derudover eksisterer der kontrolstrategier til balancering af kondensatorspændingerne for NPC-baserede DAB-konvertere, som kan eliminere spændingsforskellen og dermed reducere belastningen på komponenterne i om-

formeren. Disse tidligere foreslåede spændingsbalanceringsmetoder afhænger dog af identifikation af polariteten af strømmen i transformeren, hvilket kan være udfordrende at identificere under forskellige driftsbetingelser eller parameter variationer. Derudover kan der forekomme strøm- og effekt variationer samtidig med at balancerings-strategien udføres, hvilket i værste tilfælde kan resultere i en overbelastning af konverteren.

Endvidere kan der være problemer med detektere fejl (åbne transistorer) i konverteren (open-circuit-fault (OCF)) og dette er ikke blevet undersøgt for multi-level DAB-konvertere. De tidligere OCF-detekteringsmetoder for DAB-konvertere med to niveauer kan ikke lokalisere den defekte transistor nøjagtig nok på grund af det øgede antal transistorer, der anvendes til multi-level DAB-konvertere. Derudover kan nogle af de traditionelle fejltolerante styringsstrategier ikke anvendes til multi-level DAB-konvertere og der er et behov for at finde nye metoder. Ikke desto mindre giver NPC DAB-omformeren med tre niveauer flere veje for strømmene og dermed potentiale for at forbedre DAB-omformerens drift under fejl og eksempelvis øge effektoverførselsevnen sammenlignet med traditionelle metoder.

For at løse ovennævnte udfordringer foreslår dette ph.d. projekt flere nye kontrolstrategier til at forbedre effektiviteten og pålideligheden af 2/3-niveau DAB-konvertere. For at opnå en generel optimal kontrolstrategi til forbedring af effektiviteten foreslås en minimumstrøms/-spændingskontrolmetode, som er baseret på analytiske løsninger. For i praksis at forenkle beregningen af de analytiske løsninger findes numeriske løsninger først for visse arbejdspunkter, hvor optimale løsninger bestemmes. Derefter findes komplette analytiske løsninger ved brug af Karush-Kuhn-Tucker (KKT) betingelser, som anvendes i optimeringsalgoritmer. Ydermere er der designet et forenklet kontrol-system baseret på de analytiske løsninger for at kunne opnå online ændring af reguleringsvariablerne som justeres i forhold til arbejdspunkterne.

To styringsstrategier for balancering af kondensatorspændingen er udviklet til at løse de tidligere diskuterede problemer med spændingsbalanceringen. De to er henholdsvis en modelbaseret og strømbaseret styre-strategi. I de tilfælde, hvor transformatorstrømmen let kan bestemmes, f.eks. under soft-switching (tabsfri skift af strømmene i transistorerne), anvendes en komplementær switching-stategi (CSS), som er i stand til at forbedre dynamikken under styringen af balanceringen af kondensatorspændingen. Ved brug af CSS-metoden erstattes utilsigtede switch-tilstande, som identificeres via kendskabet til transformatorens strømpolaritet. En langt bedre spændingsbalancering er opnået, hvor også strøm- og effekt variation effektivt kan undertrykkes. I andre tilfælde, hvor strømpolariteten i transformeren er vanskelig at bestemme, når driftsbetingelserne/parametrene ændrer sig meget, kan den modelfrie styringsmetode anvendes, hvor yderligere to switch-tilstande kan bruges og afkobler balanceringsstyringen fra polariteten af strømmen i transformeren.

For at lokalisere en defekt transistor under drift af konverteren foreslås en fejldiagnosemetode, hvor midtpunktsspændingerne for hvert transistor-bro anvendes som diagnosesignaler, og den defekte transistor kan nøjagtig lokaliseres ud fra middelværdierne og driften af konverteren. Desuden foreslås en fejltolerant kontrolstrategi baseret på en komplementær transistor-blokeringsmetode (CSB), som kan reducere DC-overspændingen og over-strømmen, som følge af OCF og bringe DAB-konverteren tilbage til sikker drift i sådanne tilfælde. Sammenlignet med en traditionel fejltolerant kontrol-metode, kan den foreslåede CSB-metode forbedre effektoverførselsevnen betydelig efter konstateret fejl i omformeren.

Preface

This Ph.D. thesis summarizes the research outcomes of the project entitled "Efficient and Reliable Control of Multi-Level Dual-Active-Bridge Converters". This project is supported by AAU Energy, Aalborg University, Denmark, and China Scholarship Council (CSC). Besides, part of the publications are supported by Reliable Power Electronic based Power Systems (REPEPS) by THE VELUX FOUNDATIONS. I appreciate a lot for the support from the above institutions.

Firstly, I want to sincerely thank my supervisors Prof. Frede Blaabjerg, Assist. Prof. Ariya Sangwongwanich, and Prof. Yongheng Yang for their valuable guidance and suggestions on my Ph.D. study and my life in Aalborg. It was their professional advice, endless encouragement and patience that brought me back to be positive when I lost my way, and supported me to complete my project. I have learned a lot from their rigorous working attitude and rich professional knowledge, which will definitely benefit my future career.

I am grateful for Mr. Andreas Hensel and Mr. Juergen Thoma for inviting me to visit Fraunhofer ISE. During the three-month study with their guidance, I have learned a lot, which can hardly be obtained from universities. I thank them a lot for giving me enough flexibility to deal with my journals and the project there. It was a busy but delightful experience to work with them.

In addition, I would like to thank my friends and colleagues at AAU and Fraunhofer ISE for their company. Thanks a lot for my friends' concern across the ocean from China. Their kindness and friendship make my life bright.

Finally, I want to express my sincere gratefulness to my parents and sisters. Their support and selfless love is the source of my confidence which keeps me going.

Chaochao Song
Aalborg University, December 10, 2022

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Chapter 1

Introduction

1.1 Background

Concerns on the consumption of fossil fuels and environmental issues have become more critical, enabling an increasing utilization of renewable energy sources [1–5]. In recent years, due to the growth of DC loads (e.g., batteries and electrical vehicles) in the distributed energy generation systems, increasing demands for higher power-transfer capability, efficiency and power quality, and development of the medium-voltage (MV) power devices (e.g., power semiconductors), medium-voltage DC (MVDC) structure has been capturing global focus since the MVDC systems can obtain higher efficiency, reliability, and flexibility compared with traditional AC network [6–10]. Therefore, MVDC network is also a promising solution for renewable power plants, electrified railway systems, large ships, and industrial and urban buildings [10, 11]. Under such a condition, many efforts for exploring the key technologies of the MVDC systems, e.g., interfacing DC-DC converters, network configuration, insulation and protection, have been made by industry and academia [10–15]. A technical roadmap done by CIGRE Working Group shows a milestone of MVDC research, where various MVDC-related projects have been developed by Siemens, University of Nottingham, Scottish Enterprise, and other institutions since 1997 [10].

The MVDC technology has also been applied to the large-scale photovoltaic (PV) plants. Fig. 1.1 shows a typical MVDC-structure PV system, where the energy storage system is integrated into the grid to suppress voltage fluctuations and other issues caused by the intermittent power generation of the PV system, and achieve schedulable power flow [16]. In addition, an auxiliary power supply system is employed to supply a low voltage (e.g., 24 V) to various auxiliary systems in the PV system, e.g., control systems and gate-driving systems. The DC-link voltages in MVDC systems are generally

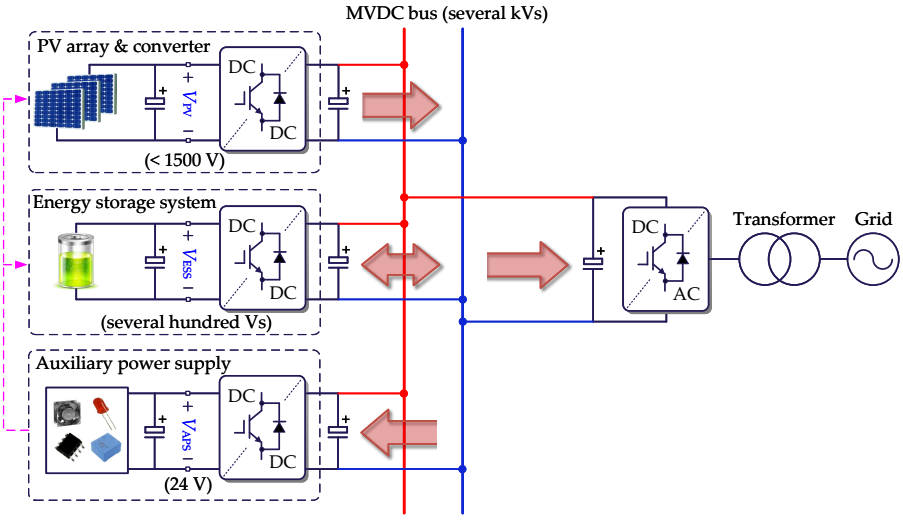


Fig. 1.1: Typical medium-voltage DC (MVDC) network for large-scale photovoltaic (PV) plants.

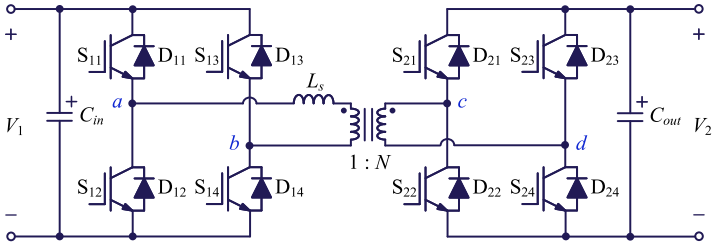


Fig. 1.2: Traditional two-level dual-active-bridge (DAB) converter.

from several kilovolts (kV) to 35 kV, and the recommended rated DC voltages are 1.5 kV, 3 kV, 6 kV, 12 kV, 18 kV, 24 kV, and 30 kV according to the IEEE Standard [9, 11, 17]. 1.5-kV PV systems have been exploring widely, and the MVDC network with higher DC-link voltages is also ongoing [18, 19]. For instance, a 3-kV DC large-scale PV system is built in Fraunhofer ISE in Germany [20, 21], whose structure is similar to Fig. 1.1, and the terminal voltage in the DC bus is planned to be increased to 20 kV in the future [12]. Institute of Electrical Engineering of Chinese Academy of Sciences is exploring a PV MVDC grid-connected system with the DC-link voltage of 10 kV [22]. Siemens launched MVDC PLUS in 2017, which connects large-scale PV plants into an up-to-150 MW power grid, where the medium DC voltage will reach 30 kV [12, 23].

In the MVDC systems, the MV interfacing DC-DC converters play a critical role to transfer power and maintain DC voltages between the low-voltage

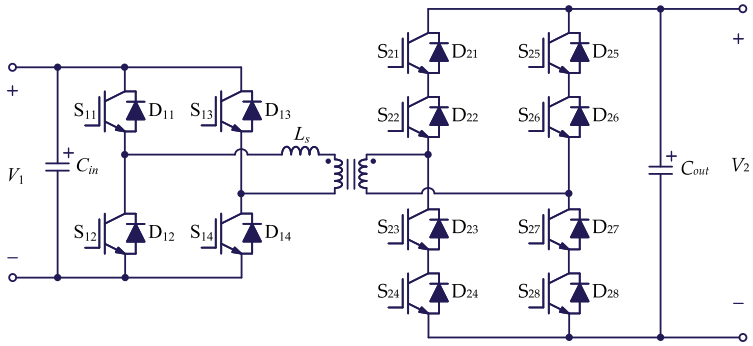


Fig. 1.3: Two-level DAB converter with series switches (TL-DAB-SS).

DC (LVDC) bus and MVDC bus, which require high voltage-blocking capability and high step-up ratios. However, such DC-DC converters suitable for the MVDC network have not been fully developed and commercialized [12]. Among various topologies of DC-DC converters, the dual-active-bridge (DAB) converter is widely applied to LVDC systems due to the superiority of inherent soft-switching, galvanic isolation, high step-up capability and power density [24–28], as shown in Fig. 1.2. However, limited by the application of MV power semiconductors, a single two-level DAB can hardly withstand a medium DC voltage [29]. Thus, various topologies which can increase the voltage-blocking capability for the DAB converters have been explored:

• **Two-level DAB converter with series switches (TL-DAB-SS)**: As shown in Fig.1.3, two power switches (e.g., S_{21} and S_{22}) are series-connected as a module. These two switches will be turned on/off synchronously so that each of them withstands half of the voltage. Under ideal conditions, this topology has identical switching characteristics and modulation schemes as the traditional two-level DAB. However, voltage sharing of the two series switches may not balance, since the two series switches cannot be perfectly synchronized owing to the tolerances between various semiconductors and synchronization failure between different gate pulses. This will result in power distribution imbalance and damage the devices in certain cases. In addition, the degrees of freedom (DoFs) for modulation are limited in this topology, which is not conducive to performance improvement [24, 25].

• **Cascaded DAB converter**: Cascaded converter is an effective solution for MVDC systems, where the two-level H-bridges are employed as the series modules to withstand higher voltages [6, 30–33]. The amount of cascaded modules can be modified flexibly according to the DC voltages and voltage-rating of the switches. Input-parallel-output-series (IPOS) is one of the most popular structures among various cascaded DAB converters (when LVDC is the input and MVDC is the output) [6, 30, 31]. As shown in Fig. 1.4 (a), the en-

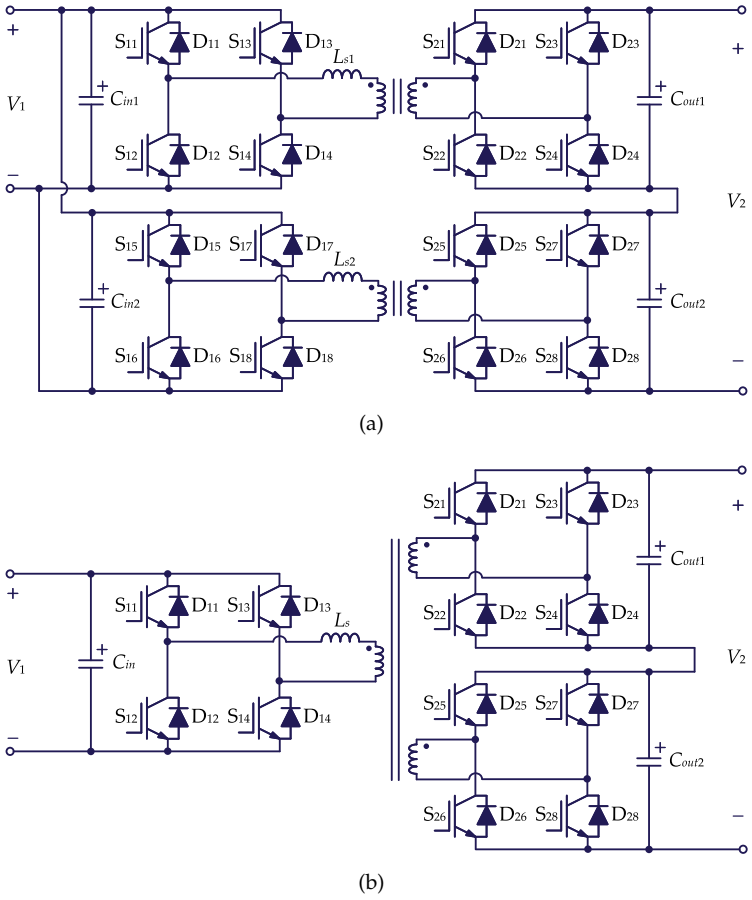


Fig. 1.4: Cascaded DAB converters with: (a) input-parallel-output-series (IPOS) structure and (b) three-port structure.

tire two-level DAB is applied as the module, and thus, the modulation for the two-level DAB converter can be directly used in the IPOS converter. However, additional control schemes for voltage and power sharing between different modules should be considered. Otherwise, the circulating current caused by parameter tolerances and other factors will be increased, affecting the converter efficiency and other performances. Furthermore, the amount of power components (for a two-module structure) including the power semiconductors and isolation transformers is twice that of the traditional two-level DAB converter, and also increases significantly compared to that of the TL-DAB-SS. To reduce the amount of the power components and related hardware cost, the cascaded DAB based on the three-port transformer (TP-DAB) was proposed [32, 33], where only H-bridges (instead of entire two-level DAB converters)

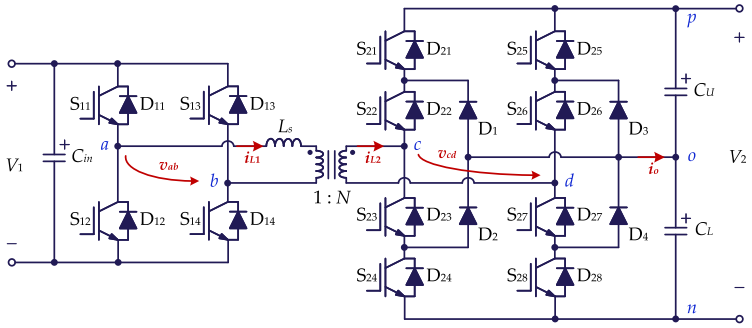


Fig. 1.5: Neutral-point-clamped (NPC)-based multi-level DAB converter: V_1 and V_2 are two DC-link voltages, v_{ab} and v_{cd} are transformer terminal voltages, i_{L1} and i_{L2} are transformer currents, i_o is the neutral-point current, L_s is the series inductor, N is the transformer turns ratio, p, o and n are three ports of the NPC bridge.

are series-connected on the MV side, as shown in Fig. 1.4 (b). Therefore, the amount of power devices is the same as that of the TL-DAB-SS. However, the coupling among the three ports increases the modeling and control complexity [32, 33].

• **Multi-level DAB converter**: With the development of the MV power semiconductors, e.g., 3.3-kV, 6-kV, and 15-kV SiC MOSFET, it becomes feasible to access the MVDC system by using one single multi-level DAB converter. Based on the TL-DAB-SS, four diodes are added to utilize the neutral-point voltage, as shown in Fig. 1.5. By doing so, S_{21} and S_{22} (as well as other switch pairs) are not required to be ON/OFF synchronously. Thus, the voltage/power sharing issues between the two switches can be avoided. The voltage imbalance between two DC-link capacitors should be considered, which can be addressed by modifying the phase-shift angles or duty cycles. In addition, the multi-level topology supplies more DoFs compared to the two-level DAB converter, and thus, further enhance the converter performance (e.g., efficiency) [34, 35]. Furthermore, the transformer structure is identical with the two-level DAB, and thus, the modeling and control methods proposed in the two-level DAB can be extended to multi-level DAB converters.

Apart from the above discussed converters, there are certain topologies, which can increase the voltage-blocking capability of the DC-DC converters, e.g., modular multilevel converter (MMC). However, the complicated control especially for the capacitor voltage balancing and the requirement for increased components limit the application of MMC-based converters in MVDC systems with the DC voltage of several kVs. The MMC-based converters are more suitable for high-voltage DC (HVDC) systems with a voltage rating of several hundreds of kVs [6, 36]. According to the above analysis, the multi-level DAB converters have more potential to be employed to the

MVDC systems due to relatively low modeling and control complexity and high DoFs for enhancing the converter performance. The multi-level DAB shown in Fig. 1.5, employing a neutral-point-clamped (NPC) bridge on the MV side, is named two-three (2/3)-level DAB converter hereafter. It was mainly proposed for high step-up applications [34, 37, 38], which means the two DC-link voltages are different significantly, e.g., the energy storage and auxiliary power supply systems in large-scale PV plants shown in Fig. 1.1. Unfortunately, the prior-art research in terms of the modulation schemes for enhancing the converter performance mainly focuses on the traditional two-level DAB instead of the multi-level DAB converters. Therefore, this project mainly aims to propose efficient and reliable modulation for the 2/3-level DAB. As such, several challenges are considered:

- **Challenge I - Generic efficient control**: Due to the increased DoFs, the multi-level DAB converter is generally optimized by applying high-DoF control strategies, e.g., five-level control [39]. However, the complexity for obtaining a generic and simple optimal modulation strategy which can be used for a wide range of operating parameters will be significantly increased.

- **Challenge II - Capacitor voltage balancing**: Capacitor voltage balancing control should be applied to avoid unbalanced voltage stresses on different power devices and other issues. Identification of the transformer current polarity and power fluctuations are critical for the voltage balancing, which have not been fully addressed in previous research.

- **Challenge III - Fault diagnosis and tolerant control**: Owing to the increased number of switches in the NPC bridge, the previous fault diagnosis methods used in the two-level DAB cannot locate specific faulty switch in the multi-level DAB. In addition, the post-fault performance of the DAB converter (e.g., power-transfer capability) can be enhanced by suitably re-arranging the structure of the NPC bridge, which has not been explored yet.

The above challenges and their corresponding state of the art will be elaborated in the following.

1.2 State of the Art

1.2.1 Efficient Control Strategies

Phase-shift control is generally applied to various DAB converters, including the 2/3-level topology, where the phase-shift angles between different

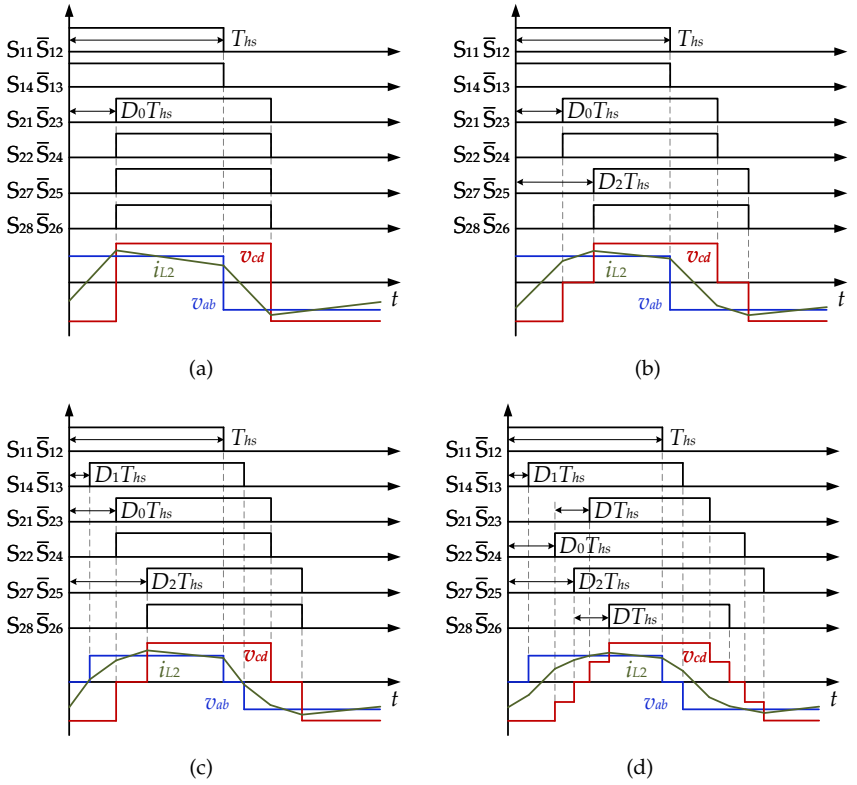


Fig. 1.6: Various phase-shift control strategies for 2/3-level DAB converter with: (a) single-phase-shift (SPS) control, (b) extended-phase-shift (EPS) control, (c) triple-phase-shift (TPS) control, and (d) five-level control: T_{hs} is half of a switching period, D is the duty-cycle ratio, D_0, D_1, and D_2 are phase-shift ratios.

gate pulses are used as the control variables to modify the power flow [24–27]. Single-phase-shift (SPS) control is the most traditional control scheme, where only one phase-shift ratio D_0 (between the pulses for S_{11} and S_{21}) is employed, as shown in Fig. 1.6 (a) [40, 41]. The SPS control is easy to implement. Unfortunately, the efficiency of the DAB converters will be significantly affected by the reduced soft-switching range and increased RMS current if the two DC voltages are not matched [24, 25]. To address this, multi-phase-shift (MPS) control strategies were developed by adding more DoFs in the modulation. Fig. 1.6 (b)-(d) show various MPS control strategies, which are divided according to the amount of the control variables [39, 42]. Among these MPS strategies, the five-level control has more potential for improving the performance of the NPC-based DAB converters. Therefore, much research for the NPC-based DAB converters has been developed based on the five-level control [37–39, 43, 44].

Table 1.1: Current-Related Modulation Schemes Proposed for Different DAB Converters. Source: **[J1]**.

DAB converters	References	Optimization methods	Modulation	Solutions
Two-level	[45]	Global optimal condition method	TPS control	Analytical
	[42]	Lagrange multiplier method		
	[49]	Particle swarm optimization		
	[51]	Differential extremum method		
	[50]		EPS control	
Multi-level	[39, 43]	Numerical computation algorithms	Five-level control	Numerical
	[52]	Particle swarm optimization	Three-level control	

The optimal control strategies for improving the efficiency has been explored widely for various DAB converters, where different efficiency indices, e.g., RMS current, soft-switching, peak current, and power loss, have been analyzed [45–52]. Based on the types of optimal solutions, these modulation strategies can be divided into numerical-solution-based (NSB) control and analytical-solution-based (ASB) control strategies. For the former, the control variables (i.e., phase-shift ratios and duty cycles) can be expressed by the DC-link voltages and transferred power, and thus, the control variables can be calculated and regulated online based on the operating conditions. On the other hand, in the NSB control strategies, the numerical solutions need to be pre-calculated offline and then pre-stored in a look-up table in microcontrollers [39, 52]. Consequently, when the operating conditions/parameters (e.g., DC-link voltages) of the DAB converters change, the numerical solutions should be re-calculated and then updated to the microcontrollers, which significantly increase the control complexity and limit their implementation. Therefore, the ASB control is more applicable in practice, especially when the operating conditions/parameters change in a wide range. Due to the simpler models, which are beneficial for obtaining the analytical solutions, the current-related modulation schemes were widely researched, as shown in Table 1.1. It can be seen that ASB control strategies have not been proposed for the multi-level DAB. This is because the traditional optimal methods for obtaining the analytical solutions can hardly be used with the increased number of the control variables for the five-level control. Therefore, the ASB control strategies based on the five-level control, which can achieve generic and simple implementation, are required for the DAB converter.

1.2.2 Capacitor Voltage Balancing Control

Capacitor voltage imbalance may occur on the NPC bridge due to the asymmetry in the gate pulses, DC-link capacitors (tolerances or uneven degradation), or hardware layouts [43, 53–55]. The unbalanced voltages will increase

the voltage stresses and degrade the lifetime of the capacitors and other devices. These devices will be severely damaged when the increased voltage exceeds their voltage-blocking capability, and the safety of the system will be significantly affected [54]. Furthermore, the voltage imbalance will also distort the transformer terminal voltage v_{cd} and current i_{L1}. Thus, the modeling accuracy, and the stable and optimal operation of the converter will be affected.

Some voltage balancing control strategies were put forward to tackle the above issues [38, 43, 53–56]. During most of them, the charges flow through the neutral point is controlled by regulating the intervals of certain switching states dynamically, and thus, the voltage imbalance can be suppressed. However, there are two limitations of these previous voltage balancing methods:

1) Independent of the transformer current i_{L2}: For the original switching states employed in the steady state (which are also used to modify the capacitor voltages in most previous methods), with different polarity of i_{L2}, the direction of the charges flow through the neutral point is opposite. Therefore, to obtain required neutral-point charges, the transformer current polarity is necessary to be determined. Unfortunately, the transformer current polarity is affected by various factors, e.g., DC-link voltages and operating modes. Thus, for the application where the operating conditions change in a wide range, the transformer current polarity will be challenging to be identified online. Consequently, the transformer current models should be pre-calculated offline, and the current polarity can then be identified. Furthermore, with different modulation, e.g., minimum-RMS-current modulation, and soft-switching modulation, the transformer current models will be different. Thus, the implementation of the previous voltage balancing methods requires heavy offline calculations for the transformer current polarity.

2) Transformer current and power fluctuations: The above capacitor voltage balancing methods will also lead to transferred power/transformer current fluctuations as the voltage v_{cd} will change along with the modified phase-shift ratios, which will affect the dynamics to some extent. In certain cases, it may lead to the entire system shut-down if the overshoot current activates the protection system.

Hence, voltage balancing methods, which can be independent of the transformer current polarity and achieve smooth dynamics should be explored.

1.2.3 Fault Diagnosis and Tolerant Control

The reliability issues should be ensured for the multi-level DAB as the amount of power components increases. Among various reliability-related research, the fault diagnosis and tolerant control accounts for a majority. Two typical faults are generally analyzed for the power electronics converters, i.e., short-circuit fault (SCF) and open-circuit fault (OCF) [57–59, 63, 64, 66] of

Table 1.2: Fault Diagnosis and Tolerant Methods for Various DAB Converters. Source: **[J4]**.

Fault Diagnosis Methods			
References	DAB converters	Diagnostic signals	Characteristics
[57]	Two-level DAB	Transformer voltage and current residual	1) Faulty switch can be identified; 2) A current sensor and a winding in the magnetic core are added; 3) Diagnostic period is within three switching cycles.
[58]		Average transformer terminal voltages	1) Faulty switch can be identified; 2) Two voltage sensors for the terminal voltages are added; 3) Diagnostic period is within one switching cycle.
[59–62]		Average midpoint voltages	1) Faulty switch can be identified; 2) Voltage sensors for midpoint voltages of four bridge arms are added; 3) Diagnostic period is within one switching cycle.
[63]	Three-phase two-level DAB	DC component in phase currents	1) Faulty phase (i.e., bridge arm) can be identified instead of the specific switch; 2) Current sensors for all phase currents are added.
[64]		DC bias of phase and magnetization currents	1) Faulty switch can be identified; 2) Current sensors for all phase currents are added.
Fault-Tolerant Methods			
References	DAB converters	Methods	Characteristics
[65]	Hybrid DABs with series-resonant and phase-shifted DABs	Replace faulty module by using redundant one	1) Suitably used in a cascaded-DAB system with redundant modules; 2) Easy but the hardware cost increases significantly.
[60, 62, 66]	Two-level DAB	Primary side lower power - secondary side bypass arm (PLP-SBA)	Current overshoots and DC bias can be reduced to a safe range.
[63, 67]	Three-phase two-level DAB	Remove the faulty arm and operate the three-phase DAB in single-phase mode	Current overshoots and DC bias can be almost eliminated.
[68]		Block the gate pulses of the two switches in the faulty arm.	Current overshoots and DC bias can be reduced with lower transferred power.

the devices. A severe voltage overshoot and/or current overshoot generally appears when an SCF occurs, which can be used as fault diagnostic signals. Accordingly, software and hardware protection will be employed to shut down the DAB converters to avoid severe damage. On the other hand, for the OCF, the tolerant methods to address its negative effects can generally bring the post-fault converters back to safe operation instead of shutting it down, although some performance, e.g., power-transfer capability may be degraded. In addition, the accurate OCF identification brings more challenges in the multi-level DAB converters owing to the increased switches and complex

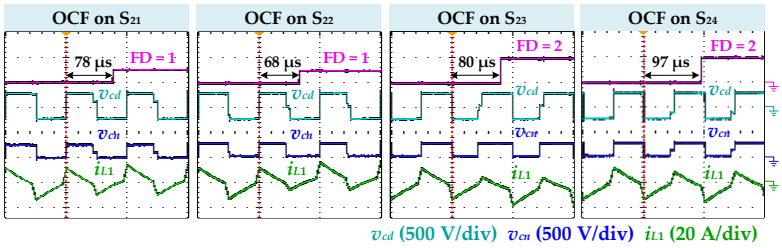


Fig. 1.7: Experimental results when the average midpoint voltage v_{cn} is applied as the fault diagnosis (FD) signal to the 2/3-level DAB converter. Source: **[J4]**.

post-fault characteristics. Therefore, the research of the OCF has attracted much attention in recent years.

When an OCF occurs in the DAB converter, negative effects, e.g., current overshoots, DC bias, and unbalanced capacitor voltages, will be seen, which significantly affect the converter reliability with increased current and voltage stresses on power devices, and result in potential saturation of the transformer [60, 61, 66]. To avoid these negative effects, the faulty switch should be located first, and then, fault-tolerant methods are required to suppress negative OCF effects. Unfortunately, the traditional OCF analysis mainly focused on the two-level DAB instead of NPC-based DAB converters, as summarized in Table 1.2. The faulty switch is generally identified by the post-fault characteristics extracted from the transformer terminal voltages v_{ab}/v_{cd}, transformer current i_{L1}/i_{L2} (i.e., inductor current), or midpoint voltages v_{cn}/v_{dn}. However, if these diagnostic signals are applied to the NPC bridge, the exact faulty switch cannot be identified since two possible switches have similar post-fault characteristics. For instance, if the average midpoint voltages (which were used in the two-level DAB converter in [59–61]) are applied as diagnostic signals directly, two possible switches (e.g., S_{21} and S_{22}) cannot be distinguished, as shown in Fig. 1.7. Therefore, it calls for fault diagnosis methods which can identify specific faulty switch.

As for the fault-tolerant methods, fault-redundant methods are usually applied to the multi-level module-cascaded converters, which employ redundant power switches or modules to replace the faulty ones to avoid the negative effects. However, these methods usually have an increased cost, and relatively slow dynamics [65]. For a single DAB converter, the fault-tolerant control usually tries to remove the faults and maintain the normal operation by adjusting the modulation configuration instead of changing hardware structure [62, 67, 68]. For instance, a "primary side lower power-secondary side bypass arm" (PLP-SBA) method is employed in the two-level DAB [59, 66], which makes the DAB converter operate in lower power conditions when OCFs occur on primary-side switches to avoid overshoot current, and bypasses the faulty bridge arm when OCFs occur on secondary-side switches to obtain a higher

power range. However, due to the increased number of switches in the NPC bridge, the 2/3-level topology has increased potential to improve post-fault power-transfer capability by modulation reconfiguration, which should be explored to enhance the post-fault performance of the converter.

1.3 Project Motivation

1.3.1 Research Questions

The overall research question of this Ph.D. project is "How to achieve efficient and reliable operation of an multi-level DAB converter applied to MVDC systems". Considering the previous research challenges analyzed in the state-of-the-art, several sub-questions are formulated:

- **Q1.** How to improve the converter efficiency through generic and simple modulation strategies?
- **Q2.** How to maintain the capacitor voltage balancing under a five-level control scheme without current polarity identification and power fluctuation?
- **Q3.** How to achieve accurate OCF diagnosis and improve the post-fault performance through a fault-tolerant control?

1.3.2 Project Objectives

The project objectives are summarized based on the above questions as:

- **O1.** Investigate the optimal modulation schemes based on analytical solutions to enhance the converter efficiency.
  To address **Q1**, the optimal modulation strategies based on the five-level control scheme should be designed, e.g., minimum-current-stress control, which need to compromise efficiency and implementation complexity. In this way, analytical solutions are required to achieve online modification of the control variables.
- **O2.** Analyze the capacitor voltage balancing control strategies to obtain smooth dynamics and low implementation burdens.
  To address **Q2**, the capacitor voltage balancing methods, which can suppress the power/current fluctuations, are required to be developed. In addition, for the conditions where the transformer current polarity is difficult to be determined, the voltage balancing methods, which can be decoupled from the transformer current polarity should be investigated to simplify the implementation.

- **O3.** Propose accurate and fast OCF diagnosis methods and fault-tolerant control methods which can enhance the post-fault power-transfer capability.
  To address **Q3**, a fault diagnosis system should be designed to accurately locate the faulty switch with a fast diagnostic speed. Subsequently, a fault-tolerant control is required to suppress negative OCF effects, and increase the maximum transferred power after the OCF occurs.

1.4 Project Limitations

Some limitations of this project are given. These could be considered in future research.

- **L1.** This project mainly focuses on control strategies of the DAB converter. However, the issues under a certain application, e.g., bidirectional power flow in the energy storage systems, have not been analyzed.
- **L2.** A trade-off between efficiency and implementation complexity is made in the proposed minimum-current-stress control strategy, while soft-switching is not taken into account in the optimization. The control strategies considering both the soft-switching and current stress are worthy being explored, where the method to obtain the analytical solutions and simplify the implementation is a key component.
- **L3.** The reliability-related research is limited to the fault-tolerant control and voltage balancing control, while other reliability aspects, e.g., thermal distribution, have not been explored in this project.
- **L4.** Limited by the laboratory conditions, the theoretical analysis was validated based on a down-scaled setup. Although all of the operating conditions/parameters (the various DC-link voltages and the entire power range) have been considered in the proposed control strategies, which is sufficient to verify their effectiveness, some additional non-ideal issues may exist in the practical prototype.

1.5 Thesis Outline

The structure of this thesis is shown in Fig. 1.8, where it can be seen that two main parts are included, i.e., Report and Selected Publications. There are five chapters in the Report based on the research outcomes, i.e., J1-J4 and C1-C3, which are presented in Section 1.6. The chapters are summarized as:

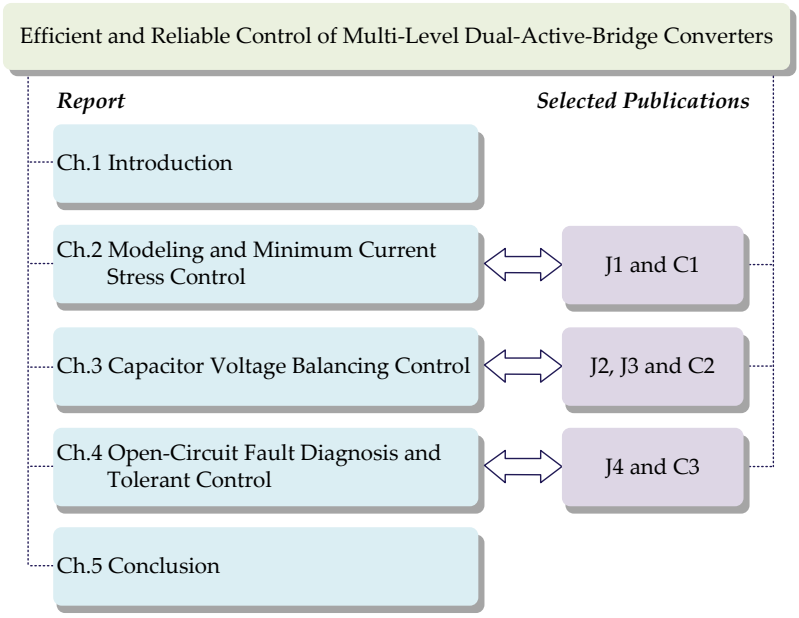


Fig. 1.8: Chapters of this thesis and the corresponding selected publications.

- **Chapter 1** gives the introduction of the Ph.D. project, including the project background, state-of-the-art of the control schemes for NPC-based DAB converters, and research motivations. The thesis structure is also presented in this chapter.
- **Chapter 2** investigates the basic switching characteristics, operating constraints and modeling for the 2/3-level DAB converter. Accordingly, optimal modulation techniques to achieve minimum current stress is analyzed to enhance the efficiency based on analytical solutions under all operating conditions.
- **Chapter 3** presents two capacitor voltage balancing control schemes for different applications. For the conditions that the current polarity during certain intervals can be easily identified, a complementary-switching-state (CSS) method can be applied to improve the dynamics. Otherwise, if the current polarity is challenging to be determined due to various operating parameters, a fixed-switching-state (FSS) method can be employed to make the voltage balancing independent of the current polarity.
- **Chapter 4** discusses the OCF diagnosis and tolerant methods for the NPC bridge in the multi-level DAB converters. Midpoint voltages

are used as the diagnostic signals in the proposed fault diagnosis method, which is able to locate the specific faulty switch. Then, a fault-tolerant control scheme based on a complementary-switch-blocking (CSB) method is presented to reduce the negative OCF effects and enhance the post-fault power-transfer capability of the DAB converters.

- **Chapter 5** provides the concluding remarks, main contributions, and future research perspectives of the Ph.D. project.

1.6 List of Publications

The outcomes during this Ph.D. project have been disseminated as journal and conference papers, and **J1-J4** and **C1-C3** are related to this thesis, as listed below.

Journal Papers

J1. **C. Song**, A. Sangwongwanich, Y. Yang, Y. Pan, and F. Blaabjerg, "Analysis and Optimal Modulation for 2/3-Level DAB Converters to Minimize Current Stress With Five-Level Control" *IEEE Trans. Power Electron.*, 2022. Status: revision in review.

J2. **C. Song**, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Capacitor Voltage Balancing for Multi-Level Dual-Active-Bridge DC-DC Converters" *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2566-2575, Mar. 2023.

J3. **C. Song**, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "A Model-Free Capacitor Voltage Balancing Method for Multi-Level DAB Converters" *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 79-84, Jan. 2023.

J4. **C. Song**, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Open-Circuit Fault Diagnosis and Tolerant Control for 2/3-Level DAB Converters" *IEEE Trans. Power Electron.*, 2022. Status: revision in review.

Conference Papers

C1. **C. Song**, Y. Yang, A. Sangwongwanich, Y. Pan, and F. Blaabjerg, "Modeling and Analysis of 2/3-Level Dual-Active-Bridge DC-DC Converters with the Five-Level Control Scheme," in *Proc. IEEE APEC*, pp. 1958-1963, Jun. 2021.

C2. **C. Song**, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Capacitor Voltage Balancing Control Scheme for 2/3-Level DAB Converters," in *Proc. IEEE IECON*, pp. 1-6, Oct. 2021.

C3. **C. Song**, Y. Yang, A. Sangwongwanich, and F. Blaabjerg, "Open-Circuit Fault Analysis and Fault-Tolerant Control for 2/3-Level DAB Converters," in *Proc. IEEE ECCE-Asia*, pp. 696-701, May. 2021.

Chapter 2

Modeling and Minimum Current Stress Control

2.1 Background

As discussed in Section **1.2.1**, the modulation strategies based on five-level control have not yet been comprehensively addressed to enhance the efficiency and simplify the implementation. The optimal control based on analytical solutions is an effective scheme for the applications where the operating conditions or parameters (e.g., DC-link voltages and transferred power) vary in a wide range during the operation. That is because the control variables expressed by analytical solutions can be automatically regulated along with various parameters without being pre-calculated offline, which simplify the control structure significantly.

Various parameters of the DAB converters can be considered, e.g., peak or RMS current of the inductor L_s [45, 47–52], reactive power [46, 69], and power losses [70, 71]. Minimizing the current stress is employed as the control objective in this chapter for two purposes, i.e., 1) to enhance the reliability by decreasing the current stress on the power devices, and also to avoid the system to run into an overcurrent trip; 2) to improve the efficiency since the RMS current can be decreased along with the peak current during most operating modes [25]. The conduction losses, copper losses, and magnetic losses are mainly determined by the RMS current [50, 71]. Furthermore, among various optimization indices including the RMS current, the peak current model is the simplest, which is beneficial to obtain the analytical solutions.

Thus, this chapter presents an optimal modulation strategy by reducing the peak current using analytical solutions. Firstly, models of transferred power are established by using an equivalent-wave method **[J1]**, **[C1]**. Subsequently, the minimum-current-stress control strategy is proposed, where the analytical solutions are obtained by combining the Karush-Kuhn-Tucker (KKT) conditions with numerical-solution analysis **[J1]**.

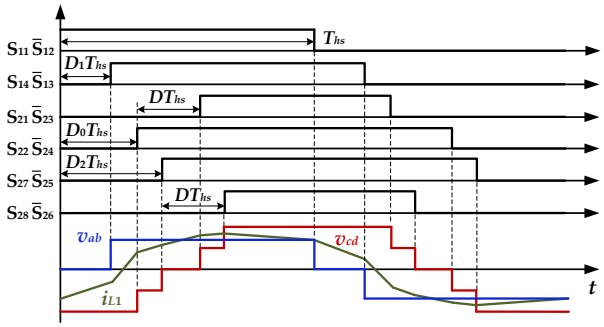


Fig. 2.1: Five-level control for 2/3-level DAB converter. Source: **[J1]**.

2.2 Analysis and Modeling of 2/3-Level DAB

2.2.1 Basic Analysis With Five-Level Control

Waveforms of the primary-side transformer current i_{L1} (also known as inductor current), and transformer terminal voltages v_{ab} and v_{cd} with the five-level control are shown in Fig. 2.1. Four control variables (i.e., DoFs) are employed to control the power flow, i.e., three phase-shift ratios D_0, D_1, and D_2, and a duty-cycle ratio D, which also affect the current stress, power losses, and other performances. The control variables are generally limited between 0 and 1 to avoid an increase in the number of operating modes and complexity, and also refrain from high current stress. In addition, the relationship between D_0 and D_2 (i.e., $D_0 > D_2$ or $D_0 < D_2$) will not change the waveform of the secondary-side voltage v_{cd}, and thus not affect the transferred power range and other performances. A similar condition also occurs on the relationships between $D_0 + D$ and D_2 **[C1]**. Thus, to simplify the analysis, only the condition of $D_0 \leq D_2 \leq (D_0 + D)$ is discussed.

Furthermore, since $D_2 + D$ is the largest phase shift, its maximum value needs to be analyzed. When $(D_2 + D) > (1 + D_0)$, which means S_{28} is ON after S_{21} is turned OFF, the two highest levels $\pm V_2$ will be replaced by 0, as shown in Fig. 2.2, and the voltage v_{cd} will be three-level (instead of five-level) in practice. That is because in such a condition, the four switches in diagonal position, e.g., S_{21}, S_{22}, S_{27}, and S_{28} will not be ON or OFF at the same time. As a result, the transferred power range will be affected, and the current stress may be increased significantly. Fig. 2.3 gives some comparative experimental results between the conditions $(D_2 + D) < (1 + D_0)$ and $(D_2 + D) > (1 + D_0)$ under the same parameters, where the peak current increases from 9.4 A to 27 A under the condition of $(D_2 + D) > (1 + D_0)$. To avoid this issue, $(D_2 + D) < (1 + D_0)$ should be satisfied. To sum up, the constraints for the control variables with the five-level control are obtained as given in **[J1]**:

$$\begin{cases} 0 \leq D_1 \leq 1 \\ 0 \leq D_0 \leq D_2 \leq (D_0 + D) \leq (D_2 + D) \leq (1 + D_0) \end{cases} \tag{2.1}$$

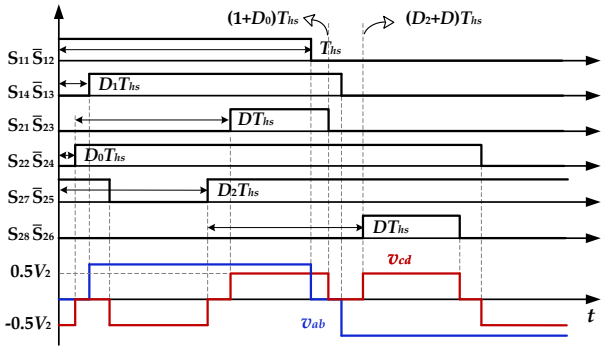
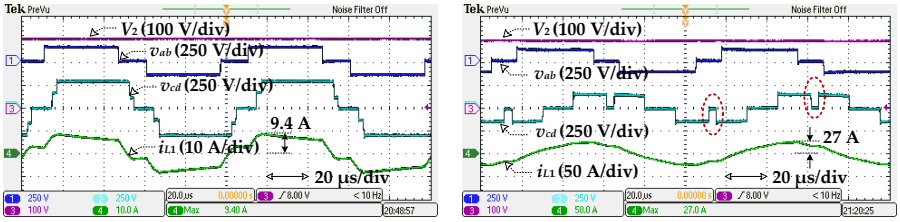


Fig. 2.2: Waveforms for 2/3-level DAB converter under $(D_2 + D) > (1 + D_0)$. Source: **[J1]**, **[C1]**.



(a) (b)

Fig. 2.3: Experimental results with the five-level control scheme under the condition V_1 = 150 V, V_2 = 300 V, R = 115 Ω and: (a) D_1 = 0.25, D_2 = 0.15, D_0 = 0.1, D = 0.25. (b) D_1 = 0.25, D_2 = 0.5, D_0 = 0.1, D = 0.7. Source: **[J1]**.

2.2.2 Power-Transfer Modeling

With the above operating constraints, the operating modes can be divided according to the relationships among the phase-shift angles. Subsequently, power modeling of each mode can be developed.

The transferred power of the DAB converter can be expressed as

$$P = \frac{1}{T_{hs}} \int_0^{T_{hs}} v_{ab}(t) i_{L1}(t) dt = \frac{1}{T_{hs}} \int_0^{T_{hs}} N v_{ab}(t) i_{L2}(t) dt \tag{2.2}$$

where the transformer currents i_{L1} and i_{L2} are obtained from

$$\begin{cases} \dfrac{di_{L1}(t)}{dt} = \dfrac{N v_{ab}(t) - v_{cd}(t)}{N L_s} \\ i_{L2}(t) = \dfrac{i_{L1}(t)}{N} \end{cases} \tag{2.3}$$

As shown in Fig. 2.1, the waveform of the transformer current i_{L1} is piecewise with different slopes in various sections. Thus, if the transferred power is calculated by piecewise integration between v_{ab} and i_{L1} based on (2.2), it will cause a heavy computational burden, especially when considering various operating modes. To

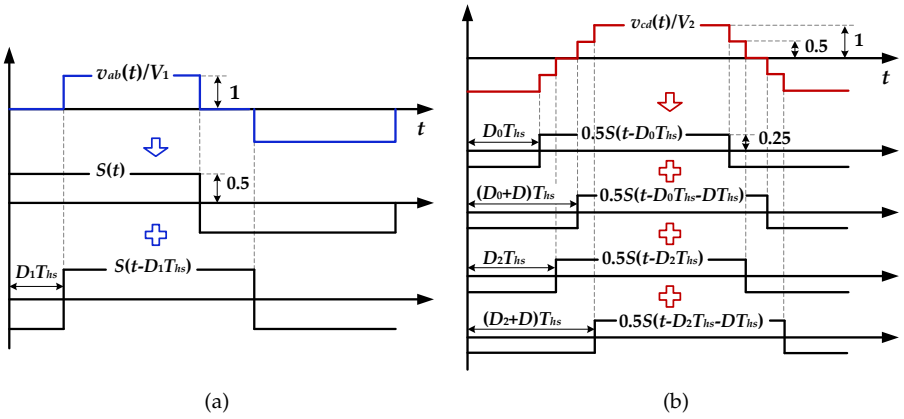


Fig. 2.4: Equivalent waveforms for: (a) v_{ab} and (b) v_{cd}. Source: **[J1]**, **[C1]**.

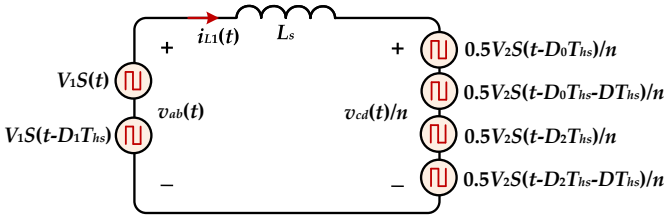


Fig. 2.5: Equivalent circuit of the 2/3-level DAB converter. Source: **[J1]**, **[C1]**.

address this challenge, the transferred power is calculated by an equivalent-waveform method in this chapter.

As shown in Fig. 2.1, the waveforms of v_{ab} and v_{cd} are three-level and five-level, respectively, which can be decomposed into different square waveforms, as shown in Fig. 2.4. Among the equivalent waveforms, $S(t)$ is the basic waveform, while other waveforms can be acquired by phase shifting the basic waveform, i.e., $S(t-x)$, where x is the phase-shift angles. There is only one phase-shift angle D_1T_{hs} on the primary side. Hence, v_{ab} can be decomposed into $S(t)$ and $S(t-D_1T_{hs})$. On the other hand, the secondary-side voltage v_{cd} can be decomposed into $S(t-D_0T_{hs})$, $S(t-(D_0+D)T_{hs})$, $S(t-D_2T_{hs})$, and $S(t-(D_2+D)T_{hs})$. By doing so, the primary and secondary voltages can be represented according to Fig. 2.5. Thus, the normalized transformer current model can be obtained as

$$i_{L1}(t)=\frac{1}{L_s}\left\{V_1\sum_{i=1}^{2}T_r(t-x_iT_{hs})-\frac{V_2}{2N}\sum_{j=1}^{4}T_r(t-x_jT_{hs})\right\} \tag{2.4}$$

where x_i and x_j are the phase-shift angles of the primary and secondary sides, respectively, i.e., $x_i\in\{0,D_1\}$, and $x_j\in\{D_2,D_0,D_2+D,D_0+D\}$, and $T_r(t)$ denotes the

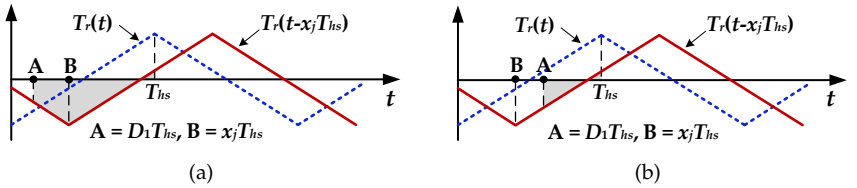


Fig. 2.6: Waveforms for calculating the integration of $T_r(t - x_j)$ when: (a) $D_1 \leq x_j$ and (b) $D_1 > x_j$. Source: **[J1]**, **[C1]**.

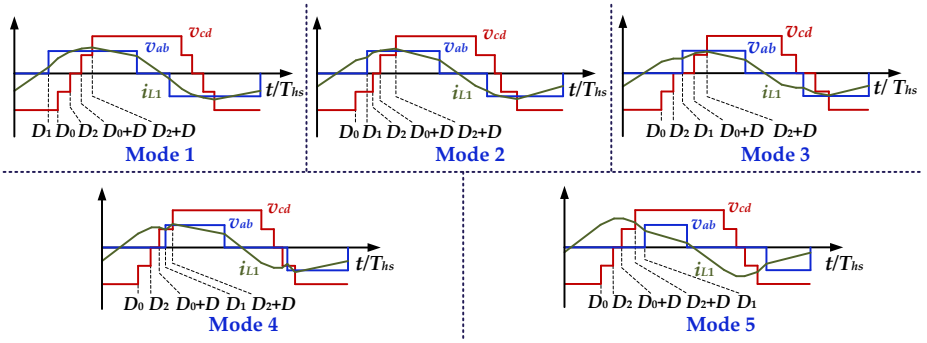


Fig. 2.7: Operating modes with five-level control. Source: **[J1]**.

integration of $S(t)$ with the expression (over one switching period) of

$$T_r(t) = \begin{cases} 0.5t - 0.25T_{hs}, & 0 \leq t < T_{hs} \\ -0.5t + 0.75T_{hs}, & T_{hs} \leq t < 2T_{hs} \end{cases} \tag{2.5}$$

By combining (2.2) and (2.4), the unified power model can be obtained as

$$P = \frac{-V_1 V_2}{2NL_r T_{hs}} \sum_{j=1}^{4} \int_{D_1 T_{hs}}^{T_{hs}} T_r(t - x_j T_{hs}) dt \tag{2.6}$$

Furthermore, two conditions, i.e., $D_1 \leq x_j$ and $D_1 > x_j$, should be considered for calculating

$$\int_{D_1 T_{hs}}^{T_{hs}} T_r(t - x_j T_{hs}) dt \tag{2.7}$$

As shown in Fig. 2.6, during $D_1 \leq x_j$, two intervals $[D_1 T_{hs}, x_j T_{hs}]$ and $[x_j T_{hs}, T_{hs}]$ with different expressions of $T_r(t - x_j)$ should be considered for obtaining the transferred power. As for the condition of $D_1 > x_j$, only one interval $[D_1 T_{hs}, T_{hs}]$ should be taken into account. Therefore, only the relationships between D_1 and x_j (j= 1, 2, 3, 4) needs to be considered to calculate the transferred power for various operating modes.

Table 2.1: Normalized Peak Current in the Five Modes. Source: **[J1]**.

Modes	Normalized peak current model i_0		
	$0 < k \leq 0.5$	$0.5 < k \leq 1$	$k > 1$
1	$2\left[-kD_1 + 2kD_0 + (2k-1)D - k + 1\right]$	$2(-kD_1 + (2k-1)D_2 + D_0 + (2k-1)D - k + 1)$	$2\left[-kD_1 + D_2 + D_0 + D + k - 1\right]$
2			
3			
4	$2\left[kD_1 - D - k + 1\right]$	$2\left[kD_1 - D - k + 1\right]$	$2\left[-kD_1 + D_2 + D_0 + D + k - 1\right]$
5			

Accordingly, the five modes are divided according to:

$$\begin{cases} D_1 \leq D_0 \leq D_2 \leq (D_0 + D) \leq (D_2 + D), & \text{Mode 1} \\ D_0 < D_1 \leq D_2 \leq (D_0 + D) \leq (D_2 + D), & \text{Mode 2} \\ D_0 \leq D_2 < D_1 \leq (D_0 + D) \leq (D_2 + D), & \text{Mode 3} \\ D_0 \leq D_2 \leq (D_0 + D) < D_1 \leq (D_2 + D), & \text{Mode 4} \\ D_0 \leq D_2 \leq (D_0 + D) \leq (D_2 + D) < D_1, & \text{Mode 5} \end{cases} \tag{2.8}$$

whose waveforms are illustrated in Fig. 2.7, and their transferred power expressions can be obtained as (2.9), where the normalized transferred power P_0 is defined as $P_0 = P/P_N$, and $P_N = V_1 V_2 T_{hs}/(4NL_s)$ is the maximum transferred power of the DAB converter.

$$P_0 = \begin{cases} 2(-D_1^2 - D_2^2 - D_0^2 - D^2 + D_1D_2 + D_1D_0 + D_1D - D_2D \\ \qquad -D_0D - D_1 + D_2 + D_0 + D), & \text{Mode 1} \\ 2(-0.5D_1^2 - D_2^2 - 0.5D_0^2 - D^2 + D_1D_2 + D_1D - D_2D \\ \qquad -D_0D - D_1 + D_2 + D_0 + D), & \text{Mode 2} \\ 2(-0.5D_2^2 - 0.5D_0^2 - D^2 + D_1D - D_0D - D_2D - D_1 + D_2 \\ \qquad +D_0 + D), & \text{Mode 3} \\ 2(0.5D_1^2 - 0.5D_2^2 - 0.5D^2 - D_1D_0 - D_2D - D_1 + D_2 + D_0 \\ \qquad +D), & \text{Mode 4} \\ 2(D_1^2 - D_1D_2 - D_1D_0 - D_1D - D_1 + D_2 + D_0 + D), & \text{Mode 5} \end{cases} \tag{2.9}$$

Furthermore, the peak current of each mode is calculated according to (2.3), as shown in Table 2.1, where k is the voltage conversion ratio, which is defined as $k = NV_1/V_2$, and the normalized peak current i_0 is defined as $i_0 = i_p/I_N$, where i_p is the peak current, and $I_N = V_2 T_{hs}/(4NL_s)$ is the maximum average transformer current.

2.3 Minimum-Current-Stress Control

According to (2.9) and Table 2.1, various combinations of four control variables D, D_0, D_1, and D_2 can achieve the same transferred power while different peak currents.

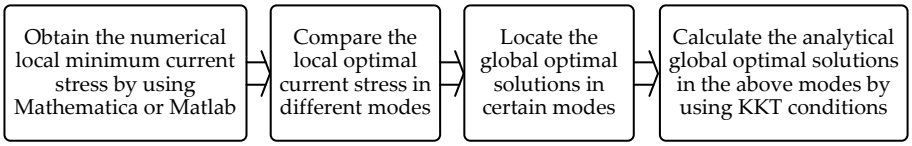


Fig. 2.8: Steps for calculating the analytical solutions. Source: **[J1]**.

To minimize the current stress, the optimum combinations of D_0, D_1, D_2, and D under different operating parameters should be identified. Accordingly, a generic minimum-current-stress control strategy for various operating conditions/parameters is proposed **[J1]**.

2.3.1 Optimal Analytical Solutions

The above optimization problem can be described as: For a reference transferred power P_0^* and with the consideration of the operating constraints for each mode, the optimal solutions should be obtained to minimize the peak current. That is

$$\begin{aligned} \min \quad & i_0(\boldsymbol{X}) \\ s.t. \quad & P_0(\boldsymbol{X}) - P_0^* = 0 \\ & f_i(\boldsymbol{X}) \leq 0, i = 1, 2, \cdots m \end{aligned} \tag{2.10}$$

in which $\boldsymbol{X} = (D_1, D_2, D_0, D)$ denotes the set of control variables, and $f_i(\boldsymbol{X})$ represents the operating constraints of each mode. KKT conditions are generally applied to obtain the analytical solutions for such an optimization problem with inequality constraints, whose unified expressions are shown as

$$\begin{cases} E(\boldsymbol{X}, \lambda, \mu_i) = i_0(\boldsymbol{X}) + \lambda(P_0(\boldsymbol{X}) - P_0^*) + \sum_{i=1}^{m} \mu_i f_i(\boldsymbol{X}) \\ \dfrac{\partial E}{\partial \boldsymbol{X}}\Big|_{\boldsymbol{X}=\boldsymbol{X}^*} = 0, \mu_i f_i(\boldsymbol{X}^*) = 0, f_i(\boldsymbol{X}^*) \leq 0, \lambda \neq 0, \mu_i \geq 0 \end{cases} \tag{2.11}$$

where $E(\boldsymbol{X}, \lambda, \mu_i)$ is the Lagrangian polynomial, $\boldsymbol{X}^* = (D_1^*, D_2^*, D_0^*, D^*)$ is the set of optimal solutions, λ and μ_i are the KKT multipliers. However, it is challenging to obtain the analytical solutions by directly using KKT conditions. That is because 1) there are complex control variables and constraints in the optimization to be solved, and 2) the power-transfer ranges may overlap in different operating modes. Therefore, the numerical solutions are employed to simplify the calculation for the analytical solutions. The calculation process is shown in Fig. 2.8, which will be elaborated in the following. Note that the DAB converter will be controlled by using the analytical solutions, and the numerical solutions are merely used to simplify the calculations.

The condition of $0 < k \leq 0.5$ is calculated as an example to show the calculation process. Fig. 2.9 shows the numerical local minimum peak current of each mode by using Mathematica. Note that local minimum current stress refers to the minimum values in each mode, while global minimum current stress refers to the minimum values considering all the modes, which is required for the minimum-current-stress

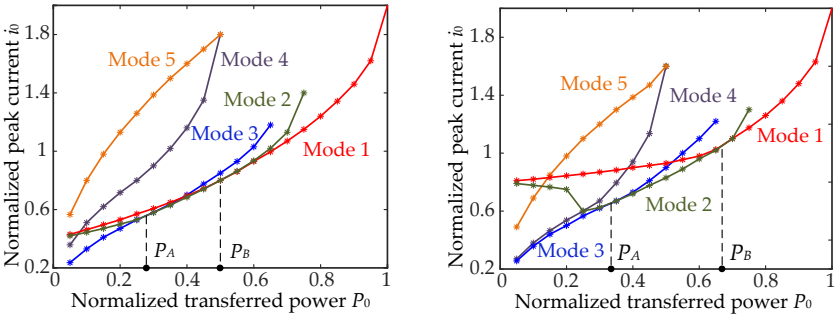


Fig. 2.9: Local minimum peak current under various modes with: (a) $k = 0.2$ and (b) $k = 0.4$. Source: **[J1]**.

control. For instance, when $P_B < P_0 \leq 1$, the global minimum current stress locates in Mode 1 since its current stress level is lower than any other mode, as shown in Fig. 2.9. Similarly, the global minimum values locate in Modes 2 and 3 during $P_A < P_0 \leq P_B$ and $0 < P_0 \leq P_A$, respectively. Therefore, the global optimal solutions are also located in the three modes during the corresponding power ranges, which are shown in Fig. 2.10. In addition, the characteristics obtained from the numerical solutions can be used to further simplify the calculation for the analytical solutions by the KKT conditions. For instance, as shown in Fig. 2.10, during $P_B < P_0 \leq 1$, the optimal solution D_1^* is 0, and thus, $D_1^* = 0$ can be applied when calculating the optimal solutions of Mode 1, and other three control variables should be obtained by the KKT conditions.

According to the above, the KKT conditions of Mode 1 can be rewritten as

$$\begin{cases} E = 2\left[2kD_0 + (2k-1)D - k + 1\right] + \lambda[2(-D_0^2 - D_2^2 \\ \quad -D^2 - D_2D - D_0D + D_2 + D_0 + D) - P_0^*)] \\ \quad +\mu_1(D_0 - D_2) + \mu_2(D_2 - D_0 - D) \\ \quad +\mu_3(D_2 + D - 1) + \mu_4(-D_0) \\ \dfrac{\partial E}{\partial D_2} = 0, \dfrac{\partial E}{\partial D_0} = 0, \dfrac{\partial E}{\partial D} = 0 \\ \lambda \neq 0, \mu_i \geq 0, i = 1,2,3,4 \\ \mu_1(D_0 - D_2) = 0, \mu_2(D_2 - D_0 - D) = 0, \\ \mu_3(D_2 + D - 1) = 0, \mu_4(-D_0) = 0, D_0 - D_2 \leq 0, \\ D_2 - D_0 - D \leq 0, D_2 + D - 1 \leq 0, -D_0 \leq 0 \end{cases} \tag{2.12}$$

In addition, it can be obtained from Fig. 2.10 and (2.12) that $f_i(\boldsymbol{X}^*) < 0$ during $P_B < P \leq 1$, and thus $\mu_i = 0 (i = 1,2,3,4)$ due to $\mu_i f_i(\boldsymbol{X}^*) = 0$. Therefore, the relationships among the optimal solutions can be acquired as

$$D_1^* = 0, D_2^* = \frac{1 - D^*}{2}, D_0^* = \frac{1}{2} + \frac{k+1}{2(k-1)} D^* \tag{2.13}$$

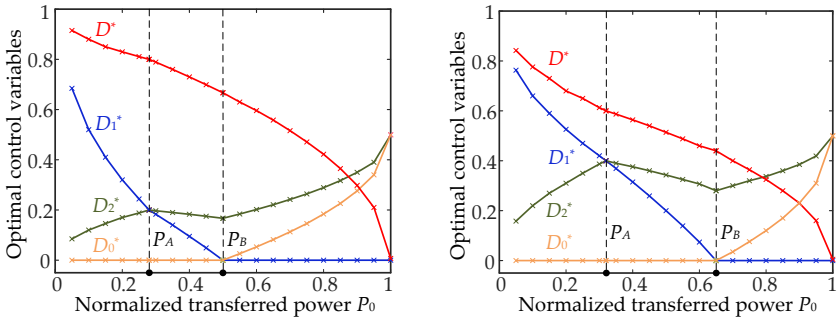


Fig. 2.10: Optimal numerical solutions with: (a) $k = 0.2$ and (b) $k = 0.4$. Source: **[J1]**.

The analytical solutions in Mode 1 can be calculated by substituting (2.13) to (2.9) as

$$\begin{cases} D_1^* = 0 \\ D_2^* = \dfrac{1}{2} - \dfrac{1-k}{2}\sqrt{\dfrac{1-P_0}{3k^2-2k+1}} \\ D_0^* = \dfrac{1}{2} - \dfrac{1+k}{2}\sqrt{\dfrac{1-P_0}{3k^2-2k+1}} \\ D^* = (1-k)\sqrt{\dfrac{1-P_0}{3k^2-2k+1}} \end{cases} \tag{2.14}$$

Since the above solutions are required under the general constraints in (2.1) and the mode constraints in (2.8), the transferred power range of Mode 1 during $0 < k \leq 0.5$ can be obtained as

$$\frac{2k(2-k)}{(k+1)^2} \leq P_0 \leq 1 \tag{2.15}$$

With a similar analysis, the optimal analytical solutions under various voltage conversion ratios and power ranges are obtained, as shown in Table 2.2. Fig. 2.11 illustrates the comparative curves between the numerical solutions obtained by Mathematica and the analytical solutions obtained by KKT conditions, where it can be seen that the numerical and analytical solutions are well aligned. Therefore, the analytical solutions obtained in Table 2.2 are the global optimal solutions for minimizing the current stress. With the obtained analytical solutions, the optimum control variables can be modified along with the changed operating parameters, instead of pre-calculating the numerical solutions.

2.3.2 Closed-Loop Control System

The closed-loop control system should be designed according to the obtained optimal analytical solutions. However, owing to the nonlinearity of the relationships between the control variables (i.e., D_0, D_1, D_2, and D) and the transferred power/voltage conversion ratio k, it is challenging for the DAB converter to achieve

Table 2.2: Analytical Solutions for Minimizing Current Stress with Various Voltage Conversion Ratios. Source: **[J1]**.

Ranges of k	Optimal control variables				Transferred power ranges
	D_1^*	D_2^*	D_0^*	D^*	
$0 < k \leq 0.5$	$1-(1-k)\sqrt{\frac{P_0}{(2-3k)k}}$	$\sqrt{\frac{kP_0}{2-3k}}$	0	$1-\sqrt{\frac{kP_0}{2-3k}}$	$0 < P_0 \leq k(2-3k)$
	$(1+k)\sqrt{\frac{1-P_0}{3k^2-2k+1}}-1$	$k\sqrt{\frac{1-P_0}{3k^2-2k+1}}$	0	$(1-k)\sqrt{\frac{1-P_0}{3k^2-2k+1}}$	$k(2-3k) < P_0 \leq \frac{2k(2-k)}{(k+1)^2}$
	0	$\frac{1}{2}-\frac{1-k}{2}\sqrt{\frac{1-P_0}{3k^2-2k+1}}$	$\frac{1}{2}-\frac{1+k}{2}\sqrt{\frac{1-P_0}{3k^2-2k+1}}$	$(1-k)\sqrt{\frac{1-P_0}{3k^2-2k+1}}$	$\frac{2k(2-k)}{(k+1)^2} \leq P_0 \leq 1$
$0.5 < k \leq 1$	$1-k\sqrt{\frac{P_0}{(1-k)(3k-1)}}$	$\sqrt{\frac{(1-k)P_0}{3k-1}}$	0	$1-k\sqrt{\frac{P_0}{(1-k)(3k-1)}}$	$0 < P_0 \leq (1-k)(3k-1)$
	$(2-k)\sqrt{\frac{1-P_0}{3k^2-4k+2}}-1$	$(1-k)\sqrt{\frac{1-P_0}{3k^2-4k+2}}$	0	$(1-k)\sqrt{\frac{1-P_0}{3k^2-4k+2}}$	$(1-k)(3k-1) < P_0 \leq \frac{2(1-k^2)}{(2-k)^2}$
	0	$\frac{1}{2}-\frac{k}{2}\sqrt{\frac{1-P_0}{3k^2-4k+2}}$	$\frac{1}{2}+\frac{k-2}{2}\sqrt{\frac{1-P_0}{3k^2-4k+2}}$	$(1-k)\sqrt{\frac{1-P_0}{3k^2-4k+2}}$	$\frac{2(1-k^2)}{(2-k)^2} < P_0 \leq 1$
$k > 1$	$1-\sqrt{\frac{P_0}{2(k-1)}}$	$1-\sqrt{\frac{P_0}{2(k-1)}}$	$\sqrt{\frac{(k-1)P_0}{2}}$	0	$0 < P_0 \leq \frac{2(k-1)}{k^2}$
	$(k-1)\sqrt{\frac{1-P_0}{k^2-2k+2}}$	$\frac{k-2}{2}\sqrt{\frac{1-P_0}{k^2-2k+2}}+\frac{1}{2}$	$\frac{k-2}{2}\sqrt{\frac{1-P_0}{k^2-2k+2}}+\frac{1}{2}$	0	$\frac{2(k-1)}{k^2} < P_0 \leq 1$

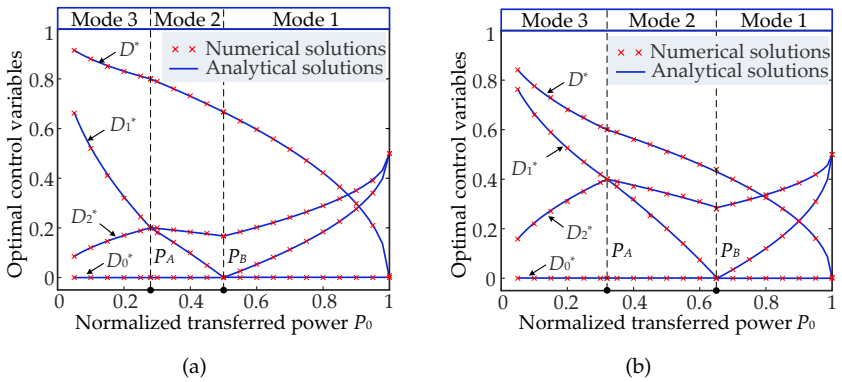


Fig. 2.11: Comparison between the numerical and analytical solutions with: (a) $k = 0.2$ and (b) $k = 0.4$. Source: **[J1]**.

fast dynamics and smooth transition along with the changed operating parameters by directly using the expressions in Table 2.2 (i.e., in terms of P_0 and k). Thus, the closed-loop control structure should be simplified based on the analytical solutions in Table 2.2.

Fig. 2.12 shows the proposed simplified closed-loop control structure, where x is the output of the proportional-integral (PI) controller, which is used to identify different modes during various power ranges, and V_{2ref} is the reference output voltage. As shown in Fig. 2.11, the duty-cycle ratio D^* decreases monotonically along with the increased power during $0 < k \leq 0.5$, which is thus expressed as $D^* = 1 - x$, and other three control variables can be calculated following (2.13). Finally, the ranges of x should be divided corresponding to the three power ranges (i.e., $0 < P_0 \leq P_A$, $P_A < P_0 \leq P_B$, and $P_B < P_0 \leq 1$) since x is utilized to indicate the transferred power. The two boundaries of D^* corresponding to P_A and P_B can be obtained as $D^* = 1 - k$ and

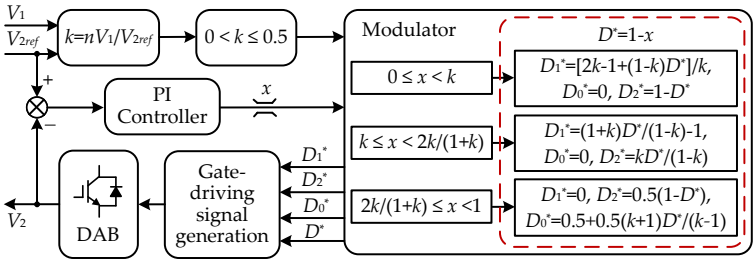


Fig. 2.12: Closed-loop control structure for the proposed minimum-current-stress control strategy when $0 < k \leq 0.5$. Source: **[J1]**.

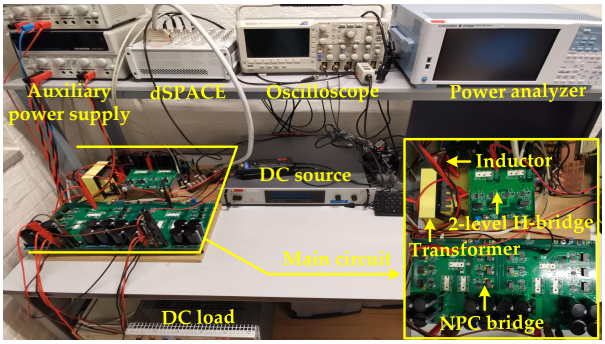


Fig. 2.13: Prototype of the 2/3-level DAB converter. Source: **[J1]**.

$D^* = (1-k)/(1+k)$, respectively. Since D^* is expressed as $1-x$ in the closed-loop control system, the two boundaries of x can be obtained as $x = k$ and $x = 2k/(1+k)$. In this way, the three power ranges where different modes are applied are converted to three ranges of x, and thus, the current sensors which are used to determine the transferred power online are not required for this closed-loop control system. Then, it can simplify the control and reduce the hardware requirement.

2.4 Experimental Verification

A down-scaled experimental prototype is developed to validate the effectiveness of the proposed control strategies, as shown in Fig. 2.13. The main parameters for experimental tests are summarized in Table 2.3. Simulations based on PLECS and MATLAB/Simulink are also performed with the same parameters.

Above all, the performance of the obtained transferred power model is validated by some simulation and experiments. Fig. 2.14 shows the theoretical, simulated, and experimental transferred-power curves under various reference output voltages, where the results are obtained in an open-loop control system. As shown in the comparative curves, the experimental and simulation results are well aligned, and slightly lower than the theoretical curve. The difference between the experimental/simulation and

Table 2.3: Main Parameters of the Simulation and Experimental Tests.

Parameters	Values
Rated power P	2.5 kW
Rated input/output voltage V_1/V_2	200/400 V
Switching frequency f_s	10 kHz
Series inductor L_s	100 μH
Transformer turns ratio N	2
DC-link capacitors C_{in}, C_U, C_L	680 μF
Power switches	Semikron SK35GB12T4
Control system	dSPACE MicroLabBox

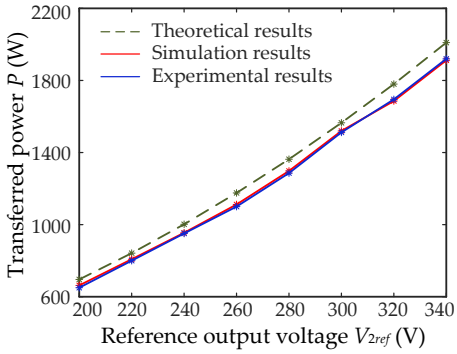


Fig. 2.14: Comparative curves of the transferred power among theoretical, simulation, and experimental results with V_1 = 150 V and R = 57.5 Ω (R is the DC load). Source: **[J1]**.

theoretical results is mainly due to the power losses, which are ignored during the modeling. Notably, the power losses were also not considered in traditional piecewise integration modeling methods unless power losses are the optimization objective. Thus, the proposed power model by using the equivalent-wave method can achieve similar performance as that of the traditional piecewise integration modeling methods, while the modeling complexity is reduced significantly.

Fig. 2.15 shows the experimental results with various control strategies including traditional SPS control, minimum-current-stress (MCS)-TPS control, traditional five-level control proposed in [39], and the proposed MCS-five-level control. As shown in Fig. 2.15, the peak current is 28.4 A in the SPS control, 18.8 A in the MCS-TPS control, 18.4 A in the traditional five-level control, and 16.4 A in the proposed control scheme. Meanwhile, the converter efficiency is measured by a power analyzer, which is increased from 84.5% (in the SPS control) to 90.8% with the proposed control scheme.

Comparative curves of the peak current and efficiency among various control strategies with various transferred power are shown in Fig. 2.16, where NS denotes the control strategy by using the optimal numerical solutions obtained by Mathematica. As shown in Fig. 2.16, the proposed MCS-five-level control strategy can decrease the

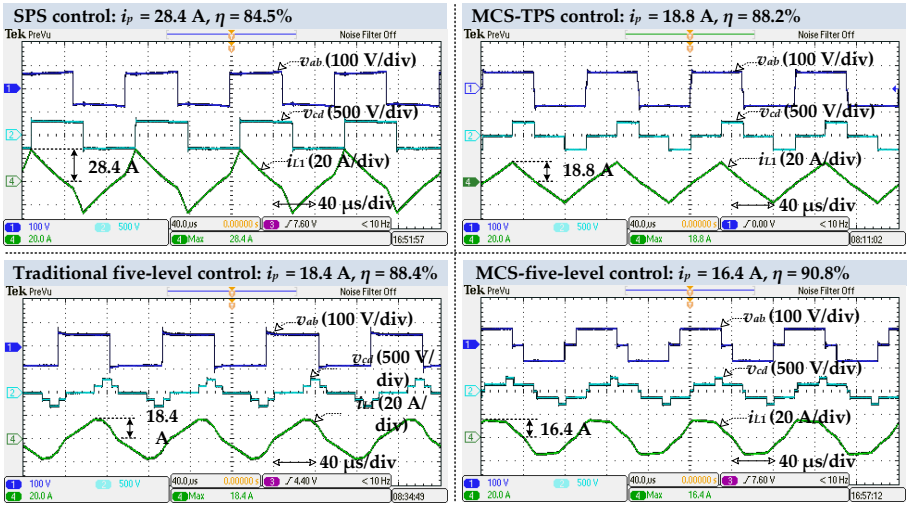


Fig. 2.15: Experimental results under the condition of V_1 = 70 V, V_2 = 300 V, and P = 580 W with the SPS control, MCS-TPS control, traditional five-level control in [39], and the proposed MCS-five-level control. Source: **[J1]**.

current stress and enhance the efficiency with various transferred power compared to the traditional control strategies. In addition, the experimental results of the proposed control and NS control are similar. However, the main advantage of the proposed strategy compared to the NS strategy (and also the five-level control strategy in [39]) is that the employed analytical solutions can simplify the control system without pre-calculating the control variables when the operating conditions/parameters (e.g., input/output voltage) change in a wide range.

Fig. 2.17 gives the comparative results of these control strategies with various input voltages (i.e., various k). As shown in Fig. 2.17, the current stress and efficiency can be improved by using the proposed control strategy with various input voltages, especially when k is far away from unity, i.e., V_1 is 150 V in Fig. 2.17.

Fig. 2.18 shows the dynamic waveforms when the transferred power and output voltage change. In Fig. 2.18 (a), the transferred power changes between 577 W and 1363 W under the condition of V_1 = 120 V and V_1 = 300 V. As for Fig. 2.18 (b), the output voltage changes between 280 V to 320 V under the condition of V_1 = 150 V, i.e., k changes between 1.07 and 0.94. As shown in Fig. 2.18, the transition between different power and output voltages can be achieved smoothly by using the proposed closed-loop control system.

2.5 Summary

In this chapter, the constraints for the control variables were analyzed for the 2/3-level DAB. Based on the obtained constraints, five operating modes were identified and the transferred power model of each mode was obtained by using an equivalent-

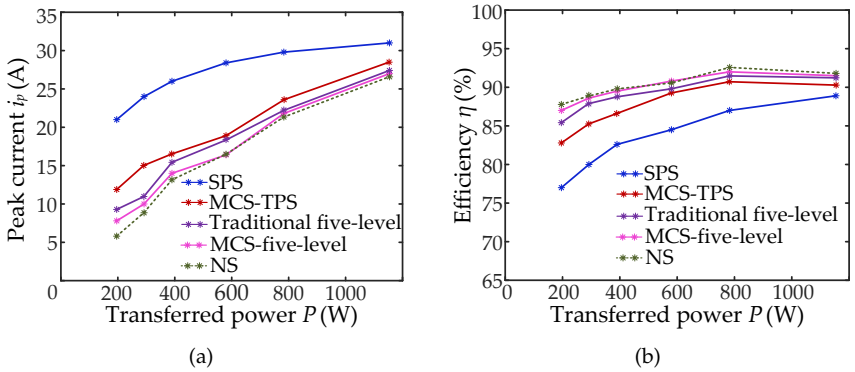


Fig. 2.16: Comparative curves under various control strategies with respect to the transferred power in terms of (a) peak current curves and (b) efficiency curves with V_1 = 70 V and V_2 = 300 V. Source: **[J1]**.

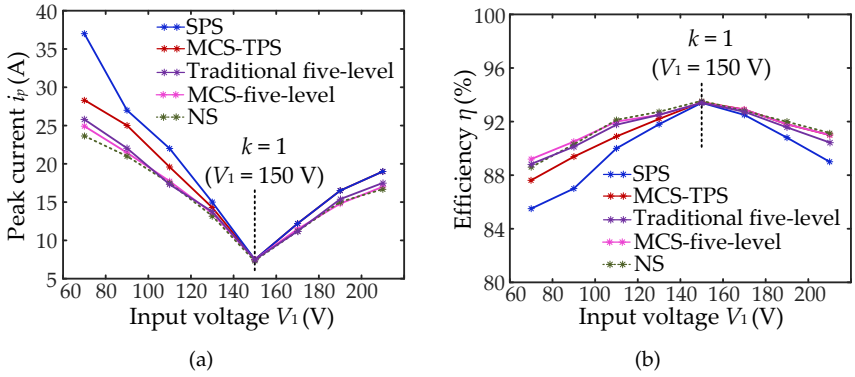
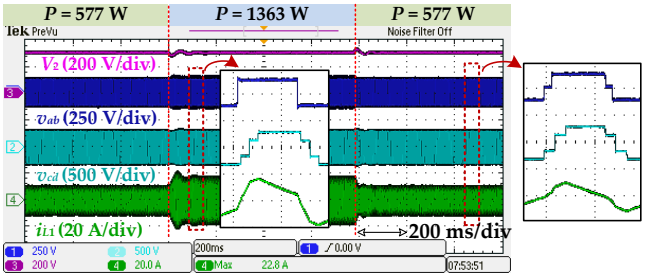


Fig. 2.17: Comparative curves under various control strategies with respect to the input voltage in terms of (a) peak current curves and (b) efficiency curves with V_2 = 300 V and P = 1000 W. Source: **[J1]**.

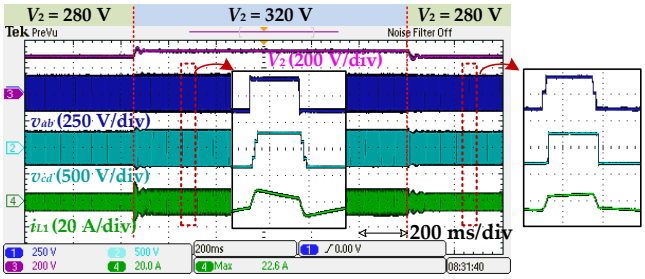
wave method to reduce the modeling complexity. Subsequently, a generic MCS control scheme and its corresponding closed-loop control system were proposed to minimize the peak current and enhance the efficiency. The analytical solutions, obtained by combining the numerical-solution analysis and KKT conditions, were utilized to realize online regulation of the control variables along with the operating conditions/parameters.

Related Publications

J1. **C. Song**, A. Sangwongwanich, Y. Yang, Y. Pan, and F. Blaabjerg, "Analysis and Optimal Modulation for 2/3-Level DAB Converters to Minimize Current Stress



(a)



(b)

Fig. 2.18: Dynamic waveforms under the closed-loop control with step changes in (a) transferred power and (b) output voltage. Source: **[J1]**.

With Five-Level Control" *IEEE Trans. Power Electron.*, 2022. Status: revision in review.

C1. **C. Song**, Y. Yang, A. Sangwongwanich, Y. Pan, and F. Blaabjerg, "Modeling and Analysis of 2/3-Level Dual-Active-Bridge DC-DC Converters with the Five-Level Control Scheme," in *Proc. IEEE APEC*, pp. 1958-1963, Jun. 2021.

Chapter 3

Capacitor Voltage Balancing Control

3.1 Background

According to the analysis in Section **1.2.2**, there are two critical issues to be explored for capacitor voltage balancing of the multi-level DAB converters: 1) current and power fluctuations and 2) identification for the polarity of the transformer current i_{L2}. The former issue affects the converter dynamics, while the latter increases the control complexity. In order to solve them, two voltage balancing control schemes are proposed in **[J2]**, **[J3]**, **[C2]**, and their suitable applications are discussed by comparing them with the traditional voltage balancing methods.

In this chapter, the relationships between the neutral-point current and the transformer current are explored under various switching states. A typical traditional voltage balancing method, i.e., modified-phase-shift (MPS) method, is analyzed to demonstrate the above two issues. Subsequently, a complementary-switching-state (CSS) method is proposed to suppress the power and current fluctuations, where the adverse switching states are replaced by their CSSs **[J2]**, **[C2]**. By doing so, the required charges to the neutral point can be increased to assist voltage balancing, and the waveform of the voltage v_{cd} can be kept unchanged to improve the dynamics. However, the MPS and CSS methods require the identification of the transformer current polarity, which can be challenging when the operating conditions vary in a wide range. Therefore, in such applications, a fixed-switching-state (FSS) method is proposed, where two additional switching states are applied to obtain certain-direction neutral-point current regardless of the transformer current polarity **[J3]**. Fig. 3.1 illustrates the general implementation structures of different voltage balancing control strategies. Finally, the performance of different voltage balancing methods are validated and compared by simulations and experiments.

Table 3.1: Switching States for NPC Bridge in the DAB Converter. Source: **[J2]**.

Switching state	ON switches (first arm*)	ON switches (second arm*)	v_{cn}/v_{dn}
[P]	$\{S_{21}, S_{22}\}$	$\{S_{25}, S_{26}\}$	V_2
[O]	$\{S_{22}, S_{23}\}$	$\{S_{26}, S_{27}\}$	$0.5V_2$
[N]	$\{S_{23}, S_{24}\}$	$\{S_{27}, S_{28}\}$	0

first arm*: composed of $S_{21}-S_{24}$; second arm*: composed of $S_{25}-S_{28}$

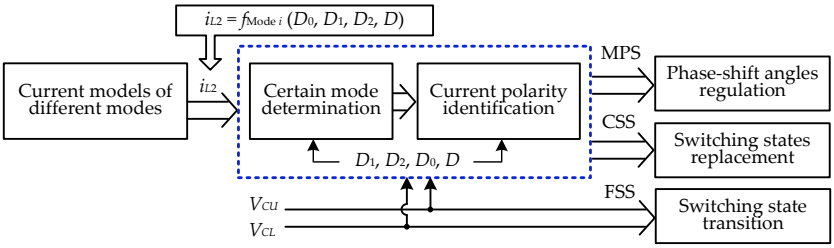


Fig. 3.1: Implementation of various capacitor voltage balancing control strategies. Source: **[J3]**.

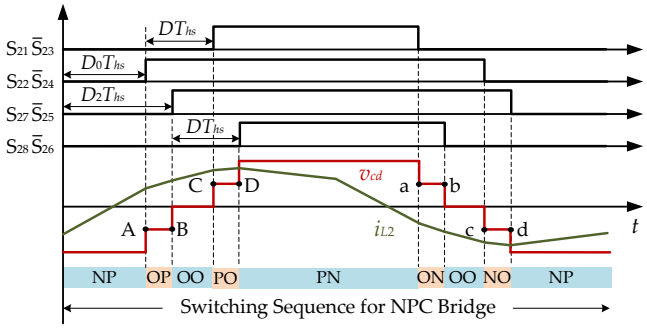


Fig. 3.2: Waveforms and switching states of the NPC bridge with the five-level control. Source: **[J2]**.

3.2 Relationships between neutral-point current and transformer current

As shown in Fig. 3.2, to simplify the analysis, the switching states of NPC bridge with the five-level control are expressed by [P], [O], and [N], which are defined in Table 3.1. Since the current flows through the neutral point o only during the four switching states [PO], [OP], [NO], and [ON], these switching states are generally regulated to balance the capacitor voltages. However, the direction of the neutral-point current, which determines that a certain capacitor (i.e., C_U or C_L) will be charged or discharged, is determined by the polarity of the transformer current i_{L2} for a certain switching state. For instance, Fig. 3.3 shows the current-flow paths for the switching state [OP] with

Table 3.2: Direction of the Neutral-Point Current Under Various Switching States. Source: **[J2]**, **[C2]**.

Intervals	Switching states	Polarity of i_{L2}	Value of v_{cd}	Current-flow path	Direction of i_o.
[A, B]	[OP]	$i_{L2} > 0^*$	$-0.5V_2$	$S_{25} \rightarrow S_{26} \rightarrow S_{23} \rightarrow D_2$	$i_o > 0^*$
		$i_{L2} < 0$		$D_1 \rightarrow S_{22} \rightarrow D_{26} \rightarrow D_{25}$	$i_o < 0$
[C, D]	[PO]	$i_{L2} > 0$	$0.5V_2$	$D_3 \rightarrow S_{26} \rightarrow D_{22} \rightarrow D_{21}$	$i_o < 0$
		$i_{L2} < 0$		$S_{21} \rightarrow S_{22} \rightarrow S_{27} \rightarrow D_4$	$i_o > 0$
[a, b]	[ON]	$i_{L2} > 0$	$0.5V_2$	$D_{28} \rightarrow D_{27} \rightarrow S_{23} \rightarrow D_2$	$i_o > 0$
		$i_{L2} < 0$		$D_1 \rightarrow S_{22} \rightarrow S_{27} \rightarrow S_{28}$	$i_o < 0$
[c, d]	[NO]	$i_{L2} > 0$	$-0.5V_2$	$D_3 \rightarrow S_{26} \rightarrow S_{23} \rightarrow S_{24}$	$i_o < 0$
		$i_{L2} < 0$		$D_{24} \rightarrow D_{23} \rightarrow S_{27} \rightarrow D_4$	$i_o > 0$

$i_{L2} > 0^*$: i_{L2} flows from the primary to secondary side; $i_o > 0^*$: i_o is injected into the neutral point

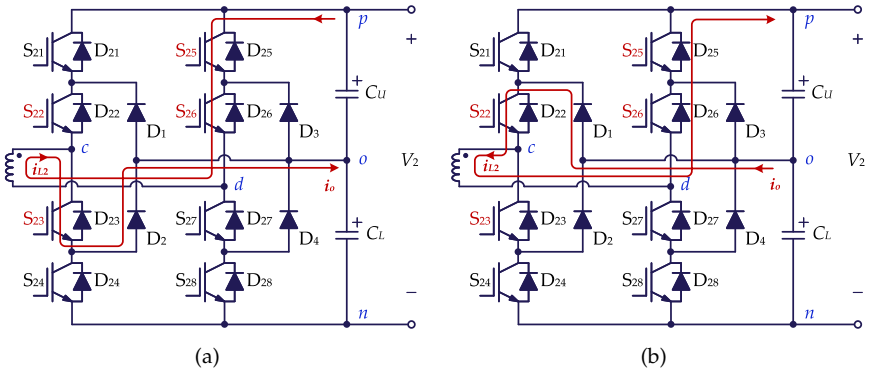


Fig. 3.3: Current-flow paths under the switching state [OP] when: (a) $i_{L2} > 0$ and (b) $i_{L2} < 0$. Source: **[J2]**, **[C2]**.

both positive and negative transformer current. It can be seen from Fig. 3.3 that with opposite transformer current polarity, the direction of the current i_o (i.e., the charges) will also change. Similarly, the relationships between the neutral-point current and the transformer current polarity for the other three switching states can be summarized in Table 3.2. Therefore, the transformer current polarity information is required to be considered when the switching states are regulated.

A typical MPS voltage balancing control strategy is shown in Fig. 3.4 when $V_{CU} > V_{CL}$ and the average transformer currents I_{L2} [A, B] > 0 and I_{L2} [C, D] > 0 (i.e., I_{L2} [a, b] < 0 and I_{L2} [c, d] < 0 due to the symmetry of the transformer current) [38], where the solid lines denote the waveforms after the MPS method is applied, and the dotted lines denote the waveforms in steady state. Since $i_o > 0$ is required for the condition of $V_{CU} > V_{CL}$, according to Table 3.2, a required positive i_o can be achieved during [A, B] and [c,d]. Thus, the two switching states during [A, B] and [c, d], i.e., [OP] and [NO], are defined as beneficial switching states, and the other two switching states, i.e., [PO] and [ON], which will further accelerate the voltage imbalance, are defined as adverse switching states. Therefore, the dwell time

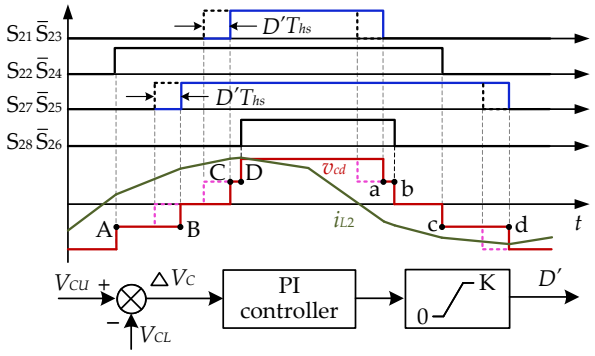


Fig. 3.4: A traditional capacitor voltage balancing control strategy based on MPS method under the condition of $V_{CU} > V_{CL}$ when I_{L2} [A, B] > 0, and I_{L2} [C, D] > 0. The dotted lines denote the waveforms in steady state without the voltage balancing control. Source: **[J2]**, **[C2]**.

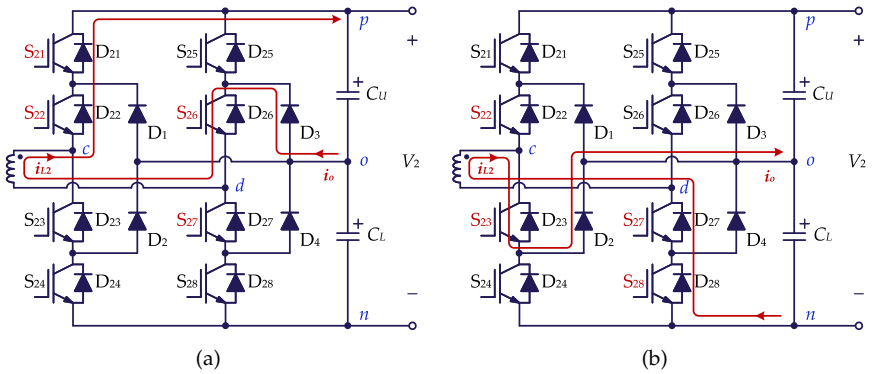


Fig. 3.5: Current-flow paths during the interval [C, D] with: (a) original switching state [PO], and (b) its complementary switching state [ON]. Source: **[J2]**.

of [OP] and [NO] are increased while the other two intervals are decreased by an additional phase-shift ratio D' for balancing the capacitor voltages. Since the voltage v_{cd} changes when the voltage balancing control is enabled, the transformer current i_{L2} will fluctuate according to (2.3), which will cause transferred power fluctuations and current overshoots. Furthermore, if the peak current exceeds the rated value, the converter will be shut down and the entire system will not be able to operate.

3.3 CSS Voltage Balancing Method

Based on the above analysis, the current fluctuations can be minimized if the voltage v_{cd} can be kept unchanged during the voltage balancing. Therefore, the CSS pairs are defined as the two switching states, which can achieve: 1) opposite

Table 3.3: Capacitor Conditions with the CSS Method Under Mode I. Source: **[J2]**.

Intervals	Steady state		Balancing state	
	Formed capacitors	Conditions	Formed capacitors	Conditions
[A, B]	C_U	Discharged	C_U	Discharged
[C, D]	C_U	Charged	C_L	Charged
[a, b]	C_L	Discharged	C_U	Discharged
[c, d]	C_L	Charged	C_L	Charged

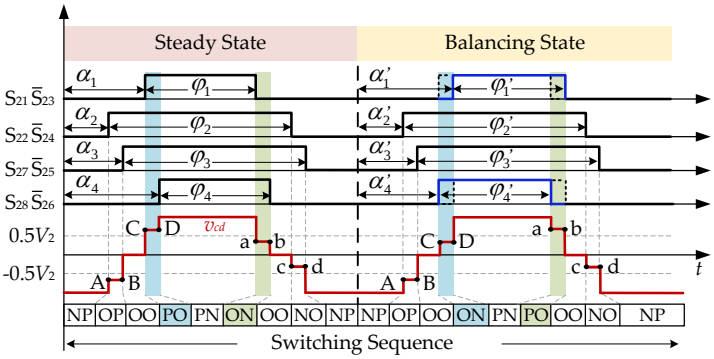


Fig. 3.6: Implementation of the CSS voltage balancing control under Mode I: $I_{L1}[A,B] > 0$ and $I_{L1}[C,D] > 0$ during $V_{CU} > V_{CL}$. The dotted lines are the steady-state waveforms without the voltage balancing control. Source: **[J2]**, **[C2]**.

current-flow direction of i_o and 2) identical voltage v_{cd}. Accordingly, two CSS pairs can be obtained from Table 3.2, i.e., [OP] and [NO], [PO] and [ON]. There are two beneficial and two adverse switching states due to the symmetry, and if the adverse ones are replaced by their corresponding CSSs, the required neutral-point charges can be increased without affecting the waveform of the voltage v_{cd}. As a result, smooth dynamics can be achieved.

For instance, it can be obtained from Fig. 3.4 that [PO] and [ON], which are during the intervals [C, D] and [a, b], are adverse for voltage balancing when $V_{CU} > V_{CL}$. After replacing them by using their corresponding CSSs, i.e., replacing [PO] by [ON] during the interval [C, D], and replacing [ON] by [PO] during the interval [a, b], the capacitors that the neutral-point current flows through will change, as shown in Table 3.3. For example, during the interval [C, D], the original switching state is [PO], and the current conduction path is shown in Fig. 3.5 (a). The upper capacitor C_U is charged during this interval, and thus it is adverse for the voltage balancing under the condition of $V_{CU} > V_{CL}$. On the other hand, if [PO] is replaced by its CSS [ON], the lower capacitor C_L will be charged, as shown in Fig. 3.5 (b). By doing so, all the four switching states can assist voltage balancing after applying the CSS method. Meanwhile, the voltage v_{cd} will not change after the replacement. Hence, the power and current fluctuations caused by changed voltage v_{cd} during the balancing can be significantly suppressed.

The CSS control strategy under the above condition can be implemented as shown in Fig. 3.6, which is defined as Mode I. φ_i and α_i are the duty cycles and phase-shift angles during the steady state, which can be expressed as

$$\begin{cases} \alpha_1 = (D_0 + D)T_{hs}, \alpha_2 = D_0 T_{hs}, \alpha_3 = D_2 T_{hs}, \alpha_4 = (D_0 + D)T_{hs} \\ \varphi_1 = \varphi_4 = (1 - D)T_{hs}, \varphi_2 = \varphi_3 = (1 + D)T_{hs} \end{cases} \tag{3.1}$$

and α_i' and φ_i' are those during the balancing state after the CSS control is activated. As shown in Fig. 3.6, to achieve the CSS replacement, the phase-shift angle of S_{21} should be increased by $(\alpha_3 - \alpha_2)$, and that of S_{28} should be decreased by the same phase-shift angle, while other control variables are kept unchanged. Therefore, the balancing-state control variables can be calculated as

$$\text{Mode I}: \begin{cases} \alpha_1' = \alpha_1 + (\alpha_3 - \alpha_2), \alpha_2' = \alpha_2, \alpha_3' = \alpha_3, \alpha_4' = \alpha_4 - (\alpha_3 - \alpha_2) \\ \varphi_i' = \varphi_i (i = 1, 2, 3, 4) \end{cases} \tag{3.2}$$

For the other three conditions, i.e., I_{L2} [A, B] > 0 and I_{L2} [C, D] < 0 (Mode II), I_{L2} [A, B] < 0 and I_{L2} [C, D] > 0 (Mode III), I_{L2} [A, B] < 0 and I_{L2} [C, D] < 0 (Mode IV), the implementations of the CSS method are shown in Fig. 3.7, and the expressions of the phase-shift angles and duty cycles during the balancing state can be obtained in a similar way as

$$\text{Mode II}: \begin{cases} \alpha_i' = \alpha_i (i = 1, 2, 3, 4) \\ \varphi_1' = \varphi_1 + (\alpha_3 - \alpha_2), \varphi_2' = \varphi_2 + (\alpha_3 - \alpha_2) \\ \varphi_3' = \varphi_3 + (\alpha_3 - \alpha_2), \varphi_4' = \varphi_4 + (\alpha_3 - \alpha_2) \end{cases} \tag{3.3}$$

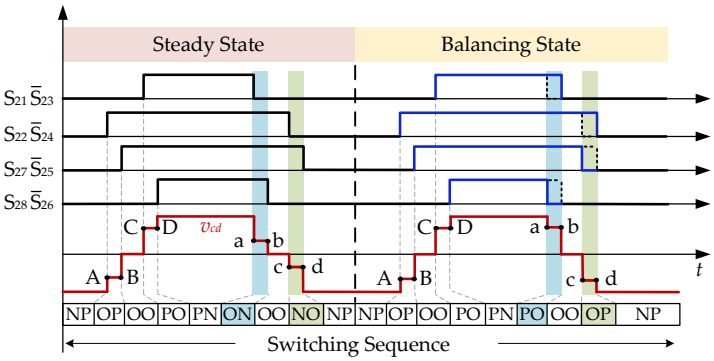
$$\text{Mode III}: \begin{cases} \alpha_1' = \alpha_1 + (\alpha_3 - \alpha_2), \alpha_2' = \alpha_2 + (\alpha_3 - \alpha_2) \\ \alpha_3' = \alpha_3 - (\alpha_3 - \alpha_2), \alpha_4' = \alpha_4 - (\alpha_3 - \alpha_2) \\ \varphi_1' = \varphi_1 - (\alpha_3 - \alpha_2), \varphi_2' = \varphi_2 - (\alpha_3 - \alpha_2) \\ \varphi_3' = \varphi_3 + (\alpha_3 - \alpha_2), \varphi_4' = \varphi_4 + (\alpha_3 - \alpha_2) \end{cases} \tag{3.4}$$

$$\text{Mode IV}: \begin{cases} \alpha_1' = \alpha_1, \alpha_2' = \alpha_2 + (\alpha_3 - \alpha_2) \\ \alpha_3' = \alpha_3 - (\alpha_3 - \alpha_2), \alpha_4' = \alpha_4 \\ \varphi_i' = \varphi_i, (i = 1, 2, 3, 4) \end{cases} \tag{3.5}$$

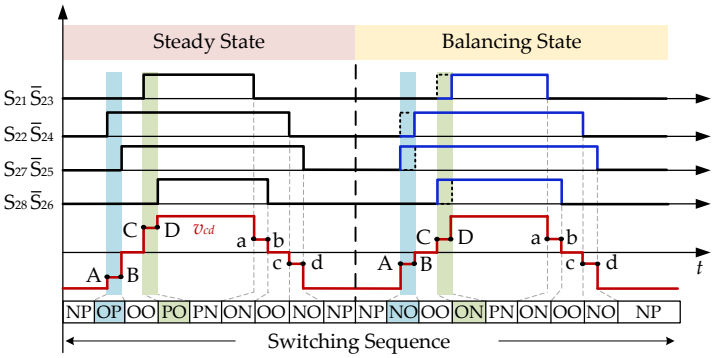
In addition, as the required neutral-point current will be opposite for the conditions of $V_{CU} > V_{CL}$ and $V_{CU} < V_{CL}$, the implementation for the condition of $V_{CU} < V_{CL}$ can be summarized in Table 3.4. The control structure of the CSS method is shown in Fig. 3.8. When the difference between the two capacitor voltages, i.e., $\triangle V_C$, exceeds the threshold V_{thr}, the voltage balancing control is enabled, and certain modes will be selected according to the transformer current polarity, which is determined by the current model.

3.4 FSS Voltage Balancing Method

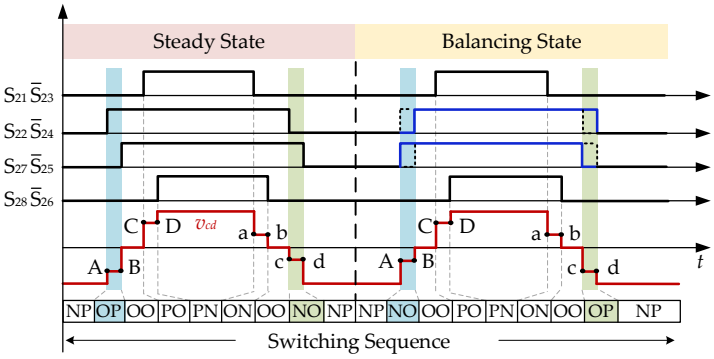
The CSS method can improve the converter dynamics by reducing power and current fluctuations after the voltage balancing control is enabled. However, the employed switching states to regulate the capacitor voltages requires the current polarity



(a)



(b)



(c)

Fig. 3.7: Implementation of the CSS voltage balancing control when $V_{CU} > V_{CL}$ under: (a) Mode II, (b) Mode III, and (c) Mode IV. Source: **[J2]**, **[C2]**.

Table 3.4: Implementation of the CSS Voltage Balancing Control During Various Conditions.

Voltage difference	Current polarity	Diagram	Implementation
$V_{CU} > V_{CL}$	I_{L2} [A, B] > 0 , I_{L2} [C, D] > 0	Fig. 3.6	Eq. (3.2)
	I_{L2} [A, B] > 0, I_{L2} [C, D] < 0	Fig. 3.7 (a)	Eq. (3.3)
	I_{L2} [A, B] < 0, I_{L2} [C, D] > 0	Fig. 3.7 (b)	Eq. (3.4)
	I_{L2} [A, B] < 0, I_{L2} [C, D] < 0	Fig. 3.7 (c)	Eq. (3.5)
$V_{CU} < V_{CL}$	I_{L2} [A, B] > 0 , I_{L2} [C, D] > 0	Fig. 3.7 (c)	Eq. (3.5)
	I_{L2} [A, B] > 0, I_{L2} [C, D] < 0	Fig. 3.7 (b)	Eq. (3.4)
	I_{L2} [A, B] < 0, I_{L2} [C, D] > 0	Fig. 3.7 (a)	Eq. (3.3)
	I_{L2} [A, B] < 0, I_{L2} [C, D] < 0	Fig. 3.6	Eq. (3.2)

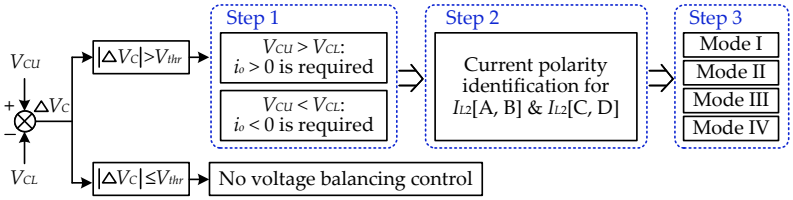


Fig. 3.8: Control structure of the CSS voltage balancing control strategy. Source: **[J2]**.

identification in the MPS and CSS methods. However, the transformer current polarity model is affected by various factors like DC-link voltages and transferred power, and will also be different under various operating modes. Therefore, it will be challenging to acquire a generic model to identify the transformer current polarity when the DAB converter is employed in the applications where the operating conditions/parameters may vary in a wide range. Furthermore, the parameter variations and operating mode changes may affect the performance of these model-based voltage balancing control strategies, including the traditional MPS control and the proposed CSS control, which results in an increased balancing period and even further voltage imbalance. Therefore, the CSS voltage balancing control can be used in the applications where the transferred power and/or DC-link voltages vary in a limited range since the current polarity can easily be determined in such conditions. Accordingly, a novel control strategy which can be decoupled from the current polarity is proposed in **[J3]**.

As analyzed previously, the original four switching states, i.e., [PO], [OP], [NO], and [ON], cannot achieve a model-free voltage balancing control. Therefore, other switching states should be employed during the balancing to address this issue. Figs. 3.9 and 3.10 show the current-flow paths for two switching states [$N_{(+)}N_{(+)}$] and [$P_{(-)}P_{(-)}$] (defined in Table 3.5), which fulfill the above requirements. As shown in Fig. 3.9, for the condition of $V_{CU} > V_{CL}$, i_o will be injected into the neutral point regardless of the transformer current polarity under the switching state [$N_{(+)}N_{(+)}$]. Similarly, as shown in Fig. 3.10, for the condition of $V_{CU} < V_{CL}$, a negative i_o can always be obtained under the switching state [$P_{(-)}P_{(-)}$].

These two switching states provide a possibility to realize a model-free voltage balancing method. However, the dwell time and position where the two switching states are applied should be properly determined. Several principles should be taken into account when designing the voltage balancing control strategy, i.e.,

Table 3.5: Additional Switching States for Voltage Balancing Control. Source: **[J3]**.

Switching state	ON switches (first arm)	ON switches (second arm)
$[P_{(+)}]$	$\{S_{21}\}$	$\{S_{25}\}$
$[P_{(-)}]$	$\{S_{22}\}$	$\{S_{26}\}$
$[N_{(+)}]$	$\{S_{23}\}$	$\{S_{27}\}$
$[N_{(-)}]$	$\{S_{24}\}$	$\{S_{28}\}$

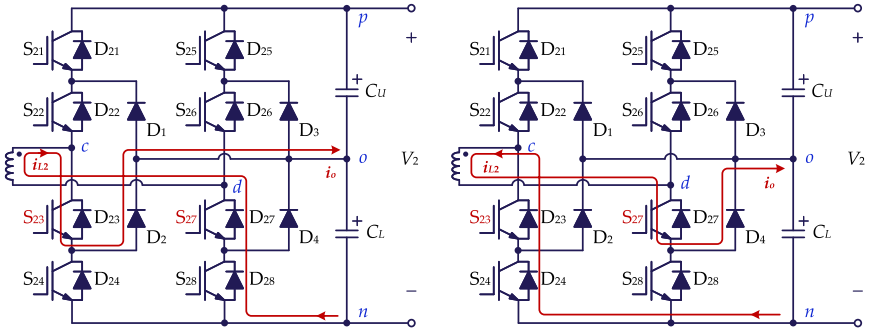


Fig. 3.9: Current-flow path with $[N_{(+)}N_{(+)}]$ when: (a) $i_{L2} > 0$ and (b) $i_{L2} < 0$. Source: **[J3]**.

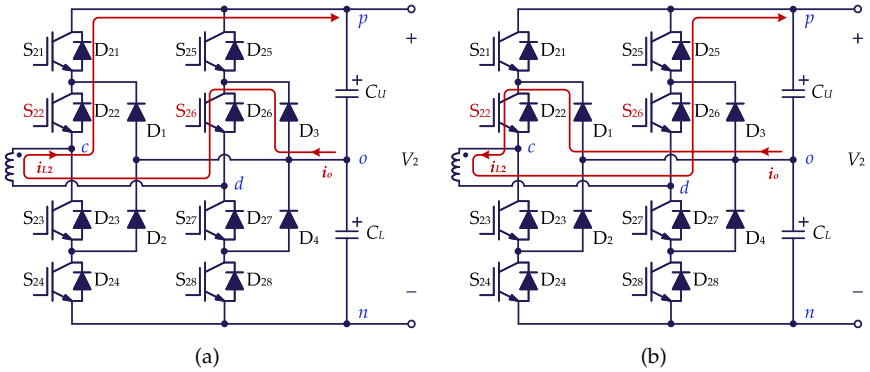


Fig. 3.10: Current-flow path with $[P_{(-)}P_{(-)}]$ when: (a) $i_{L2} > 0$ and (b) $i_{L2} < 0$. Source: **[J3]**.

- The gate-driving signals should be kept symmetrical in a switching period to maintain a symmetrical voltage v_{cd} and to avoid DC bias.
- To simplify the implementation, the amount of control variables should not be increased after the voltage balancing control is activated, i.e., the intervals where $[N_{(+)}N_{(+)}]$ and $[P_{(-)}P_{(-)}]$ are employed should be ensured by the exiting four duty-cycle and phase-shift ratios.

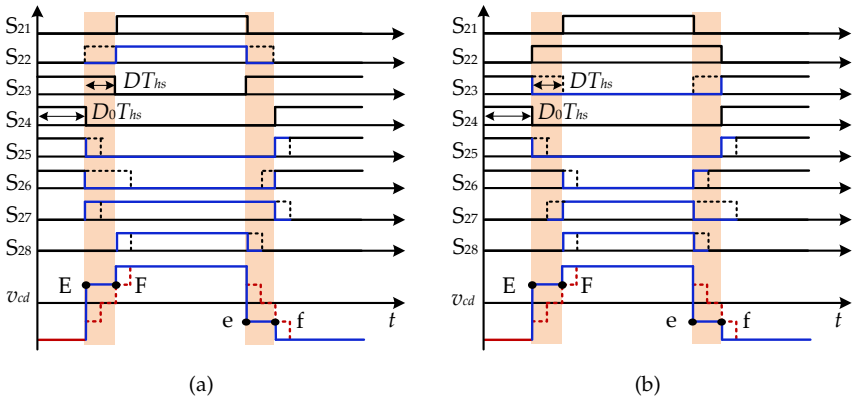


Fig. 3.11: Dynamic waveforms of the FSS method by employing: (a) $[N_{(+)}N_{(+)}]$ when $V_{CU} > V_{CL}$, and (b) $[P_{(-)}P_{(-)}]$ when $V_{CU} < V_{CL}$. The dotted lines are the steady-state waveforms without voltage balancing control. Source: **[J3]**.

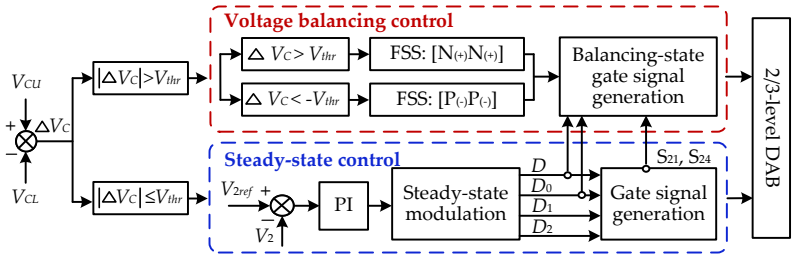


Fig. 3.12: Control structure of the FSS method. Source: **[J3]**.

- Certain gate pulses should be kept unchanged after enabling the FSS control, which are used as basic signals to obtain the entire switching sequence. Otherwise, complicated pulse generation is required, resulting in complex implementation.

The dynamic waveforms with the proposed FSS method is shown in Fig. 3.11, where the dotted lines are the steady-state waveforms, and the solid lines are the waveforms when the FSS control is enabled. The corresponding control structure is shown in Fig. 3.12. As shown in Figs. 3.11 and 3.12, the fixed switching state, i.e., $[N_{(+)}N_{(+)}]$ during $V_{CU} > V_{CL}$, or $[P_{(-)}P_{(-)}]$ during $V_{CU} < V_{CL}$, is employed at the two intervals [E, F] and [e, f]. During the voltage balancing, the waveform of the voltage is controlled by D_0 and D, as shown in Fig. 3.11, without introducing additional control variables. Moreover, the gate-driving signals of S_{21} and S_{24} will not change during the

voltage balancing, which can be used to obtain the other gate-driving signals as

$$\begin{aligned} V_{CU} > V_{CL} &: \begin{cases} S_{22} = S_{21}, S_{23} = \overline{S}_{21}, S_{28} = S_{21} \\ S_{25} = S_{24}, S_{26} = S_{24}, S_{27} = \overline{S}_{24} \end{cases} \\ V_{CU} < V_{CL} &: \begin{cases} S_{26} = \overline{S}_{21}, S_{27} = S_{21}, S_{28} = S_{21} \\ S_{22} = \overline{S}_{24}, S_{23} = S_{24}, S_{25} = S_{24} \end{cases} \end{aligned} \tag{3.6}$$

By doing so, the above three principles for the implementation of the FSS method can be satisfied.

3.5 Comparison of Various Balancing Methods

3.5.1 Experimental Comparison

Experimental tests are performed to compare different voltage balancing methods, and then, the advantages, disadvantages, and suitable applications for each voltage balancing method are summarized.

Fig. 3.13 shows the experimental waveforms when applying the CSS and FSS methods and the traditional MPS method when the initial capacitor voltage difference is 50 V, where the transformer current polarity for the MPS and CSS methods is determined offline. As shown in Fig. 3.13 (a) and (b), there are fluctuations in the transformer current and the output voltage (i.e., transferred power) after the MPS method is activated. The dynamics, including the settling time t_b, peak current i_{pb}, and fluctuating output voltage $\triangle V_2$ (i.e., the error between the balancing-state output voltage and the steady-state output voltage), with the MPS control scheme are different under various upper threshold K (see Fig. 3.4). Note that in order to avoid waveform distortion due to the changed switching sequence, the additional phase-shift ratio should satisfy $D' \leq D$, and thus, the threshold K is also less than D. In Fig. 3.13 (a) and (b), K is set as 0.15 (i.e., the maximum value) and 0.075, respectively. After the MPS voltage balancing control is enabled, the difference between the two capacitor voltages can become equal by using t_{b1}. However, due to the current and power fluctuations, the converter is able to enter a new steady state, i.e., the output voltage is kept constant at the reference value, after another regulating interval of t_{b2}. Therefore, the total settling time t_b is $t_b = t_{b1} + t_{b2}$. From Fig. 3.13 (a) and (b), it can be seen that the balancing time t_{b1} can be shorten with an increased K. However, it will result in a larger fluctuation on the output voltage and transformer current. Thus, the regulating time t_{b2} will be increased to realize the reference output voltage. Hence, when applying the MPS control method in practice, the value of K should be suitably chosen after compromising the settling time and current/power fluctuations.

As for the CSS method, the current fluctuations can be effectively reduced, as shown in Fig. 3.13 (c), and the output voltage can be kept constant. Thus, after the two capacitor voltages are balanced, the DAB converter enters the new steady state shortly. Therefore, the entire settling time t_b is equal to the balancing time t_{b1}. In addition, as shown in Fig. 3.13 (d), the fluctuations during the voltage balancing also occur with the FSS method, which is similar to the MPS method.

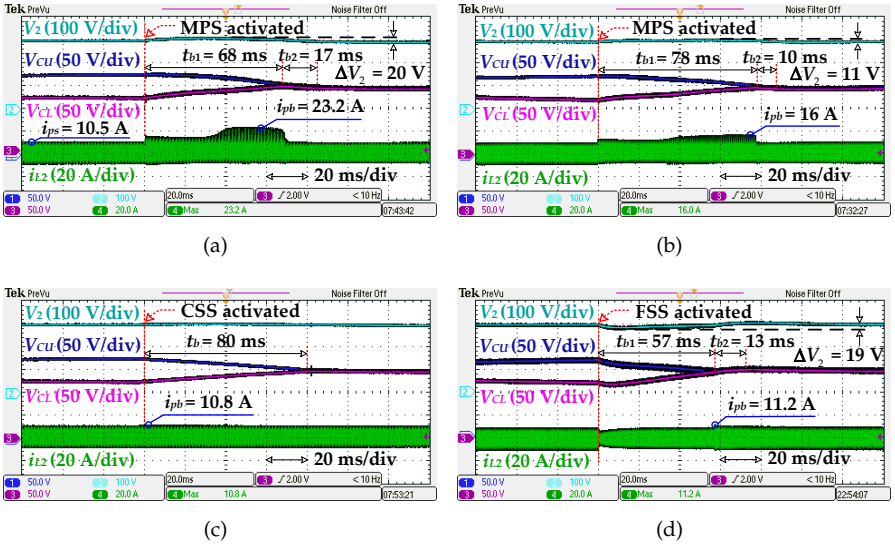


Fig. 3.13: Experimental waveforms after applying various voltage balancing control schemes when $V_{CU} - V_{CL}$ = 50 V under V_1 = 140 V, V_2 = 300 V, P = 1580 W, D = 0.15, D_1 = 0.05, D_2 = 0.2, and D_0 is set as the output of the PI controller in closed-loop control with: (a) traditional MPS method under K = 0.15, (b) traditional MPS method under K = 0.075, (c) proposed CSS method, and (d) FSS method. Source: **[J3]**.

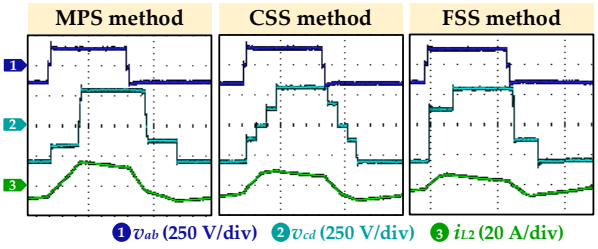


Fig. 3.14: Zoom-in experimental results after applying different voltage balancing control schemes. Source: **[J3]**.

Furthermore, the zoom-in transient waveforms of the above voltage balancing control schemes are shown in Fig. 3.14. The transient waveforms will become asymmetrical during the balancing with the MPS method, and thus resulting in DC bias and high peak current. As for the CSS method, the transient waveforms can be maintained unchanged. Thus, the current fluctuations will be significantly suppressed. In addition, the transient waveforms can be kept symmetrical with the FSS method, which can avoid significant current overshoots. However, since the waveform of the voltage v_{cd} changes after the FSS method is enabled, the transformer current will also fluctuate.

Fig. 3.15 illustrates the comparative curves of the settling time t_b and current increment after applying the above three voltage balancing control schemes with

Table 3.6: Control Variables of the Experiments in Fig. 3.15.

Transferred power (W)	Control variables
390	$D_1 = 0.20$, $D_2 = 0.10$, $D = 0.15$
570	$D_1 = 0.15$, $D_2 = 0.10$, $D = 0.15$
780	$D_1 = 0.10$, $D_2 = 0.12$, $D = 0.12$
1150	$D_1 = 0.05$, $D_2 = 0.15$, $D = 0.10$
1580	$D_1 = 0.05$, $D_2 = 0.20$, $D = 0.15$
1920	$D_1 = 0.05$, $D_2 = 0.30$, $D = 0.15$
2250	$D_1 = 0.05$, $D_2 = 0.35$, $D = 0.10$

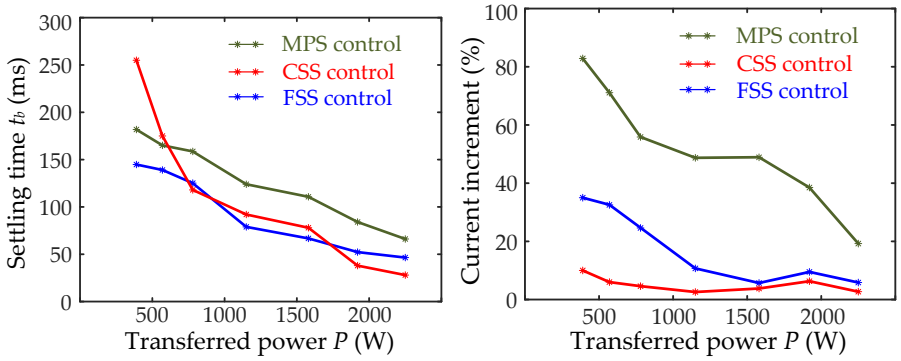
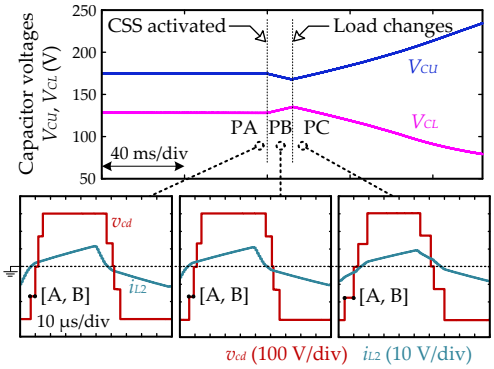


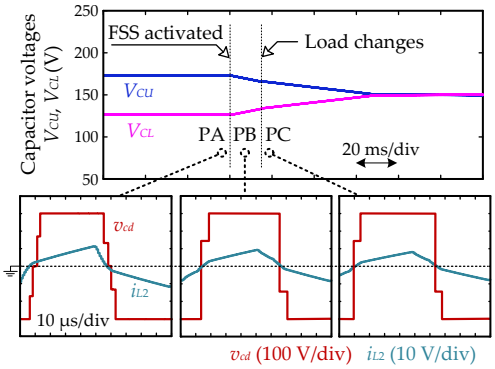
Fig. 3.15: Curves with various voltage balancing control strategies in terms of: (a) balancing time and (b) current increment at different power levels.

respect to different transferred power levels, where the corresponding control variables are shown in Table 3.6. It should be noted that the upper threshold K of the traditional MPS control scheme is set as half of the maximum value (i.e., K = 0.5D) considering the trade-off between the balancing time and current fluctuations. The current increment is expressed as $(i_{pb} - i_{ps})/i_{ps}$, where i_{pb} and i_{ps} are the peak currents in the balancing state and steady state, respectively. As shown in Fig. 3.15, the CSS method can achieve the lowest current fluctuations and relatively short settling time under various transferred power. Besides, the dynamics under the FSS method can also be improved compared to the traditional MPS method. Furthermore, the major advantage of the FSS method is the model-free feature, which can simplify the control complexity significantly.

Since the MPS and CSS methods rely on the current models, the performance of them will be affected by operating mode changes or parameter variations. For instance, Fig. 3.16 demonstrates the simulation results when the DC load (i.e., transferred power) changes. The switching states of the CSS method are determined as beneficial or adverse based on the transformer current polarity when the voltage balancing control is activated, i.e., at PA. It can be seen from the waveform of i_{L2} at PA in Fig.



(a)



(b)

Fig. 3.16: Simulation results with a step change in the DC load (i.e., the transferred power changes from 1580 W to 1200 W) after the voltage balancing is activated with V_1 = 200 V and V_2 = 300 V under: (a) CSS method and (b) FSS method. Source: **[J3]**.

3.16 (a) that the transformer current during the interval [A, B] is positive. However, after the load changes, the transformer current during [A, B] becomes negative, which can be seen from the waveforms at PC. Since the transformer current is generally not re-identified before the balancing is completed, the beneficial/adverse switching state during [A, B] will be wrongly determined, and the required neutral-point charges will be reduced, which will further result in an increased balancing time and even worsen the voltage imbalance, as shown in Fig. 3.16 (a). The MPS control scheme has similar characteristics as it is also dependent on the transformer current polarity. However, the above issue will not occur in the FSS control due to its model-free feature, which can be seen in Fig. 3.16 (b). Therefore, it is evident that the FSS method has higher robustness against operating mode changes and parameter variations.

Table 3.7: Characteristics of Different Capacitor Voltage Balancing Control Schemes.

Balancing methods	Decoupled from the current i_{L2}	Dynamics	Robustness against parameter variations	Control complexity
MPS method	✗	worst	low	difficult
CSS method	✗	best	low	medium
FSS method	✓	medium	high	easy

3.5.2 Applications of Voltage Balancing Control Strategies

The characteristics of different voltage balancing control strategies are summarized in Table 3.7. For the traditional MPS method, in addition to identification of the current polarity, the upper threshold K should also be determined based on practical tests in order to avoid high current overshoots, which may trigger the protection system and shut down the DAB converter. Thus, the practical implementation of the MPS method will be the most challenging among the three methods. The identification of the transformer current polarity is also required for the CSS method. Therefore, its implementation will be more complicated than the FSS method which does not require the knowledge of the transformer current polarity.

On the other hand, the CSS method can provide the best dynamics with the lowest current and power fluctuations as well as short settling time. Therefore, if the transformer current can be easily determined in certain applications, the CSS method should be employed. When the transferred power and DC-link voltages change in a limited range, certain operating modes can be ensured. Thus, it will be easy to determine the current polarity under certain modes. In addition, when the DAB converter operates in zero-voltage-switching (ZVS) state, according to the ZVS constraints [72]:

$$i_{L2}(\mathrm{A}) > 0, i_{L2}(\mathrm{B}) > 0, i_{L2}(\mathrm{C}) > 0, i_{L2}(\mathrm{D}) > 0 \tag{3.7}$$

it can be obtained that during the intervals [A, B] and [C, D], the transformer current will always be positive. Furthermore, in the above applications, the robustness of the CSS method can be enhanced due to the fixed operating modes or current polarity. On the other hand, if the current polarity is difficult to be determined due to the operating parameters and modes changes in a wide range, e.g., energy storage systems, the FSS method has the superiority of low control complexity and high robustness.

3.6 Summary

In this chapter, two voltage balancing control strategies were proposed to address current fluctuations and coupling with the transformer current polarity. Above all, the direction of neutral-point current under different transformer current polarity during each switching state were obtained. Accordingly, the CSS voltage balancing method was proposed to enhance the dynamics by reducing the transferred power and current fluctuations, In the CSS method, the adverse switching states will be replaced by the corresponding CSSs to regulate the direction of the charges and keep

the voltage v_{cd} unchanged. However, the CSS method and the traditional voltage balancing methods rely on the current polarity, which is challenging to obtain when the operating conditions/parameters vary in a wide range. To address this issue, FSS method was proposed, where two additional switching states were applied to obtain the required neutral-point current regardless of the transformer current polarity. Finally, experimental tests have demonstrated the performance of various voltage balancing methods. The suitable applications of different strategies has also been discussed.

Related Publications

J2. **C. Song**, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Capacitor Voltage Balancing for Multi-Level Dual-Active-Bridge DC-DC Converters" *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2566-2575, Mar. 2023.

J3. **C. Song**, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "A Model-Free Capacitor Voltage Balancing Method for Multi-Level DAB Converters" *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 79-84, Jan. 2023.

C2. **C. Song**, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Capacitor Voltage Balancing Control Scheme for 2/3-Level DAB Converters," in *Proc. IEEE IECON*, pp. 1-6, Oct. 2021.

Chapter 4

Open-Circuit-Fault Diagnosis and Fault-Tolerant Control

4.1 Background

As analyzed in Section **1.2.3**, the open-circuit-fault (OCF) issues have not been fully explored for the multi-level DAB converters. The previous OCF diagnosis methods for the two-level DAB are general impossible to identify the specific faulty switch of the multi-level DAB converters due to more complicated post-fault characteristics as many devices are used. Moreover, the fault-tolerant control schemes for the two-level DAB converter, e.g., the bypass-arm (BPA) control scheme [59, 66], can be used to suppress the OCF effects, e.g., current overshoots and DC bias. However, these methods fail to make the most of the potential of the multi-level topology (i.e., more choices of current-flow paths) to enhance the post-fault performance of the converter, e.g., increase the post-fault power-transfer range. Therefore, an OCF diagnosis method and a fault-tolerant control scheme for the 2/3-level DAB converter are proposed in this thesis **[J4]**, **[C3]**.

Since the primary-side H-bridge is identical with the two-level DAB converter, the prior-art fault diagnosis and tolerant methods in [59–62, 66] can be directly applied when a fault occurs on the primary side (i.e., S_{11}, S_{12}, S_{13}, and S_{14}). Therefore, this chapter mainly focuses on the OCF issues of the secondary-side NPC bridge. The fault diagnosis requires an accurate and fast detection. Based on the post-fault characteristics of the midpoint voltages v_{cn} and v_{dn}, the exact faulty switch can be identified by using the mean value and duty cycle after waveform transition of the midpoint voltages **[J4]**, **[C3]**. On the other hand, a complementary-switch-blocking (CSB) fault-tolerant control strategy is proposed **[J4]**, **[C3]**, where the gate pulse for the complementary switch of faulty switch will be blocked to counteract the negative effects. Thus, the current overshoots, DC bias, and other issues induced by the OCF can be effectively suppressed. At the same time, the post-fault power range can be extended compared to the traditional fault-tolerant control schemes, e.g., the BPA control scheme.

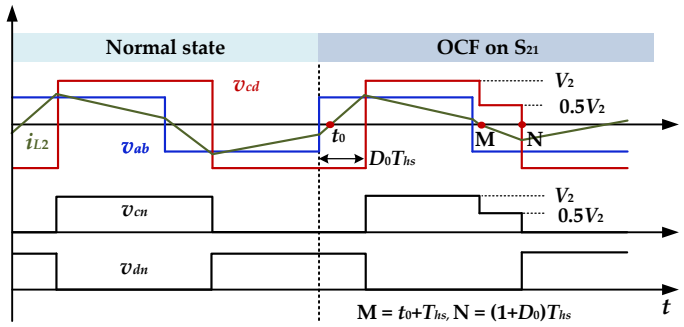


Fig. 4.1: Pre-fault and post-fault waveforms if an OCF occurs on S_{21} (see Fig. 4.2). Source: **[J4]**, **[C3]**.

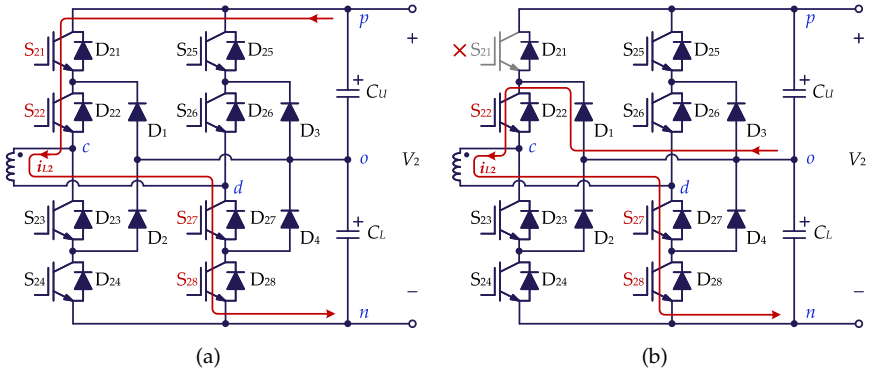


Fig. 4.2: Current-flow paths during the interval [M, N] (in Fig. 4.1) when: (a) S_{21} operates normally, and (b) an OCF occurs on S_{21}. Source: **[J4]**, **[C3]**.

4.2 Fault Diagnosis Based on Midpoint Voltages

The faulty switch is generally identified based on the post-fault waveforms of the terminal voltage v_{cd}, transformer current i_{L2}, or midpoint voltages v_{cn} and v_{dn}. These post-fault waveforms will be affected by the ranges of voltage conversion ratio and zero-crossing point of the transformer current. Furthermore, the post-fault waveforms will also be different depending on the applied control schemes, i.e., SPS and MPS control. To achieve a general fault diagnosis method, which can be employed for various control strategies and operating conditions (e.g., DC-link voltages), the post-fault waveforms should be comprehensively analyzed. To reduce the analysis complexity, the post-fault characteristics will first be analyzed based on the SPS control, and the resultant fault diagnosis method will be verified with the MPS control, e.g., five-level control, by both theoretical analysis and experimental tests.

Table 4.1: OCF Characteristics During the Faulty Interval Under the Condition of $0.5 < k \leq 1$. Source: **[J4]**.

OCF on	$i_{L2}(t_1) < 0$			$i_{L2}(t_1) \geq 0$		
	Current conduction path	v_{cd}	v_{cn} or v_{dn}	Current conduction path	v_{cd}	v_{cn} or v_{dn}
S_{21}	$D_1 \rightarrow S_{22} \rightarrow S_{27} \rightarrow S_{28}$	$0.5V_2$	$v_{cn} = 0.5V_2$	$-^*$;* $D_1 \rightarrow S_{22} \rightarrow S_{27} \rightarrow S_{28}$	nV_1; $0.5V_2$	$v_{cn} = nV_1$; $0.5V_2$
S_{22}	$D_{24} \rightarrow D_{23} \rightarrow S_{27} \rightarrow S_{28}$	0	$v_{cn} = 0$	$-$; $D_{24} \rightarrow D_{23} \rightarrow S_{27} \rightarrow S_{28}$	nV_1; 0	$v_{cn} = nV_1$; 0
S_{23}	$S_{25} \rightarrow S_{26} \rightarrow D_{22} \rightarrow D_{21}$	0	$v_{cn} = V_2$	$-$; $S_{25} \rightarrow S_{26} \rightarrow D_{22} \rightarrow D_{21}$	-nV_1; 0	$v_{cn} = V_2$-nV_1; V_2
S_{24}	$S_{25} \rightarrow S_{26} \rightarrow S_{23} \rightarrow D_2$	-$0.5V_2$	$v_{cn} = 0.5V_2$	$-$; $S_{25} \rightarrow S_{26} \rightarrow S_{23} \rightarrow D_2$	-nV_1; -$0.5V_2$	$v_{cn} = V_2$-nV_1; $0.5V_2$
S_{25}	$D_3 \rightarrow S_{26} \rightarrow S_{23} \rightarrow S_{24}$	-$0.5V_2$	$v_{dn} = 0.5V_2$	$-$; $D_3 \rightarrow S_{26} \rightarrow S_{23} \rightarrow S_{24}$	-nV_1; -$0.5V_2$	$v_{dn} = nV_1$; $0.5V_2$
S_{26}	$D_{28} \rightarrow D_{27} \rightarrow S_{23} \rightarrow S_{24}$	0	$v_{dn} = 0$	$-$; $D_{28} \rightarrow D_{27} \rightarrow S_{23} \rightarrow S_{24}$	-nV_1; 0	$v_{dn} = nV_1$; 0
S_{27}	$S_{21} \rightarrow S_{22} \rightarrow D_{26} \rightarrow D_{25}$	0	$v_{dn} = V_2$	$-$; $S_{21} \rightarrow S_{22} \rightarrow D_{26} \rightarrow D_{25}$	nV_1; 0	$v_{dn} = V_2$-nV_1; V_2
S_{28}	$S_{21} \rightarrow S_{22} \rightarrow S_{27} \rightarrow D_4$	$0.5V_2$	$v_{dn} = 0.5V_2$	$-$; $S_{21} \rightarrow S_{22} \rightarrow S_{27} \rightarrow D_4$	nV_1; $0.5V_2$	$v_{dn} = V_2$-nV_1; $0.5V_2$

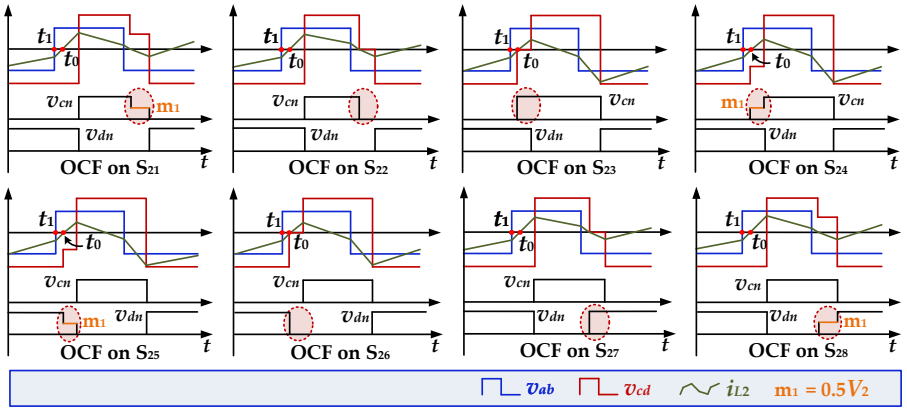
$-^*$: transformer current is 0 ;*: two different current-flow paths (i.e., voltage levels) in the faulty interval

4.2.1 Post-Fault Characteristics Analysis

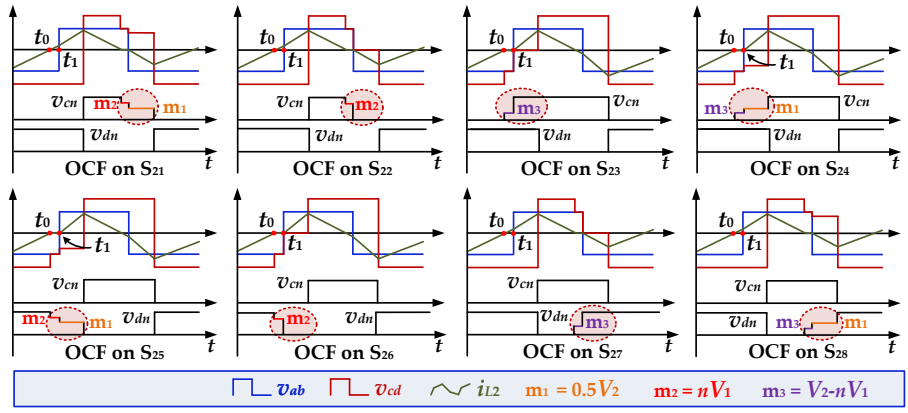
Fig. 4.1 illustrates the transient waveforms when an OCF occurs on S_{21}, where t_0 is the zero-crossing point of i_{L2}. During [M, N], if S_{21} can be turned on/off normally, the current conduction path can be as shown in Fig. 4.2 (a), and the terminal voltage v_{cd} and midpoint voltage v_{cn} will be V_2. However, if an OCF occurs on S_{21}, as shown in Fig. 4.2 (b), the current flows from the neutral point o instead of the positive port p, and thus, the terminal voltage v_{cd} and midpoint voltage v_{cn} will be $0.5V_2$. As a consequence, the waveform of the transformer current i_{L2} becomes asymmetrical, resulting in an increased DC bias and peak current, and capacitor voltage imbalance, if no fault-tolerant control is employed. On the other hand, the difference between pre-fault and post-fault waveforms can be applied to identify the faulty switch.

According to Fig. 4.1, the faulty interval starts from the zero-crossing point of the transformer current i_{L2}. Therefore, the position of t_0 (i.e., the transformer current polarity) will affect the post-fault waveforms. Fig. 4.3 illustrates the post-fault waveforms when an OCF occurs on different switches under $0.5 < k \leq 1$, where $m_1 = 0.5V_2$, $m_2 = nV_1$ and $m_3 = V_2 - nV_1$ are new voltage levels in the midpoint voltages v_{cn} and v_{dn} after the OCF occurs, and $i_{L2}(t_1)$ is the current at the rising edge of the gate pulse for S_{11}. As shown in Fig. 4.3, the post-fault voltages and transformer current are different under the conditions of $i_{L2}(t_1) < 0$ and $i_{L2}(t_1) \geq 0$. The current-flow paths during the faulty intervals are summarized in Table 4.1. In addition, for the other two conditions, i.e., $0 < k \leq 0.5$ and $k > 1$, the post-fault characteristics can be obtained in a similar way. Details are directed to **[J4]**. It should be noted that the fault diagnosis method and fault-tolerant control scheme are proposed after considering all conditions (i.e., different ranges of k and different positions of the zero-crossing point), and thus, they can be applied to various operating conditions.

Since the post-fault waveforms of the terminal voltage v_{cd} are the same when the OCF occurs on two different switches, e.g., S_{21} and S_{28}, and a similar condition applies also for the transformer current i_{L2}, it is impossible to locate the exact faulty switch if v_{cd} or i_{L2} is applied as the diagnostic signal. However, this issue can be avoided if the midpoint voltage v_{cn} or v_{dn} is used for fault diagnosis, since the post-fault midpoint



(a)



(b)

Fig. 4.3: Post-fault waveforms when the OCF occurs on different switches under $0.5 < k \leq 1$ when: (a) $i_{L2}(t_1) < 0$ and (b) $i_{L2}(t_1) \geq 0$. Source: **[J4]**.

voltages are unique when the OCF occurs on each switch. Therefore, a fault diagnosis control scheme is developed by using the post-fault midpoint voltages.

4.2.2 Fault Diagnosis

The fault diagnosis control based on the midpoint voltages is shown in Fig. 4.4, which can be divided into three steps as follows:

- *Step 1:* The mean value of the midpoint voltages v_{cn} and v_{dn} is $0.5V_2$ during normal state in ideal conditions. When an OCF occurs, the mean values of the midpoint voltages will change. If the error exceeds the threshold α, the fault diagnosis control will be enabled. It should be noted that the threshold

α is related to various non-ideal factors, e.g., dead-time, measurement errors, switching noise, and parasitics. It is challenging to calculate these non-ideal factors separately. Instead, it is more effective and realistic to determine the threshold α by measuring the total errors in practice since the above factors rely highly on the surrounding conditions and circuit design. α = 4 V is determined by experimental tests in the prototype after considering the sensitivity and reliability of the fault diagnosis.

- *Step 2:* If $\overline{v}_{cn} < 0.5V_2 - \alpha$, the possible faulty switch can be either S_{21} or S_{22}, where $\overline{v}_{cn}$ is the average midpoint voltage. Otherwise, either S_{23} or S_{24} is the possible faulty switch. However, the fault on the two possible switches cannot be differentiated by using the average midpoint voltages. Similar condition is also applied in the second-arm switches (i.e., S_{25}, S_{26}, S_{27}, and S_{28}), when using the average midpoint voltage $\overline{v}_{dn}$. Therefore, waveform transition, i.e., Step 3, is applied.
- *Step 3:* The exact faulty switch can be identified by waveform transition as shown in Fig. 4.4. After the waveform transition, the waveform of the midpoint voltage v_{cn} or v_{dn} can be converted to square waveforms with different duty cycles (i.e., v_{0c} and v_{0d}), and the faulty switch can then be located. The threshold β is applied during the identification of the duty cycle of the converted voltage v_{0c} after the waveform transition, which is also affected by the noise in normal state. After experimental tests, $\beta = 0.015$ is designed.

4.3 Fault-Tolerant Control

To suppress the current overshoots and DC bias caused by OCFs, the fault-tolerant method should be applied when the fault diagnosis system locates the faulty switch. The bypass-arm (BPA) method is a popular fault-tolerant method for the two-level DAB. If it is used in the multi-level DAB converter, when a switch is diagnosed as the faulty one (e.g., S_{21}), the other three switches in the same bridge arm (i.e., S_{22}, S_{23}, and S_{24}) should be blocked to achieve safe operation for the converter. However, this method fails to make the most of the increased number of switches (i.e., current-flow paths) to further improve the post-fault performance, e.g., increase the power-transfer capability of the converter. Therefore, a CSB control method is proposed **[J4]**, **[C3]**.

4.3.1 CSB Fault-Tolerant Method

According to the analysis of the post-fault waveforms, the negative OCF effects are induced by the asymmetrical post-fault voltage v_{cd}. Thus, if this voltage waveform can be kept symmetrical after employing the fault-tolerant method, the DC bias, current overshoots, and capacitor voltage imbalance can be suppressed. For example, when an OCF occurs on S_{21}, the faulty interval occurs during $[t_0 + T_{hs}, (1 + D_0)T_{hs}]$, where the voltage v_{cd} decreases from V_2 to $0.5V_2$, as shown in Fig. 4.5. If a complementary interval is applied during $[t_0, D_0T_{hs}]$, where the voltage v_{cd} can decrease from $-V_2$ to $-0.5V_2$, the post-fault waveforms will remain symmetrical, and the impact caused by the faulty switch S_{21} can be counteracted, which can be seen in Fig. 4.5.

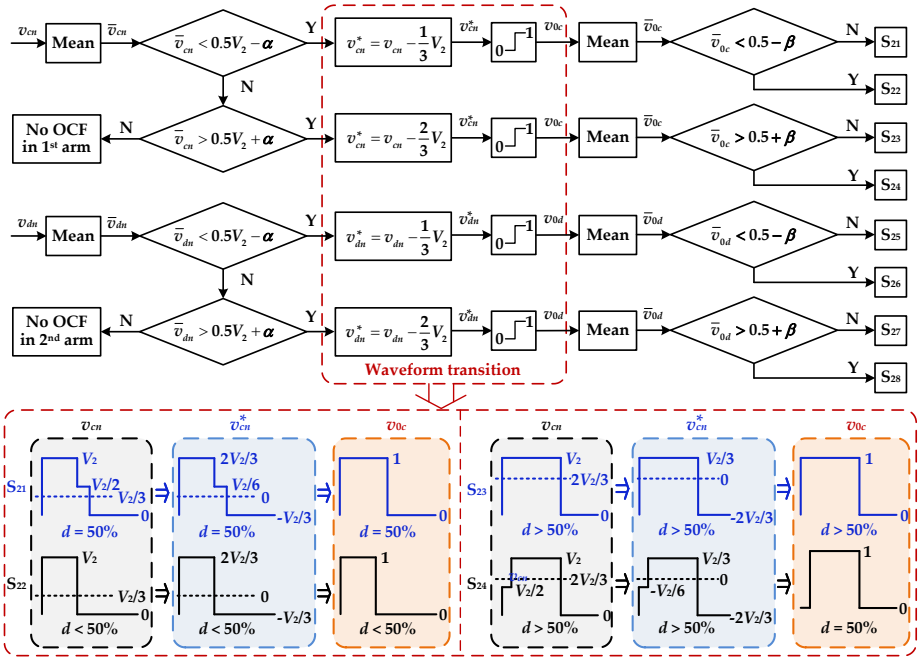


Fig. 4.4: Control structure of the proposed fault diagnosis method. Source: **[J4]**, **[C3]**.

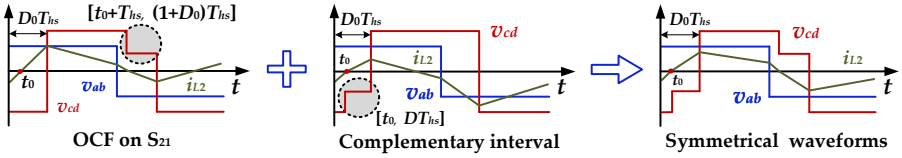


Fig. 4.5: Process for the proposed CSB fault-tolerant control scheme. Source: **[J4]**.

As shown in Fig. 4.3, when an OCF occurs on S_{24} or S_{25}, the faulty interval is the same as the complementary interval in Fig. 4.5. Thus, if S_{21} is diagnosed as the faulty switch, the negative effects can be suppressed by blocking the gate pulse of S_{24} or S_{25}. However, during the faulty interval for S_{21}, it can be seen from Fig. 4.2 (b) that the current is drawn from the neutral point. In order to avoid capacitor voltage imbalance, the current should be injected into the neutral point during the complementary interval. Fig. 4.6 shows the current-flow paths during the faulty intervals when an OCF occurs on S_{24} and S_{25}, where it can be seen that the required neutral-point current can be obtained during the faulty interval for S_{24} instead of S_{25}. Thus, S_{24} is the complementary switch of S_{21}. This means when an OCF occurs on S_{21}, the gate pulse of S_{24} should be blocked. With a similar analysis, the complementary-switch pairs can be identified as: S_{21} and S_{24}, S_{22} and S_{23}, S_{25} and S_{28}, S_{26} and S_{27}.

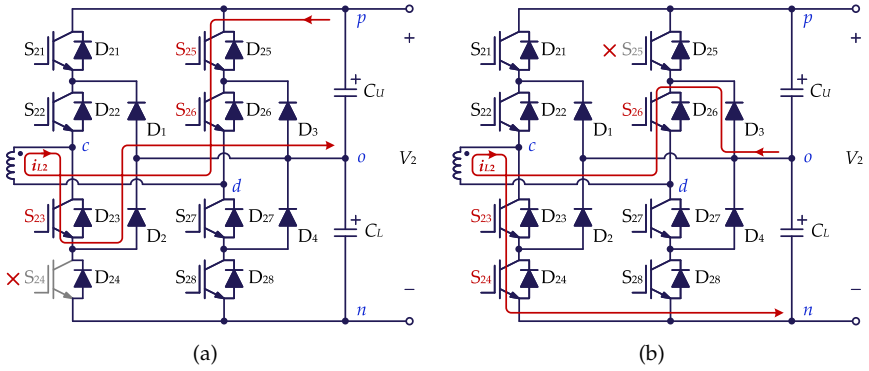


Fig. 4.6: Current-flow paths during the faulty intervals when the OCF occurs on: (a) S_{24} and (b) S_{25}.

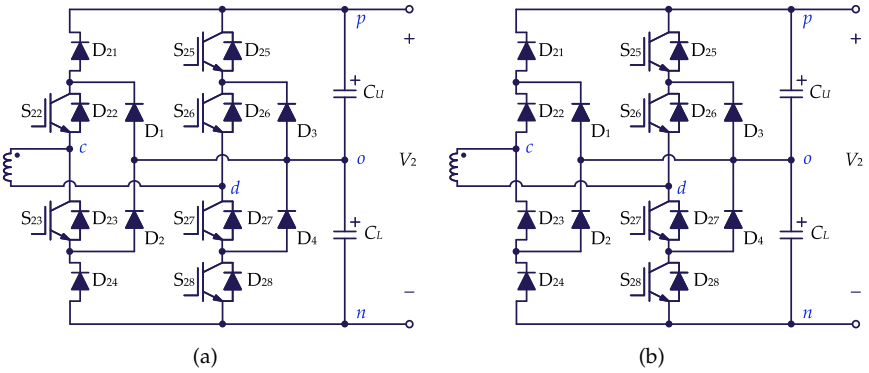


Fig. 4.7: Equivalent circuits with the CSB method when the OCF occurs on: (a) S_{21} and (b) S_{22}. Source: **[J4]**.

4.3.2 Post-Fault Power-Transfer Capability

With the above analysis, when an OCF occurs on an outer switch (e.g., S_{21}) or an inner switch (e.g., S_{22}), the equivalent circuits after applying the CSB method can be shown in Fig. 4.7. It should be noted that if an OCF occurs on an inner switch, after blocking its complementary switch, the current cannot flow through any switch in the faulty bridge arm (except the anti-parallel diodes). Thus, in the equivalent circuit, i.e., Fig. 4.7 (b), all the four switches in the faulty bridge arm are blocked.

When an outer switch is diagnosed as the faulty one, the post-fault waveforms after applying the CSB method are shown in Fig. 4.8. According to the expressions of the transformer current and transferred power, i.e., (2.3) and (2.2), the normalized transferred power P_0 and the corresponding power range of each mode can be obtained, as shown in Table 4.2, where it can be seen that the power ranges are seamless between

Table 4.2: Expressions of t_0, P_0, and the Ranges of D and P_0 for Mode C1 to C6. Source: **[J4]**.

Range of k	Modes	Expression of t_0	Expression of P_0	Range of P_0
$0.5 < k \leq 1$	C1	$\frac{2(k-1)+3D_0}{4k+3}$	$-t_0^2 - 2(2k+1)t_0 - 3D_0^2 + 6D_0 + 2(k-1)$	$\frac{2(-2k^2+k+1)}{3} < P_0 \leq 0.5\frac{16k^2+24k+5}{(4k+3)^2}$
	C2	$\frac{3D_0}{2(1-k)}$	$2(k-1)t_0^2 + 6D_0t_0 - 3D_0^2$	$0 \leq P_0 \leq \frac{2(-2k^2+k+1)}{3}$
$0 < k \leq 0.5$	C3	$\frac{2(k-1)+3D_0}{4k+3}$	$-t_0^2 - 2(2k+1)t_0 - 3D_0^2 + 6D_0 + 2(k-1)$	$0 < k \leq 0.25 : \varnothing^*$ $0.25 < k \leq 0.5 :$ $\frac{2(-2k^2+k+1)}{3} < P_0 \leq \frac{16k^2+24k+5}{(4k+3)^2}$
	C4	$\frac{2k-1-3D_0}{4k-3}$	$(8k-5)t_0^2 + 6D_0t_0 + 4(1-2k)t_0 - 3D_0^2 + 2k - 1$	$0 < k \leq 0.25 :$ $0 \leq P_0 \leq \frac{16k^2-24k+11}{2(4k-3)^2}$ $0.25 < k \leq 0.5 :$ $0 \leq P_0 \leq \frac{2(-2k^2+k+1)}{3}$
$k > 1$	C5	$\frac{2(k-1)+3D_0}{4k+3}$	$-t_0^2 - 2(2k+1)t_0 - 3D_0^2 + 6D_0 + 2(k-1)$	$\frac{k^2-1}{k^2} < P_0 \leq \frac{16k^2+24k+5}{(4k+3)^2}$
	C6	$\frac{2(k-1)-3D_0}{4k-3}$	$(8k-7)t_0^2 + 6D_0t_0 - 8(k-1)t_0 - 3D_0^2 + 2(k-1)$	$0 \leq P_0 \leq \frac{k^2-1}{k^2}$

*$\varnothing$: no power range under certain operating constraints

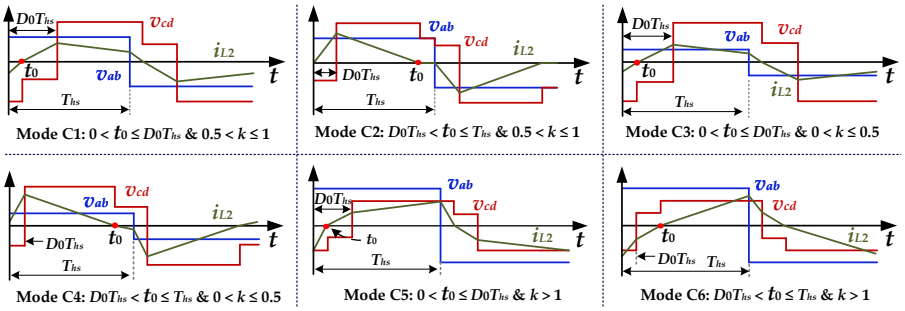


Fig. 4.8: Steady-state waveforms after applying the proposed CSB method when the OCF occurs on an outer switch under various operating conditions. Source: **[J4]**.

the two modes for a certain range of k. Thus, the power ranges under various voltage conversion ratios can be obtained as

$$\begin{cases} 0 < k \leq 0.25 : 0 \leq P_0 \leq \dfrac{16k^2 - 24k + 11}{2(4k-3)^2} \\ k > 0.25 : 0 \leq P_0 \leq \dfrac{16k^2 + 24k + 5}{(4k+3)^2} \end{cases} \tag{4.1}$$

On the other hand, when an OCF occurs on an inner switch, the steady-state waveforms with the CSB method are illustrated in Fig. 4.9. Similarly, the power ranges

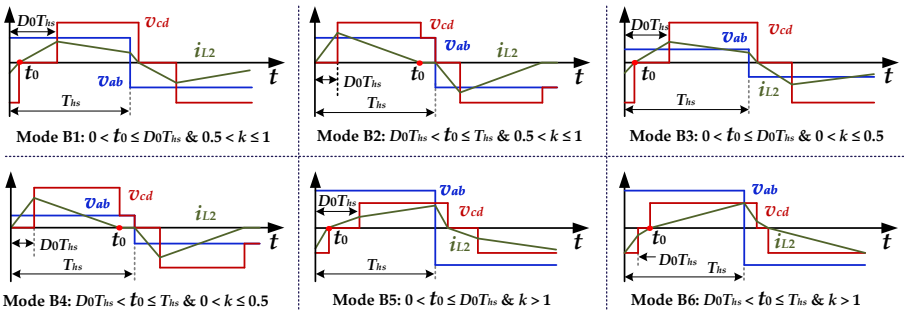


Fig. 4.9: Steady-state waveforms after applying the proposed CSB method when the OCF occurs on an inner switch under various operating conditions. Source: **[J4]**.

under various voltage conversion ratios can be obtained as

$$\begin{cases} 0 < k \leq 0.5 : 0 \leq P_0 \leq \dfrac{k}{2(1-k)} \\ k > 0.5 : 0 \leq P_0 \leq \dfrac{4k^2+4k-1}{(2k+1)^2} \end{cases} \tag{4.2}$$

For the traditional BPA method, when an OCF occurs on a switch (regardless of outer or inner switch), the other three switches in the same bridge arm will be blocked. Thus, the post-fault equivalent circuit and waveforms, and also the power range will be the same as those when the OCF occurs on an inner switch with the proposed CSB method, i.e., Figs. 4.7 (b) and 4.9. However, when an OCF occurs on the outer switch, the power-transfer capability with the two fault-tolerant control schemes will be different. Fig. 4.10 shows comparative curves of the post-fault transferred power with the BPA and CSB methods, where it can be seen that the upper boundary of the transferred power can be increased by applying the proposed CSB method compared to the BPA method, especially when the voltage conversion ratio k is much smaller than unity. If the transferred power is P_1 in normal state, and then an OCF occurs on an outer switch, the transferred power will be decreased to P_2 with the traditional BPA method. On the other hand, the transferred power will be maintained unchanged with the proposed CSB method as $P_1 < P_3$.

4.4 Fault Diagnosis and Tolerant in MPS Control

Although the above fault diagnosis and tolerant methods are analyzed based on SPS control, they can also be employed to the MPS control schemes including EPS, TPS and five-level control schemes. The five-level control scheme is taken as an example to analyze the effectiveness of the proposed methods.

Fig. 4.11 shows the transient waveforms when an OCF occurs in the first bridge arm under the five-level control. The midpoint voltage v_{cn} has similar characteristics with those of the SPS control scheme, as shown in Fig. 4.11, i.e., 1) the average

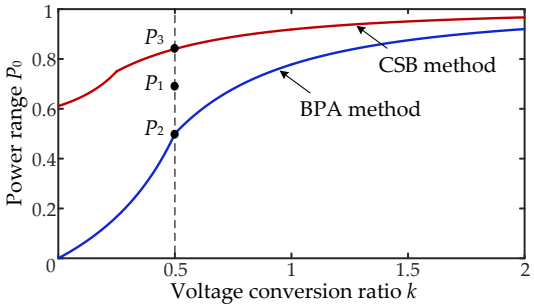


Fig. 4.10: Maximum transferred power in the fault-tolerant operation by employing the BPA and CSB methods when an OCF occurs on an outer switch. Source: **[J4]**.

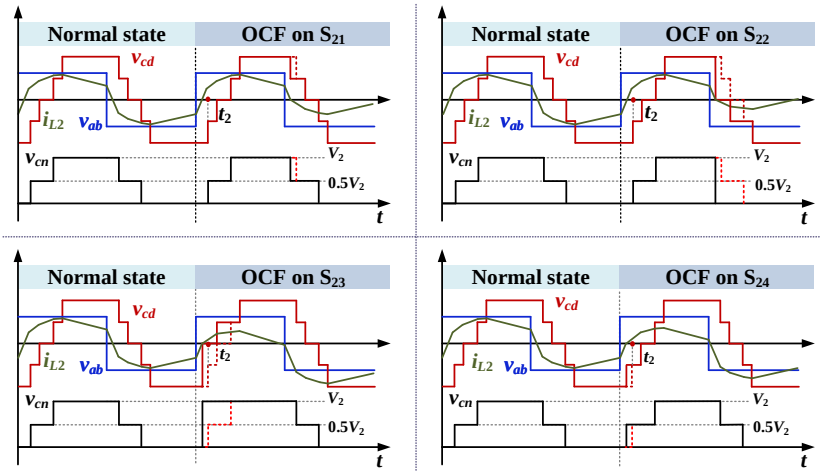


Fig. 4.11: Post-fault waveforms with the five-level control scheme under the condition $0.5 < k \leq 1$ and $i_L(t_2) \geq 0$. Source: **[J4]**.

midpoint voltage is $0.5V_2$ in normal state, and 2) the average midpoint voltage is less than $0.5V_2$ when an OCF occurs on S_{21} or S_{22}, and larger than $0.5V_2$ when an OCF occurs on S_{23} or S_{24}. Thus, the constraints of the former two steps in Section **4.2.2** can be satisfied. As for Step 3, Fig. 4.12 illustrates the waveform transition process for the post-fault midpoint voltage under the five-level control, where it can be seen that after the waveform transition, the two possible faulty switches (e.g., S_{21} and S_{22}) can be differentiated by the duty cycle of the converted voltage v_{0c}. Therefore, the proposed fault diagnosis method can also work under the five-level control.

As for the fault-tolerant control strategy, the complementary switch pairs are also satisfied under the MPS control, e.g., S_{21} and S_{24}, S_{22} and S_{23}, as shown in Fig. 4.11. Fig. 4.13 illustrates the proposed fault-tolerant method with the five-level control scheme when an OCF occurs on S_{22}, where it can be seen that by blocking its complementary switch S_{23}, the post-fault waveforms will remain symmetrical, and thus, the negative

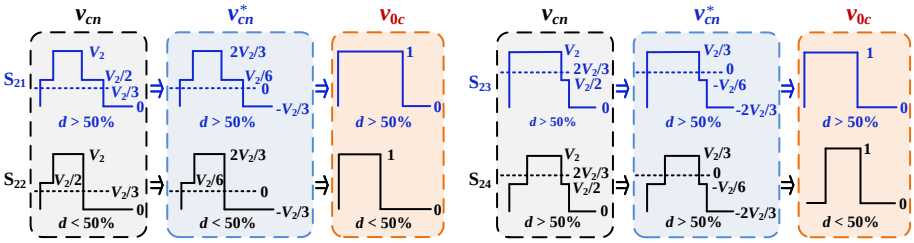


Fig. 4.12: Waveform transition with the five-level control scheme. Source: **[J4]**.

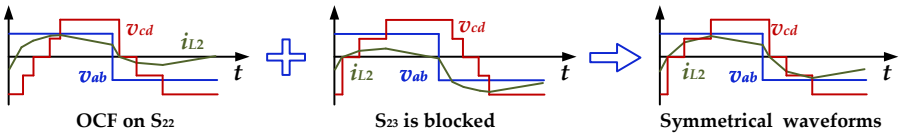


Fig. 4.13: Waveforms when the OCF occurs on S_{22} by using the proposed CSB method with the five-level control. Source: **[J4]**.

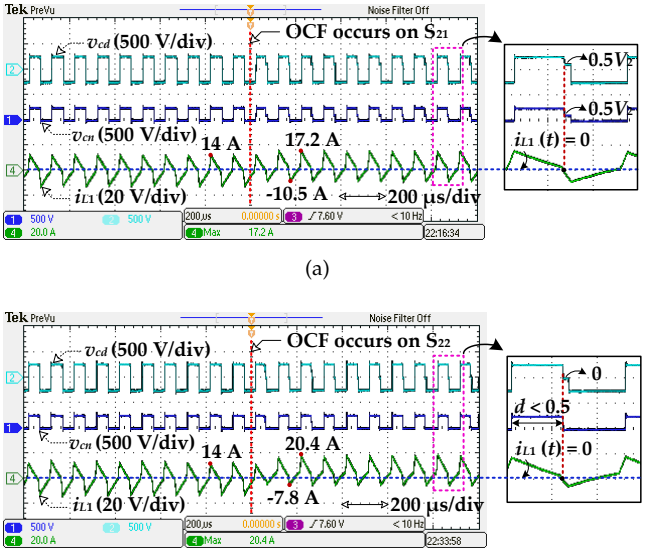
OCF effects like current overshoots can be decreased, and the DAB converter can operate in safe condition. In summary, the proposed fault diagnosis and tolerant control schemes can be applied to both SPS and MPS control schemes.

4.5 Experimental Validation

Fig. 4.14 shows some experimental results when an OCF occurs on S_{21} and S_{22}, where it can be seen that the post-fault waveforms of the transformer current and the voltages are distorted. A positive DC bias appears in i_{L2}, and thus, the peak current increases significantly. In addition, as shown in Fig. 4.14, the current overshoots and DC bias will be more significant when the OCF occurs on the inner switches, e.g., S_{22}, compared to the outer switches. To avoid these negative effects, fault diagnosis and fault-tolerant methods should be employed.

To locate the faulty switch, the fault diagnostic signals, i.e., the midpoint voltages v_{cn} and v_{dn}, are sampled and then the diagnosis control is carried out in the dSPACE MicroLabBox. Fig. 4.15 illustrates the experimental results of the proposed fault diagnosis method, where FD is used to differentiate various faulty switches, i.e., FD = 1, 2, 3, or 4 denotes the OCF conditions on S_{21}, S_{22}, S_{23}, or S_{24}, respectively. Compared to the traditional fault diagnosis method, as shown in Fig. 1.7 in Section **1.2.3**, the exact faulty switch can be located with the proposed fault diagnosis method, and the diagnostic period is around one switching cycle.

After the fault switch is identified, the proposed fault-tolerant control scheme is enabled. As shown in Fig. 4.16, the post-fault waveforms can remain symmetrical with the proposed CSB method, and thus, the current overshoots and DC bias can be decreased significantly compared to that in Fig. 4.14. In addition, the two capacitor voltages are kept balanced.



(a)

(b)

Fig. 4.14: Experimental waveforms of the 2/3-level DAB under the condition V_1 = 100 V, V_2 = 250 V, and P = 550 W when an OCF occurs on: (a) S_{21}, and (b) S_{22}. Source: **[J4]**.

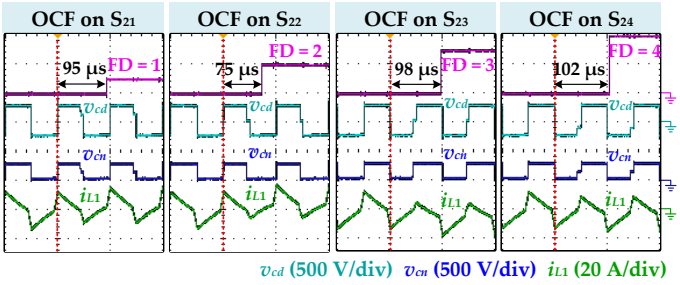
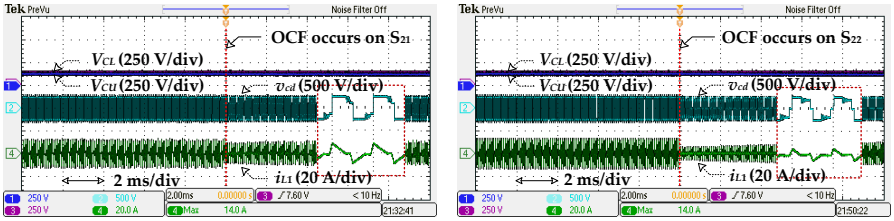


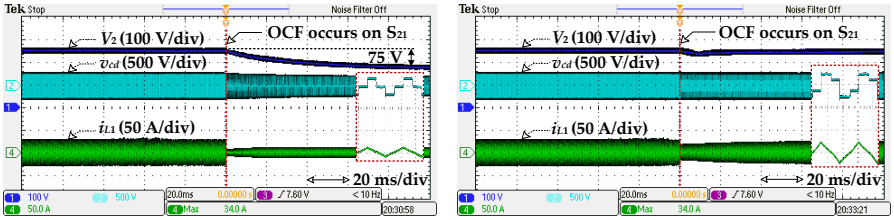
Fig. 4.15: Experimental waveforms with the proposed fault diagnosis method when the OCF occurs on different switches. Source: **[J4]**.

The post-fault power-transfer capability with different fault-tolerant methods can be verified by the experimental results in Figs. 4.17 and 4.18. Fig. 4.17 gives the experimental waveforms with the BPA and proposed CSB methods after an OCF occurs on S_{21}. As shown in Fig. 4.17 (a), the output voltage reduces from 250 V to 175 V, i.e., the power reduces from 400 W to 196 W, after the traditional BPA scheme is applied. Since the experiments are carried out in a closed-loop control system, the output voltage/transferred power cannot be kept unchanged even when the phase-shift ratio reaches the maximum value. However, the output voltage can be maintained constant at the reference value with the CSB method, which can be seen in Fig. 4.17 (b). That means the power-transfer range is expanded compared to the traditional



(a) (b)

Fig. 4.16: Experimental waveforms by applying the CSB scheme under the condition V_1 = 100 V, V_2 = 250 V, and P = 550 W when the OCF occurs on: (a) S_{21}, and (b) S_{22}. Source: **[J4]**.



(a) (b)

Fig. 4.17: Experimental waveforms when the OCF occurs on S_{21} under the condition V_1 = 50 V, V_{2ref} = 250 V, and R = 156 Ω after employing: (a) BPA scheme, and (b) CSB scheme. Source: **[J4]**.

BPA method. Furthermore, Fig. 4.18 shows the comparative results of the maximum transferred power (i.e., D = 0.5) among the pre-fault state and post-fault state with the two methods. The input voltage varies from 50 V to 170 V, and the reference output voltage is 250 V (i.e., k varies from 0.4 to 1.36). As shown in Fig. 4.18, the maximum post-fault transferred power is decreased for both the BPA and CSB methods compared to that in normal state. However, the post-fault power-transfer capability is enhanced by using the CSB method with various voltage conversion ratios.

Fig. 4.19 shows the experimental waveforms of the proposed fault-tolerant control scheme under the five-level control with V_1 = 100 V, V_{2ref} = 250 V, and R = 78 Ω. In order to show the OCF effects (e.g., current overshoots and DC bias), the CSB control scheme is enabled 2 ms later after the OCF occurs. As shown in Fig. 4.19, transformer current and the voltages remain symmetrical, and thus, current overshoots and DC bias can be suppressed after applying the proposed fault-tolerant method, which validates the effectiveness of the proposed CSB method under the MPS control schemes.

4.6 Summary

In this chapter, a fault diagnosis method and a fault-tolerant control scheme have been proposed for the NPC-based DAB converter. The fault diagnosis was designed

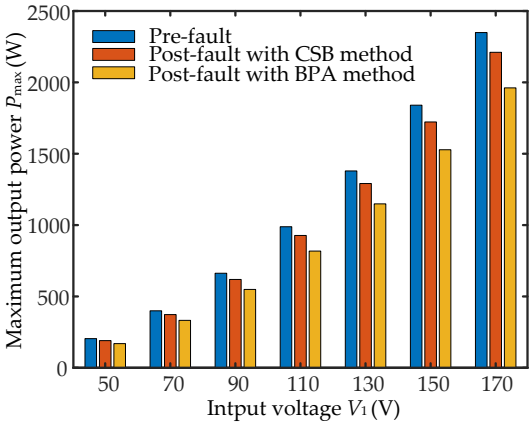


Fig. 4.18: Power-transfer capability comparison between the BPA scheme and CSB scheme with different input voltages. Source: **[J4]**.

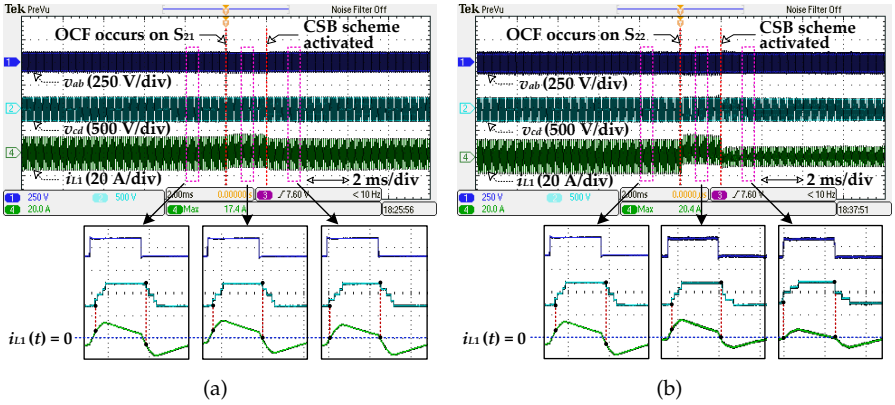


Fig. 4.19: Experimental waveforms by applying the CSB scheme in the five-level control with $D_1 = 0$, $D_2 = 0.15$, $D_0 = 0.1$, and $D = 0.15$ when the OCF occurs on: (a) S_{21}, and (b) S_{22}. Source: **[J4]**.

based on the post-fault midpoint voltages, which can be applied to various conditions, e.g., different voltage conversion ratios and operating power ranges. Subsequently, the fault-tolerant control scheme based on the complementary switch pairs was proposed. When an OCF occurs on a switch, its complementary switch will be blocked to mitigate the current overshoots and DC bias. Moreover, the post-fault power-transfer capability can be improved with the proposed fault-tolerant method. The proposed fault diagnosis and tolerant methods are generic for various control schemes including SPS control and MPS control.

Related Publications

J4. **C. Song**, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Open-Circuit Fault Diagnosis and Tolerant Control for 2/3-Level DAB Converters" *IEEE Trans. Power Electron.*, 2022. Status: revision in review.

C3. **C. Song**, Y. Yang, A. Sangwongwanich, and F. Blaabjerg, "Open-Circuit Fault Analysis and Fault-Tolerant Control for 2/3-Level DAB Converters," in *Proc. IEEE ECCE-Asia*, pp. 696-701, May. 2021.

Chapter 5

Conclusions

This chapter summarizes the research results for the project - *Efficient and Reliable Control of Multi-Level Dual-Active-Bridge Converters*. The main contributions and future research perspectives of this project are also discussed in the following.

5.1 Summary

The main focus of this project is to improve the efficiency and reliability of the multi-level DAB converters in terms of control strategies. The challenges and limitations of the conventional methods with respect to achieving the efficient and reliable control for the multi-level DAB converters have been discussed. Subsequently, the optimal control strategies for addressing these challenges have been proposed. A summary for each chapter is shown as follows:

In *Chapter 1*, the state-of-the-art for the MVDC networks and the corresponding DC-DC converters, which provide higher voltage-blocking capability have been reviewed. After comparing the characteristics of different MV-network DC-DC converters, this Ph.D. project focuses on the 2/3-level DAB converter topology, since it is a promising solution for the applications which require galvanic isolation, high step-up ratios and power density, and/or bi-directional power flow capability, e.g., energy storage or auxiliary power supply systems in large-scale PV plants. Afterwards, the prior-art research of the control strategies for improving the efficiency and reliability (with respect to capacitor voltage balancing and OCF-tolerant) has been reviewed. Since the efficient and reliable control strategies for the multi-level DAB converter have not be explored comprehensively, three research objectives of this Ph.D. project are outlined: 1) generic optimal control strategy to enhance the efficiency under various operating conditions/parameters, 2) capacitor voltage balancing control strategies for improving dynamics and reducing implementation complexity, and 3) generic and accurate fault diagnosis method and fault-tolerant control with improved post-fault performance.

In *Chapter 2*, a generic optimal control strategy for minimizing the current stress and thus improving the efficiency has been proposed. Transferred power model was first developed based on an equivalent-wave method to reduce the modeling

complexity. Subsequently, according to the obtained peak current and transferred power models, and defined operating constraints, the modulation for minimizing peak current was developed. Obtaining the analytical solutions is a critical issue for achieving online modification of the control variables when the operating parameters vary in a wide range. In this chapter, the analytical solutions were obtained by combining the numerical-solution analysis and the KKT conditions. Moreover, on the basis of the obtained analytical solutions, a closed-loop control system was developed to simplify the control structure.

In *Chapter 3*, two capacitor voltage balancing control strategies have been proposed to suppress the negative effects caused by unbalanced neutral-point voltages, and thus, enhancing the reliability of the DAB converter. To ensure a smooth transition when the voltage balancing is activated and avoid system shut-down due to the high overshoot current, the CSS method was proposed, where the adverse switching states are replaced by their CSSs to increase the required charges to the neutral point and at the same time maintain the voltage waveform unchanged. By doing so, the voltage imbalance will be eliminated without introducing power and current fluctuations. However, as the CSS method is highly dependent on the transformer current polarity, it is suitably applied to the conditions where the operating parameters vary in a limited range, since the transformer current polarity can easily be determined under such conditions. Otherwise, the model-free FSS method with two additional switching states can be applied to obtain the required neutral-point current without being affected by the transformer current model.

Finally, in *Chapter 4*, the fault diagnosis and tolerant methods have been proposed to suppress the negative effects like current overshoots, and thus ensure safe operation of the post-fault DAB converter. After analyzing the post-fault characteristics under various operating conditions, i.e., different transferred power and voltage conversion ratios, the OCF diagnosis method was developed based on the midpoint voltages. Afterwards, the fault-tolerant control scheme based on CSB method was proposed, where the complementary switch is blocked to counteract the effect caused by the faulty switch with symmetrical post-fault waveforms. Compared to the traditional fault-tolerant control, the power-transfer capability of the post-fault converter can be enhanced. Furthermore, the proposed methods can be used in both SPS and MPS control schemes.

5.2 Main Contributions

The main contributions of this Ph.D. project are summarized as follows:
A) Generic Optimal Control Strategy for Improving Efficiency

- Due to the increased number of the control variables in the multi-level DAB converters, it is challenging to obtain analytical solutions by using the traditional optimization methods. In this thesis, an optimization method by combining the numerical-solution analysis and the KKT conditions was employed to obtain the analytical solutions;
- A generic minimum-current-stress control strategy was proposed by using the obtained analytical solutions, where the control variables can be modified online

during the operating conditions/parameters change. This cannot be achieved in the previous control strategies based on the numerical solutions, where the control parameters should be pre-calculated.

B) Capacitor Voltage Balancing Control Strategies

- A CSS method was proposed to achieve smooth dynamics during the voltage balancing, which can be applied to the conditions where the transformer current can be easily identified;
- Another FSS method was proposed for the applications where the operating parameters vary in a wide range, and the determination of the current polarity is difficult to achieve, since the neutral-point charges can be independent of the transformer current polarity.

C) OCF Diagnosis and Tolerant Control Methods

- The post-fault characteristics of the DAB converter under various transferred power and voltage conversion ratios were comprehensively analyzed, which provided the necessary basis for fault diagnosis;
- The state-of-the-art fault diagnosis methods cannot locate the exact faulty switch when being used in the 2/3-level DAB. Hence, a fault diagnosis method based on the mean value and duty cycle of the midpoint voltages was developed, which can be applied to various operating conditions and different control strategies;
- To enhance the post-fault performance in terms of power-transfer capability, a fault-tolerant control based on the CSB method was proposed. The proposed fault-tolerant method can be flexibly employed to different control strategies.

5.3 Research Perspectives

This Ph.D. project has developed solutions for the control-related issues of the 2/3-level DAB converter including current stress minimization, voltage balancing, and OCF diagnosis and tolerant control. However, many challenging issues remain:

- For the DAB converters, two control objectives are generally considered for improving the efficiency, i.e., current-related indices (e.g., peak or RMS current) and soft-switching. The former one strongly influences the conducting losses, while the latter one can be applied to decrease switching losses. For traditional two-level DAB, due to limited number of control variables, both aspects were considered for certain modulation strategies. However, with the increased DoFs, it becomes challenging to obtain the analytical solutions for the multi-level DAB converters even though only one optimization objective (e.g., peak current) is applied. It is evident that analytical solutions will be more difficult to be derived when the soft-switching is also considered in the optimization. A trade-off between efficiency and implementation complexity is made in the proposed minimum-current-stress control strategy in Chapter 2. However, the optimal method to obtain the analytical solutions when both the current-related indices and soft-switching are considered is worth being explored to further improve the efficiency.

- This project explored several control strategies for single DAB converter, which are generic for various applications, e.g., voltage balancing control. However, in the actual systems, a coordinated control among different converters should also be taken into account. For instance, if the DAB converter is applied to energy storage systems, e.g., in Fig. 1.1, the DAB converter should be coordinatively controlled together with other power converters (e.g., the DC-DC converter connecting the PV array and MVDC bus) to realize power dispatching and support the DC-link voltages.
- Single three-level DAB converter can be employed to the applications with the voltage rating of several kVs. When the DC-link voltage is higher, e.g., tens of kVs, achieving MV connection will be difficult for a single multi-level topology as the voltage-blocking capability of the semiconductors is limited. In that case, cascaded converters with the module of three-level DAB converter can be employed, and thus, the issues for series-connected converter, e.g., voltage and power distribution should be explored. It should be noted that the control complexity for the cascaded converters will be generally increased along with the amount of the modules. Thus, by employing the multi-level topology as the module, the modulation of the cascaded converters can be simplified compared to the two-level topology.
- Reliability-oriented control strategies have been proposed in this thesis, including capacitor voltage balancing control and fault-tolerant control, to avoid high voltage and current stress as well as DC bias. However, other reliability issues, such as thermal distribution for the inner and outer switches of the NPC bridge, and lifetime estimation of the components, have not been analyzed for the DAB converter.

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