Series-Connection of Medium Voltage SIC Mosefets with Self-Powered Design

Wang, Rui

DOI (link to publication from Publisher):
10.54337/aau543669441

Publication date:
2023

Document Version
Publisher's PDF, also known as Version of record

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BY
RUI WANG

DISSERTATION SUBMITTED 2023

AALBORG UNIVERSITY
DENMARK

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Dissertation submitted

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Dissertation submitted: May 2, 2023

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PhD Series: Faculty of Engineering and Science, Aalborg University

Department: AAU Energy

ISSN (online): 2446-1636
ISBN (online): 978-87-7573-713-0

Published by:
Aalborg University Press
Kroghstræde 3
DK – 9220 Aalborg Ø
Phone: +45 99407140
aauf@forlag.aau.dk
forlag.aau.dk

Printed in Denmark by Stibo Complete, 2023

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Rui Wang's research interests involve wide bandgap power semiconductor devices, active gate drivers and series-connection technology for these devices, as well as corresponding medium-voltage converter design.

ABSTRACT

Medium-voltage (MV) high-power power electronics technology, which contributes to less copper cost and loss, becomes significantly promising as the power demand of society increases continuously. Owing to rapid advancement of power semiconductor devices featuring wide bandgap material, the emerging MV silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) rated from 3.3 kV to 15 kV can exceptionally simplify the structure and decrease the control complexity level of MV high-power converters. Besides this, it facilitates high frequency, high efficiency, and high-temperature operation. Nevertheless, there still exist some hardware design challenges which hinder this evolution.

To enhance the effectiveness by using MV SiC devices to replace the dominance of silicon (Si) insulated gate bipolar transistors (IGBTs) in MV converter applications, this thesis initially presents the importance and necessity of researching gate driver (GD) design considering the prominent fast-switching characteristic of SiC device. Then it is clarified that, common mode noise and isolation burden are two significant issues encountered in the GD design. Furthermore, series-connection is researched in this thesis, which is categorized into two groups named as direct and indirect series-connections based on intended synchronous and asynchronous switching operations. Maintaining the advantage of fast switching of SiC devices also brings on a significant challenge for the voltage balancing (VB) design of direct series-connection.

On the above basis, for some indirect series-connections of power devices using modular design with large submodule capacitor, targeting the self-powered auxiliary power supply (APS) for powering GDs, etc., a single gate-driven SiC MOSFET stack is suggested to construct it with a flyback topology, where simplified structure and easier control are the prominent advantages. Further, a thorough analysis of the single gate-driven MOSFET stack's short-circuit characteristics is conducted and a hardware improvement is proposed to reinforce its resistance against the short-circuit in the presence of both hard switch fault and fault under load.

For direct series-connection and some other indirect series-connections without large submodule capacitors, a converter-based self-powered GD is suggested for MV SiC device, which integrates the device and GD into a single unit and makes it scalable to series-connection. Most importantly, it eliminates the common mode path from the GD to the ground and reduces the isolation burden from the total bus voltage to the unit voltage. By conducting experiments, the effectiveness of this self-powered GD has been verified in the cases of DC to DC and DC to AC conversions. On this basis, an adaptive impedance optimization for this self-powered GD is proposed to achieve a better tradeoff between snubber loss and VB performance of series-connected SiC MOSFETs in static and dynamic conditions. Finally, in conjunction with an active delay control strategy, the achieved dynamic VB performance is further enhanced.

Keywords: medium voltage, SiC MOSFET, auxiliary power supply, gate driver, series-connection, voltage balancing, short-circuit fault, self-powered, common-mode noise.

DANSK RESUME

Teknologien for mellemspænding (MV) effektelektronik, som bidrager til lavere kobberomkostninger og tab, bliver stadig mere betydningsfuld, som samfundets behov for energi fortsætter med at stige. På grund af den hurtige udvikling af nye halvledermaterialer i dag, kan nye MV siliciumcarbid (SiC) metal-oxid-halvleder-felteffekttransistor (MOSFET) med en blokeringsspænding fra 3,3 kV til 15 kV i høj grad forenkle strukturen og reducere styringskompleksiteten af MV effektelektronik-konvertere. De muliggør høj operations-frekvens, høj effektivitet og høj drifttemperatur. Ikke desto mindre er der stadig visse hardware-designudfordringer, der hæmmer denne udvikling.

For at opnå fordelene af at bruge MV SiC-enheder til at erstatte dominansen af silicium (Si) isolerede gate-bipolare transistorer (IGBT) i MV effektelektronik, præsenterer denne afhandling først vigtigheden og nødvendigheden af at undersøge gate-driver (GD) design på grund af den hurtige skiftekarakteristik af SiC-enhederne. Derefter påpeges det, at støj og spændingsisolering er to væsentlige udfordringer, der opstår i gate-driver-designet. Baseret på state-of-the-art kategoriseres seriel-forbindelse i denne afhandling i to grupper som direkte og indirekte seriel-forbindelse i henhold til den tilsigtede synkrone og asynkrone skiftning. At opretholde fordelene ved hurtig skiftning af SiC-enheder medfører også en betydelig udfordring for spændingsbalancering ved direkte seriel-forbindelse.

Derefter foreslås en enkelt gate-drevet SiC-MOSFET-stak til at konstruere en selv-drevet GD med en flyback-topologi. Den enkelt gate-drevet GD fjerner problemet med støj og høj isoleringsbyrde der ellers findes i de nuværende GD, og derudover er en forenklet struktur og nemmere kontrol de markante fordele. Yderligere analyseres denne enkelt-gate drevne SiC-MOSFET-stak i forhold til kortslutningsfejl, og det identificeres hvordan en tilføjelse af et kredsløb kan gøre en SiC-MOSFET-stak robust imod kortslutning.

For direkte serieforbindelser, samt visse andre indirekte serieforbindelser uden store submodul-kondensatore, foreslås en konverter-baseret selvforsynende GD til MV SiC-enheder, som integrerer enheden og GD i et enkelt modul og gør den skalerbar til serieforbindelse. Vigtigst af alt eliminerer den fælles støj-vej fra GD til jord og reducerer isolationsbelastningen fra den samlede indgangs-spænding ned til enhedsspændingen. Ved at udføre eksperimenter er effektiviteten af denne selvforsynende GD blevet bekræftet i både DC-DC og DC-AC-konverteringer. På denne baggrund, foreslås en adaptiv impedansoptimeret styring af denne selvforsynende GD for at opnå en bedre afvejning mellem tab og spændingsbalancering af serieforbundne SiC MOSFET'er under både statiske og dynamiske tilstande. Endelig kan den dynamiske spændingsbalancering forbedres yderligere ved tilføjelse af aktiv forsinkelseskontrolstrategi.

Nøgleord: mellem-spænding, SiC MOSFET, hjælpestrømforsyning, gate-driver, serieforbindelse, spændingsbalancering, kortslutningsfejl, selv-forsynet, fælles tilstandsstøj.

ACKNOWLEDGEMENTS

This thesis makes a summary of the research achievements I have accomplished in the Ph.D. project conducted at AAU Energy, Aalborg University, Denmark. I would like to thank Medium Voltage BASIC & Center of Digitalized Electronics (CoDE) project for partially funding my Ph.D. project. In addition, I would also like to thank the Chinese Scholarship Council for granting me a CSC scholarship and the Otto foundation for supporting my study abroad.

I would like to extend my sincere thanks to Stig Munk-Nielsen, my supervisor, for providing me with the professional and valuable mentorship. I appreciate his support and encouragement, which assisted me in overcoming the research dilemma. This experience, as a precious treasure, would establish my essential confidence in my future research. I would also like to sincerely express the gratitude to my co-supervisor Asger Bjørn Jørgensen for crucial guidance, patient discussion, and kind assistance regarding the research and my writing skill. I would also like to thank my supervisor at KTH Royal institute, Hans-Peter Nee, for the productive discussion during my three-month study abroad in Stockholm, Sweden.

I would like to thank Hongbo Zhao as the Ph.D. mentor of mine, for providing substantial assistance with my research as well as career guidance. I would also like to thank the other co-authors in my appended publications, Wentao Liu, Shaokang Luan, Zhixing Yan, and Dipen Narendra Dalal, for their valuable contributions. I would like to thank my colleagues, Szymon Michal Beczkowski, Jannick Kjær Jørgensen, Yuan Gao, Zhongchao Sun, Faheem Ahmad, Benjamin Futtrup Kjærsgaard, Masaki Takahashi, Pawel Piotr Kubulus and Thore Stig Aunsborg, for the creative discussions. I would like to thank the project coordinator, Bonnie Steffensen, who assisted me with the reimbursing of conferences and travel expenses.

Finally, I would like to deeply express the gratitude to my family. Without your endless support, unconditional trust, significant encouragement, and unselfish love, I could not start and accomplish this journey.

Aalborg, April 2023

Rui Wang

TABLE OF CONTENTS

TABLE OF FIGURES

CHAPTER 1. INTRODUCTION

In recent decades, the advance of power electronics technology has extensively promoted the industry development, and power electronics converters are ubiquitous today, from tiny integrated modules of a few watts to giant converters of tens of megawatts. Among them, high-power converters based on fully-controlled power semiconductor devices play a crucial role in industrial applications for satisfying the requirement of solid power controllability. As the demand for power rating keeps growing, they are developing towards higher voltage for the purpose of saving copper loss and cost, which leads to the widespread use and promising future of medium voltage (MV) (1 kV - 35 kV) converters [1].

In terms of power generation, MV converters plays a crucial role in the utilization of renewable energy such as offshore wind turbines, large photovoltaic plants, etc. In terms of power consumption, MV converters are used to directly obtain power from the MV grid for fast charging of large electric vehicles, power supply of data centers, etc. Additionally, MV converters can also be applied as motor drives in areas like fans in the cement industry, compressors in the chemical industry, pumps in the water industry, etc. [2], which are taken as the example for the following elaboration as the products of some companies are listed in Table 1-1.

Manufacturer	Product	Voltage (AC)	Power
INGETEAM [3]	MV700	6.0/6.9 kV	1.7-11.1 MW
	MV100	3.3-4.16 kV	0.8-12.7 MW
SIEMENS [4]	GH150	4.16-13.8 kV	4-35 MVA
	GH180	2.3-11 kV	0.14-17 MVA
ABB [5]	ACS2000	4.0-6.9 kV	0.25-3.68 MW
	ACS5000	6.0-13.8 kV	2-36 MW
	MEGADRIVE-LCI	2.1-2*25 kV	2-150 MW
AMTECH [6]	AXPERT-HIVERT	3.3-11 kV	0.25-12.5 MW
DELTA [7]	MVD3000	3.3-11 kV	0.25-10.9 MW

Table 1-1 Industrial MV motor drives

As is widely known, the performance of power devices is of great significance to converters, and the above commercial products are all based on Silicon (Si) devices.

For relatively lower voltage, taking Ingeteam MV100 for instance, a back-to-back three-level converter based on Si insulated-gate-bipolar-transistor (IGBT) is qualified [3]. To meet higher voltage requirement such as 13.8 kV AC output voltage, modular multi-level converter need to be adopted as in the design of SIMENS GH150 [4].

Compared with the Si devices, Silicon Carbide (SiC) devices enable operation at higher blocking voltage, temperature and higher switching speed with less power loss [8]. Although till now, Si IGBTs still dominate in the field due to their standardized fabrications, mature designs, and improved performances. Thanks to the development of SiC technology, MV SiC metal-oxide-semiconductor field-effect transistor (MOSFET) rated from 3.3 kV to 15 kV has attracted attention due to its superior switching characteristics and become a promising power device to challenge the hegemony of Si IGBT [9]. Consequently, to prompt this evolution, it is essential to research its reliable gate driver (GD) design and series-connection design to comply with the high voltage standard and faster switching speed.

1.1. STATE-OF-THE-ART

1.1.1. GATE DRIVER DESIGN OF MV SIC MOSFET

Since both SiC MOSFET and Si IGBT have a similar gate structure, their driving mechanisms and corresponding GD designs are also comparable. Referring to the design of Si IGBT, GD of SiC MOSFET also requires adequate positive/negative voltage to assure the reliable turning on/off, reliable over-voltage protection and short-circuit protection to prevent damage to the device, active miller clamping circuit to prevent the device from being falsely turned on caused by crosstalk, etc.

While the difference is that, SiC MOSFET as a wide bandgap device requires a higher positive voltage to reduce the on-state loss and a lower negative voltage to avoid the gate breakdown (recommended as +20 V / -5 V). Besides, the fast switching characteristic of SiC MOSFET requires the response speeds of protection circuits to be faster, and the influences of parasitic parameters should be given greater consideration. Further, when moving towards MV SiC MOSFET from low-voltage SiC MOSFET, the challenge lies in the isolation, where both the signal transmission and power transmission are focused on. In MV cases, optical fibers are generally used in the signal transmission to achieve isolation. By contrast, the methods for isolation of the power transmission are numerous and rather important.

Most of GDs utilize the external-powered design which requires an external grounded power supply to power GD, as shown on the left side of Fig. 1-1. Therefore, considering the above voltage difference between input side and output side of GD, it is necessary to ensure sufficient isolation to prevent high voltage breakdown, and it is vital as well to ensure a sufficiently low coupling capacitance to prevent forming a large common mode current induced by high *dv/dt* during the switching process of

MV SiC MOSFET, which may cause interference to the driving signal when flowing through the GD. Hence, two ways are suitable for the power transfer design on GD, where one is based on power over fiber, and the other is based on transformer [10]. Since transferred power by the former one is limited and efficiency is low, a lot of research are targeting the latter one. To greatly reduce the coupling capacitance while maintaining high voltage isolation, the material, size and the winding design of magnetic cores are studied [11]-[12]. For further improvement, a method of PCB based planar winding can be adopted [13], and a method of high-density current-transformer can be applied [14]. Nowadays, wireless power transfer is a popular solution for GD design where the magnetic core is removed, which has claimed 120 W output power, 92.78% full-power efficiency, and 27 kV isolation capability [15].

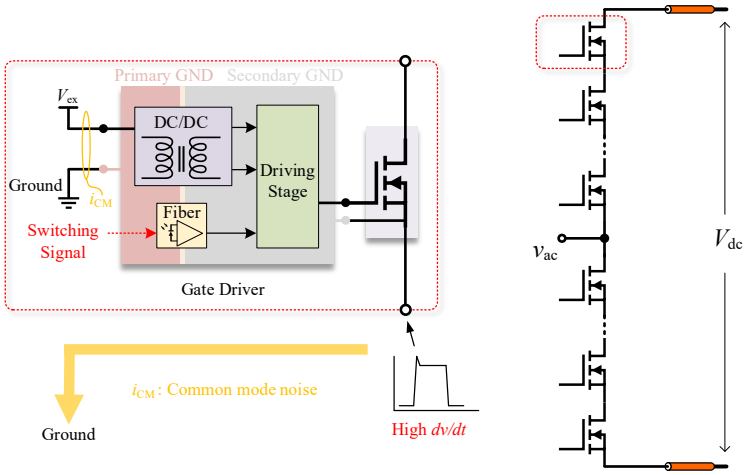


Figure 1-1. Direct series-connection of MV SiC MOSFETs

In contrast, self-powered GD design, where GD extracts power from the main loop directly, enables the power device, its GD, and the associated power extracting part to be included in a single unit. It can greatly ease the high voltage isolation burden. Besides this, low coupling capacitance is achieved as well since the common mode current path from the GD to the ground is eliminated. Additionally, since the external power source is not used, it is appropriate for extended design. Nevertheless, this self-powered concept has only yet been realized in a number of methods for thyristors, IGBTs, and lower voltage MOSFETs.

1.1.2. SERIES-CONNECTION DESIGN OF MV SIC MOSFETS

Considering the design margin of using MV SiC MOSFET, a single device limited by its blocking voltage is only suitable for a small number of medium voltage cases. To accommodate the higher voltage application scenarios, series-connection of MV SiC

MOSFETs is called for, which is divided into direct series-connection and indirect series-connection in this thesis.

Direct series-connection is the straightforward method to improve the blocking voltage of device by connecting more devices in series, as shown on the right side of Fig. 1-1, and the working principle is to make the series-connected power devices switch synchronously. However, there exists a well-known challenge that unbalanced voltage distribution occurs among devices. Voltage unbalancing of series-connected devices in a stack can result in devices withstanding higher voltages than their own blocking capabilities when operating at the expected total voltage, and the overvoltage breakdown of one device can further lead to breakdown of the full stack as a severe consequence. Static voltage unbalancing of series-connected devices is induced by the leakage current discrepancy of devices and it is generally solved by placing balancing resistors in parallel. With dynamic voltage unbalancing being the major problem, it is caused by inconsistencies of GDs of devices, devices characteristics, etc., and a significant voltage unbalancing could occur during the switching transients. For low-voltage devices, literatures have given extensive analysis and provided many valuable solutions [16]. For MV SiC MOSFETs, the direct series-connection is only studied in a few papers [17]-[21], and adding resistor-capacitor snubbers is the common voltage balancing (VB) method, which causes large power loss for good VB performance.

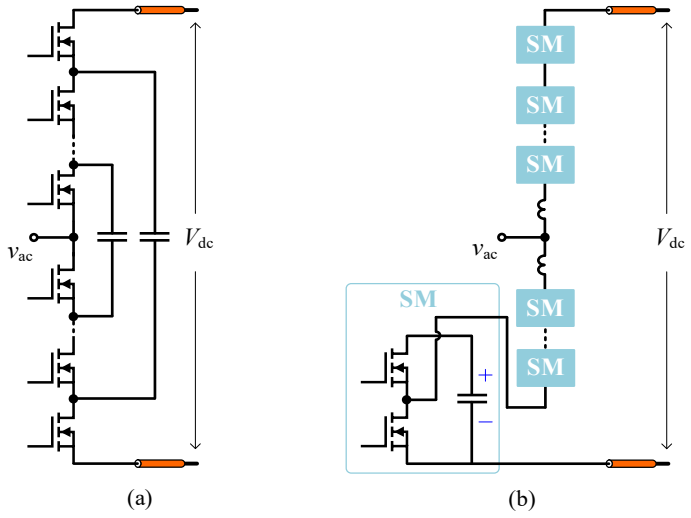


Figure 1-2. Indirect series-connection of MV SiC MOSFETs (a) multi-level converter with flying capacitor (b) modular multi-level converter

In contrast to direct series connection, indirect series-connection manages to avoid the dynamic voltage unbalancing by means of topology modifications of the converters [22], and thus the electromagnetic interference (EMI) issue will be

reduced, or the filter requirement will be lower by means of switching series-connected power devices asynchronously.

Fig. 1-2(a) presents a prevalent method of using flying capacitors to implement this goal. The transient voltages of devices are clamped by the capacitors to assure safety, and the balancing of charging and discharging of capacitors are controlled by the specific modulation of the converter. With large flying capacitors to clamp voltages temporarily, considerable driving delays of devices in the stack can be set intentionally to realize multi-level modulation, which facilitates reduction of the harmonic content of output voltage and alleviation of EMI issue [23]. However, the large capacitors occupy a large volume of the converter based apparatus and increase the total cost. Therefore, a quasi-two-level modulation becomes attractive with small flying capacitors despite of sacrificing the benefit of low harmonic content [24]-[25]. A similar design by adopting the diode clamping method is also prevalent, and using multi-level modulation for low harmonic content while using quasi-two-level modulation for the lower requirements of diodes [26].

Although the above flying capacitor converter and diode clamping converter are effective in MV design, their topologies become more and more complicated as the series count of devices increases to meet the higher voltage requirement. Instead, the modular multi-level converter (MMC), as another type of indirect series-connection is preferred in the higher voltage cases, as shown in Fig. 1-2(b). Similarly, in order to achieve multi-level output voltage with low harmonic content, the submodule (SM) capacitance needs to be large which increases the size and cost, and using quasi-two-level modulation can be one tradeoff solution [27]-[28].

It is worth noting that, to alleviate the common mode noise and isolation problems as described above, auxiliary power supply (APS) is integrated into the SM to power GDs, which benefits from the modular design and the intrinsic SM capacitor [29]. Since APS extracts the power from the SM capacitor, it also utilizes a self-powered concept, which is known as self-powered APS. Different from the above illustrated self-powered GD which is combined with a single power device to be considered as a unit, as this self-powered APS is combined with a SM as a unit, it will still suffer from the common mode noise to some extent inside the SM, while self-powered GD features the elimination of common mode noise theoretically.

Although using MV SiC MOSFETs can reduce the series count compared with using low-voltage ones and simplify the complexity, the input voltage of the self-powered APS becomes higher and its corresponding design as a high-input-voltage low-output-lower converter needs to be considered. Due to cost saving, low-voltage devices are generally adopted in the design. Therefore, lots of optimization methods have been proposed, including input-series structure [30], multi-cell series-parallel converter [31], high-voltage tapped-inductor buck converter [32], etc. However, they make the topology and control scheme complicated.

1.2. RESEARCH OBJECTIVES

The research aims to identify some potential challenges of the direct and indirect series-connection of MV SiC MOSFETs with self-powered design, and then to provide corresponding analyses and solutions:

- For self-powered auxiliary power supply design in the SM of MMC, an appropriate DC to DC topology with high-input-voltage, simple control and low cost needs to be chosen.

- For self-powered gate driver design, although greatly reduced by using self-powered concept, the high-input-voltage and large *dv/dt* (*di/dt*) still cause potential isolation and interference problems to itself. Besides, a suitable topology for constantly self-powering should be taken into account.

- For direct series-connection design, the fast switching characteristic of MV SiC MOSFET brings more difficulty to the active voltage balancing. Hence, an effective voltage balancing strategy is required.

1.3. ORIGINAL CONTRIBUTIONS

Based on the above research objectives, the novelty in this thesis and the original contributions are as follows:

- To simplify the topology and ease the control burden, a flyback converter is selected to construct the self-powered auxiliary power supply. For satisfying the high-input-voltage requirement, a single gate-driven stack consisting of directly series-connected SiC MOSFETs with low-voltage rating is proposed as the primary switch of this flyback converter, which possesses the capability of automatic voltage balancing [**Publication IV, Publication V**]. Further, its short-circuit characteristic is studied and analyzed, and the potential for over-current limitation in the single gate-driven stack is firstly pointed out. As a result, the single gate-driven SiC MOSFET stack is improved to increase its ability to resist short-circuit faults, and these enhancements have significantly strengthened the stack's capability of anti-short circuit fault [**Publication II**].

- A scalable self-powered gate driver with converter-based design is suggested, where the SiC MOSFET stack with automatic voltage balancing capability is used to build a high-input-voltage power extracting converter, and it makes commercial gate driver available as its following gate driving part. It works efficiently without the aid of the main loop power device's switching. In addition, the self-powered gate driver is controlled as a clamping resistor-capacitor-diode (RCD) snubber by using the open-loop

design of the power extraction converter, which is scalable to the series-connection of power devices [**Publication III**].

- Adaptive-impedance optimization of the self-powered gate driver with converter-based design is proposed for obtaining a better static and dynamic voltage balancing performance of series-connected SiC MOSFETs. Further, as a passive voltage balancing strategy, it facilitates the small-signal model establishment for combining with an active delay control method, which contributes to a well-balanced voltage distribution [**Publication I, Publication VI**]. In addition, the startup problem of using self-powered gate drivers is also evaluated, and a potential improvement method is provided and further demonstrated experimentally [**Publication VII**].

1.4. PUBLICATIONS

APPENDED PUBLICATIONS

This thesis is prepared as a summary of published papers, and the following papers are appended as part of this thesis.

In journals:

I. **R. Wang**, A. B. Jørgensen, W. Liu, H. Zhao Z. Yan and S. Munk-Nielsen, "Voltage Balancing of Series-connected SiC MOSFETs with Adaptive-impedance Self-powered Gate Drivers," in *IEEE transaction on Industrial Electronics*, doi: 10.1109/TIE.2022.3231281, 2022, Early Access.

II. **R. Wang**, A. B. Jørgensen, H. Zhao and S. Munk-Nielsen, "An Improved Single Gate Driven SiC MOSFET Stack with Strong Anti-short Circuit Fault Capabilities," in *IEEE Transactions on Power Electronics*, vol. 37, no. 11, pp. 13577-13586, Nov. 2022.

III. **R. Wang**, A. B. Jørgensen, D. N. Dalal, S. Luan, H. Zhao and S. Munk-Nielsen, "Integrating 10kV SiC MOSFET into Battery Energy Storage System with A Scalable Converter-based Self-powered Gate Driver," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 1, pp. 351-360, Feb. 2023.

IV. **R. Wang**, A. B. Jørgensen, and S. Munk-Nielsen, "An Enhanced Single Gate Driven Voltage-balanced SiC MOSFET Stack Topology Suitable for High-voltage Low-power Applications," in *IET Power Electronics*, vol. 15, no. 3, pp. 251-262, Feb. 2022.

At conferences:

V. **R. Wang**, H. Zhao and S. Munk-Nielsen, "Comparison of Two Types of Single Gate Drivers for SiC MOSFET Stacks in Flyback Converters," in *2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia*, 2021, pp. 36-40.

VI. **R. Wang**, A. B. Jørgensen, H. Zhao and S. Munk-Nielsen, "Design and analysis of a voltage clamping active delay control method for series-connected SiC MOSFETs," in *24th European Conference on Power Electronics and Applications*, 2022, pp. 1-8.

VII. **R. Wang**, A. B. Jørgensen, W. Liu, H. Zhao, Z. Yan, D. N. Dalal and S. Munk-Nielsen, "Auxiliary Power Supply Startup Evaluation and Improvement of the Input-series System With Small Submodule Capacitances," in *2023 IEEE Applied Power Electronics Conference and Exposition*, 2023, Accepted.

OTHER PUBLICATIONS

In addition to the appended papers, a contribution has been made during the Ph.D. project period.

1. H. Zhao, S. Luan, Z. Shen, A. J. Hanson, Y. Gao, D. N. Dalal, **R. Wang**, S. Zhou, and S. Munk-Nielsen, "Rethinking Basic Assumptions for Modeling Parasitic Capacitance in Inductors," in *IEEE Transactions on Power Electronics*, vol. 37, no. 7, pp. 8281-8289, July 2022.

2. H. Zhao, Z. Yan, S. Luan, D. N. Dalal, J. K. Jørgensen, **R. Wang**, X. Zhou, S. M. Beczkowski, B. Rannestad and S. Munk-Nielsen, "A Comparative Study on Parasitic Capacitance in Inductors with Series or Parallel Windings," in *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 15140-15151, Dec. 2022.

1.5. THESIS OUTLINE

The thesis is constructed in the following manner:

Chapter 1 introduces the background and illustrates the state-of-the-art within gate driver design and series-connection design of MV SiC MOSFETs, followed by the defined research objectives. Chapter 2 presents detail of the proposed single gate-driven SiC MOSFET stack, which is designed for high-input-voltage low-output-power applications represented by the self-powered auxiliary power supply in MMC. Chapter 3 delves deeper into the short-circuit properties of the single gate-driven stack

and expounds on the specific measures taken to facilitate the automatic resolution of any short-circuit faults.

Chapter 4 presents the designed self-powered gate driver for MV SiC MOSFET and verifies its effectiveness in experiments. Chapter 5 proposes a novel approach called adaptive-impedance optimization for the self-powered gate driver, aimed at improving the voltage balancing performance of MV SiC MOSFETs in both static and dynamic conditions. Based on it, a hybrid voltage balancing strategy is further proposed, followed by the converter performance demonstration.

Chapter 6 marks the conclusion of the thesis, providing a summary of the research conducted and a discussion on possible avenues for future work.

In the final section, the bibliography and the appended publications are included.

CHAPTER 2. A SINGLE GATE-DRIVEN STACK FOR SELF-POWERED AUXILIARY POWER SUPPLY

The information in this chapter is based on **Publication IV and Publication V**.

As a typical topology of indirect series-connection of devices, modular multi-level converter (MMC) is selected as an instance for illustration, and Fig. 2-1 presents intuitive comparison between the external-powered approach and the self-powered one for the gate drivers (GDs), protections, etc.

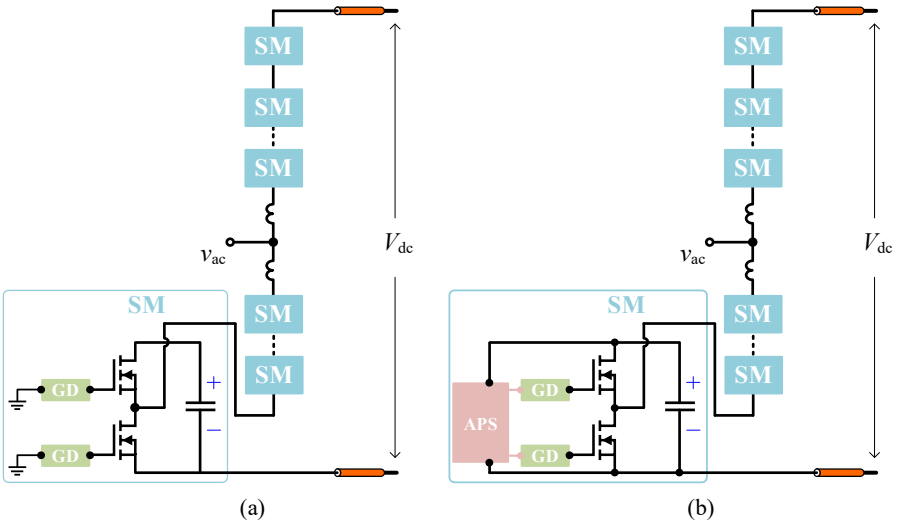


Figure 2-1. MMC hardware with the (a) external-powered (b) self-powered approach

In Fig. 2-1(a), the GD is powered through an external grounded power supply, which necessitates its ability to withstand the high voltage and *dv/dt* during the switching transient of the device, especially for the top submodule (SM). Instead, in Fig. 2-1(b), a self-powered auxiliary power supply (APS) is integrated as an essential part in the SM hardware design, and the isolation burden of GD is eased from the total bus voltage to the SM bus voltage and the *dv/dt* immunity requirement is decreased, which also facilitates the modular design. Therefore, the design of self-powered APS is significant. To simplify the topology and control complexity, utilizing the flyback topology is an effective option in this APS design. However, owing to the high-input-

voltage condition when using medium voltage (MV) SiC MOSFET in the SM design, it necessitates the employment of a low-power device with an equivalent voltage rating as the primary switch in the flyback topology, which is unavailable or expensive in some cases, making direct series-connection of low-voltage power devices an appealing solution.

2.1. SINGLE GATE DRIVER CONCEPT

For the direct series-connection, compared with the conventional approach of using individual GD for each device, single GD shows its compactness where the upper devices in the stack can be driven by some simple passive components whereas only the device at the bottom requires a standard GD. However, this approach will lead to inherent delays in the gate driving loops of series-connected devices and result in significant voltage unbalancing [33]-[36]. Therefore, it is widely researched in the field of solid-state circuit breaker where only one-time turning-off is required, and the energy absorbing components such as varistors are deployed for the transient voltage balancing (VB) purpose. For converter design, several VB methods have also been proposed. In [37]-[38], the commonly used resistor-capacitor-diode (RCD) snubbers are utilized for VB, but this method presents the issue of high loss if a balanced voltage distribution is desired. Additionally, each device requires an extra power supply in its gate loop, which raises the overall cost. In [39], two series-connected devices are respectively accompanied by two compensation capacitors that are placed in parallel for VB, however, the performance is highly dependent on the conditions. These parameters must be precisely selected for a particular situation and adjusted as the power loop varies, or else the voltage unbalancing will become unacceptable.

Therefore, the challenge of enhancing the adaptability of a single GD while reducing loss still needs to be addressed. Despite that the authors in [40] managed to achieve the goal by incorporating a controller to regulate the driving speed, this design was complex and only applied to the series-connection case of two SiC MOSFETs. Meanwhile, the authors in [41] utilized a unique snubber topology with good voltage adaptability to balance voltages through automatic balancing loops, but it still used a traditional gate driver design and required a complicated startup circuit. Hence, in this chapter, a novel improved single gate-driven SiC MOSFET stack that integrates the benefits in [40] and [41] is proposed, as depicted in Fig. 2-2. It includes a specifically designed single GD (the blue part), and an optimized RCD snubber (the green and red parts) which is defined as an automatic VB RCD^2 circuit.

2.2. WORKING PRINCIPLE OF THE SUGGESTED SINGLE GATE-DRIVEN STACK

Fig. 2-2 depicts a stack of SiC MOSFETs consisting of four devices T_i (i = 1 ~ 4) connected in series, where the count is chosen when employing 1.7 kV / 5 A devices to satisfy the voltage requirement of 5 kV in the self-powered APS and taking some

design margin into account. It is observed that only the SiC MOSFET at the bottom necessitates a standard GD while the upper devices are driven through additional coupling capacitors C_{ai} ($i = 1 \sim 3$) which connects the gate electrode of T_i to the source electrode of its adjacent device. Resistor R_{si} ($i = 1 \sim 4$) is for static VB, while R_{gi} ($i = 1 \sim 4$) and D_{ai} (D_{bi}) are respectively utilized as the gate resistor and the gate protection Zener diode. In contrast to the commonly known RCD snubber, the resistance in the automatic VB RCD[2] circuit is selected to be large for saving loss. VB of T_i ($i = 1 \sim 4$), that is, the balancing of drain-source voltage v_{dsi}, is improved by placing diodes D_{ci} ($i = 1 \sim 3$) between snubber capacitors, which takes advantage of the sequential lagging single GD. Next, on the basis of the depicted turning-on and turning-off processes, the working detail will be illustrated as follows.

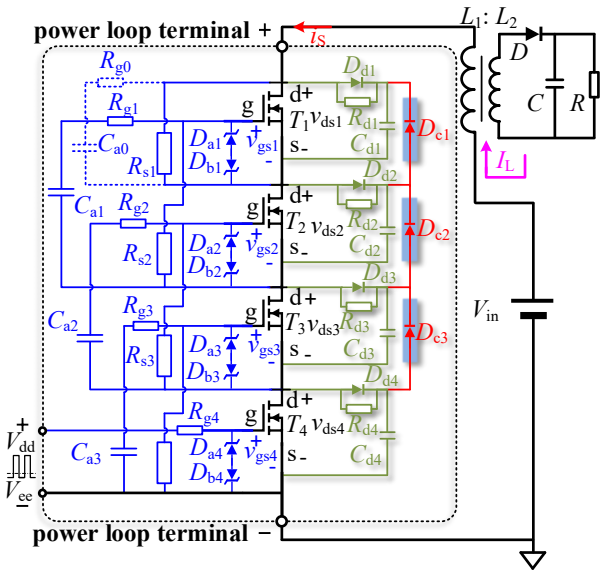


Figure 2-2. Topology of the improved single gate-driven SiC MOSFET stack

2.2.1. TURNING-ON PROCESS

Fig. 2-3 illustrates that the process of turning-on can be segmented into four stages, labeled as Stage I through IV.

Stage I [$t_0 \sim t_1$]: during this stage, the gate-source voltage v_{gs4} of T_4 equals the negative driving voltage V_{ee}, and there is a key current loop to assure the reliable off-state of this stack as depicted in Fig. 2-4(a). Since the Zener voltage of D_{bi} and the resistance of R_{si} can be chosen properly (considering the forward voltage drop of D_{ai} as well) [42], v_{gsi} ($i = 1 \sim 3$) of T_i will also be equivalent to V_{ee}, and v_{dsi} will be in static balance.

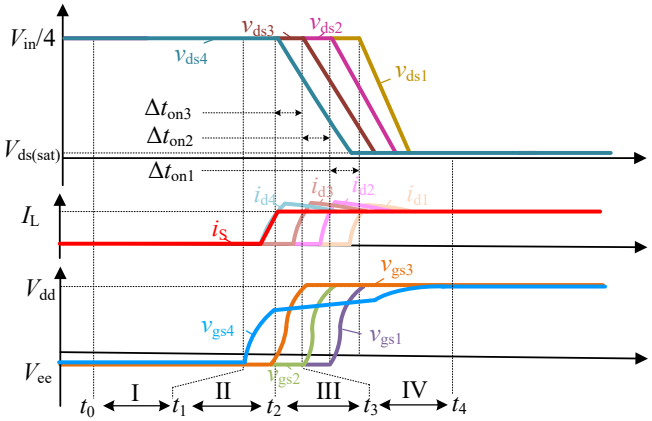


Figure 2-3. Turning-on process of the proposed stack

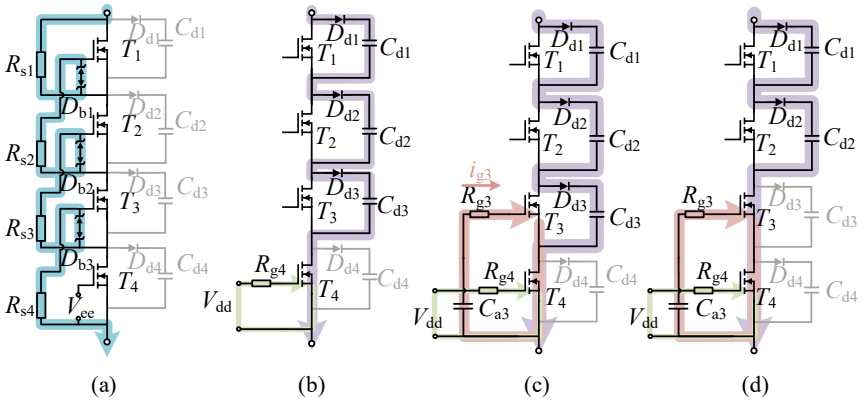


Figure 2-4. Key circuit status in (a) Stage I, (b) Stage II, (c) Stage III, (d) Stage VI

Stage II [$t_1 \sim t_2$]: v_{gs4} begins to increase from V_{ee} to the positive driving voltage V_{dd} when T_4 receives the turning-on signal. When T_4 reaches the saturation region, it triggers the load current I_L to initiate the commutation process from the secondary side to the stack, and the stack current i_S will increase from zero. Since T_i (i = 1 ~ 3) remains in its cutoff region, as seen in Fig. 2-4(b), i_S will instead flow through C_{di} (i =1 ~ 3) which is relatively large in our approach to avoid voltage unbalancing.

Stage III [$t_2 \sim t_3$]: when i_S approaches the load current I_L at t_2, v_{ds4} begins to decrease, and it induces the current forming in the gate loop of T_3 as depicted in Fig. 2-4(c). As

a result, there is an increase in the drain current of T_4 (i_{d4}) when compared to i_S, and the following relationship can be established as:

$$i_{M4}=i_{d4}+i_{ds4}+i_{gd4}=I_L+i_{g3}+i_{ds4}+i_{gd4}. \tag{2-1}$$

where i_{M4} represents the channel current inside T_4, i_{g3} represents the gate current of T_3 which flows into the gate capacitance C_{in3} via R_{g3}, and i_{ds4} and i_{gd4} denote the currents across the drain-source capacitance C_{gd4} and the Miller capacitance C_{ds4}, respectively.

By incorporating the transconductance parameter G_M and the threshold voltage V_{th}, the relationships can be obtained as follows:

$$\begin{cases} i_{M4}=G_M(v_{gs4}-V_{th}), & v_{gs4}>V_{th} \\ i_{g3}\approx\dfrac{-dv_{ds4}/dt}{(1/C_{a3}+1/C_{in3})} \\ i_{gd4}/C_{gd4}\approx i_{ds4}/C_{ds4}=-dv_{ds4}/dt \end{cases}. \tag{2-2}$$

Combining Eq. (2-1) and Eq. (2-2), dv_{ds4}/dt can be solved as:

$$\frac{dv_{ds4}}{dt}\approx-\frac{G_M(v_{gs4}-V_{th})-I_L}{C_{gd4}+C_{ds4}+1/(1/C_{a3}+1/C_{in3})}. \tag{2-3}$$

From Eq. (2-2), it is observed that i_{g3} is highly dependent on dv_{ds4}/dt, which in turn causes an increase of v_{gs3}. By adjusting the Zener breakdown voltage of D_{ai}, v_{gs3} will be eventually clamped at V_{dd}. When T_3 reaches the saturation region as well, the current will be transferred from C_{d3} to T_3, and the drain current i_{d3} of T_3 gets increased.

Stage IV [$t_3 \sim t_4$]: at t_3, i_{d3} reaches I_L as well, and the proposed stack switches to the status as depicted in Fig. 2-4(d). Next, v_{ds3} decreases with the Δt_{on3} lag behind v_{ds4}. In a similar way, the status changes of gate and power loops of T_i (i=1~3) are analogous to those of T_4. After Δt_{on2}, v_{ds2} also decreases, followed by the decrease of v_{ds1} after Δt_{on1}, and dv_{dsi}/dt (i=1~3) is determined as:

$$\begin{cases} \dfrac{dv_{dsi}}{dt}\approx-\dfrac{G_M(v_{gsi}-V_{th})-I_L}{C_{gdi}+C_{dsi}+1/(1/C_{a(i-1)}+1/C_{in(i-1)})}, & i=2,3 \\ \dfrac{dv_{ds1}}{dt}\approx-\dfrac{G_M(v_{gs1}-V_{th})-I_L}{C_{gd1}+C_{ds1}} \end{cases}. \tag{2-4}$$

In Eq. (2-4), the dv_{ds1}/dt of T_1 is steeper since T_1 has one less charging/discharging branch (the resistance-capacitance $R_{g0}C_{a0}$ branch is not included in this section). In comparison, the voltage fall time in v_{dsi} (i = 2 ~ 4) is relatively similar.

At t_4, the full flow of I_L through T_i ($i = 1 \sim 4$) and the arrival of v_{gs4} at V_{dd} signify that the turning-on process of the stack is completed.

2.2.2. TURNING-OFF PROCESS

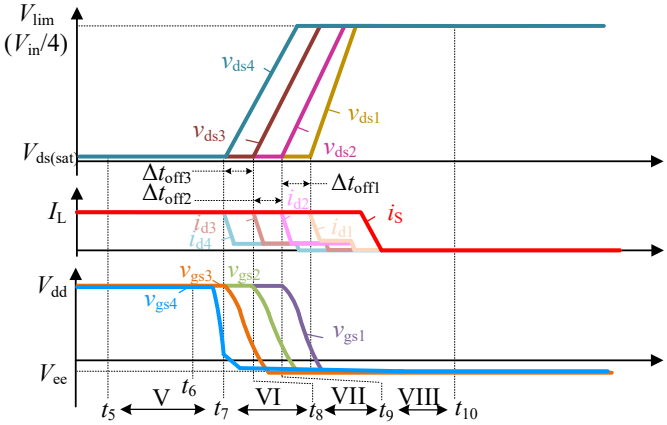


Figure 2-5. Turning-off process of the proposed stack

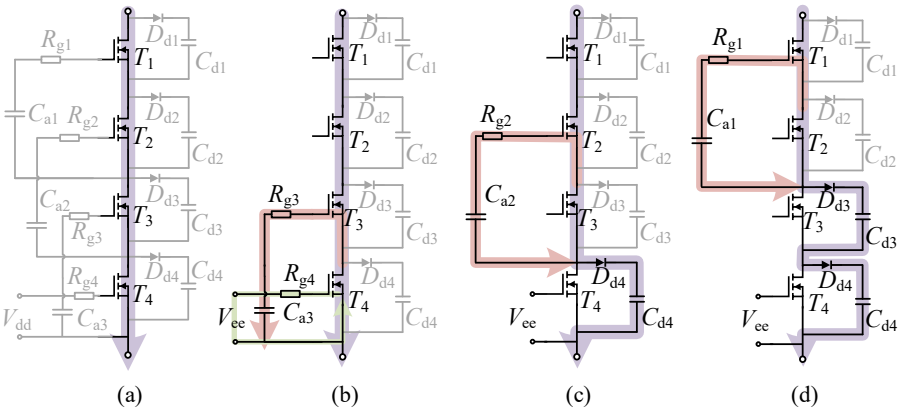


Figure 2-6. Key circuit status in (a) Stage V, (b) Stage VI, (c) Stage VII, (d) Stage VIII

Fig. 2-5 illustrates that the process of turning-off can be segmented into four stages as well, labeled as Stage V through Stage VIII.

Stage V [$t_5 \sim t_7$]: v_{gsi} is equal to V_{dd} and the stack is in on-state during this stage, which is depicted in Fig. 2-6(a). At t_6 when T_4 receives the turning-off signal, its driving voltage is caused to change from V_{dd} to V_{ee}. Therefore, v_{gs4} begins to decrease from V_{dd} gradually.

Stage VI [$t_7 \sim t_8$]: At t_7, T_4 reaches the saturation region from linear region as v_{gs4} is decreasing and v_{ds4} begins to increase, which induces discharging on the gate side of T_3, as depicted in Fig. 2-6(b). By setting the Zener breakdown voltage of D_{bi}, v_{gs3} will be finally clamped at V_{ee}. In the meantime, Eq. (2-3) is still applicable in this situation, and thus dv_{ds4}/dt can be also estimated.

Stage VII [$t_8 \sim t_9$]: At t_8, T_3 also reaches the saturation region, and v_{ds3} increases Δt_{off3} later than v_{ds4}. In the same manner, the rising rate of v_{ds3} can also be determined in accordance with Eq. (2-4), which further results in discharging on the gate side of T_2. As depicted in Fig. 2-6(c), when v_{ds4} reaches the limiting value V_{lim} (approximate to $V_{in}/4$ in this case), i_S will flow through C_{d4} rather than T_4. Since C_{d4} is relatively large and the rising of v_{ds4} will be significantly slower, therefore, the voltage unbalancing is avoided as well.

Stage VIII [$t_9 \sim t_{10}$]: At t_9, v_{ds2} begins to increase and it lags Δt_{off2} behind v_{ds3}, and the stack is changed to the status as depicted in Fig. 2-6(d). The overvoltage of v_{ds3} is also prevented as it is clamped to V_{lim}. After Δt_{off1}, v_{ds1} will begin to increase as well, and the rising slopes of v_{ds1} and v_{ds2} can be calculated by Eq. (2-4). Similarly, dv_{ds1}/dt is higher due to the absence of one charging/discharging branch, while both v_{ds1} and v_{ds2} will be limited to V_{lim} as well. Finally, at t_{10}, the turning-off process of the stack is completed.

2.2.3. AUTOMATIC BALANCING PROCESS AND NON-IDEAL FACTORS

Based on the above analysis, the VB of the stack is realized in both the turning-on and turning-off processes with the aid of the clamping circuit. To make it work effectively under the continuously switching process of the stack, not only should the voltage of C_{di} ($i = 1 \sim 4$) be balanced, but also the charging of discharging should be balanced. Next, the explanation is given as follows.

As the stack is repeatedly switched on and off in this converter application, the switching delays of T_i ($i = 1 \sim 4$) will cause the energy accumulation of C_{di}, and the energy ΔE_i accumulated during one switching cycle can be expressed as:

$$\begin{cases} \Delta E_1 = V_{lim} I_{L(on)} (\Delta t_{on1} + \Delta t_{on2} + \Delta t_{on3}) \\ \Delta E_2 = V_{lim} I_{L(on)} (\Delta t_{on1} + \Delta t_{on2}) + V_{lim} I_{L(off)} \Delta t_{off3} \\ \Delta E_3 = V_{lim} I_{L(on)} \Delta t_{on1} + V_{lim} I_{L(off)} (\Delta t_{off2} + \Delta t_{off3}) \\ \Delta E_4 = V_{lim} I_{L(off)} (\Delta t_{off1} + \Delta t_{off2} + \Delta t_{off3}) \end{cases} . \quad (2\text{-}5)$$

where the load currents during turning-on and turning-off are distinguished as $I_{L(on)}$ and $I_{L(off)}$, and $I_{L(off)} > I_{L(on)}$ (ignoring turning-on current overshoot). Since the self-powered APS is a high-input-voltage and low-output-power application, both $I_{L(off)}$ and $I_{L(on)}$ are small, and the magnitude of dv_{dsi}/dt during turning-on process is larger as compared to that during turning-off process. Further, Δt_{oni} and Δt_{offi} ($i = 1 \sim 3$) can be obtained as:

$$\begin{cases} \Delta t_{oni} \approx \dfrac{C_{ini}(V_{dd} - V_{ee})}{i_{gi}} \approx \dfrac{C_{ini}(V_{ee} - V_{dd})(1/C_{ai} + 1/C_{ini})}{dv_{ds(i+1)}/dt} \\ \Delta t_{offi} \approx \dfrac{C_{ini}(V_{ee} - V_{dd})}{i_{gi}} \approx \dfrac{C_{ini}(V_{dd} - V_{ee})(1/C_{ai} + 1/C_{ini})}{dv_{ds(i+1)}/dt} \end{cases}, i=1\sim3 \tag{2-6}$$

Consequently, it is concluded from Eq. (2-6) that Δt_{offi} is much larger than Δt_{oni}. Further, it is solved from Eq. (2-5) that $\Delta E_4 > \Delta E_3 > \Delta E_2 > \Delta E_1$, and it provides the prerequisite of the automatic VB process as illustrated below.

As depicted in Fig. 2-2, the automatic balancing RCD[2] circuit is made up of R_{di} ($i = 1 \sim 4$), C_{di}, D_{di} and D_{ci} ($i = 1 \sim 3$). It generates extra current loops during the turning-on process of the stack, as depicted in Fig. 2-7(a). Since C_{d4} stores the most energy as described above, when the voltage across C_{d4} (v_{cd4}) becomes greater than that across C_{ds3} (v_{cd3}), D_{c3} will conduct during the on-state of T_4 and bring v_{cd4} and v_{cd3} back to equality. Similarly, v_{cdi} ($i = 1 \sim 4$) across C_{di} will be equalized during the on-state of the stack, making it easy to select R_{di} which serves to consume ΔE_i. In this way, v_{cdi} across C_{di} is kept at V_{lim} by releasing accumulated ΔE_i during each switching cycle. As a result, C_{di} can be regarded as a constant voltage source, therefore, the proposed stack operates as intended.

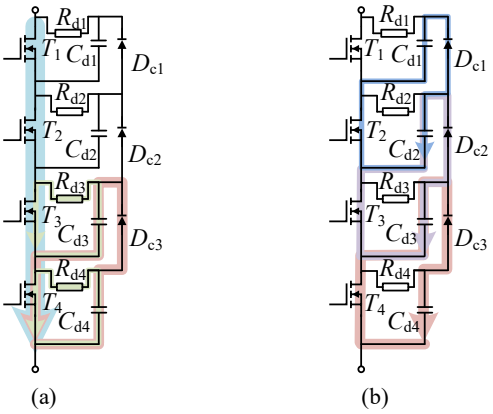


Figure 2-7. (a) automatic balancing current loops (b) non-ideal reverse current loops

It has been known that using small resistors in well-known RCD snubbers to control SiC MOSFET switching transients and VB can result in significant additional losses. From this perspective, passive methods are not favored compared to active control methods with complex structure and control strategy. Instead, in the proposed topology, a large R_{di} is chosen to consume only a small amount energy ΔE_i as per Eq. (2-5), and the parameter selection criteria are as follows:

In practical applications, it is not feasible to choose the largest possible value for C_{di} due to the associated increase in volume. Therefore, after v_{ds4} reaches V_{lim}, dv_{ds4}/dt could be expressed as:

$$\frac{dv_{ds4}}{dt} \approx \frac{I_{L(off)}}{C_{d4}+C_{gd4}+C_{ds4}+1/(1/C_{a3}+1/C_{in3})} \approx \frac{I_{L(off)}}{C_{d4}}. \tag{2-7}$$

Following a duration of $t_{sum}=\Delta t_{off3}+\Delta t_{off2}+\Delta t_{off1}$, it is anticipated that the increment of v_{ds4} will be a small value ΔV, and it can be solved as:

$$\Delta V = \frac{dv_{ds4}}{dt} t_{sum} \approx \frac{I_{L(off)} t_{sum}}{C_{d4}}. \tag{2-8}$$

In Eq. (2-8), when ΔV is defined in advance and $I_{L(off)}t_{sum}$ is estimated, C_{d4} along with the same C_{di} (i = 1 ~ 3) could be selected.

In Fig. 2-7(a), the equivalent discharging model of $R_{di}C_{di}$ during the on-state can be simplified due to the negligible voltage drop of v_{Cdi} (i=1 ~ 4). Based on the principle that v_{Cdi} returns to be V_{lim} after one switching cycle, the relationship exists as:

$$\frac{C_{di}[(\Delta V+V_{lim})^2-V_{lim}{}^2]}{8} \approx \frac{T_{on}V_{lim}{}^2}{R_{di}}, \quad i=1\sim4. \tag{2-9}$$

where T_{on} refers to the duration of the on-state within one switching cycle.

Once V_{lim} is defined and other parameters are determined, R_{di} (i = 1 ~ 4) can be selected as well using Eq. (2-9).

It is worthy of noting that the above analysis is conducted under ideal conditions. However, practical components used in real-world applications may not be ideal, and thus, necessitating their consideration. In selecting R_{di}, non-ideal components such as diodes can introduce additional energy consumption paths, making it possible to choose an even larger R_{di}. Additionally, two main influences must be considered:

(1) Due to the reverse recovery and parasitic capacitance of D_{ci} (i = 1 ~ 3) during the turning-off process, it induces reverse current loops as depicted in Fig. 2-

7(b). Hence, it is necessary to include an additional discharging loop during the turning-off process of T_i (i = 2 ~ 4), and Eq. (2-3) and Eq. (2-4) should be amended. As a result, v_{dsi}/dt (i = 2 ~ 4) will be smaller while v_{ds1}/dt will remain unchanged, which may cause v_{ds1} to increase to V_{lim} earlier than v_{ds2}.

(2) Since the transformer and the diode D on the secondary side have parasitic capacitances, during the turning-on process of the stack, the high dv/dt will induce an additional current flowing through the stack, which could result in $I_{L(on)}>I_{L(off)}$.

According to Eq. (2-6), each of the aforementioned factors could result in a disagreement with the conclusion $\Delta E_4>\Delta E_3>\Delta E_2>\Delta E_1$ and have a negative impact on the proposed topology's VB. Therefore, a $R_{g0}C_{a0}$ branch is placed in parallel with T_1 additionally, as indicated by the dash line in Fig. 2-2. By reducing v_{ds4}/dt in this manner, $\Delta E_4>\Delta E_3>\Delta E_2>\Delta E_1$ can be assured and effective VB is achieved.

2.3. EXPERIMENTAL RESULTS IN SELF-POWERED AUXILARY POWER SUPPLY APPLICATION

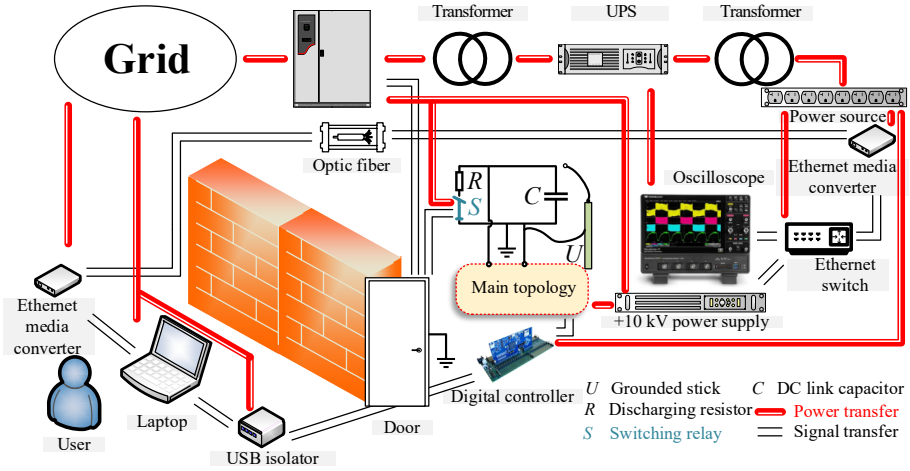


Figure 2-8. Diagram of medium voltage testing platform

The MV testing platform is built based on the diagram depicted in Fig. 2-8. To ensure the safety of conducting MV experiments, the device or circuitry under test is placed inside the cage, and the user is working outside with a laptop and corresponding communication system through optic fiber to realize remote control. The 10 kV adjustable DC power supply gets powered from the grid, and it outputs the expected MV input voltage for test. Since it charges the DC link capacitor C every time and the

remaining energy of C can be large when the test is finished, a discharging resistor R and a MV switching relay S are series-connected and then put in parallel with C to discharge the energy. S is triggered on/off every time when the door is open/close to assure safety of the user's inside operation, besides this, a grounded stick U should be put in physical contact with C to further assure the complete discharge of C before the inside operation. In addition, a digital controller is connected with the laptop through MV isolation to ensure online hardware control. Moreover, high-precision and high-bandwidth oscilloscope, high-voltage probe with differential isolation, low-voltage probe with optical isolation, high-voltage and low-voltage passive probe, current probe, etc. for measuring purposes are put inside the cage and remote recording of experimental data is achieved.

Based on the above, the proposed SiC MOSFET stack's experimental performance is further examined, where the complete self-powered APS schematic and the corresponding hardware photograph are shown in Fig. 2-9. Discontinuous current mode (DCM) is employed in this flyback topology by choosing LT3798 as the offline controller [43], which enables zero current switching (ZCS) of the MOSFETs during turning-on and ZCS of the diode during turning-off, and. It is essential to note that the proposed stack could suffer from temporary gate oscillations of upper devices due to the power loop voltage oscillation under the DCM condition of the flyback converter, and the consideration together with the detailed comparison to another type of single gate driver stack is provided in **Publication V**. Because LT3798 only provides +10 V / 0 V as the output, a circuitry for boosting pulse is added as depicted in the grey part in Fig. 2-9(a), and the driving voltage V_{dd}/V_{ee} of T_4 becomes +20 V / 0 V which is suitable for SiC MOSFET. Besides this, the other colored parts in this self-powered APS including controller powering, DCM detecting, voltage sensing, and current sensing are dedicatedly designed for the normal operation, achieving the anticipated closed-loop control.

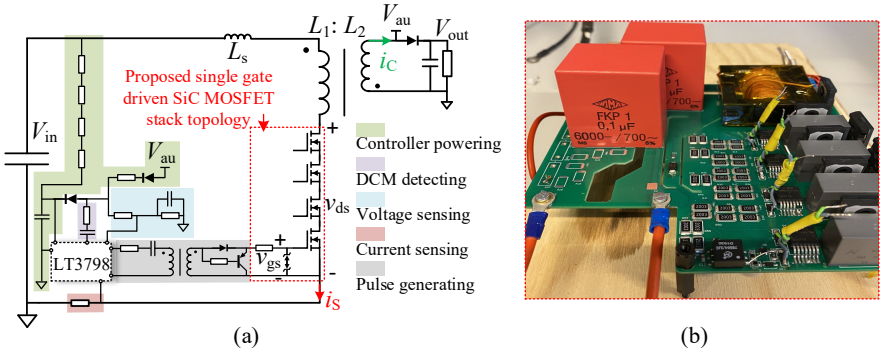


Figure 2-9. The self-powered auxiliary power supply: (a) schematic (b) photograph

Name	Parameter
T_i (i=1~ 4)	C2M1000170J (1.7 kV/5 A)
D_{ai} (i=1~ 4)	PTZ18B (18 V)
D_{bi} (i=1~ 4)	TDZ6_2B (6.2 V)
D_{ci} (i=1~ 3), D_{di} (i=1~ 4)	C5D05170H (1.7 kV/5 A)
R_{si} (i=1~ 4)	500 kΩ
R_{gi} (i=1~ 4)	20 Ω
C_{ai} (i=1~ 3)	47 pF
C_{di} (i=1~ 4)	50 nF

Table 2-1. Parameters of components in the proposed SiC MOSFET stack

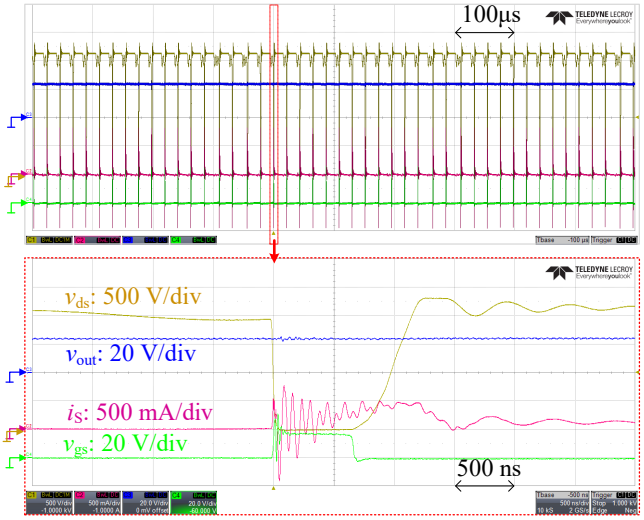


Figure 2-10. Overall performance of the self-powered auxiliary power supply

In the experiments, the parameter setting is listed in Table 2-1. With the expected output voltage V_{out} set as 24 V, the performance of APS under the condition of the input voltage V_{in} = 2 kV is shown in Fig. 2-10, and two oscillations of the voltage v_{ds} across the stack can be observed. Occurrence of the first one is due to devices' output capacitances and the transformer leakage inductance, where the peak value of v_{ds} is

clamped. Occurrence of the secondary one is due to devices' output capacitances and the transformer magnetizing inductance, as the secondary current i_C approaches zero during every switching cycle. With the aid of the DCM detecting circuitry, when v_{ds} rings to its valley, LT3798 sends the signal to turn on the stack in order to reduce the energy loss. It can be observed that v_{ds} abruptly dips to zero from the waveform valley as the gate-source voltage v_{gs} turns to +20 V and i_S increases gradually from zero. After a while, v_{gs} turns back to 0 V and v_{ds} rises to the limiting value.

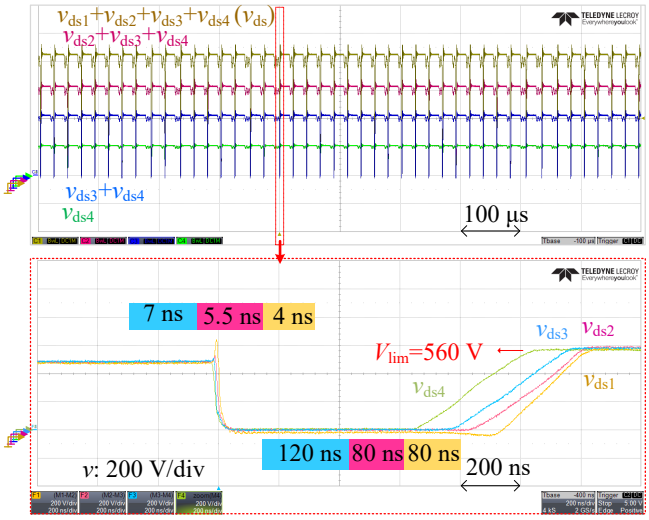
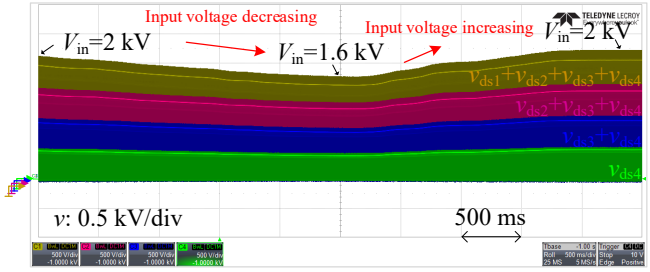
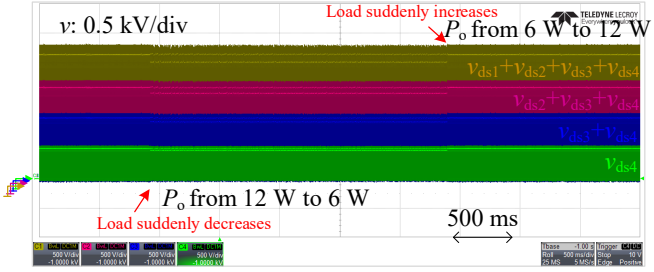


Figure 2-11. Voltage balancing performance of SiC MOSFETs in the proposed stack

For the VB performance in the stack, the results are displayed in Fig. 2-11. During turning-on process, it is observed that v_{ds4} drops firstly, then v_{ds3}, v_{ds2} and v_{ds1} with the sequential delays of 7 ns, 5.5 ns and 4 ns. During turning-off process, v_{ds4} is the first one to rise, followed by v_{ds3}, v_{ds2} and v_{ds1} with the sequential delays of 120 ns, 80 ns and 80 ns. Most importantly, the voltages are limited at 560 V and good VB is performed in the stack. Additionally, Fig. 2-12 further presents the VB during the input voltage transient and output load transient to verify its robustness. As V_{in} is reduced from 2 kV to 1.6 kV and subsequently increased back to 2 kV in Fig. 2-12(a), the voltage across each SiC MOSFET in the stack remains evenly balanced. In Fig. 2-12(b), the output power P_o is abruptly reduced to 6 W from 12 W, and LT3798 makes the adjustment to decrease the switching frequency as the output power becomes lower. Despite this change, the voltages across the SiC MOSFETs remain well balanced. Following this, P_o is abruptly increased back to 12 W, and the switching frequency returns to be a higher value with good VB being observed. These results demonstrate the good performance of the stack under different circumstances.



(a)



(b)

Figure 2-12. Voltage balancing during (a) input voltage transient (b) output load transient

In addition, an experimental comparison is presented to demonstrate the proposed stack' advantages, in comparison to the clamping RCD snubber method and the active delay control method. As previously mentioned, the conventional method for driving T_i ($i = 1 \sim 4$) in the stack necessities individual pulses for driving, resulting in the need for four sets of driving chips with the optic fiber isolations and four sets of isolated power supplies [44]. Despite delicately designing the gate loops to make them as identical as possible, voltage unbalancing still occurs. Adding clamping RCD snubber is considered as an approach for VB without the scarifying of switching speed of SiC MOSFET, besides this, actively adjusting the switching delay which requires the extra voltage feedback design can achieve the same goal. Comparatively, the proposed single gate-driven stack design is significantly simpler and only one set of driving chip, optic fiber, and isolated power supply is required. Hence, under the same testing condition and with the similar VB performance, the loss distributions of above three approaches are compared as shown in Fig. 2-13, and the detail regarding of parameters setting and switching waveforms are presented in **Publication IV**.

It is concluded that, with the clamping RCD snubber method, the losses of four groups are similar as illustrated in Fig. 2-13(a), including T_i turning-on loss, turning-off loss, and R_{di} loss. Importantly, it results in significant R_{di} ($i = 1 \sim 4$) loss since C_{di} discharges through R_{di} during the entire on duration. On the other hand, the active

delay control method significantly reduces the loss comparatively, which is estimated to be 93.07% by adding up, as shown in Fig. 2-13(b). In contrast, the proposed method also significantly reduces the total loss compared to the clamping RCD snubber method as depicted in Fig. 2-13(c), which is estimated to be 89.45%. It should be noticed that, with the proposed method, the turning-on losses of T_2, T_3, and T_4 are similar while larger than T_1 due to the automatic balancing process. Despite that the proposed stack incurs more loss compared to the active delay control method, the loss is not significant, and it is acceptable for high-voltage low-power applications. In return, the proposed stack significantly simplifies the gate driver design as well as the power loop VB design, and it becomes a cost-effective solution.

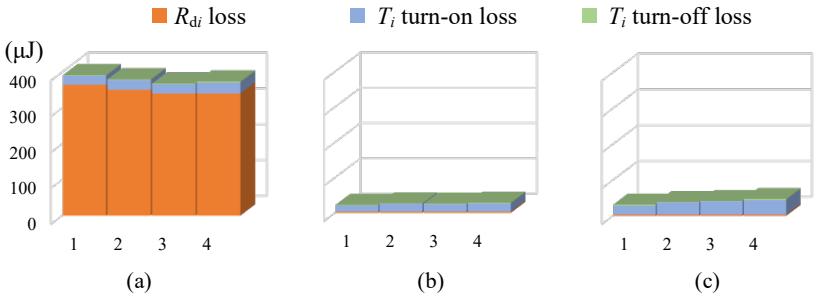


Figure 2-13. Loss distribution results with (a) the clamping RCD snubber method (b) the active delay control method (c) the proposed method

CHAPTER 3. ANTI-SHORT CIRCUIT IMPROVEMENT OF THE SINGLE GATE-DRIVEN STACK

The information in this chapter is based on **Publication II**.

As introduced in Chapter 2, the single gate-driven SiC MOSFET stack offers the merit of being highly compact and low-cost. As a series structure, not only is the normal working principle significant, but also the short-circuit (SC) fault protection is crucial.

For a single SiC MOSFET against SC faults such as fault under load (FUL) and hard switch fault (HSF), extensive research has been conducted on the protection mechanisms. In [45], when SiC MOSFET enters its desaturation region after SC fault occurs, its on-state voltage drop is compared with a threshold to detect the SC fault, and then the protection is actively realized by pulling the driving signal to be "low". Due to the low cost and high robustness of this desaturation strategy, similar designs are commonly seen in various industries, but the requirement of a specific blanking time affects the action timeliness for protection. In [46], inside the SiC MOSFET module, a tunnel magnetoresistance is integrated in the package to directly sense the fault current, which is then regarded as the protection criterion. Additionally, there exist some indirect ways for obtaining the fault current by measuring the change rate of the drain current. For example, in [47], a Rogowski switch-current sensor is designed based on this principle, which is then placed in the power loop as a solution of current measurement. Comparatively, owing to the existence of parasitic inductance between the Kelvin source electrode (if applicable) and the power source electrode of the device, measuring the voltage drop across this inductor is a preferable method to make the estimation. To accomplish the SC fault identification, extra signal processing circuit is further required. In [48]-[49], resistive-capacitive (RC) and resistive-capacitive-diode (RCD) integrator circuits are respectively used to filter this voltage drop, and then the output voltage is compared with a preset threshold voltage. In [50], an additional quantity, the gate-source voltage of device, is further examined to better differentiate between the normal and SC states.

However, implementing the aforementioned SC protection strategies in a SiC MOSFET stack is questionable, since the voltage unbalancing of devices should be taken into consideration when the SC fault occurs [51]. Despite the fact that the short-circuit characteristics and protection of conventional stacks that have separated gate drivers (GDs) have already been studied [52]-[53], there has not been much research on the characteristics and protection in the occurrence of SC faults in single gate-driven stacks. Therefore, it is intensely valuable to fill this gap.

3.1. SHORT-CIRCUIT CHARACTERISTIC ANALYSIS OF THE SINGLE GATE-DRIVEN STACK

On the basis of the illustrated single gate-driven SiC MOSFET stack with associated clamping VB circuits depicted in Fig. 2-2, the simulated waveforms with the aid of LTspice software are shown to elaborate the SC mechanism of the stack when the FUL occurs. As presented in Fig. 3-1, it includes three working stages as follows.

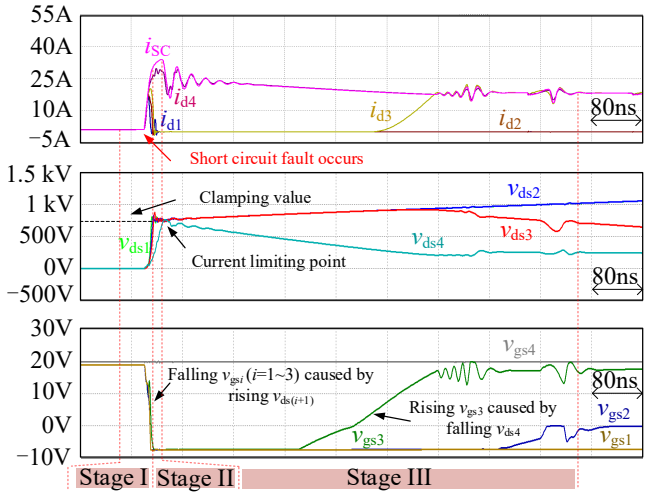


Figure 3-1. Simulated waveforms of the single gate-driven stack in the FUL occurrence

Stage I: The stack functions as usual with a low current i_{SC} flowing through it in the beginning. However, when a SC fault occurs in the load side of some pulsed power application, i_{SC} experiences a sudden and significant increase. As T_i (i = 1 ~ 4) enters its saturation region, v_{dsi} gets increased drastically. This relationship can be expressed as [54]-[56]:

$$i_{SC} = f(v_{gsi}, v_{dsi}, T_j) = f_1(v_{gsi}) \cdot f_2(T_j) \cdot \frac{p(v_{gsi}) \cdot v_{dsi}}{1 + q(v_{gsi}) \cdot v_{dsi}} \tag{3-1}$$

where $f_1(v_{gsi})$ stands for the transfer characteristic parameter of device, $f_2(T_j)$ stands for the parameter which indicates the influence of junction temperature T_j on i_{SC}, and $p(v_{gsi})$ and $q(v_{gsi})$ stand for the output characteristic parameters of device.

During this interval, the increasing of $v_{ds(i+1)}$ will lead to the decreasing of v_{gsi} (i = 1 ~ 3), which is similar to the working principle of the stack during the turning-off

process. As a consequence, T_4 will stay in the saturation region to prevent the increase of i_{SC}, while T_i (i = 1 ~ 3) will enter the cut-off region.

Stage II: As T_i (i = 1 ~ 3) is gradually turned off, when v_{dsi} (i = 1 ~ 3) exceeds the voltage of the clamping capacitor C_{di}, i_{SC} will commute to the clamping circuit. Correspondingly, the current i_{di} (i = 1 ~ 3) which flows through T_i will decrease to zero. Consequently, this feature causes T_i (i = 1 ~ 3) only to tolerate a short time duration of SC (the time span in this simulation is less than 20 ns). Benefiting from the clamping circuit, the voltage unbalancing of v_{dsi} (i = 1 ~ 3) during the dynamic transient can be avoided despite the turning-off inconsistency by using single GD. Therefore, v_{dsi} (i = 1 ~ 3) will increase slowly afterwards, where the increasing rate is determined by C_{di} the clamping capacitor and it is obtained as:

$$\frac{v_{dsi}}{dt} = \frac{i_{SC}}{C_{di}/3} \tag{3-2}$$

Instead, since T_4 remains in its saturation region, v_{ds4} increases as i_{SC} goes up according to Eq. (3-1). At the end of this stage, i_{SC} reaches its maximum value.

Stage III: Despite T_4 is turned on, T_i (i= 1~ 3) should be turned off in an automatic way. Since T_i (i= 1~ 4) is in a series stack, the SC current will start to decrease, which also represents the start of this stage. Eventually, T_1, T_2 and T_3 should be capable to withstand the total bus voltage V_{in} and cut off the SC current, which illustrates the potential capability of the single gate-driven stack to limit SC current.

However, v_{ds4} also gets decreased as i_{SC} decreases since T_4 is still in the saturation region. It will result in the increase of v_{gs3} again, followed by the turning on of T_3 and increasing of i_{d3}. After that, the increasing of v_{gs2} can also occur. As a result of this unstable state, v_{dsi} (i = 1~ 4) will oscillate severely, and T_1 could eventually withstand an unacceptably high voltage which violates the reliable functioning.

3.2. ANTI-SHORT CIRCUIT IMPROVEMENT OF THE STACK

According to the above conclusion, despite that the single gate-driven stack can limit the overcurrent temporarily, it would be destroyed afterwards if no additional measure is taken. Therefore, an improvement can be made based on the assumption as: if v_{gsi} (i = 1~ 3) could remain negative after its state is changed by the SC fault, the stack's advantageous potential of limiting the overcurrent could be fully unlocked.

For purpose of accomplishing this target, the following principle can be derived as: in the normal working condition, C_{a3} in the stack for driving T_3 should sustain energy as normal, as depicted in Fig. 2-2 and described in Chapter 2; However, in the SC fault condition, C_{a3} should sustain only a minimal or negligible amount of energy, and it would fail in turning on T_3 during the current limiting process. Consequently,

based on the above, an improved SiC MOSFET stack is proposed based on the single gate driver, and the full topology is depicted in Fig. 3-2.

Compared to the original stack presented in Fig. 2-2, the improvement is made as: in the gate loop of T_3, a varistor R_V and an auxiliary low-power MOSFET T_{aux} are added, where R_V is placed in series with R_{g3} and T_{aux} is placed in parallel with C_{a3}. When the SC fault occurs, a low impedance loop for C_{a3} can be provided by turning on T_{aux} to release the capacitor energy storage. While in the meantime, the stack's normal switching process is not influenced. As follows, its working principle with the improved part will be illustrated respectively under normal condition, the FUL condition and the HSF condition.

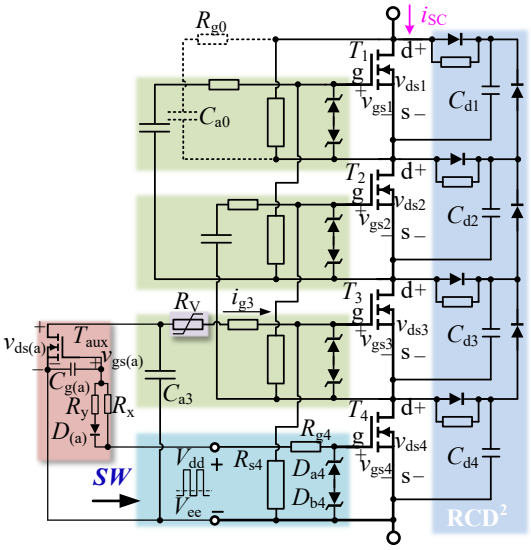


Figure 3-2. Topology of the improved single gate-driven SiC MOSFET stack

3.2.1. WORKING PRINCIPLE OF THE IMPROVED STACK

The normal condition: By setting the turning-on signal of T_{aux} lagging T_4 by Δt_1, C_{a3} will work as normal as analyzed in Chapter 2 which provides enough driving power for the turning-on of T_3, as depicted in Fig. 3-3(a). As an implementation, Δt_1 can be adjusted by adding the gate turning-on resistor R_x and the gate capacitor $C_{g(a)}$ as:

$$\Delta t_1 = R_x (C_{g(a)} + C_{iss(a)}) \ln \frac{V_{ee} - V_{dd}}{V_{th(a)} - V_{dd}} - R_{g4} C_{iss(4)} \ln \frac{V_{ee} - V_{dd}}{V_{th(4)} - V_{dd}} \tag{3-3}$$

where $C_{iss(a)}$ and $C_{iss(4)}$ stand for the input capacitances of T_{aux} and T_4, respectively, $V_{th(a)}$ and $V_{th(4)}$ are their threshold voltages.

As v_{ds4} decreases to zero during the turning-on process, v_{gs3} becomes equal to V_{dd}. In contrast, the gate-source voltage $v_{gs(aux)}$ of T_{aux} increases to $V_{th(a)}$ at a significantly lower speed. When T_{aux} is fully turned on, the discharging loop on the gate side of T_3 will still not be formed since V_{dd} is smaller than the maximum continuous voltage of the chosen R_V, and thus v_{gs3} remains in the original state.

When the turning-off signal is received, the turning off of T_{aux} leads T_4 by Δt_2, and thus it will not influence the energy storage of C_{a3} when v_{ds4} is increasing. In the implementation, Δt_2 is adjusted according to the added gate turning-off resistor R_y and $C_{g(a)}$, and a diode $D_{(a)}$ is added to separate the turning-on and turning-off gate loops. As long as the impedance in parallel with C_{a3} becomes high beforehand, C_{a3} will sustain sufficient driving energy as usual during the turning-off process, so that the next normal turning-on process is ensured.

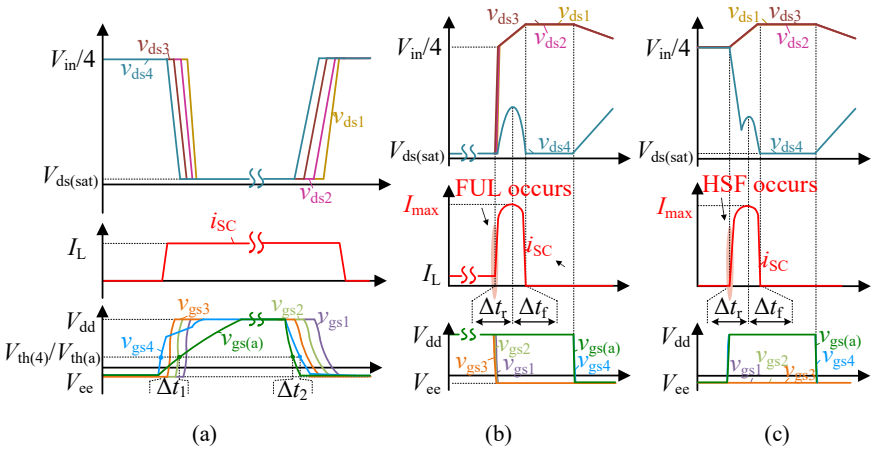


Figure 3-3. Working process of the improved stack in (a) normal (b) FUL (c) HSF conditions

The FUL condition: As depicted in Fig. 3-3(b), i_{SC} is equal to the load current I_L in the beginning, and the stack operates in its normal on-state. With a sudden occurrence of the SC fault, i_{SC} is increased rapidly, followed by the increasing of v_{dsi} ($i = 1 \sim 4$). As analyzed above, the increasing of v_{dsi} ($i = 2 \sim 4$) triggers the discharging in the gate loop of T_i ($i = 1 \sim 3$) and results in v_{gsi} decreasing to V_{ee}. Since the switching signal is "1", v_{gs4} and $v_{gs(a)}$ remain V_{dd}. Therefore, only T_4 is turned on while others are turned off, leading to the action of automatic turning-off. After a time interval defined as Δt_r, i_{SC} increases to the maximum value I_{max} from I_L. Afterwards, after another time interval Δt_f, i_{SC} decreases to zero.

Different from the description in Section 3.1, when i_{SC} is increasing, C_{a3} can not sustain the energy storage, since T_{aux} is turned on and the impedance in parallel with C_{a3} becomes low when the FUL occurs. Actually, R_V and T_{aux} provides an extra current flow branch for i_{SC}, which prevents the formation of the gate loop charging of T_3 during the decrease of v_{ds4}. As a result, v_{gs3} remains negative. Eventually, the fact that v_{dsi} ($i = 1 \sim 3$) becomes equal to $V_{in}/3$ when both v_{ds4} and i_{SC} approaches zero, shows that the improved stack has the anti-FUL capability as desired. Moreover, when the switching signal *SW* is actively changed to "0" after the SC fault is cleared, v_{gs4} and $v_{gs(a)}$ will turn negative, causing v_{ds4} to increase and v_{dsi} to decrease gradually. Finally, v_{dsi} ($i = 1 \sim 4$) returns back to $V_{in}/4$.

The HSF condition: As depicted in Fig. 3-3(c), the SC fault has already occurred when *SW* is "0", and it results in a rapid increase of i_{SC} when *SW* is changed to "1". In this case, v_{ds4} decreases significantly slower compared to that during the normal turning-on process. As $v_{gs(a)}$ increases to V_{dd} from V_{ee}, T_{aux} enters to the triode region from the cut-off region, the energy stored in C_{a3} is therefore released. Therefore, when v_{ds4} is decreasing, the charging in the gate loop of T_3 is not formed as well, and v_{gs3} remains to be V_{ee}. Further, T_1 and T_2 are not turned on either as T_3 is not turned on. As a result, the improved stack can be automatically turned off, leaving v_{gsi} ($i = 1 \sim 3$) as V_{ee} while remaining v_{gs4} and $v_{gs(a)}$ as V_{dd}. It is worth noting that, since the parasitic inductance L_σ of the power loop exists in real application, v_{ds4} falls drastically at first, resulting in the instantaneous turning-on of T_3 before $v_{gs(a)}$ reaches $V_{th(a)}$. Once T_{aux} is turned on, the discharging in the gate loop of T_3 is formed, and T_3 is turned off immediately. Due to its extremely short duration, this research refers to it as a "fake switching process", and as a result, v_{ds4} does not decrease to zero in a smooth way as indicated in Fig. 6(b).

Using the same definition in the FUL condition, after Δt_r, i_{SC} increases to I_{max}, and after another Δt_f, i_{SC} decreases to zero. Therefore, the improved stack also has the anti-HSF capability as v_{dsi} ($i = 1 \sim 3$) is equal to $V_{in}/3$ when both v_{ds4} and i_{SC} approaches zero.

3.2.2. SIMPLIFIED MODEL OF ANTI-SHORT CIRCUIT FAULT PROCESS

As a summary of the above working principle, through analyzing and unlocking the potential of overcurrent limitation, the original single gate-driven SiC MOSFET stack gets improved to possess strong capabilities of anti-short circuit fault.

In the meantime, it is also found that despite the SC current is cut off automatically in the SC fault occurrence as T_i ($i = 1 \sim 3$) is turned off immediately, the high SC current will still mostly flow through T_4 for a certain time duration and there is a possibility of breaking down. Hence, during the process of anti-short circuit fault, the potential safety issue exists in T_4, which makes it necessary to estimate I_{max}, Δt_r and Δt_f for ensuring the safety and reliability of the improved SiC MOSFET stack. Consequently, based on the involved components during the process of anti-short circuit fault, an

equivalent circuit model can be built to make the estimation. Besides, to simplify the model, the rapid v_{dsi} (i=1~ 3) increasing process in the FUL occurrence is neglected, and the "fake switching process" in the HSF occurrence is neglected as well.

The components that make up this model are depicted in Fig. 3-4(a). The voltage excitation across T_4 in the real circuitry is represented by a voltage source V_m being equal to $V_{in}/4$. The inductor L_m and the resistor R_m stand for the loop inductance and resistance respectively. Since the SC current flows through the clamping capacitor C_{clamp} of T_i (i =1~ 3) during the process of anti-short circuit fault, three capacitors can be considered as in series-connection, and it can be represented by a capacitor C_m which is equal to $C_{clamp}/3$. Moreover, the current source i_{eq} represents the overall behavior in the saturation region of T_4 together with the parts in parallel, which can be expressed as:

$$i_{eq} = f(v_{eq}, T_j) = f_2(T_j) \cdot \frac{a \cdot v_{eq}}{1 + b \cdot v_{eq}} \tag{3-4}$$

where the voltage of this current source is denoted as v_{eq}. Since v_{gs4} remains to be V_{dd} during the entire process, compared to Eq. (3-1), i_{eq} is only relevant to T_j and v_{eq} in Eq. (3-4). Further, fitting I-V characteristic curve helps to identify parameters a and b.

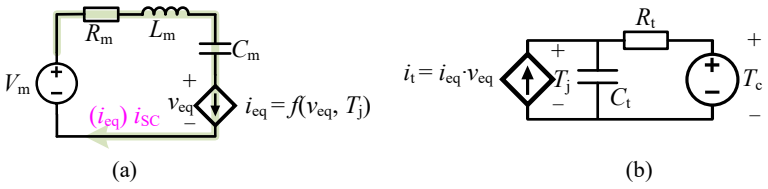


Figure 3-4. (a) simplified anti-short circuit fault model (b) thermal model

To accurately model the process of anti-short circuit fault, the thermal effect of the high SC current on the junction temperature must be considered, as presented by $f_2(T_j)$. As two frequently used junction-to-case thermal models, the complexities of Cauer and Foster RC networks increase as their orders rise [57]-[58]. Thus, only one thermal Resistor-Capacitor (R_tC_t) unit is used for simplification, as depicted in Fig. 3-4(b), and the relationships shown below exist based on the aforementioned:

$$\begin{cases} C_t \cdot dT_j / dt + (T_j - T_c) / R_t = i_t = i_{eq} v_{eq} \\ v_{eq} + v_{Cm} + v_{Lm} + i_{eq} \cdot R_m = V_m \\ v_{Lm} = L_m \cdot di_{eq} / dt \\ i_{eq} = C_m \cdot dv_{Cm} / dt \end{cases} \tag{3-5}$$

where v_{Cm} and v_{Lm} are the voltages of C_m and L_m respectively, the power dissipation of i_{eq} during the process of anti-short circuit fault is represented by the current source i_t, and the case temperature is shown by the voltage source T_c.

By fitting experimental data, it is possible to determine the relationship $f_2(T_j)$ and other unknown parameters in Eq. (3-4) and Eq. (3-5). Consequently, I_{max}, Δt_r and Δt_f can also be estimated as a result of solving i_{eq} to estimate i_{SC}, providing the design guideline of this improved single gate-driven stack. To confirm the effectiveness and validate the capability of anti-short circuit fault, the solved i_{eq} together with estimated parameters will be compared with the results from the experiments in the following section.

3.3. EXPERIMENTAL RESULTS OF ANTI-SHORT CIRCUIT FAULT PERFORMANCE

As the schematic of main circuitry depicted in Fig. 3-5(a), the improved SiC MOSFET stack is tested in a pulsed power application for the experiments. Based on that, the experimental setup is established, as presented in Fig. 3-5(b). To evaluate the anti-short circuit fault performance, a high voltage Insulated Gate Bipolar Transistor (IGBT, IXEL40N400), which is controlled by a digital signal processor (DSP), is placed in parallel with the load inductor L (30 mH) for emulating the SC faults. Since it is a single pulse test, the SC current i_{SC} is measured using a Pearson probe (Model 2877) to ensure the measurement precision. To further measure the voltage, the differential probe (HVD3605A) is used.

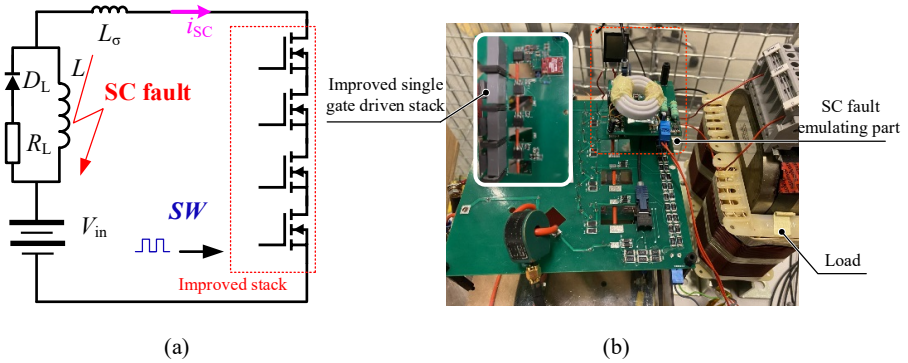


Figure 3-5. Testing platform of the improved stack: (a) schematic (b) photograph

Additionally, Table 3-1 includes a list of the essential components of the improved SiC MOSFET stack that are calculated theoretically and with the help of simulation.

During one switching cycle, v_{dsi} (i= 1~ 4) and i_{SC} of the SiC MOSFET stack under the normal condition of V_{in} = 3 kV are shown in Fig. 3-6. As *SW* is set to "1" from "0", the stack is turned on, and then i_{SC} increases gradually from zero. After a time duration of 20 μs, the signal is set back to "0" from "1", and the stack is turned off while i_{SC} decreases to zero. During the process, the good VB of four SiC MOSFETs can be observed, which proves that the improved stack's normal working process is not influenced. Besides, by combining with the parasitic capacitance which exists in parallel with the load, the large *dv/dt* of the stack during the turning-on process causes a considerable "positive overshoot" of i_{SC}. In the meantime, the small *dv/dt* during the turning-off process causes a small "negative overshoot" of i_{SC}.

Name	Parameter
T_i (i=1~ 4), T_{aux}	C2M1000170D (1700 V/5 A), STD2N105K5
D_{ai}, D_{bi} (i=1~ 4)	PTZ20B (20 V), TDZ6_2B (6.2 V)
R_{gi}, R_{si} (i=1~ 4)	25 Ω, 500 kΩ
R_{g0}, C_{ai} (i=0~ 3), R_V	25 Ω, 47 pF, 2*AVRH10C270150NA8
R_x, R_y, $C_{g(a)}$, $D_{(a)}$	100 Ω, 3.3 Ω, 1 nF, 1N4148W
RCD[2] circuit	50 kΩ, 56 nF, C5D05170H (1700 V/5 A)

Table 3-1. Parameters of components in the improved SiC MOSFET stack

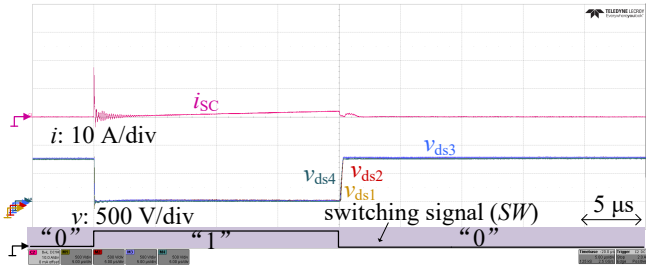
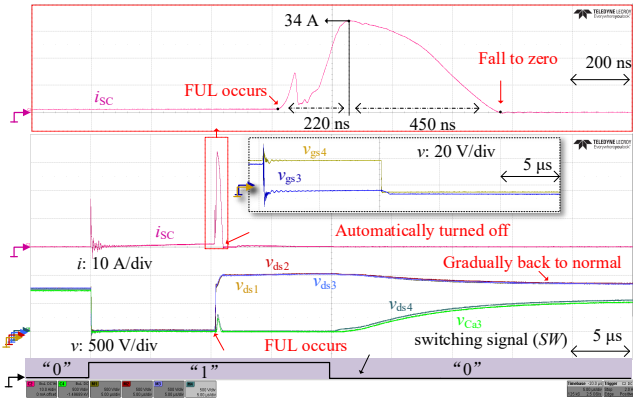


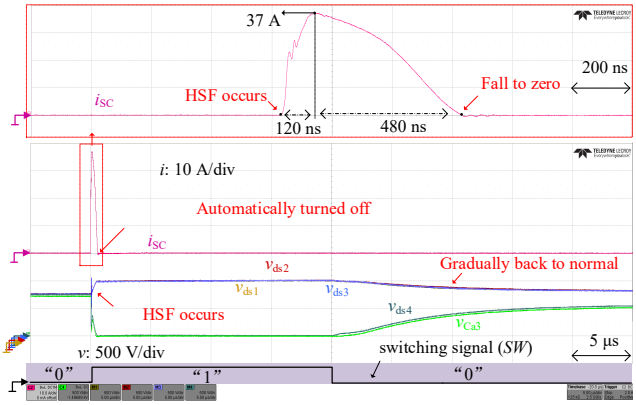
Figure 3-6. Performance of the improved stack in the normal condition

By contrast, Fig. 3-7(a) and Fig. 3-7(b) respectively show the results in the FUL and HSF conditions, where v_{dsi} (i = 1 ~ 4) and i_{SC} is recorded with the same *SW* signal in both conditions and the protection circuit is not provided. In Fig. 3-7(a), as "1" is received, i_{SC} increases slowly. After 10 μs, the SC fault occurs suddenly, and i_{SC} increases abruptly. Consistent with the analysis, T_3 is turned off as v_{gs3} decreases to -5 V, followed by T_2 and T_1 consequently, while T_4 remains in its saturation region as long as v_{gs4} is kept at +20 V. Under the actions of R_V and T_{aux}, C_{3a} is unable to sustain

sufficient energy storage as the voltage v_{Ca3} across C_{3a} is following v_{ds4}. As a result, after 220 ns, i_{SC} increases to 34 A, and then i_{SC} is constrained. After another 450 ns, i_{SC} approaches zero as expected. It indicates the automatic turning-off feature of the stack, demonstrating the improved stack's capability of anti-FUL. In Fig. 3-7(b), the SC fault occurs beforehand. When *SW* is changed to "1", i_{SC} increases abruptly from zero. i_{SC} reaches 37 A after 120 ns and gets constrained. Afterwards, after another 480 ns, i_{SC} decreases to zero, which also demonstrates the stack's capability of anti-HSF.



(a)



(b)

Figure 3-7. Performance of the improved stack in the (a) fault under load and (b) hard switch fault conditions

After the occurrence of FUL or HSF, T_1, T_2 and T_3 equally endure the whole bus voltage as it can be observed that v_{dsi} ($i = 1 \sim 3$) is equal to 1 kV, and the excellent VB is also observed in both situations. In the event that *SW* returns to "0", v_{dsi} ($i = 1 \sim 3$)

returns to normal value gradually, and finally T_1, T_2, T_3 and T_4 equally endure the whole bus voltage as it can be observed that v_{dsi} (i = 1 ~ 4) returns back to 750 V gradually.

The experiments were carried out with V_{in} ranging from 1.0 kV to 3.0 kV, and in each case, both the anti-short circuit fault and good VB performances were obtained, which proves the improved stack's robustness. Next, the estimated results of i_{SC} are compared with the recorded i_{SC} in all the experimental cases, so that the simplified model can be verified.

Identification of the simplified model's parameters: an experiment is conducted to collect data for the purpose of fitting and further identifying the parameters in Eq. (3-4) and Eq. (3-5): based on Fig. 3-2, T_4 and T_{aux} are kept constant on by setting v_{gs4} and $v_{gs(a)}$ equal to V_{dd}, whereas T_i (i= 1 ~ 3) is kept in off-state as the gate and source electrodes of device are short-circuited. Therefore, when the modified stack is connected to a DC voltage source V_{in}, the transient behavior can be recorded under lower voltage cases by oscilloscope, and the test results of v_{ds4} and i_{SC} are used to approximate v_{eq} and i_{eq} in Fig. 3-4(a).

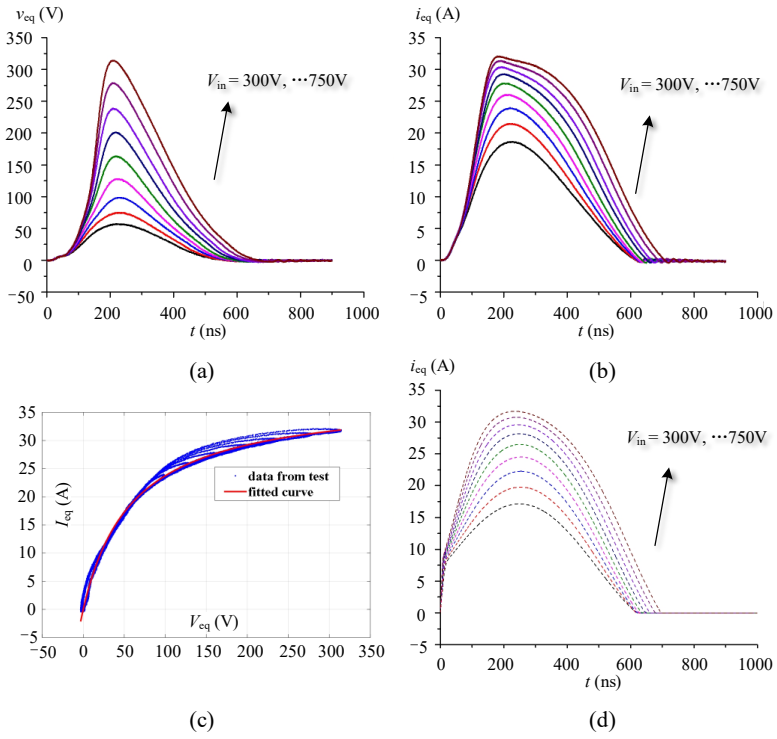


Figure 3-8. (a) measured v_{eq} (b) measured i_{eq} (c) I-V characteristic fitting (d) solved i_{eq}

As shown in Fig. 3-8(a) and Fig. 3-8(b), respectively, v_{eq} and i_{eq} under various voltage instances (V_{in} = 300 V, …750 V) are achieved in this way. It is discovered that despite i_{eq} and v_{eq} get increased as V_{in} increases, their relationship is not linear. the relationship between v_{eq} and i_{eq}, also named as the I-V characteristic curve, is generated with a fitting tool by importing those experimental data, as illustrated in Fig. 3-8(c). It can be seen that some data points are above the fitted curve in addition to others being along the curve, indicating that the junction temperature T_j has an effect on the I-V characteristic. Afterwards, by fitting the current curves in Fig. 3-8(b), the remaining unknown parameters can be determined. Finally, the simplified model can be derived, and Fig. 3-8(d) presents the solved current curves. Based on the foregoing, the estimated SC current i_{SC} of experiments under the occurrence of SC faults is calculated using the solved current i_{eq} as follows.

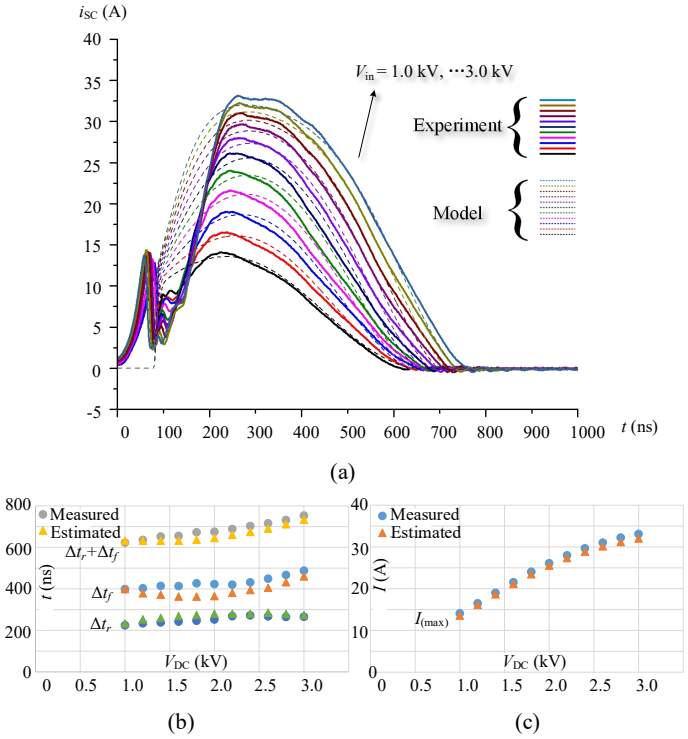


Figure 3-9. Comparisons between experiment and simplified model in the FUL condition (a) i_{SC} (b) Δt_r, Δt_f, $\Delta t_r+\Delta t_f$ (c) $I_{(max)}$

Estimation in the FUL occurrence: in Fig. 3-9(a), in the FUL occurrence of this stack, the comparison results from both the experiment and the established model are displayed. Since the anti-FUL process's rapidly increasing process of v_{dsi} (i = 1 ~ 3)

is ignored by this simplified model, it is shown that their initial stages diverge. To compensate this influence, the parameters of model are fine-tuned as illustrated in detail in **Publication II**.

Since the goal of the established model is to make estimations for I_{max}, Δt_r, and Δt_f, it will be sufficient to assess the safety and reliability of the improved stack, rather than trying to make the solved i_{SC} and the real i_{SC} in an excellent agreement. As a result, using the data in Fig. 3-9(a), Fig. 3-9(b) displays both the measurement and estimation results of Δt_r, Δt_f, $\Delta t_r+\Delta t_f$ in various V_{in} instances, and Fig. 3-9(c) displays the corresponding results of I_{max}. It is seen that the estimations and measurements of Δt_r and Δt_f differ slightly, but the deviation of $\Delta t_r+\Delta t_f$ is limited within 50 ns. In the meantime, the deviation of I_{max} is also limited within 2 A. It indicates that the anti-FUL process of the improved stack is well predicted by the simplified model.

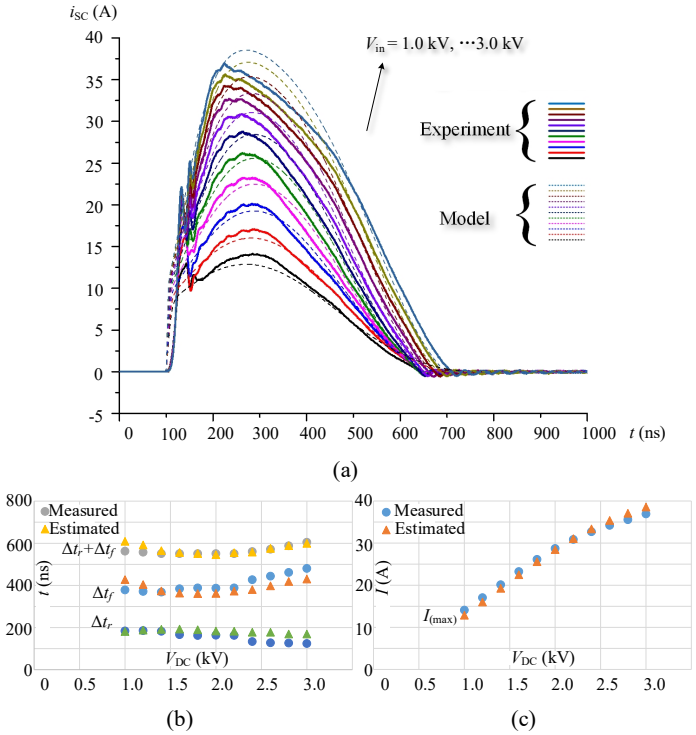


Figure 3-10. Comparisons between experiment and simplified model in the HSF condition (a) i_{SC} (b) Δt_r, Δt_f, $\Delta t_r+\Delta t_f$ (c) $I_{(max)}$

Estimation in the HSF occurrence: In Fig. 3-10(a), in the HSF occurrence, the comparison results from the experiment and the established model are displayed.

Although the estimations and measurements of curves also differ to a certain degree for the reason of this model's simplification, the trends remain to be consistent. Further, based on the data in Fig. 3-10(a), the measurement and estimation results of Δt_r, Δt_f, $\Delta t_r+\Delta t_f$, I_{max} are provided in Fig. 3-10(b) and Fig. 3-10(c). The variance of $\Delta t_r+\Delta t_f$ is found to be limited within 40 ns, in the meanwhile, the deviation of I_{max} is limited within 2 A, demonstrating that the anti-HSF process of this stack is well predicted as well by the simplified model.

CHAPTER 4. A SELF-POWERED GATE DRIVER WITH CONVERTER-BASED DESIGN

The information in this chapter is based on **Publication III**.

By contrast to MMC which has intrinsic submodule capacitor to facilitate the self-powered auxiliary power supply (APS) design, the effective way to ease the common mode (CM) noise and isolation burden of gate drivers (GDs) for direct series-connection is self-powered GD design, as its comparison with conventional GD design is presented in Fig. 4-1. Besides, the self-powered GD design is also suitable for some cases in the flying capacitor indirect series-connection, etc.

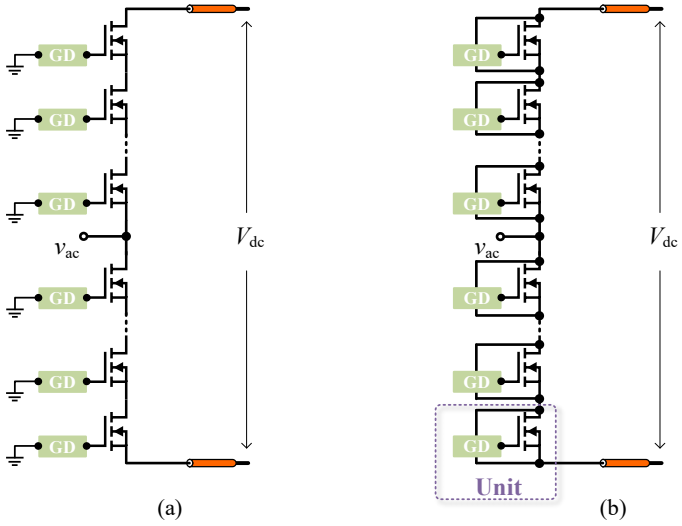


Figure 4-1. Direct series-connection with the (a) conventional (b) self-powered gate driver

As depicted in Fig. 4-1(b), the self-powered GD directly extracts the power from the two power loop terminals of the device. Yet so far it has just been realized in a number of different approaches for thyristors, also some MOSFETs and IGBTs with lower voltage rating. The GD in [59]-[60] is powered by a modified snubber circuit that functions as a linear regulator, but the major flaw lies in its low efficiency. Resonant circuits are further fitted in [61]-[63] to store extra power for the GD to increase the efficiency, and they capitalize on the benefits of the power devices'

dynamic switching property. Using additional transistors to construct the auxiliary circuits can also realize the same function as in [64]-[65]. Unfortunately, because they could only give a small amount of quiescent power, they are not suitable for more advanced GDs which require higher quiescent power. In order to power the GD of the gate-commutated thyristor (GCT) as in [66], based on the RC snubber circuit of the GCT, a two-stage converter is integrated in the snubber loop. Although in the GCT's quiescent state, dynamic current pulses are not created either to charge the supply of GD, the static snubber currents will have low magnitudes in the applications of current source rectifiers, which nonetheless help to manage the charging. Further, a promising floating supply method is suggested in [67]. It can supply enough driving power by using a clamping snubber circuit across each IGBT and connecting a commercial DC to DC converter to generate power. However, in series-connection applications, the characteristic of constant-power-load of the commercial product, can result in static voltage unbalancing of devices. Therefore, additional auxiliary circuits are required as well as the modulation techniques are needed to make up for it, which constrains the scalability.

As for MV SiC MOSFETs, the "self-powered" GD designs for them are still unknown, since the corresponding GDs described in prior publications are on the basis of the "external-powered" approach.

4.1. COMMON MODE NOISE ANALYSIS OF GATE DRIVER

To better understand the advantage of self-powered approach regarding of common mode noise issue, with the configuration of directly series-connected power devices, a bidirectional DC to DC converter is taken as an example, as depicted in Fig. 4-2. Targeting at 10 kV DC bus voltage V_{dc}, 10 kV SiC MOSFETs is chosen as S_i (i = 1 ~ 4) by considering the design margin. The power loop is connected to a large inductor L, which is subsequently connected to a battery V_b.

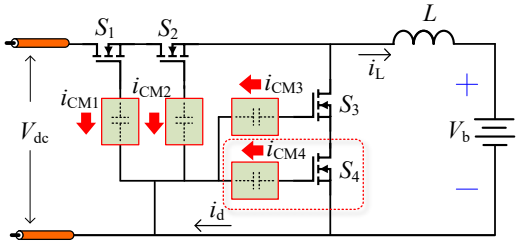


Figure 4-2. Common mode noises indication of a bidirectional DC to DC converter

As for crucial GDs as the research focus in this thesis, an external grounded power supply is configured to provide their power as in the conventional way, which is

indicated in Fig. 1-1. In this instance, the withstanding voltage of GD, that is, the voltage difference between its primary and secondary sides, hits V_{dc} when S_1 and S_2 are turned on. As a result, both the signal and power transfer stages of GD must be isolated with V_{dc}. Additionally, the parasitic capacitances that exist in those stages should be given the consideration, since both of them contribute to CM noises. In the signal isolation stage, the utilization the optic fiber connector can make the parasitic capacitance negligible, and thus the parasitic capacitance in the power isolation stage, which could come from the isolated power supply specifically, is the main issue.

By analyzing the charging process from V_{dc} to V_b, the shown bidirectional DC to DC converter acts like a buck converter. In this manner, the large voltage variation *dv/dt* at switching nodes that occur during the switching transients of S_1 and S_2 can be regarded as noise sources which cause the emergent CM currents. Next, with the aid of LTspice, a simulation is conducted to help present the induced CM interference and provide a clear illustration of the phenomenon.

The parameter values are chosen as: L = 30 mH, V_b = 800 V, and V_{dc} = 10 kV. In addition, S_i (i = 1 ~ 4) is replaced by the established LTspice simulation model of 10 kV SiC MOSFET, which was created and verified in [68]. In accordance with the commercial product as the advanced isolation power supply in [69], the gate driver's parasitic capacitance from the device to the ground is set as 15 pF. Theoretically, this commercial isolated power supply is only advised for the GD designs of low-voltage SiC MOSFETs. By combining with the proposed self-powered design, it will become applicable for 10 kV SiC MOSFET, and the demonstration will be provided in the following section. As a basis for analysis, it is set up in an external-powered manner in the current instance.

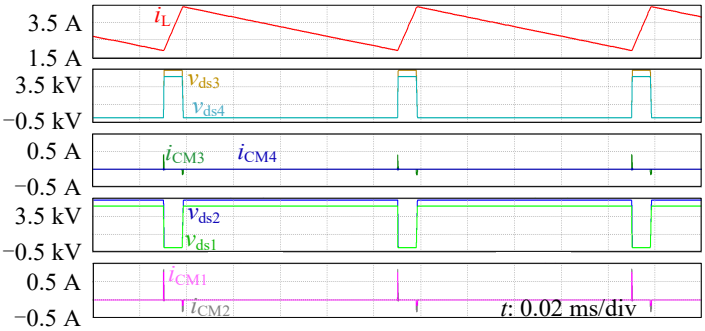


Figure 4-3. Simulation results of common mode noises when running

The simulation result based on the above setting are shown in Fig. 4-3. Controlled by the switching actions of devices, the load current i_L gets increased and decreased

accordingly. During the switching transient, the CM current i_{CMi} (i = 1 ~ 4), which flows via the individual GD of S_i (i = 1 ~ 4), can be observed. Specifically, since the highest *dv/dt* occurs at the middle point, i_{CM2} is the largest, and then i_{CM1} and i_{CM3} follows, while i_{CM4} is always kept zero. Considering the interferences to the control signals of GDs, the CM currents must be reduced. Under extreme circumstances, they might result in the failure of GDs and driven power devices. Besides this, the impact of i_{CMi} on VB of the drain-source voltage v_{dsi} (i = 1 ~ 4) of S_i is also concerned. By utilizing the identical model in this simulation, the difference of S_i is neglected. Also, other driving parameters are preset as the same. As a result, observed from Fig. 4-3, it is demonstrated that the voltage unbalancing between v_{ds1} and v_{ds2} (v_{ds3} and v_{ds4}) can be caused by the difference between i_{CM1} and i_{CM2} (i_{CM3} and i_{CM4}).

Consequently, in order to lessen the detrimental effects brought on by CM noises, an improved design of GD is crucial. In contrast, adopting a self-powered GD can realize the CM noise elimination since it does not require the external power source, and it benefits the integration of the device and GD into a unit, which will be shown next along with the suggested self-powered GD design.

4.2. STRUCTURE OF THE SUGGESTED SELF-POWERED GATE DRIVER WITH CONVERTER-BASED DESIGN

Among various snubber circuits, the clamping snubber circuit, which works to absorb the overshoot of S_1 (S_2) during the switching transient while not affecting the initial switching speed, is considered as a good option for fast switching SiC MOSFET. The clamping function is realized by the capacitor C with a stable voltage across it when the converter is continuously running. Additionally, voltage balancing (VB) of S_1 and S_2 during the static state can be realized with the resistor R and diode D in this case.

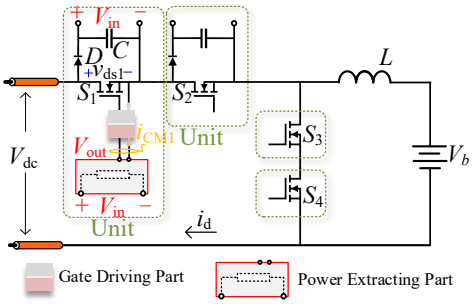


Figure 4-4. Overall configuration of the self-powered gate driver with converter-based design

Typically, the resistor dissipates the majority of the absorbed energy with the adopted clamping RCD snubber. Instead, since the snubber circuit shares the same

voltage potential with the power device, part of the energy lost in the snubber could be recycled to power the GD. Therefore, in the proposed design shown in Fig. 4-4, R is swapped out for a designed power extracting part in the proposed converter-based self-powered GD design, which extracts energy from C to power the gate driving part. Since the GD does not require the switching of the driven device, it has access to sufficient quiescent and dynamic power. Also, since the GD does not need an external power source, it significantly simplifies the high voltage isolation design, where the isolation requirement of the GD changes from V_{dc} to a single unit's voltage. Moreover, the CM current of GD that flows to the ground is eliminated. Therefore, the designed unit is suitable for series-connection, rather than thinking about a redesign to fit the voltage rating.

The gate driving part of this converter-based self-powered GD in Fig. 4-4 is rather easier to develop compared to external-powered GD, since its isolation and common mode immunity capabilities are not required as already indicated. However, such a power extracting part brings other difficulties with its design:

(1) Given that voltage V_{in} of the clamping capacitor could be up to 5 kV while output voltage V_{out} of the power extracting part is only around 20 V in this application, how should the topology and switching device be selected?

(2) How to start this power extracting converter?

(3) If this converter performs like a commercial DC to DC converter with the constant-power-load characteristic, it will cause voltage unbalancing issue of the series connected units in the static state, and how to solve it?

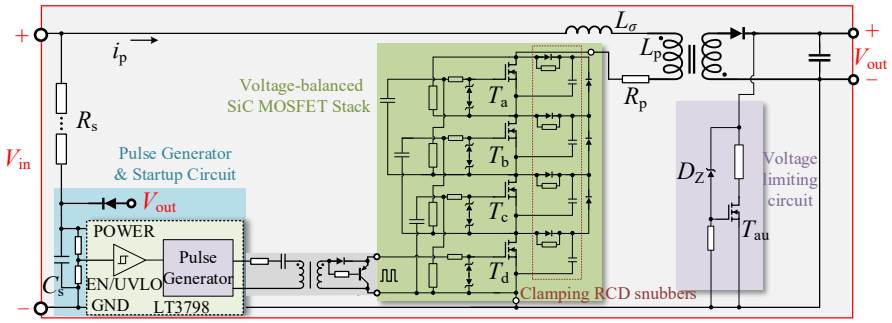


Figure 4-5. Detail of the power extracting part

On the basis of the aforementioned considerations, Fig. 4-5 provides the detail of the designed power extracting part, and the appropriate resolution to above difficulties are given as follows:

(1) For the simplicity of the flyback converter, it is chosen as the fundamental topology. However, considering the high cost of using a low-power device with the same high-voltage rating as the driven device in the design, four low-voltage and low-power SiC MOSFETs are directly series-connected as the primary switch. The applied SiC MOSFET stack combines the benefits of the automatic VB snubber circuit and the single gate driver, as already described in Fig. 2-2 in Chapter 2, and it is highly appropriate for this flyback converter featuring high-voltage and low-power.

(2) A high resistance resistor-capacitor circuit is employed to store energy in the capacitor, and the stored energy through the voltage hysteresis function is sufficient to supply startup of the flyback converter.

(3) An open-loop control is developed in place of the flyback converter's normal closed-loop control, where a fixed pulse generator controls the SiC MOSFET stack's switching, and a voltage limiting circuit controls the output voltage. In this manner, it will function exactly like a pure resistor and the constant-power-load feature disappears. As a consequence, it will not lead to voltage unbalancing in the static state.

It is noted that, the flyback converter uses discontinuous conduction mode (DCM), and it is modified by adding a resistor R_p into the primary power loop for alleviating the power loop voltage/current oscillation since the extra loss is not considerable.

As shown in Fig. 4-4, the grounds of both the power extracting part and the following gate driver part are common. Therefore, in this modified flyback topology, the primary ground and the secondary ground can be directly connected. As a result of this configuration, plenty of commercial gate driver units can be adopted in the proposed converter-based self-powered GD as the gate driving part's isolation is no longer required. By defining the primary magnetic inductance of the transformer as L_p, and the leakage inductance as L_σ, the following relationship holds since the primary loop can be equivalent to an LR circuit:

$$V_{in} = (L_p + L_\sigma) di_p / dt + i_p R_p \tag{4-1}$$

Using Eq. (4-1), i_p is determined as follows:

$$i_p = \frac{V_{in}}{R_p} - \frac{V_{in}}{R_p} e^{-\frac{t}{(L_p + L_\sigma)/R_p}} \tag{4-2}$$

During one switching cycle, since the on time Δt_{on} is predefined and known, the energy E_p that is accumulated by the transformer and the energy E_{in} that is extracted from V_{in} can be respectively calculated according to Eq. (4-2) as follows:

$$\begin{cases} E_{\mathrm{p}} = 0.5 L_{\mathrm{p}} i_{\mathrm{p}}^{\ 2} = 0.5 L_{\mathrm{p}} \left(\dfrac{V_{\mathrm{in}}}{R_{\mathrm{p}}} - \dfrac{V_{\mathrm{in}}}{R_{\mathrm{p}}} \mathrm{e}^{-\frac{\Delta t_{\mathrm{on}}}{L_{\mathrm{p}}/R_{\mathrm{p}}}} \right)^2 \\ E_{\mathrm{in}} = \dfrac{\Delta t_{\mathrm{on}} V_{\mathrm{in}}^{\ 2}}{R_{\mathrm{p}}} - \dfrac{(L_{\mathrm{p}} + L_{\sigma}) V_{\mathrm{in}}^{\ 2}}{R_{\mathrm{p}}^{\ 2}} + \dfrac{(L_{\mathrm{p}} + L_{\sigma}) V_{\mathrm{in}}^{\ 2}}{R_{\mathrm{p}}^{\ 2}} \mathrm{e}^{-\frac{\Delta t_{\mathrm{on}}}{(L_{\mathrm{p}} + L_{\sigma})/R_{\mathrm{p}}}} \end{cases} \tag{4-3}$$

As seen in Fig. 4-5, the capacitor on the secondary side of the transformer receives the released energy E_{p} every time the SiC MOSFET stack switches from the on-state to the off-state, for powering the following gate driving part. During the process of energy accumulating, once V_{out} is greater than the preset voltage of the depicted voltage limiting circuit, the auxiliary transistor T_{au} will be turned on, and the surplus energy will be dissipated to maintain a nearly constant V_{out}. Specifically, the threshold voltage V_{th} of T_{au} and the Zener breakdown voltage V_{Z} of Zener diode D_{Z} determine the maximum value of V_{out}.

Hence, the power P_{out} for the gate driving part and P_{in} from V_{in} can be respectively calculated as:

$$\begin{cases} P_{\mathrm{out}} = 0.5 f L_{\mathrm{p}} \left(\dfrac{V_{\mathrm{in}}}{R_{\mathrm{p}}} - \dfrac{V_{\mathrm{in}}}{R_{\mathrm{p}}} \mathrm{e}^{-\frac{\Delta t_{\mathrm{on}}}{L_{\mathrm{p}}/R_{\mathrm{p}}}} \right)^2 \\ P_{\mathrm{in}} = \dfrac{f \Delta t_{\mathrm{on}} V_{\mathrm{in}}^{\ 2}}{R_{\mathrm{p}}} - \dfrac{f (L_{\mathrm{p}} + L_{\sigma}) V_{\mathrm{in}}^{\ 2}}{R_{\mathrm{p}}^{\ 2}} + \dfrac{f (L_{\mathrm{p}} + L_{\sigma}) V_{\mathrm{in}}^{\ 2}}{R_{\mathrm{p}}^{\ 2}} \mathrm{e}^{-\frac{\Delta t_{\mathrm{on}}}{(L_{\mathrm{p}} + L_{\sigma})/R_{\mathrm{p}}}} \end{cases} \tag{4-4}$$

where the modified flyback converter's switching frequency is defined as f.

According to Eq. (4-4), if both f and Δt_{on} are fixed in the meantime that L_{p}, L_{σ}, and R_{p} are known after the design of transformer is defined, P_{in} is equivalent to the passive power loss of a constant resistor R_{eq}, and R_{eq} can be calculated as:

$$\frac{1}{R_{\mathrm{eq}}} = \frac{f \Delta t_{\mathrm{on}}}{R_{\mathrm{p}}} - \frac{f (L_{\mathrm{p}} + L_{\sigma})}{R_{\mathrm{p}}^{\ 2}} + \frac{f (L_{\mathrm{p}} + L_{\sigma})}{R_{\mathrm{p}}^{\ 2}} \mathrm{e}^{-\frac{\Delta t_{\mathrm{on}}}{(L_{\mathrm{p}} + L_{\sigma})/R_{\mathrm{p}}}}. \tag{4-5}$$

As a result, combing with the diode D and capacitor C placed in the front of the primary stage of this power extracting part, it can perform the characteristic of a clamping RCD snubber. By further defining the conversion efficiency $\eta = P_{\mathrm{out}}/P_{\mathrm{in}}$, it can be solved as:

$$\eta = \frac{0.5 L_{\mathrm{p}} (1 - \mathrm{e}^{-\frac{\Delta t_{\mathrm{on}}}{L_{\mathrm{p}}/R_{\mathrm{p}}}})^2}{\Delta t_{\mathrm{on}} R_{\mathrm{p}} - (L_{\mathrm{p}} + L_{\sigma})(1 - \mathrm{e}^{-\frac{\Delta t_{\mathrm{on}}}{(L_{\mathrm{p}} + L_{\sigma})/R_{\mathrm{p}}}})} \tag{4-6}$$

η denotes the amount of energy that can be recycled from the "RCD snubber" to power the following gate driving part. Depending on the power rating requirement of the gate driving part, η could be adjusted correspondingly according to Eq. (4-6).

In conclusion, the power device (10 kV SiC MOSFET) and proposed converter-based self-powered GD can be combined as a single unit. Irrelevant to the power device switching, it takes the energy directly from the power loop and converts it for powering the following gate driving part constantly. Besides, the open-loop control approach is scalable to the case where power devices are required in series-connection since it is equivalent to a passive resistor which helps to improve the VB performance.

In addition to the above theoretical analysis, some imperative details should also be noticed in the hardware design. As mentioned, in a resistor-capacitor R_sC_s branch, the capacitor together with the hysteresis function is adopted to supply power for the startup of this modified flyback converter. Therefore, in this hysteresis, the voltage V_p /V_n determines whether the pulse generator in Fig. 4-5 is enabled/disabled. When this voltage across C_s surpasses V_p, driving pulses are produced to start this modified flyback converter. Hence, the startup energy E_s can be computed as follows:

$$E_s = 0.5C_s(V_p^2 - V_n^2) \tag{4-7}$$

After starting the power extracting part, V_{out} will also be fed back to the primary side as the power supply of the pulse generator, enabling the continuous and normal operating of this power extracting part.

In the suggested design, a commercial off-line controller, LT3798, is used as the pulse generator with the hysteresis function integrated inside, as depicted in Fig. 4-5. By disabling the feedback circuits of LT3798, the output pulse will have a fixed frequency and a fixed on-time duration (f = 3.5 kHz, Δt_{on} = 600 ns). In addition, since the controller's output "high" is only +10 V while the recommended "high" for SiC devices is +20 V, a pulse transformer which has 1: 2 turns ratio is added after the output of LT3798 to satisfy the requirement. Furthermore, in this case, the power rating of the gate driving part and the startup voltage $V_{in(s)}$ are identified in advance, and thus R_p = 1.6 kΩ and L_p = 950 μH are selected by Eq. (4-4) in accordance with the confirmed f and Δt_{on}.

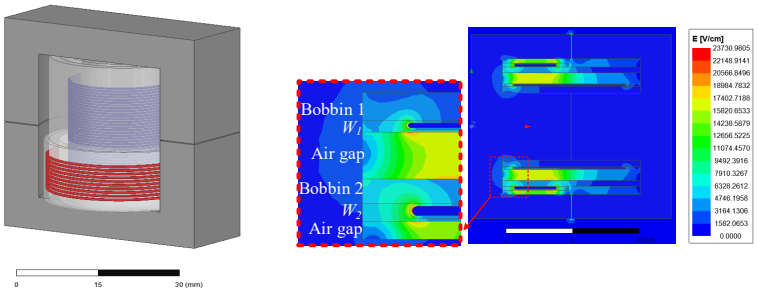
On the basis of the above, it is possible to calculate the voltage drop ΔV across C in Fig. 4-4 after each on time duration from the following relationship as:

$$E_{in} \approx 0.5C[(V_{in(s)} + \Delta V)^2 - V_{in(s)}{}^2] \tag{4-8}$$

As E_{in} is known, the tradeoff between C and ΔV exists according to Eq. (4-8), and a larger C contributes to a smaller ΔV, that is, the reduction of voltage ripple.

After choosing the components parameters in this power extracting converter, its flyback transformer design merits consideration as well. Generally, two key points are focused on: (1) the insulation between the primary winding and the secondary winding could withstand 5 kV; and (2) the interwinding capacitance is anticipated to be low, as it would cause the flowing of the CM current through the SiC MOSFET stack during switching transients.

As shown in Fig. 4-6(a), two ferrite E cores are combined as the magnetic core of the transformer in order to make it compact. Since the transformer's primary voltage could reach 5 kV, primary and secondary windings are separated by insulating materials and air gaps. As a result, the efficiency is inevitably decreased as the leakage inductance L_σ is increases, according to Eq. (4-6). Based on this, with the software assistance of ANSYS Maxwell, a 2-D electrostatic finite element analysis (FEM) simulation is conducted to examine the electrical field distribution in order to prevent partial discharges at high voltages, as illustrated in Fig. 4-6(b).



(a) (b)

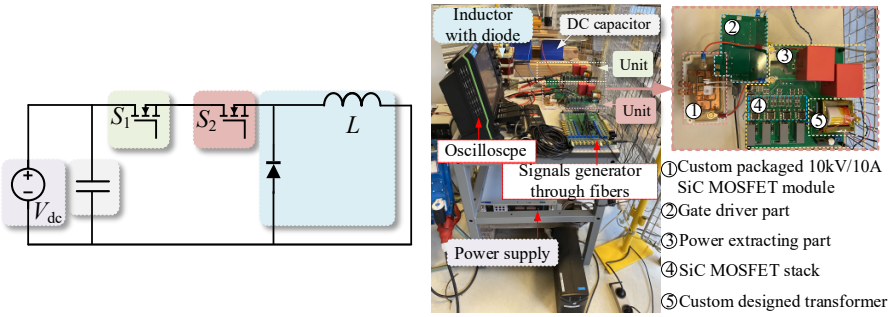
Figure 4-6. The designed transformer (a) 3D-CAD model (b) electric field distribution with the aid of ANASYS Maxwell

The primary and secondary bobbins of the transformer are made from two 3D-printed hollow cylinders, and the primary winding W_1 and the secondary winding W_2 are placed on their surface respectively. Moreover, both two windings are encircled by a layer of Kapton tape. In the parameter setting of simulation, 5 kV is set to W_1 and 0 V is set to W_2, and it is observed from Fig. 4-6(b) that the maximum electrical field in the air is approximately 19 kV/cm. This value is relatively high because of the compactness of the transformer design, and if a larger transformer core is used, the value could be smaller. As the air has the withstanding capability up to 30 kV/cm, the transformer design is suitable in this suggested converter-based self-powered GD. In the meanwhile, it is obtained from the simulation that the interwinding capacitance of transformer is only 4.2 pF, which is further measured to be 4.8 pF with the aid of an impedance analyzer, Keysight E4990A. Consequently, the designed transformer is qualified in this application.

4.3. EXPERIMENTAL VERIFICATION OF THE SUGGESTED GATE DRIVER

In this section, the experimental verification is provided on the basis of the above analysis. Similarly, the energy flowing from the grid side to the battery side in Fig. 4-4 is taken as an example, where S_1 and S_2 are a 10 kV/10 A SiC MOSFET module with the custom package and it is integrated with the suggested converter-based self-powered GD as a single unit, while S_3 and S_4 are replaced by a 10 kV/10 A SiC Schottky diode for the purpose of freewheeling.

In addition, V_{dc} is created using a remote-controlled DC power supply, which is in parallel with a 100 µF DC link capacitor. L is a custom designed 30 mH MV inductor while V_b is excluded (considered as short-circuit) as the design can get verified with the aid of other components. Consequently, Fig. 4-7(a) and Fig. 4-7(b) displays the experimental schematic and its photograph respectively. As seen on the right side in Fig. 4-7(b), inside the unit, the power extracting part of the GD is made up of a series stack of 1.7 kV/5 A SiC MOSFETs (C2M1000170J), and the gate driving part is powered by a commercial DC to DC power supply module (MGJ6D242005LMC) with the output voltages of -5 V, +5 V, and +20 V.



(a) (b)

Figure 4-7. Testing platform of the self-powered gate driver with converter-based design: (a) schematic (b) photograph

Firstly, the feasibility of the suggested self-powered GD with converter-based design is verified by only one unit. As presented in Fig. 4-8, during the startup process, it can be observed that, as V_{dc} increases gradually and reaches the startup voltage (which is 2 kV in this case), the SiC MOSFET stack of the power extracting part begins to be turned on and off periodically, transferring the power to the following gate driving part from the capacitor C. After a time interval, V_{out} as the output voltage of the power extracting part reaches the clamping value 20 V and a part of the output

power is fed back to continuously power LT3798. As a result, the power extracting part enters the normal operating state. At the frequency f of 3.5 kHz controlled by LT3798, voltage v_{s1} (the sum of voltages $v_{ds(i)}$ across T_i, i =a ~d) of the SiC MOSFET stack is continuously decreasing and increasing while the on time Δt_{on} is 600ns. Importantly, both the static VB and dynamic VB in the flyback converter are ensured by using the proposed stack, which is already performed in Chapter 2.

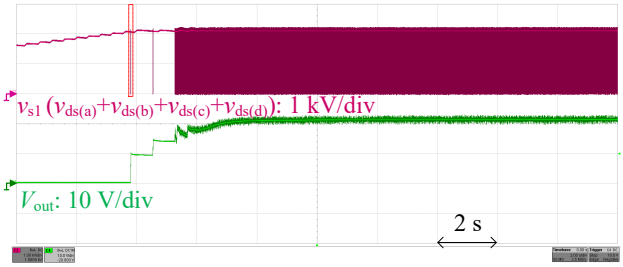


Figure 4-8. Startup process using the self-powered gate driver with converter-based design

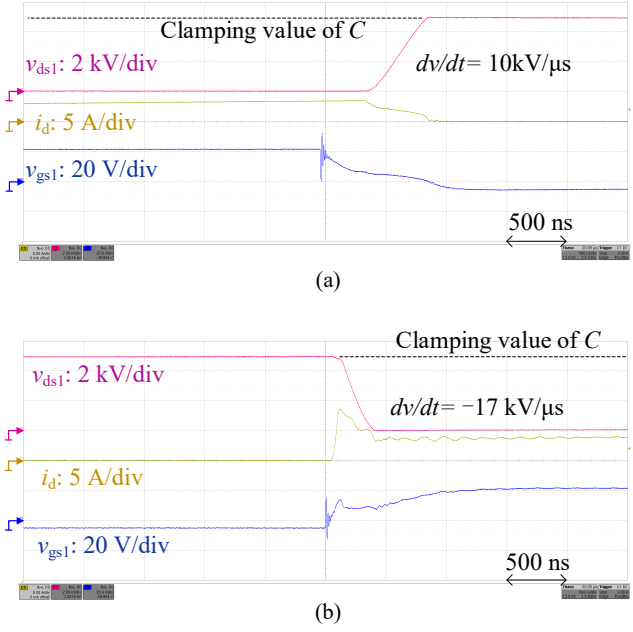
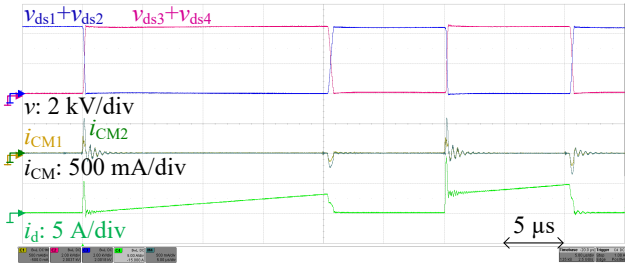


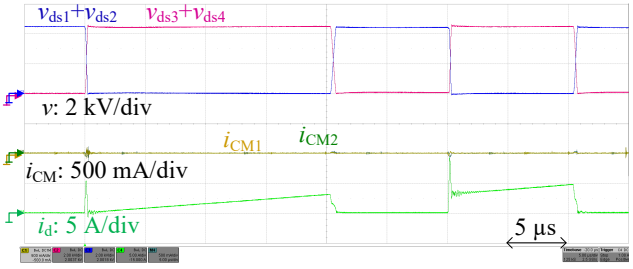
Figure 4-9. Switching waveforms of a 10 kV SiC MOSFET using the suggested self-powered gate driver with converter-based design (a) turning-off (b) turning-on

Further, in the testing conditions from 2 kV to 5 kV, the unit shows good switching performances. In the case of V_{dc} = 5 kV and the drain current i_d = 3.5 A, the switching waveforms using the proposed converter-based self-powered GD are displayed in Fig. 4-9. It can be observed that the proposed GD operates well, outputting -5 V / +20 V and providing sufficient power for the driven device. It is seen that the gate-source voltage v_{gs1} performs a temporary high frequency oscillation, which is induced by the parasitic inductance in the gate loop as the gate current increases to the peak value from zero abruptly in the beginnings of switching transients. Additionally, v_{ds1} gets clamped as it approaches the clamping voltage, which is formed by the voltage across C as indicated by the dashed lines in Fig. 4-9. During the turning-on and turning-off transients, dv_{ds1}/dt values of S_1 are respectively measured as -17 kV /µs and 10 kV /µs.

In addition, two units are connected in series to further verify the benefits of the proposed self-powered GD with converter-based design. By powering the gate driving part with an external power supply in the meantime of breaking the power connection from the power extracting part to the gate driving part, the designed GD is turned into a conventional one with the clamping RCD snubber. Therefore, the proposed GD can be compared with the conventional one in terms of CM currents which are measured at the points as depicted in Fig. 4-2 and Fig. 4-4.



(a)



(b)

Figure 4-10. Comparison results of CM currents for S_1 and S_2 with (a) conventional gate drivers (b) suggested self-powered gate drivers with converter-based design

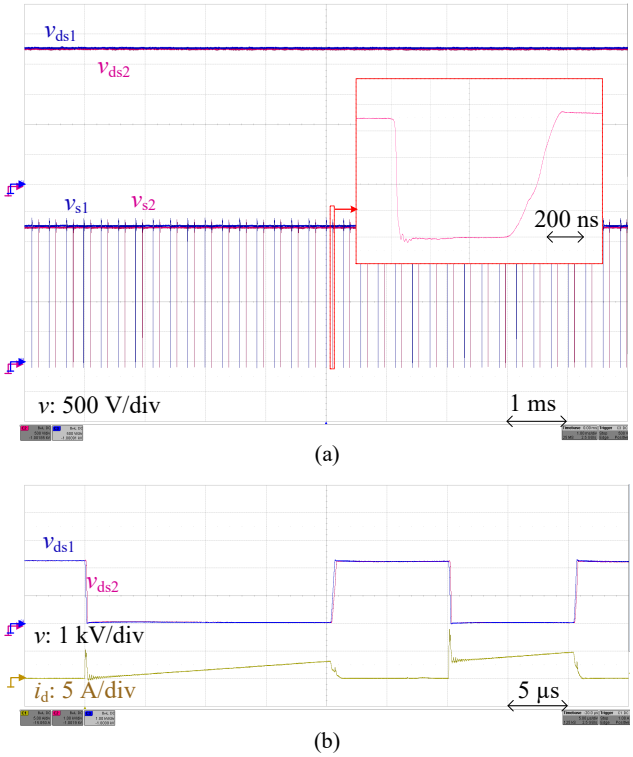


Figure 4-11. (a) static and (b) dynamic voltage balancing performance of S_1 and S_2 in a double-pulse test with suggested self-powered gate drivers

As displayed in Fig. 4-10(a), S_1 and S_2 are put to the test using two conventional GDs. Due to the limited isolation rating itself, the adopted commercial DC to DC converter in the gate driving part is theoretically not qualified for 10 kV SiC MOSFET in the external-powered manner. Therefore, the experimental comparison is only conducted in double-pulse tests, and V_{dc} is restricted below 4.5 kV. After two pulses of switching, i_d gets increased to 5 A from zero, and it is seen that the increasing of v_{ds3} and v_{ds4} are accompanied by the decreasing of v_{ds1} and v_{ds2}. During the switching transients, i_{CM2} is 600mA by the measurement and i_{CM1} is smaller because the GDs experience different *dv/dt* stresses, which is consistent with the analysis. Therefore, if V_{dc} increases, there is a significant potential risk of the GD breakdown due to the increased CM current magnitude.

In contrast, as presented in Fig. 4-10(b), S_1 and S_2 are tested with the self-powered GDs with converter-based design. Although theoretically there should be no CM current during the switching transient, the designed GD still produces a small amount of CM noise for the following possible reason: the diode' reverse recovery and the

capacitor's parasitic inductance, that exist in *D* and *C* in Fig. 4-4, could cause a tiny current from the power extracting part to flow through 10 kV SiC MOSFET during its turning-on transient. It provokes a voltage variation on the transformer's primary side, causing the parasitic capacitor between the transformer's primary and secondary sides to experience voltage variation as well, which could further result in the small CM noise.

Moreover, the static and dynamic VB of S_1 and S_2 are displayed. In the power extracting parts of GDs, the SiC MOSFET stacks are both constantly switching as f = 3.5 kHz and Δt_{on} = 600 ns, as shown in v_{s1} and v_{s2} in Fig. 4-11(a). Therefore, the open-loop design prevents the constant-power-load characteristic of the power extracting part from being present during the static state. Owing to their comparable power losses, the static VB of v_{ds1} and v_{ds2} is good as expected. Besides this, Fig. 4-11(b) presents the dynamic VB results from the double-pulse test. It is seen that the dynamic VB of v_{ds1} and v_{ds2} is good as well since the suggested GDs behave as clamping RCD snubber circuits, proving that the suggested self-powered GD with converter-based design is scalable for series-connection. It is worth noting that, the good VB performance can only be shown in the initial several pulses, and more VB designs are required in the case of continuously switching, which will be illustrated in the next chapter.

CHAPTER 5. VOLTAGE BALANCING DESIGN OF SERIES-CONNECTED MV SIC MOSFETS EQUIPPED WITH SELF-POWERED GATE DRIVERS

The information in this chapter is based on **Publication I, Publication VI and Publication VII**.

Although the above converter-based self-powered gate drivers (GDs) facilitates to voltage balancing (VB) in direct series-connection of MV SiC MOSFETs and the good VB performance is shown in a double-pulse test, voltage unbalancing will occur in the converter applications as the MV SiC MOSFETs are switching continuously. During the switching transients, due to inconsistencies of GDs, parasitic parameters, devices characteristics, etc. [70], discrepant energy amount is accumulated in the individual clamping capacitor, resulting in the discrepancy of clamping values as well as voltage unbalancing of MV SiC MOSFETs. To tackle this voltage unbalancing issue, many scholars have proposed solutions, which can generally be divided into four categories in the range of prevalent active VB strategies:

(1) *Active voltage control strategy*: in order to regulate the gate driving process and achieve VB, the closed-loop is constructed by comparing the collector-emitter voltage of each IGBT with the same voltage trajectory which is regarded as reference [71]-[72]. However, the bandwidth of analog devices on the GD limits the VB performance, and its feasibility in series-connection of SiC MOSFETs is hardly verified.

(2) *Active clamping strategy*: adding a delicately designed clamping circuit from the power side to the gate side is also an option to reduce voltage unbalancing. Once the clamping threshold is exceeded by the over-voltage of power loop, a feedback current will immediately run into the power device's gate loop, slowing the turning-off process and thus achieving VB [73]. But it increases power device loss and does not work in the cases of lower voltages.

(3) *Active gate compensation strategy*: the fundamental idea is to accurately compensate each power device's gate charge to realize VB of power devices in series, with the aid of online voltage unbalancing detection. For detecting the voltage unbalancing degree, generating *dv/dt* difference is one strategy, for example, by designing coupled inductors in the loops of resistor-capacitor (RC) snubbers [74]-[75]. As a more straightforward strategy, a digital

controller can be used to calculate the voltage unbalancing by receiving feedbacks of the voltage sampling values from analog-to-digital converters (ADCs). For compensating gate charge, in [76], an intermediate voltage is introduced by building a three-level turning-off GD, and the SiC MOSFET's turning-off gate-source voltage gets modified appropriately by adjusting the intermediate value. In [77]-[78], a miller capacitor with voltage dependency is designed and added, so that *dv/dt* of the SiC MOSFET can be regulated appropriately. In [79]-[81], a controlled current source is custom designed, which is then integrated into the traditional GD with the voltage source characteristic, and thus the VB performance is dependent on the degree of current source compensation. Yet, the system's architecture becomes more complicated, and its robustness declines.

(4) *Active delay control strategy*: using time delay chips, etc., to precisely modify the switching signal delay based on the voltage unbalancing degree is another useful tactic for good VB performance [82]-[85]. It is regarded as the finest method for direct series-connection of SiC MOSFETs in order to explore the fast-switching potential of SiC device since this method does not slow down the switching speed. Nevertheless, the closed-loop control is required as well, which increases the design burden. In addition, the parameter identification is needed for a precise system model.

Compared to the active VB strategies mentioned above, passive VB strategies such the use of snubbers result in a higher loss. Nonetheless, due to their superior robustness and reliability without the complexity of closed-loop VB control, they are frequently used in industrial applications [86]. To lessen the loss of snubbers, some novel techniques such as energy recycling topologies have been proposed, however, because of their complex construction, dedicated modulation, and restricted applicability [87]-[93], they are still not appealing. As for general passive snubber strategies, improved VB performance yet results in a larger snubber loss, hence a better trade-off is sought after between loss and VB. Additionally, for reducing static voltage unbalancing generated by the leakage current variation of the power device, paralleling VB resistors is a common method. However, in some MV high-power applications, VB resistors for a good static VB performance could have significant power loss [85], while very few articles have considered the improvement.

Based on the aforementioned, in this chapter, the VB characteristic using the proposed self-powered GDs is explored and the corresponding improvements are provided.

5.1. THE CONCEPT OF ADAPTIVE-IMPEDANCE SNUBBER

The schematic for the analysis in this study is depicted in Fig. 5-1. It involves two directly series-connected medium-voltage (MV) SiC MOSFETs, and each one is

united with its converter-based self-powered GD. It removes the requirement for an external auxiliary power supply, which facilitates the scalability to series connection as described in Chapter 4. Also, its diode-capacitor clamping structure, possesses the characteristic of not impairing the power device's switching speed until the clamping value is exceeded, which helps to maintain the fast-switching merit of SiC MOSFET in this application.

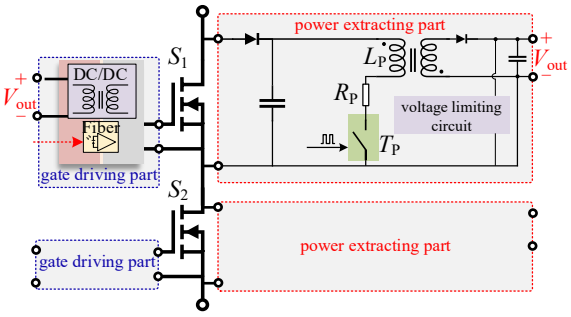


Figure 5-1. Two direct series-connected MV SiC MOSFETs equipped with the self-powered gate drivers

Due to the self-powered GD's converter-based design, it can provide additional flexibilities and opportunities for improving the passive VB performance by adjusting the power extracting part's behavior (managing the modulation of internal modified flyback converter), allowing itself to function like an adaptive-impedance "snubber". From the views of static VB and dynamic VB, respectively, the elaborations will be given as follows.

5.1.1. VOLTAGE BALANCING IN STATIC CONDITION

In general, due to the leakage current discrepancy of power device, adding the same resistor r_S in parallel with each SiC MOSFET S_i (i = 1, 2) is a common strategy for the purpose of static VB in the series-connection case, as shown in Fig. 5-2(a). In addition, r_S significantly speeds up the recovery of VB following a dynamic VB event. In conclusion, r_S is critical to the development of VB.

Hence, to determine the proper value of r_S, it is anticipated in the worst case that, during the static state, the leakage current $i_{dss(2)}$ of S_2 is significantly larger than $i_{dss(1)}$ of S_1 as $i_{dss(1)} = 0$ and $i_{dss(2)} = I_{dss(max)}$, where the maximum leakage current of S_i is defined as $I_{dss(max)}$. Afterwards, the relationship is as follows:

$$\begin{cases} v_{ds1} / r_S - v_{ds2} / r_S = I_{dss(max)} \\ v_{ds1} + v_{ds2} = v_{dc} \end{cases} \tag{5-1}$$

where v_{ds} is the overall blocking voltage of this series branch, and v_{dsi} (i = 1, 2) is the drain-source voltage of S_i.

Furthermore, it is defined in this scenario that, p_S is the static power loss, and $\Delta v_S = v_{ds1} - v_{ds2}$ is the degree of static voltage unbalance. Then it can be solved as:

$$\begin{cases} \Delta v_S = r_S \cdot I_{dss(max)} \\ p_S = \dfrac{v_{ds1}^{\,2}}{r_S} + \dfrac{v_{ds2}^{\,2}}{r_S} = \dfrac{1}{2 \cdot r_S} \cdot (v_{dc}^{\,2} + \Delta v_S^{\,2}) \end{cases} \tag{5-2}$$

In accordance with Eq. (5-2), anticipating a smaller value of Δv_S is accompanied by choosing a smaller r_S, as well as inducing a greater p_S. As a result, there is a tradeoff design between Δv_S and p_S. In the case of device aging in atrocious working conditions, or multiple device dies being parallelly connected in a power module to increase the current rating, $I_{dss(max)}$ will be increased, making the tradeoff even more significant.

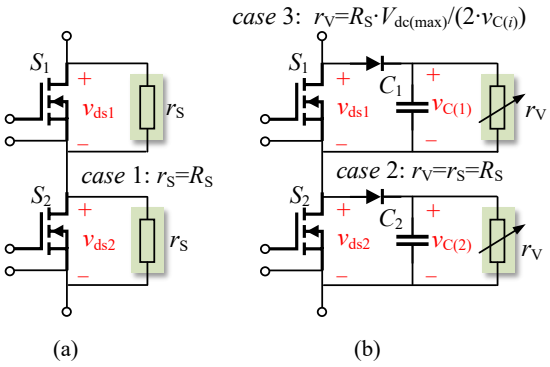


Figure 5-2. Static voltage balancing (a) by placing resistors in parallel (b) with the adaptive-impedance design

Due to the resistor's passive nature, the resistor R_S is a fixed value. Therefore, once r_S is chosen as R_S, the static VB optimization method for striking a better trade-off can not be found. This is also considered as the limitation of the common static VB strategy. By contrast, as a converter-based circuit shown in Fig. 5-1 is used in place of r_S, a variable resistor r_V can be assumed in Fig. 5-2(b) by controlling the converter's behavior in a certain way, which looks to have the potential to bypass the bottleneck and a better trade-off in Δv_S and p_S can be achieved. Next, the analysis is provided.

In Fig. 5-1, both S_1 and S_2 are constantly off during the static state, while the switch T_P is switching continuously to enable the power extracting part, and then to supply the necessary input power for the following gate driving part. The modified flyback

converter is the primary internal topology, and the operating mode is discontinuous conduction mode (DCM), as described in Chapter 4. As a continuous analysis of Eq. (4-4), by defining the power loss associated with S_i ($i = 1, 2$) as $p_{(i)}$ and the static power loss p_S as $p_{(1)}+p_{(2)}$, the following relationships are attained as:

$$\begin{cases} p_{(1)} / v_{ds1} - p_{(2)} / v_{ds2} = I_{dss(max)} \\ v_{ds1} + v_{ds2} = v_{dc} \end{cases} \tag{5-3}$$

If f in Eq. (4-4) is fixed as F_P, it is solved from Eq. (4-4) and Eq. (5-3) as:

$$\begin{cases} \Delta v_S = K_1 \cdot I_{dss(max)} \\ p_S = \dfrac{1}{2 \cdot K_1} \cdot (v_{dc}{}^2 + \Delta v_S{}^2), \end{cases} \quad K_1 = \frac{R_P}{F_P \cdot [T_{on} - \dfrac{L_p}{R_P} \cdot (1 - e^{-\frac{T_{on}}{L_P / R_P}})]} \tag{5-4}$$

where K_1 is a constant since all the parameters in the design have preset fixed values.

If, however, f has a variable value, such as $f_{(i)}$ of S_i is equal to $\alpha \cdot v_{C(i)}$ (α is a constant), where $v_{C(i)}$ is the voltage of the capacitor which is equal to v_{dsi} in the static state, the expression is handled by setting another constant value K_2 as follows:

$$\begin{cases} \Delta v_S = \dfrac{K_2}{v_{DC}} \cdot I_{dss(max)} \\ p_S = \dfrac{1}{4 \cdot K_2} \cdot (v_{dc}{}^3 + 3 \cdot v_{dc} \cdot \Delta v_S{}^2) \end{cases}, \; K_2 = \frac{R_P}{\alpha \cdot [T_{on} - \dfrac{L_p}{R_P} \cdot (1 - e^{-\frac{T_{on}}{L_P / R_P}})]} \tag{5-5}$$

To make comparisons in this study easier, the static power losses in all three cases (defined as *case* 1, *case* 2, and *case* 3), are equal when v_{dc} is the designated maximum blocking voltage $V_{dc(max)}$. The corresponding mathematical equations are unified as:

$$\begin{cases} \Delta v_S = R_S \cdot I_{dss(max)} \\ p_S \approx \dfrac{v_{dc}{}^2}{2 \cdot R_S} \end{cases}, \quad case\ 1$$

$$\begin{cases} \Delta v_S = R_S \cdot I_{dss(max)} \\ p_S \approx \dfrac{v_{dc}{}^2}{2 \cdot K_1} = \dfrac{v_{dc}{}^2}{2 \cdot R_S}, \end{cases} \quad case\ 2 \tag{5-6}$$

$$\begin{cases} \Delta v_S = \dfrac{R_S \cdot V_{dc(max)}}{2 \cdot v_{dc}} \cdot I_{dss(max)} \\ p_S \approx \dfrac{v_{dc}{}^3}{4 \cdot K_2} = \dfrac{v_{dc}{}^3}{2 \cdot R_S \cdot V_{dc(max)}} \end{cases}, \quad case\ 3$$

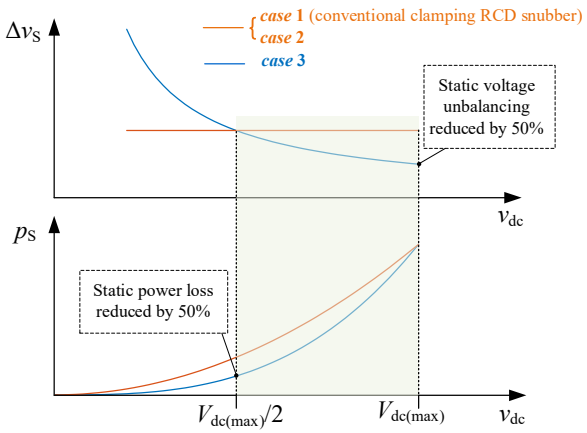


Figure 5-3. Δv_S and p_S indication versus v_{dc} in case 1, case 2, and case 3

Therefore, the functional relationship graphs regarding of the three cases can be created, as seen in Fig. 5-3. *case* 1 is depicted in Fig. 5-3 as the conventional clamping RCD snubber, which operates based on the identical principle of placing resistors in parallel as in Fig. 5-2(a). *case* 2 is depicted in Fig. 5-3 as r_V being equal to r_S (R_S), which demonstrates that the curves in *cases* 1 and *case* 2 overlap and the converter can be adjusted to act like a resistor in the conventional static VB strategy. However, the comparison of *cases* 2 and *cases* 3 in Fig. 5-3 reveals that, in the v_{dc} range from $V_{dc(max)}/2$ to $V_{dc(max)}$, Δv_S and p_S in *case* 2 are larger than in *case* 3. It suggests that, managing the power extracting part's behavior as an adaptive-impedance "snubber" could result in a better trade-off (i.e., in *case* 3, r_V is equal to $R_S \cdot V_{dc(max)}/(2 \cdot v_{dsi})$). Even though in the v_{dc} range from 0 to $V_{dc(max)}/2$, Δv_S in *case* 3 is greater than in *case* 2. The unexpected operation points could be avoided by determining the startup voltage as $V_{dc(max)}/2$, since there exists a necessary startup voltage of the power extracting part during the startup process for providing adequate power for the following gate driving part. In particular, compared to *case* 2, the static power loss of *case* 3 is decreased by 50% when $v_{dc} = V_{dc(max)}/2$, and the static voltage unbalancing of *case* 3 is reduced by 50% when $v_{dc} = V_{dc(max)}$.

In a similar way, $f_{(i)} = \beta \cdot v_{DS(i)}^2$ or $f_{(i)} = \gamma \cdot v_{DS(i)}^3$ (i = 1, 2) could be further assumed and defined, where β, γ are constants, and it could result in an even better trade-off in Δv_S and P_S. Nevertheless, it significantly narrows the appropriate v_{dc} range as well, which becomes not practicable in the actual applications. As a result, this study concentrates on the circumstances where fixed $f_{(i)}$ and $f_{(i)}=\alpha \cdot v_{DS(i)}$ exist (i.e., *case* 2 and *case* 3).

5.1.2. VOLTAGE BALANCING IN DYNAMIC CONDITION

Additionally, the adaptive-impedance snubber contributes to dynamic VB as well. In *case* 2, since the converter is controlled to perform like a passive resistor, the power extracting part operates as a conventional "clamping RCD snubber". In the stable state when S_1 and S_2 are continuously switching, if it is assumed that the power extracting part of S_2 stores less energy than that of S_1 due to the inconsistent device characteristics, GDs, etc. until the stable state is established, the clamping voltage value $v_{C(2)}$ will be lower than $v_{C(1)}$ (the effect of static voltage unbalancing is disregarded by assuming $i_{dss(1)} = i_{dss(2)}$). Since *case* 1 and *case* 2 are identical, only *case* 2 and *case* 3 are examined in the following. By defining the amount of energy that has been collected in one switching cycle as $\Delta E_{(case\,i)}$ (i=2, 3) in both cases, the correlations can be determined as:

$$\begin{cases} \dfrac{v_{C(1)}^{\ 2}}{R_S} - \dfrac{v_{C(2)}^{\ 2}}{R_S} = \dfrac{v_{C(1)}^{\ 2}}{K_1} - \dfrac{v_{C(2)}^{\ 2}}{K_1} = f_s \Delta E_{(case2)}, & case\ 1\ \&\ case\ 2 \\ v_{C(1)} - v_{C(2)} = \Delta v_D \end{cases} \tag{5-7}$$

$$\begin{cases} \dfrac{v_{C(1)}^{\ 3}}{K_2} - \dfrac{v_{C(2)}^{\ 3}}{K_2} = f_s \Delta E_{(case3)}, & case\ 3 \\ v_{C(1)} - v_{C(2)} = \Delta v_D \end{cases} \tag{5-8}$$

where the switching frequency of S_i (i = 1, 2) is f_s during the dynamic state, and the voltage unbalancing degree of $v_{C(i)}$ (i = 1, 2) is Δv_D, which can be utilized to represent the dynamic voltage unbalancing degree of S_i as well in this target case.

In order to make the analysis easier, the following assumptions are made as: (1) Δv_D is substantially smaller than v_{dc}; (2) $v_{C(1)} + v_{C(2)} \approx v_{DC}$; and (3) $\Delta E_{(case2)} \approx \Delta E_{(case3)} = K_e \cdot v_{DC}^2$, where K_e is defined as the voltage-dependent coefficient of energy. Moreover, p_D is the definition of the dynamic power loss, and f_s is equal to a fixed value F_s. Consequently, by solving from Eq. (5-7) and Eq. (5-8), the following is resolved:

$$\begin{cases} \Delta v_D = \dfrac{K_1 \cdot F_s \cdot \Delta E_d}{v_{DC}} = K_e \cdot R_S \cdot F_s \cdot v_{DC} \\ p_D \approx \dfrac{v_{DC}^{\ 2}}{2 \cdot K_1} = \dfrac{v_{DC}^{\ 2}}{2 \cdot R_S} \end{cases}, \quad case\ 1\ \&\ case\ 2 \tag{5-9}$$

$$\begin{cases} \Delta v_D \approx \dfrac{4 \cdot K_2 \cdot F_s \cdot \Delta E_d}{3 \cdot v_{DC}^{\ 2}} = \dfrac{2 \cdot K_e \cdot V_{DC(max)} \cdot R_S \cdot F_s}{3} \\ p_D \approx \dfrac{v_{DC}^{\ 3}}{4 \cdot K_2} = \dfrac{v_{DC}^{\ 3}}{2 \cdot R_S \cdot V_{DC(max)}} \end{cases}, \quad case\ 3$$

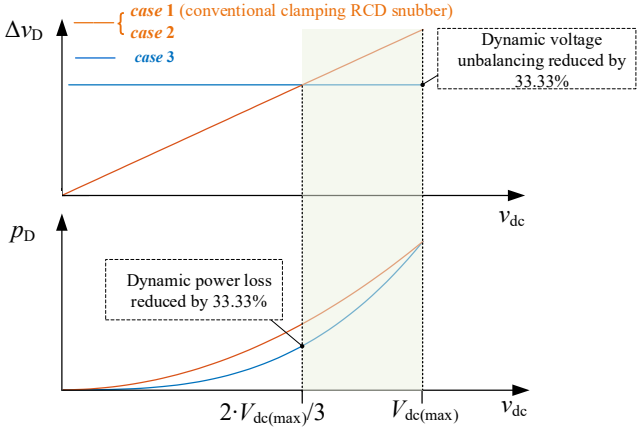


Figure 5-4. Δv_D and p_D indication versus v_{dc} in case 1, case 2, and case 3

As shown in Fig. 5-4, similar functional relationship graphs can be drawn as well to provide analysis. It is observed that *cases* 1 and *case* 2 are consistent as expected. In addition to that, it is also shown that, in the v_{dc} range from $2 \cdot V_{dc(max)}/3$ to $V_{dc(max)}$, compared to *case* 2 regarded as the linear impedance "snubber", *case* 3 regarded as the adaptive-impedance "snubber" achieves a better trade-off between v_D and P_D. When $v_{dc} = 2 \cdot V_{dc(max)}/3$, the dynamic power loss of *case* 3 is decreased by 33.3%; and when $v_{dc} = V_{dc(max)}$, the dynamic voltage unbalancing of *case* 3 is decreased by 33.3%.

5.2. DESIGN DETAIL AND HYBRID VOLTAGE BALANCING STRATEGY

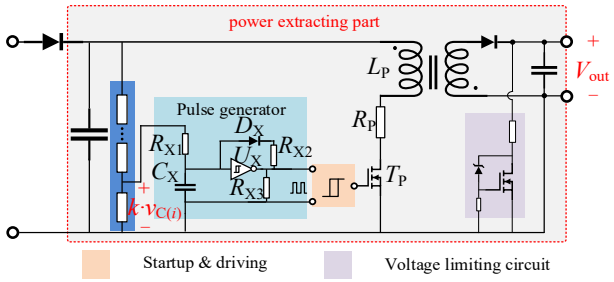


Figure 5-5. Main circuit of the designed power extracting part

In order to achieve a better trade-off of VB and loss, hardware in accordance with the adaptive-impedance "snubber" as in *case* 3 is constructed, and the power extracting

part's main circuit of is depicted in detail in Fig. 5-5. As explained, a modified flyback converter with the open-loop control is applied as the basic topology. Due to the low transmitted power, the current rating requirement for T_P is low, and the output voltage V_{out} is regulated by the voltage limiting circuit to stay within the following gate driving part's nominal input voltage range. By using a Schmitt trigger U_X, a capacitor C_X, a diode D_X, and resistors R_{X1}–R_{X3}, a voltage-dependent pulse generator can be created to regulate the switching of T_P, and its operating principle is as follows:

Figure 5-6. Equivalent circuit diagram of the designed pulse generator during (a) OFF and (b) ON duration

When the voltage v_{CX} of C_X reaches the positive threshold voltage V_{th}^+ of U_X, the output voltage pulse is at the "low" level, and when v_{CX} reaches the negative threshold voltage V_{th}^- of U_X, the output voltage pulse is at the "high" level. Therefore, the time intervals t_{off} and t_{on} correspond to the rise of v_{CX} from V_{th}^- to V_{th}^+ and the fall of v_{CX} from V_{th}^+ to V_{th}^-, respectively. According to the schematic, v_{CX} is below V_{th}^+ when the output voltage pulse is at its "high" level and D_X is reversely blocking. With the aid of the resistor divider, $v_{C(i)}$ (i = 1, 2) can be scaled down by k, and the charging from $k{\cdot}v_{C(i)}$ through R_{X1} causes v_{CX} to rise, as the equivalent circuit diagram is depicted in Fig. 5-6(a). As a result, this procedure is comparable to the RC circuit's full response, and the equation for t_{off} can be computed as:

$$t_{off}=R_{X1}\cdot C_X\cdot\ln\left(1-\frac{V_{th}^+-V_{th}^-}{V_{th}^+-k\cdot v_{C(i)}}\right) \tag{5-10}$$

When the output pulse voltage is at the "low" level of, v_{CX} is greater than V_{th}^+ and D_X becomes forward conducting. The discharging of C_X through R_{X2} is reason that causes v_{CX} to decline, and the charging of $k{\cdot}v_{C(i)}$ through R_{X1} can have an influence. Fig. 5-6(b) depicts the equivalent diagram of this circuit, and it shows the following relationship as:

$$k\cdot v_{C(i)}=R_{X1}\cdot(C_X\cdot dv_{CX}/dt+v_{CX}/R_{X2})+v_{CX} \tag{5-11}$$

Considering that, v_{CX} is a variate decreasing from V_{th}^+ to V_{th}^- while $v_{C(i)}$ (i = 1, 2) is comparatively constant, t_{on} can be solved from Eq. (5-11) as:

$$t_{on}=\frac{R_{X1}\cdot R_{X2}\cdot C_X}{R_{X1}+R_{X2}}\cdot\ln\{1+(V_{th}^{+}-V_{th}^{-})/(V_{th}^{-}-\frac{k\cdot v_{C(i)}\cdot R_{X2}}{R_{X1}+R_{X2}})\} \tag{5-12}$$

Since V_{th}^{+} and V_{th}^{-} are substantially smaller than $k\cdot v_{C(i)}$, Eq. (5-10) is simplified as:

$$t_{off}\approx R_{X1}\cdot C_X\cdot\frac{V_{th}^{+}-V_{th}^{-}}{k\cdot v_{C(i)}} \tag{5-13}$$

Similar to this, since R_{X1} is configured to be significantly greater than R_{X2} and $V_{th}^{-}/R_{X2}>> k\cdot v_{C(i)}/(R_{X1}+R_{X2})$, t_{on} is solved to be a fixed value T_{on} from Eq. (5-12) as:

$$t_{on}\approx R_{X2}\cdot C_X\cdot\frac{V_{th}^{+}-V_{th}^{-}}{V_{th}^{-}}=T_{on} \tag{5-14}$$

From Eq. (5-13) and Eq. (5-14), the output voltage pulse's frequency is roughly proportional to $v_{C(i)}$ since t_{off} is significantly larger than t_{on}. In conclusion, the pulse generator is made in a straightforward manner to fulfill the requirements of *case* 3: (1) fixed T_{on}; (2) $f_{(i)}=\alpha\cdot v_{C(i)}$. Thus, the adaptive-impedance self-powered GD is made, which possesses the improved passive "snubber" feature to make it much appealing if anticipating a less sophisticated control scheme in series-connection because it does not need any closed-loop control from active VB schemes.

It is worth noting that, if this GD has been properly constructed without the power extracting requirement from the "snubber", the proposed adaptive-impedance concept could be realized in a separate way, making it even simpler. Instead, when it is paired with the self-powered notion as explained above, the driven device may experience two safety issues and one limitation as:

(1) In the case of a possible dip in DC bus voltage in the running system, $v_{C(i)}$ (i = 1, 2) could be too low and the normal operation could not be maintained. Therefore, the output PWMs should be immediately forced to be "low" by the controller to assure the safety once the fault occurs. From the perspective of gate driver design, the under-voltage detection function can be used, and it can provide the feedback to the controller. From the perspective of power loop design, the controller can sample $v_{C(i)}$ in time, and then it can make the judgement on this basis.

(2) Another problem occurs when v_{dc} gradually rises to the operational voltage during system startup. Before $v_{C(i)}$ arrives at the startup threshold voltage, the resistor divider as shown in Fig. 5-5 determines the input impedance of this "snubber", which is a high value. After activating the power extracting part, the input impedance is altered to the intended lower value. Nevertheless, all the power extracting parts could experience the out-of-sync issue during the

startup because of the parameter mismatch, resulting in oscillation of $v_{C(i)}$ temporarily. Therefore, the oscillation should be well evaluated to assure the safety, and the comprehensive analysis is provided in **Publication VII**.

(3) The self-powered GD design still has a drawback in addition to the two safety concerns as mentioned. Since the self-powered GD obtains its energy when the SiC MOSFET is off, it can not be used when the SiC MOSFET is left on continuously and the duty cycle range is limited.

Additionally, taking into account the power ratings of both the power extracting part and the gate driving part, the latter one only needs a few watts of power in most cases, while the former one needs to extract tens of watts for obtaining a good VB performance even with adaptive-impedance optimization in the cases of severe natural voltage unbalancing. Consequently, if the active VB strategy's superior dynamic VB performance with minimal loss is expected while the added complexity of controlling is less cared, active delay control strategy can be further combined with this proposed passive technique.

Actually, the aforementioned pulse generator's output voltage pulse transfers $v_{C(i)}$ ($i = 1, 2$) into frequency, as a result, it can also transmit $v_{C(i)}$ through fiber to an external controller in addition to being utilized as the driving signal of the modified flyback converter. Therefore, a hybrid VB strategy can be suggested: on the basis of the fiber feedbacks and the proposed adaptive-impedance "snubber" design and, a controller can be added to compute the degree of voltage unbalancing in the series-connection of SiC MOSFETs, and then the switching signal delay can get online adjusted for achieving the dynamic VB.

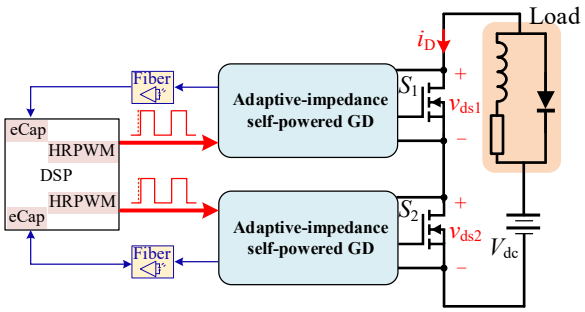


Figure 5-7. Structure of the suggested hybrid voltage balancing method

In this study, a digital signal processor (DSP) is utilized as the external controller, as depicted in Fig. 5-7. Its internal eCAP module is utilized to determine $v_{C(i)}$ by detecting the input frequency. Also, the HRPWM module inside of it has a resolution

of 150 ps, which can be sufficient to function as a delay executor with high-precision for SiC MOSFETs in series-connection. Hence, a closed-loop compensation is created, and the thorough system flowchart is displayed in Fig. 5-8 to make it apparent.

When the PWM interrupt occurs, $v_{C(1)}$ ($v_{C(2)}$) is translated as the frequency $f_{(1)}$ ($f_{(2)}$), which is then collected by the DSP and used in a calculation procedure to produce a compensation delay Δt' in the subsequent switching period. Therefore, $v_{C(1)}$ and $v_{C(2)}$ gradually approach parity owing to the dynamic equilibrium between discharging and charging of the clamping capacitor, and v_{ds1} and v_{ds2} are in good balance.

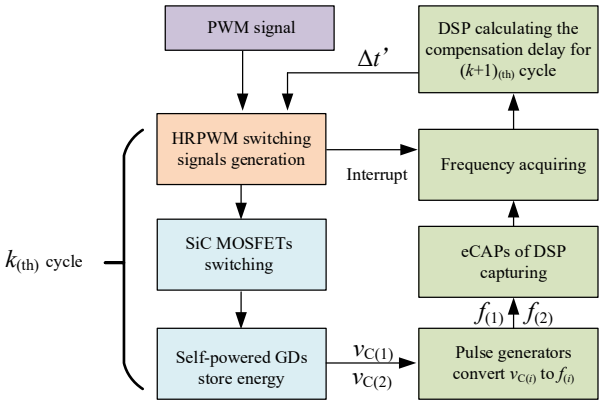


Figure 5-8. Detail of the system flowchart

Proportional-integral (PI) control algorithm is utilized in the DSP for the key calculation part, and the issue of choosing the right parameters K_p and K_i still stands. Instead of using a trial-and-error approach, establishing a small-signal model for the entire closed-loop system will be a more efficient technique to determine parameters for preserving stability. As a result, the individual blocks shown in Fig. 5-8 should be modelled appropriately.

Since v_{ds1} and v_{ds2} are typically regarded as judgments in some literatures like [82], the relationship between the voltage unbalancing degree of SiC MOSFETs in series and the derived delay is only discovered experimentally, which restricts the design flexibility. Instead, $v_{C(1)}$ ($v_{C(2)}$) is sampled and fed back for the control scheme due to the passive "snubber" existence in this proposed design, and the relationship between the difference Δv_C of $v_{C(1)}$ and $v_{C(2)}$ and Δt' can be found as:

$$\Delta t' = \frac{C_1 \cdot (v_{C(1)} - v_{C(2)})}{i_D} = \frac{C_1 \cdot \Delta v_C}{i_D} \tag{5-15}$$

where C_1 is equal to C_2, and i_D stands for the power loop current.

Moreover, from Eq. (5-13) and Eq. (5-14), the relationship between $v_{C(1)}$ ($v_{C(2)}$) and $f_{(1)}$ ($f_{(2)}$) is solved as:

$$f_{(i)} \approx \frac{k \cdot v_{C(i)}}{R_X \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}, \qquad i=1, 2 \tag{5-16}$$

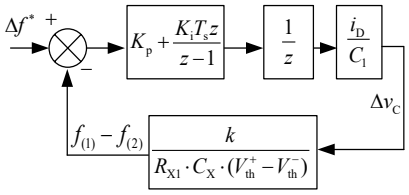


Figure 5-9. The corresponding control block diagram

Since DSP is applied in this established closed-loop system, it is a discrete system, and Fig. 5-9 shows the drawn control block diagram by defining the sample period as T_s. Therefore, the closed-loop z-transfer function is obtained as:

$$G(z) = \frac{\frac{k \cdot i_D \cdot (K_p + K_i \cdot T_s)}{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)} \cdot z - \frac{k \cdot i_D \cdot K_p}{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}}{z^2 + (\frac{k \cdot i_D \cdot (K_p + K_i \cdot T_s)}{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)} - 1) \cdot z - \frac{k \cdot i_D \cdot K_p}{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}} \tag{5-17}$$

Further, the stability conditions can be derived in accordance with the Routh–Hurwitz stability criterion as:

$$\begin{cases} \frac{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}{k \cdot i_D} > K_p > -\frac{C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-)}{k \cdot i_D} \\ \frac{2 \cdot C_1 \cdot R_{X1} \cdot C_X \cdot (V_{th}^+ - V_{th}^-) - 2 \cdot k \cdot i_D \cdot K_p}{k \cdot i_D \cdot T_s} > K_i > 0 \end{cases} \tag{5-18}$$

Hence, Eq. (5-18) helps to choose K_p and K_i appropriately.

5.3. EXPERIMENTAL VERIFICATION OF VOLTAGE BALANCING

The hardware is developed in this section after the analysis mentioned before. As the self-powered unit presented in the upper right corner of Fig. 5-10, each individual SiC

MOSFET (G2R120MT33J, 3.3kV/24A) in this unit is attached with the suggested adaptive impedance self-powered GD, which combines the power extracting part and the gate driving part. Specifically, in the power extraction part, a printed circuit board (PCB) transformer is built to ensure the capacity to tolerate high voltages, as seen in the upper left of Fig. 5-10.

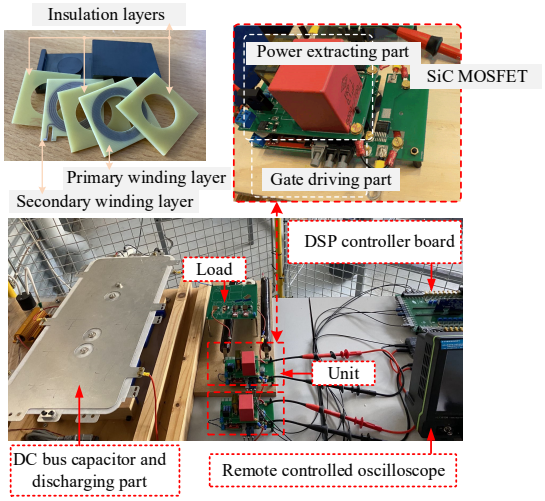


Figure 5-10. Testing platform photograph of a buck chopper circuit

Further, on the basis of the buck chopper circuit diagram shown in Fig. 5-7, the established experimental platform is presented in the bottom of Fig. 5-10.

5.3.1. PERFORMANCE OF THE ADAPTIVE-IMPEDANCE SNUBBER

Firstly, the designed pulse generator is verified for determining the correlation of $v_{C(i)}$ and $f_{(i)}$ (i = 1, 2) in Eq. (5-16). As shown in Fig. 5-11(a), T_{on} is maintained at 250 ns while $v_{C(i)}$ increases from 1 kV to 2 kV, and $f_{(i)}$ increases linearly from 26.6 kHz to 47.0 kHz, demonstrating the feasibility of the pulse generator as designed. As a result, in accordance with Eq. (5-5), it is also possible to acquire the computed r_V curve versus $v_{C(i)}$ (i = 1, 2), which implements the feature of the proposed self-powered GD's adaptive impedance. Since 1 kV to 2 kV is also the GD's intended operating range in this prototype, Fig. 5-11(b) shows the estimated power loss curve of the "snubber" versus $v_{C(i)}$. Additionally, the output power of the power extracting part is vital for providing the power of the following gate driving part, and thus the corresponding curve versus $v_{C(i)}$ is also provided. It is concluded that a significant amount of power is lost for VB purposes, and this low efficiency mode is caused by the gate driving part's low input power need.

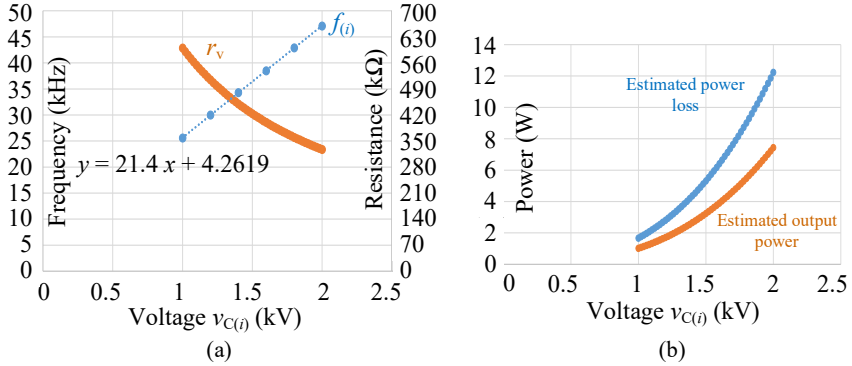


Figure 5-11. (a) correlation between $f_{(i)}$ (r_V) and $v_{C(i)}$ (b) estimated power loss and estimated output power versus $v_{C(i)}$

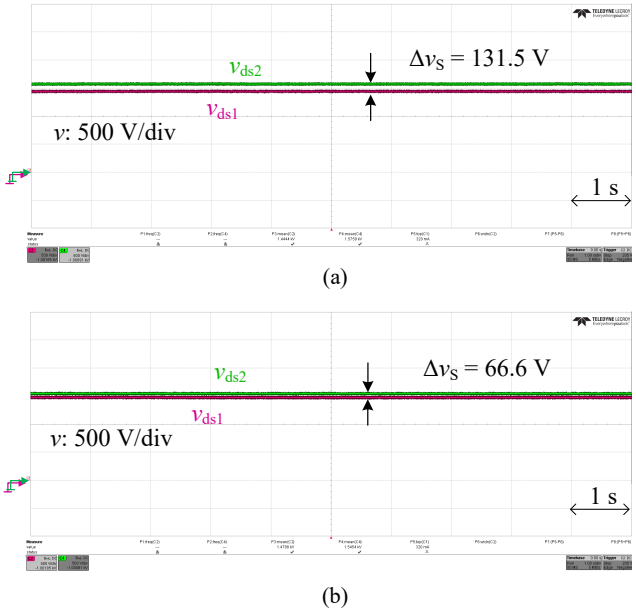


Figure 5-12. Static voltage balancing performance equipped with (a) the conventional snubber (case 1 & case 2), (b) the proposed adaptive-impedance "snubber" (case 3)

By using a fixed DC voltage source to replace the connection on the input side of the pulse generator in Fig. 5-5, the output voltage pulse will have preset and fixed on time and frequency. Therefore, the self-powered GD will be operated in a linear-

impedance mode for static VB as in *case* 2, which can be equivalent to the traditional VB resistor approach as in *case* 1. In this study, to make the comparison evident in experiments, an extra resistor is connected parallelly with S_1 to simulate the significant difference between the leakage currents of S_1 and S_2. In addition, 36.4 kHz is set as the frequency in *case* 2 to align with Fig. 5-11 while $V_{DC(max)}$ is set to be 3 kV by taking the safety margin into consideration. Based on that, Fig. 5-12(a) presents its static VB performance in *case* 2, and it can be observed that, when V_{DC} is 3 kV, the voltage unbalancing Δv_S is 131.5 V. As designed, the computed static power losses of S_1 and S_2 are respectively 4.76 W and 6.12 W, and their summation P_S is 10.88 W.

By contrast, Fig. 5-12(b) presents the static VB performance when equipping the adaptive-impedance self-powered GD in the series-connection as in *case* 3. When V_{DC} reaches 3 kV, it is seen that Δv_S is lowered to 66.6V. The flyback converter in the power extracting part of this GD is operating at close to 36.4 kHz in both *case* 3 and *case* 2 (*case* 1). Specifically, since the calculated static power losses of S_1 and S_2 are respectively 5.10 W and 5.79 W, P_S in *case* 3 is calculated to be 10.89 W. Hence, P_S is almost identical in both cases. Meanwhile, Δv_S in *case* 3 is 49.4% lower than in *case* 2 (*case* 1), which is thought to be in agreement with the 50% that was examined in analysis. Thus, the loss P_S in *case* 3 is half as in *case* 2 (*case* 1) when V_{DC} is the half of 3 kV, while Δv_S is about the same. As a result, a superior trade-off of loss and VB in the static state is demonstrated by the presented adaptive-impedance self-powered GD.

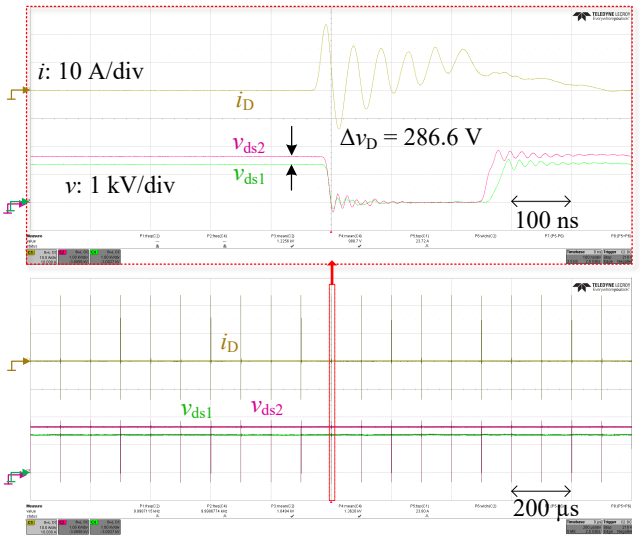


Figure 5-13. Dynamic voltage balancing performance equipped with the traditional snubber (case 1 & case 2)

The adaptive-impedance "snubber" can also aid in decreasing the dynamic voltage unbalancing brought on by the inconsistencies of device characteristics, GDs, etc. as S_1 and S_2 are continuously switching. Maintaining the identical parameter setting as the above GD design, in *case* 2 (*case* 1) presented in Fig. 5-13, under V_{DC} = 3 kV, f_s = 10 kHz and i_D = 15 A, the "snubber" operating in the traditional linear-impedance mode can lower the voltage unbalancing Δv_D to 286.6V according to the measurement. By comparison, in *case* 3 as depicted in Fig. 5-14, the proposed adaptive-impedance self-powered GD can lower Δv_D to 177.0 V. As a result, when V_{DC} is set to 3 kV, Δv_D in *case* 3 is decreased by 38.2% compared to *case* 2 (*case* 1), while the loss P_D is almost identical as the power losses are calculated to be respectively 11.02 W and 10.96 W. Since some approximations are used in the theoretical study, it is a little bit greater than the 33.3% that was examined in analysis. In conclusion, it has been demonstrated that a better trade-off of loss and VB can also be attained in dynamic situations.

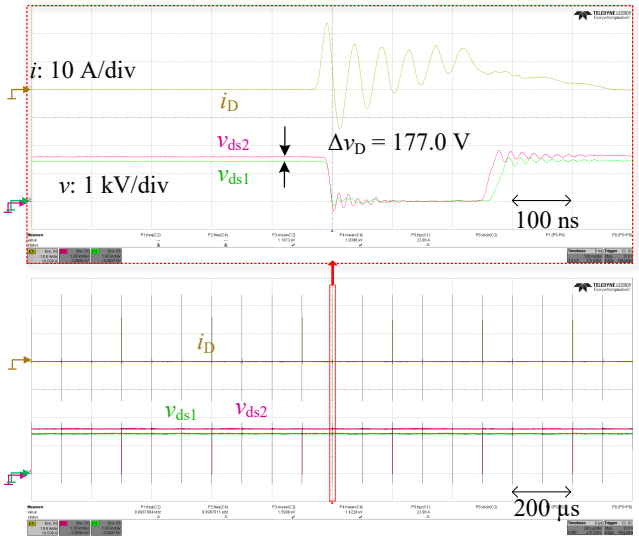


Figure 5-14. Dynamic voltage balancing performance equipped with the proposed adaptive-impedance "snubber" (case 3)

5.3.2. PERFORMANCE OF THE HYBRID VOLTAGE BALANCING STRATEGY

Based on the above, it becomes clear that, roughly 11 W of power loss is still needed to lower voltage unbalancing to 177 V even when using the proposed adaptive-impedance "snubber" optimization in this prototype, which illustrates that passive VB schemes must pay this price for the less complexity and better robustness. If GDs

inconsistence, device characteristics discrepancy, etc. are worse, tens of watts or even higher of power loss will be required for VB. Therefore, if the control complexity is cared less, an active delay control method can be united with the proposed passive "snubber" for getting a well-balanced voltage distribution performance together with less power loss.

In this manner, by capturing $f_{(i)}$ (i = 1, 2) feedbacks sent from the suggested GDs, the external DSP controller can make the calculation in time and an accurate delay compensation can be provided to S_2 during the turning-off process. As discussed, once the converter is constructed, the criterion for stability is achieved in accordance with Eq. (5-18) and no experimental identification is necessary. Therefore, the proper choosing range for K_p and K_i can be determined as the detail provided in **Publication I**, and the instability problem during the VB control can be avoided.

As a result, an excellent VB performance of S_1 and S_2 can be obtained since Δv_D is measured to be 19.9 V, as shown in Fig. 5-15. Significantly, the proposed GD does not affect the SiC MOSFET's switching speed and it simply takes in the voltage overshoot once $v_{DS(i)}$ (i = 1, 2) surpasses its clamping value. Moreover, the switching speed is also not slowed down by the active delay control approach as the dv/dt of S_i (i =1, 2) is measured to reach 110 kV/µs. As a result, the suggested hybrid VB technique helps to keep the benefit of the SiC device and leads to a minimal switching loss.

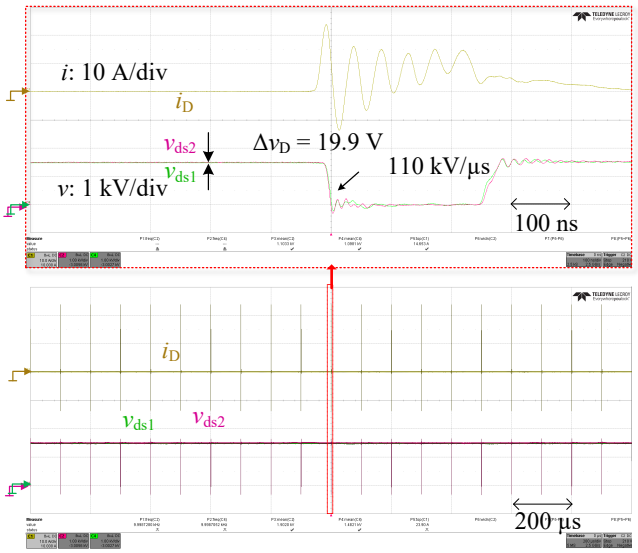


Figure 5-15. Dynamic voltage balancing performance with the proposed hybrid strategy

5.3.3. EXPERIMENTAL VERIFICATION IN DC TO AC CONVERSION

It is worth noting that, the above VB strategy is suitable in DC to DC conversion since the power loop current during every switching transient is constant when the converter is running in the stable state, which provides a basis for the active delay control method. When it comes to DC to AC conversion, the continuously changing power loop current results in performance of the above VB strategy not as good as in the DC to DC conversion. To tackle this issue, additionally compensation capacitors placed in the power side were proposed to optimize the VB performance in [17], however, it requires some customized design. Therefore, a proper choice of series-connection of power devices in DC to AC conversion is using the topology as depicted in Fig. 1-2.

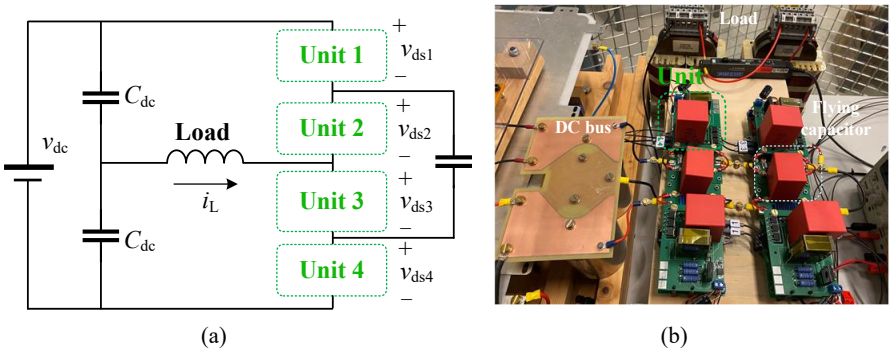


Figure 5-16. Testing platform of a half-bridge circuit: (a) schematic (b) photograph

Further, in this study, the proposed self-powered GD without adaptive-impedance and VB optimization is verified in DC to AC conversion, and the main topology is presented in Fig. 5-16(a). Only four units, which consist of MV SiC MOSFETs (G2R120MT33J, 3.3kV/24A) and its self-powered GDs, are series connected to form this half-bridge circuit, with an inductor placed in the middle as the load. Specifically, in this case, an additional resistor is placed in the series connection with the clamping diode to lower the diode's current requirement and prevent its breaking down. In addition, a 100 nF flying capacitor is used to avoid the transient voltage unbalancing. Based on that, the experimental platform is built as shown in Fig. 5-16(b).

With the sinusoidal pulse width modulation (SPWM) used on this half bridge, S_i (i =1 ~4) could experience hard switching if the load current i_L does not change its direction throughout the turning-on process. When S_i switches at 10 kHz, as seen in Fig. 5-17, both hard switching and soft switching cases can be observed. Since i_L is low, voltage overshoots of v_{ds1} and v_{ds2} are small during the turning-off process, and the observed voltage overshoots highlighted in Fig. 5-17 are brought on by the rapid turning-on of S_3 and S_4 (hard-switching). It can be observed that i_L has a sinusoidal

tendency and a significant current ripple. In addition, the enormous current spikes that result from the inductor load's parasitic capacitance and the high *dv/dt* during hard switching process can be seen. Significantly, the effective VB performance of v_{ds1} and v_{ds2} is further demonstrated owing to the flying capacitor.

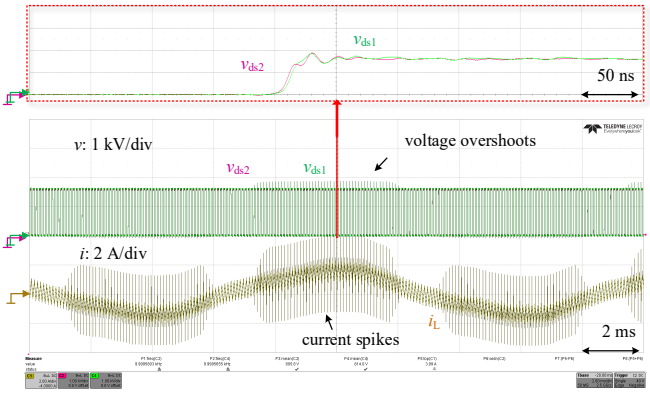
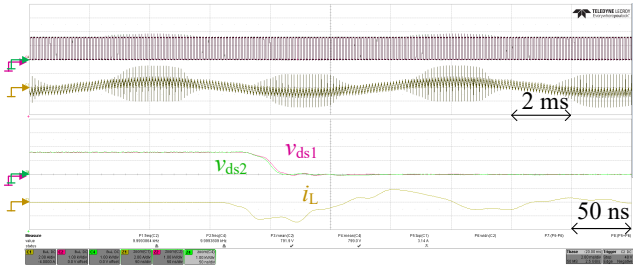
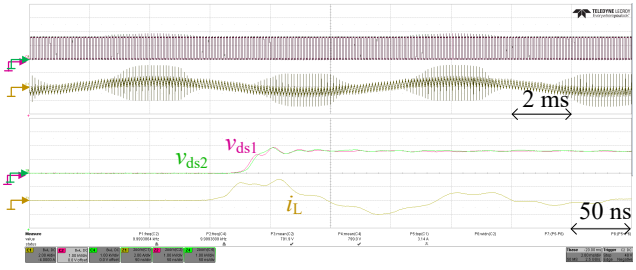


Figure 5-17. Voltage balancing with sinusoidal pulse width modulation



(a)



(b)

Figure 5-18. Performance of direct series-connection: (a) turning-on (b) turning-off process

In practice, above experimental results are in the case of direct series-connection since the synchronous switching is adopted. With the topology depicted in Fig. 5-16(a), the experimental results in the case of indirect series-connection can also been obtained, since it is a prevalent topology used in indirect series-connection as mentioned in Chapter 1. Therefore, the comparison is also given as follows.

Since the capacitance of this flying capacitor is small, the testing conditions are direct series-connection and quasi-two-level indirect series-connection. In the case of direct series-connection, the voltage rising and falling of two SiC MOSFETs are basically synchronous, as presented in Fig. 5-18. By contrast, there is an obvious delay in the indirect series-connection as presented in Fig. 5-19. The advantage of this quasi-two-level modulation is that the total *dv/dt* becomes smaller, and it can be observed that the displacement current flowing through the load inductance is also reduced accordingly. The disadvantage is that as the current increases, the required capacitance of the flying capacitor will be larger. When the capacitance value is large enough, the tolerated delay duration can be much longer, and three-level modulation becomes available.

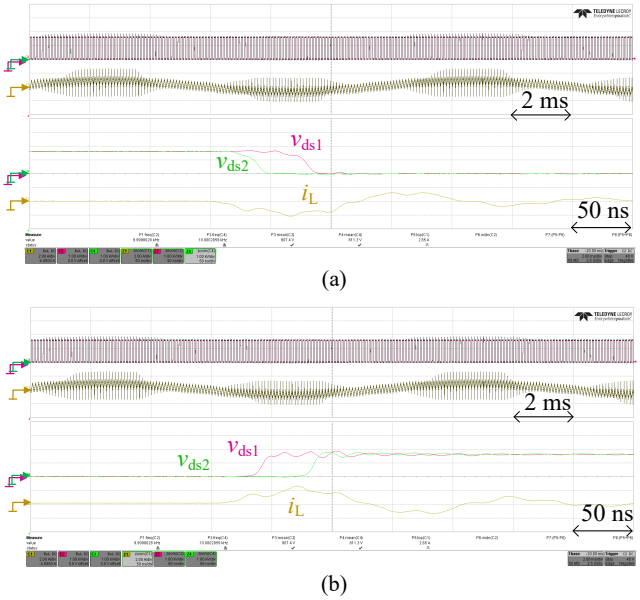


Figure 5-19. Performance of indirect series-connection: (a) turning-on (b) turning-off process

CHAPTER 6. CONCLUSION AND FUTURE WORK

6.1. CONCLUSION

Medium voltage (MV) SiC MOSFETs contribute to the topology simplification and performance optimization of MV converter design. Regarding of the corresponding hardware design challenges, this thesis focuses on issues of the gate driver and series-connection of MV SiC MOSFETs, and a thorough review is provided in Chapter 1. Further, series-connection in this thesis is divided into two categories as direct series-connection and indirect series-connection, where the former one is aiming at the synchronous switching of all series-connected power devices, and the latter one is aiming at less EMI issue and lower filter requirement by the asynchronous switching.

Based on that, the main research contributions of the thesis can be summarized as:

- A single gate-driven SiC MOSFET stack topology is proposed for high-input-voltage and low-output-power applications, which is applied in the self-powered auxiliary power supply design in some indirect series-connection situations like modular multi-level converters (MMCs). It has the advantage of simplified gate drivers of SiC MOSFET stack and automatic balancing of voltages with the aid of a low-loss passive snubber. The single gate-driven stack also possesses the potential capability of anti-short circuit, therefore, its short-circuit characteristic is further studied. On this basis, by adding the auxiliary components in the gate driver side, the stack is improved to have anti-short circuit capabilities in both short-circuit occasions of hard switch fault (HSF) and fault under load (FUL).

- A self-powered gate driver with converter-based design is proposed and combined with MV SiC MOSFET as a unit, which excludes the external auxiliary power supply. In this manner, the common mode path from the gate driver to the ground is eliminated, and the isolation requirement is decreased from the total bus voltage to a single unit. This configuration to MV SiC MOSFET makes the dissipated power in the snubber recycled to power the gate driving part, and it is scalable to the series-connection of MV SiC MOSFETs.

- The effectiveness of the proposed self-powered gate driver is experimentally verified on both occasions of DC to DC and DC to AC conversion. Based on that, the adaptive-impedance optimization of the self-powered gate driver is proposed and verified in DC to DC conversion. As an adaptive-impedance

"snubber", it shows a better tradeoff of the loss and voltage balancing of the series-connected MV SiC MOSFETs, in both the static and dynamic conditions. Further, for obtaining a better dynamic voltage balancing performance, the adaptive-impedance "snubber" can be combined with the active delay control method, where the parameter selection criteria become easier to obtain owing to the identified model.

6.2. FUTURE WORK

The effectiveness of proposed self-powered gate driver (GD) with converter-based design has been verified both in DC to DC and DC to AC scenarios. However, there are still many details to be perfected in the self-powered GD to ensure its reliable driving and protection of SiC MOSFETs:

- With the series count of power devices increasing, the problem of temporary voltage oscillation caused by the inconsistency in timing of self-powered GD startup becomes more and more worthy of attention and has become a potential threat to reliability as mentioned. Therefore, it is necessary to conduct an in-depth assessment of this oscillation and propose a solution.

- The normal operation of the self-powered GD only allows the bus voltage to fluctuate within the preset range, and there is also a limitation on the maximum duty cycle of pulse width modulation as mentioned. Therefore, a reasonable fault detection circuit should be configured. If the bus voltage fluctuation exceeds this range or the drive output power is insufficient, a fault signal should be received by the controller in time for shutdown protection.

In addition, the self-powered GD itself has the converter characteristics and possesses the advantage of high output power, making it possible to configure advanced and complex protection circuits with high power consumption:

- The short-circuit protection function of the power device is significant in the GD design for ensuring the safe operation of converter and apparatus, also the personal safety nearby. For this reason, based on the proposed self-powered GD, functions such as short-circuit protection can be embedded inside. In the meantime, considering the short-circuit withstand time of SiC MOSFET, the response time of short-circuit protection should be optimized.

- In recent years, more and more attention has been paid to the reliability and life evaluation of power semiconductor devices. Relying on the self-powered GD, status monitoring circuits of power device such as junction temperature monitoring circuits and on-state voltage drop detection circuits can be integrated into the GD design.

On the basis of the above characteristics, SiC MOSFET devices, gate driving, power supply, monitoring, protection and other functions will be integrated into one unit to form an intelligent power module. As shown in Figure 6-1, only two power terminals D and S are used for connection of the main circuit. The switching signal from the controller is received through an optical fiber interface, and the on/off of the SiC MOSFET can be controlled in real time. In addition, there is an optical fiber interface to send the information of the intelligent power module, including fault information and status monitoring information.

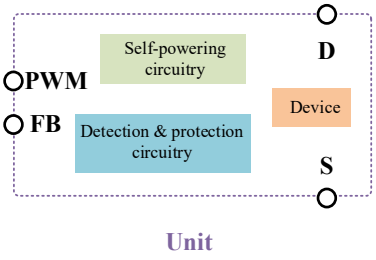


Figure 6-1. Schematic of the intelligent power module

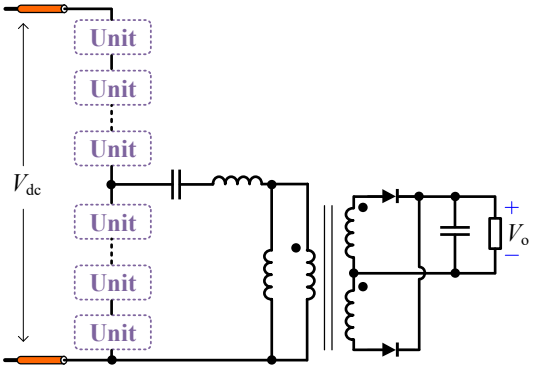


Figure 6-2. Schematic of series-connection-based LLC resonant converter

Afterwards, by a reasonable and compact layout, the intelligent power module can be directly applied in some MV high-power DC to DC scenarios, such as LLC resonant converters with direct series-connection of power devices, as depicted in Fig. 6-2, providing a reliable and stable interface for applications based on direct power acquisition from the medium-voltage grid, such as power supply for high power data centers, fast chargers, electrolysis plants, etc.

APPENDICES

Appendix A. Bibliography

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Appendix B. Publications

ISSN (online): 2446-1636
ISBN (online): 978-87-7573-713-0

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