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The Trade-off of Switching Losses and EMI Generation for SiC MOSFET with Common Source and Kelvin Source Configurations

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Index Terms—Silicon carbide (SiC), SiC MOSFET, electromagnetic interference (EMI), Kelvin source.

Abstract—In this paper, the characteristics of dI_D/dt , dV_{DS}/dt and oscillations for 3-pin and 4-pin MOSFETs using Kelvin source and common source configuration are experimentally identified. With theoretical analysis and spice simulation utilized, the common source inductance-induced negative feedback mechanism is investigated. A quantitative analysis is also performed to reveal the trade-off between switching losses and EMI generation between 3-pin and 4-pin MOSFETs.

I. INTRODUCTION

Silicon carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET) is a promising candidate for next-generation power device. The traditional packages with common source configurations are cheap and mature. Due to the merits, the packages are widely used for SiC MOSFET. In the common source configuration, the common source inductance L_S is shared by the gate loop and power loop, as shown in Fig. 1a. The dI/dt in the power loop generates a voltage drop across the L_S , which can hinder the gate voltage to turn off and turn on when L_S is few nanohenries [1]. This greatly limits the switching speed of the SiC MOSFET [2].

To improve the switching speed of the SiC MOSFETs, a new package with the kelvin source configuration was introduced, as shown in 1b. The configuration has an additional Kelvin source pin, which directly connects the source-side metallization layer on the chip. When the additional Kelvin source pin is connected to the gate loop, the voltage on the inductor L_S does not have any impact on the gate loop. With the kelvin source configuration utilized, the SiC MOSFET can achieve much higher switching speed and lower switching losses than that using common source configuration [2]. However, the fast switching induced by the kelvin source can give rise to very high dV/dt , dI/dt and

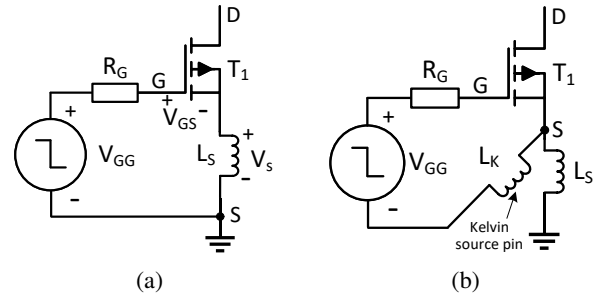


Fig. 1. The SiC MOSFET with (a) common source configuration and (b) kelvin source configuration.

high-frequency voltage and current oscillations [3], [4]. The high dV/dt , dI/dt generate common-mode and differential-mode electromagnetic interference (EMI) [5], [6]. The high level of EMI noise induces electromagnetic compatibility (EMC) problems for power converters and can destroy the device in the worst-case scenario [7].

Unfortunately, looking into the previous research [2], [8], [9], the impact of the Kelvin source and common source configuration on the dV/dt , dI/dt as well as EMI generation receive scarcely attention. In [2], the impact of the Kelvin source configuration on the switching speed and switching losses is investigated. In [8], the package design of the multi-chip SiC MOSFET module using Kelvin source configuration is presented. The papers [9] investigate the current unbalance between the parallel connected MOSFETs with Kelvin source configuration as well as related mitigation methods. Since the EMI noise can induce severe reliability problems, it is necessary to study the EMI generation of the SiC MOSFET with the common source and Kelvin source configurations.

In this paper, the EMI generation of SiC MOSFET using common source and Kelvin source configurations is investigated. The trade-off relationships between

switching losses and EMI generation for the two configurations are also identified.

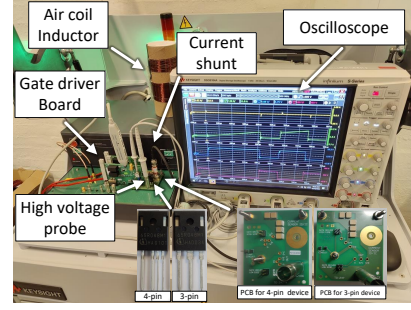
II. COMPARISON ON THE SWITCHING CHARACTERISTICS OF THE 4-PIN AND 3-PIN SiC MOSFETs

In this study, the double-pulse test is utilized to obtain the switching characteristics of SiC MOSFET. Fig. 2 shows the double-pulse test platform and its equivalent test circuit. In the test circuit, the device under test (DUT) is the low-side MOSFET T_1 . The high-side MOSFET T_2 is turned off and its anti-parallel diode is utilized as a freewheeling diode in the test. R_G is the external gate resistor. V_{DC} is the DC-bus voltage, which is connected to a capacitor C_{DC} . An air coil inductor $L_0 = 190\mu H$ is used as a load inductor. Two gate driver board is mounted to a main PCB board, which generate gate drive voltage V_{gg} at the low side and off-state voltage $V_{gg(off)}$ at the high side. To test SiC MOSFETs with common source and kelvin source configurations, two PCB boards designed for TO-247-3 and TO-247-4 packaged SiC MOSFETs are utilized. In the test, two SiC MOSFETs IMZA65R048M1H and IMW65R048M1H are utilized as DUT. IMZA65R048M1H is a 4-pin TO-247-4 packaged SiC MOSFET using Kelvin source configuration. The TO-247-3 packaged IMW65R048M1H is a 3-pin SiC MOSFET that utilizes conventional common source configuration. The chips used in the IMW65R048M1H and IMZA65R048M1H are the same. In the test, the same gate driver board is used for two devices. The power loop inductances of the two main PCB boards are also in the same range (40-50 nH).

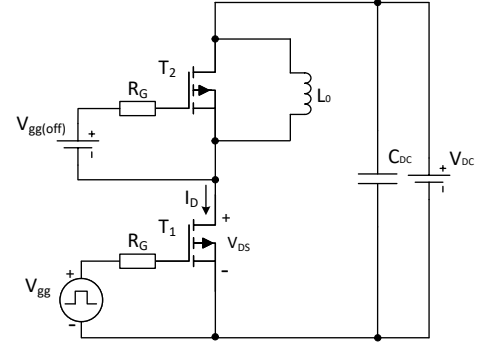
The double-pulse test is performed with DC-bus voltage $V_{DC} = 400V$ and load current $I_L = 20A$ using $R_G = 10\Omega$ and $R_G = 50\Omega$. The experimental turn-on and turn-off waveforms of 4-pin and 3-pin MOSFETs are compared, as shown in Figs. 3, 4, 5 and 6. The turn-off and turn-on transient is divided into various phases, which are marked in blue (for 4-pin devices), red (for 3-pin devices) and black (for both 3-pin and 4-pin devices).

Fig. 3 compares experimental turn-on waveforms of 4-pin and 3-pin MOSFETs using $R_G = 10\Omega$. The turn-on transient is divided into phases 1 and 2. In phase 1, the drain current I_D increase from zero to its peak value. With the kelvin source configuration utilized, the 4-pin MOSFET has a much larger dI_D/dt than that of the 3-pin MOSFET in phase 1. The larger dI_D/dt also gives rise to a much higher current overshoot for 4-pin MOSFET.

It should be noticed that the V_{DS} reduction is an indicator of dI/dt in phase 1, as shown in Fig. 3. This



(a) The test platform.



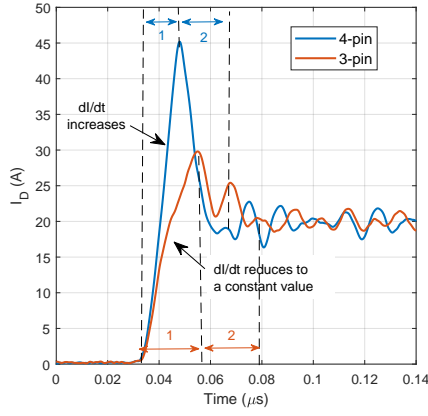
(b) The schematic circuit.

Fig. 2. Double-pulse test fixture. (a) Test platform. (b) Double-pulse test circuit.

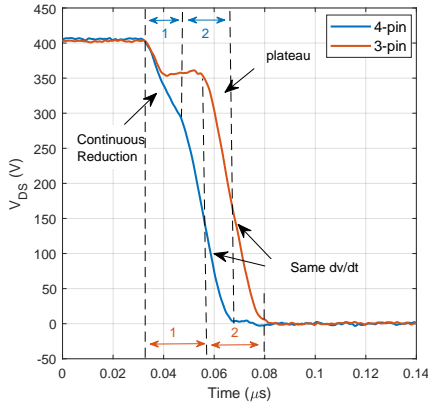
is because V_{DS} reduces in phase 1 due to the voltage drop on the power loop inductance generated by dI_D/dt . For 4-pin MOSFET, its V_{DS} reduces continuously, this shows dI_D/dt increases in phase 1. For 3-pin MOSFET, its V_{DS} of reduces initially and plateaus at a constant value in the end. The dI_D/dt of 3-pin MOSFET thereby increases in the beginning and is clamped at a constant value at the end of phase 1.

In phase 2, the I_D drop from its peak value to the load current, as shown in Fig. 3. In this phase, the reverse current of high-side MOSFET T_2 is supported by its residual charge in the N-base. With the same chip and test conditions used, the charge should be the same for the two kinds of MOSFET. However, with a much higher peak current, the N-base charge is very hard to support such high reverse current for 4-pin MOSFET. Its dI_D/dt thereby becomes much higher than that of the 3-pin MOSFET. In phase 2, the dV_{DS}/dt of 3-pin and 4-pin MOSFETs are similar since the device has the same I-V and C-V characteristics.

Fig. 4 shows the turn-on waveforms of 4-pin and 3-pin MOSFETs with $R_G = 50\Omega$. With a large resistor, the dI_D/dt is thereby much lower than that using $R_G = 10\Omega$. However the dI_D/dt of 4-pin MOSFETs is still significantly larger than that of the 3-pin MOSFETs.



(a)

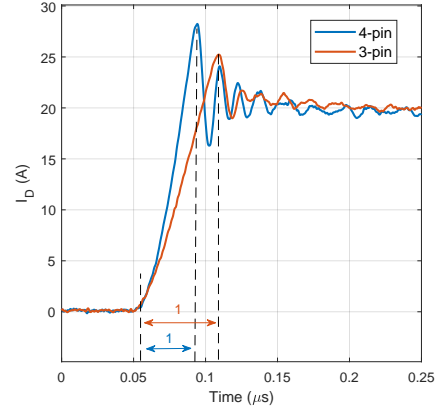


(b)

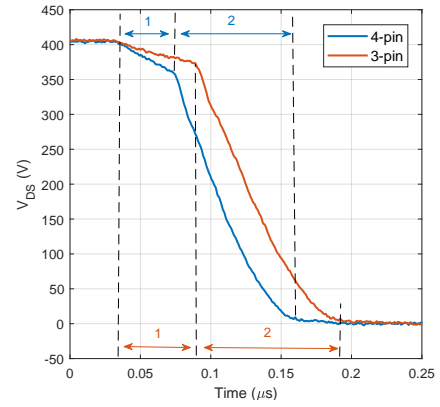
Fig. 3. Comparison of the experimental turn-on waveforms of 4-pin and 3-pin SiC MOSFETs using $R_G = 10\Omega$: (a) I_D waveforms. (b) V_{DS} waveforms.

With low dI_D/dt , the voltage generated on the power loop inductance becomes very small. This induces a very small V_{DS} reduction in phase 1 for the 4-pin and 3-pin MOSFET, as shown in Fig. 4. The dV_{DS}/dt of 4-pin and 3-pin MOSFET in phase 1 is thereby very small. The V_{DS} plateau of 3-pin MOSFET presented in Fig. 3 also vanishes. As a result, the dV_{DS}/dt of 4-pin MOSFET is only slightly larger than that of 3-pin MOSFETs in phase 2. The difference of 4-pin and 3-pin MOSFETs on the dV_{DS}/dt significantly reduces compared to that presented in Fig. 3 using $R_G = 10\Omega$.

Fig. 5 compares the experimental turn-off waveforms of 4-pin and 3-pin MOSFETs using $R_G = 10\Omega$. The turn-off transient is divided into phases 3 and 4. In phase 3, the V_{DS} increases from its on-state voltage to V_{DC} . In this phase, the high-side freewheel diode is reverse biased and can not conduct current, the I_D reduction is due to the $C_{OSS2}dV/dt$ induce displacement current on the high-side MOSFET T_2 . C_{OSS2} is the output capacitance of T_2 . Since T_2 has to support high voltage



(a)



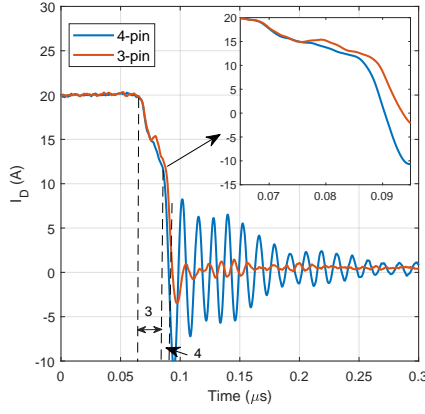
(b)

Fig. 4. Comparison of the experimental turn-on waveforms of 4-pin and 3-pin SiC MOSFETs using $R_G = 50\Omega$: (a) I_D waveforms. (b) V_{DS} waveforms.

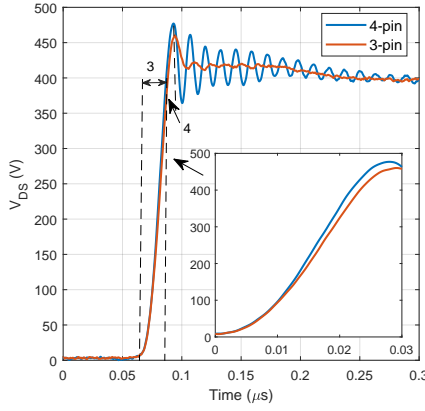
until the end of this phase, C_{OSS2} is small. As a result, dI_D/dt in this phase is relatively low in phase 3 for both 4-pin and 3-pin MOSFET. This gives rise to a low voltage $L_S dI_D/dt$ across the L_S . The impact of L_S on the turn-off speed in phase 3 is thereby very weak. As a result, the dI_D/dt and dV_{DS}/dt of 3-pin MOSFET is only slightly lower than that of the 4-pin MOSFET in phase 3.

In phase 4, the V_{DS} increases from V_{DC} to its peak value. In this phase, the high-side freewheel diode starts to forward conduct, the load current thereby transfers from the T_1 to the high-side freewheeling diode, which gives rise to the abrupt reduction of I_D . With high dI_D/dt , the L_S significantly slows down the turn-off speed. The dI_D/dt and dV_{DS}/dt of 3-pin MOSFET is significantly lower than that of 4-pin MOSFET, as shown in Fig. 5.

When phase 4 ends, the T_1 turns off and the turn-off oscillation is excited. With the kelvin source utilized, the turn-off oscillation of the 4-pin MOSFET is much



(a)



(b)

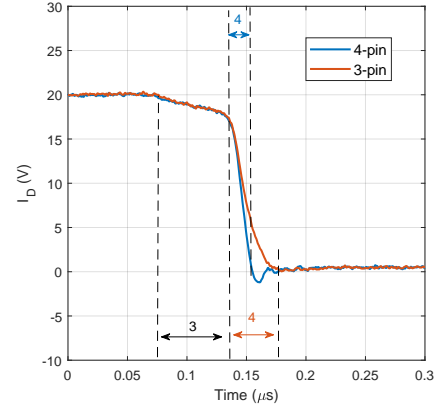
Fig. 5. Comparison of the experimental turn-off waveforms of 4-pin and 3-pin SiC MOSFETs using $R_G = 10\Omega$: (a) I_D waveforms. (b) V_{DS} waveforms.

more underdamped than that of the 3-pin MOSFET. This phenomenon shows that the L_S has a significant damping effect on the turn-off oscillation.

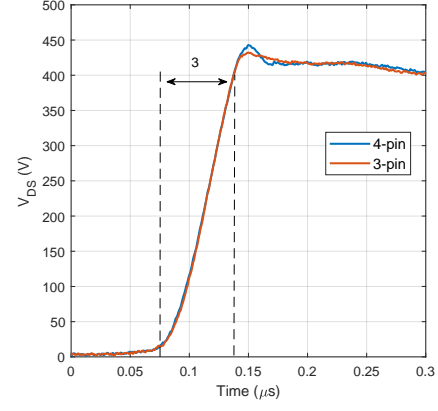
Fig. 6 compares experimental turn-off waveforms of 4-pin and 3-pin MOSFETs using $R_G = 50\Omega$. With a large gate resistor, the dV_{DS}/dt significantly decreases. This gives rise to the reduction $C_{OSS}dV/dt$ induced displacement current and the I_D reduction in phase 3 becomes very small. With very low dI_D/dt , the impact of L_S in phase 3 becomes negligible. The dI_D/dt and dV_{DS}/dt of 3-pin and 4-pin MOSFET thereby become identical in phase 1.

In phase 4, I_D abruptly decreases. With high dI_D/dt , the L_S can significantly slow down the turn-off speed. As shown in Fig. 5, the dI_D/dt of 4-pin MOSFET is thereby much higher than that of the 3-pin MOSFET.

All in all, the dI_D/dt of the 3-pin MOSFET is greatly slowed down compared to that of the 4-pin MOSFET due to the voltage $L_S dI_D/dt$ on L_S . However, the source configuration has a relatively minor impact



(a)



(b)

Fig. 6. Comparison of the experimental turn-off waveforms of 4-pin and 3-pin SiC MOSFETs using $R_G = 50\Omega$: (a) I_D waveforms. (b) V_{DS} waveforms.

on dV_{DS}/dt , especially in the case when large R_G is used. The common source configuration also has a huge impact on the turn-off voltage and current oscillations.

III. ANALYSIS ON THE IMPACT OF L_S ON THE dV_{DS}/dt , dI_D/dt AND SWITCHING OSCILLATION OF SiC MOSFET

In this section, the impact of L_S on the dV_{DS}/dt , dI_D/dt and switching oscillation of SiC MOSFET is investigated by theoretical analysis and SPICE simulation. Fig. 7 shows the simulation results. The circuit utilized in the simulation is shown in Fig. 8. In the circuit, $L_P = 40nH$ is the power loop inductance. $L_{G1} = L_{G2} = 10nH$ are the gate loop inductances. The gate resistors $R_G = 10\Omega$. To investigate the impact of the common source inductance L_S on the switching behaviour, various values of L_S which range from 0.4nH to 8nH are used. As shown in Fig. 7, when L_S becomes larger, the dI_D/dt at turn-off and turn-on transient become lower. The effective damping of the turn-off

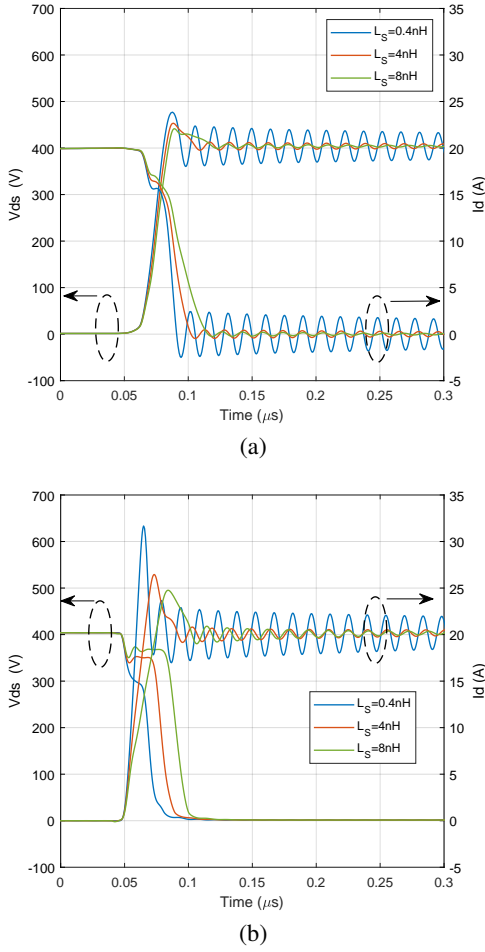


Fig. 7. Simulated 400V/20A switching waveforms using various L_s : (a) turn-off waveforms with $L_s = 0.4nH$, (b) turn-off waveforms with $L_s = 4nH$, (c) turn-off waveforms with $L_s = 8nH$, (d) turn-on waveforms with $L_s = 0.4nH$, (e) turn-on waveforms with $L_s = 4nH$, (f) turn-on waveforms with $L_s = 8nH$.

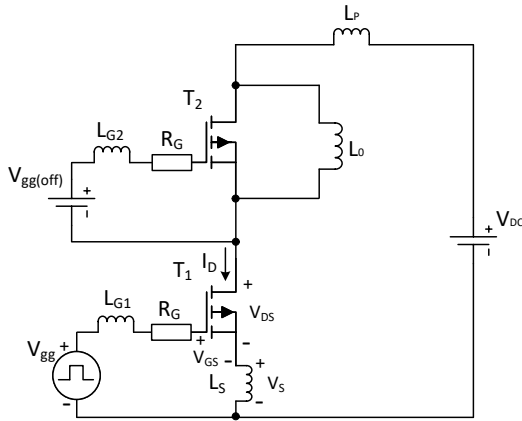


Fig. 8. The test circuit utilized for simulation.

oscillation also becomes stronger. The impact of L_s on the switching behaviour is captured by the simulation.

To clarify the impact of L_s on the switching behaviour, the voltage V_s on the L_s as well as its relationship with drain current I_D and gate-source voltage V_{GS} is investigated. Fig. 9 shows the simulated turn-on waveforms of I_D , V_{DS} , V_s and V_{GS} . As shown in Fig. 9a, in phase 1 of the turn-on transient, the positive dI_D/dt generates a high positive V_s . Similarly, in phase 4 of the turn-off transient, a large negative V_s is also generated by the negative dI_D/dt , as shown in Fig. 9b. As shown in Fig. 10, V_s contracts the V_{gs} , which hinders the gate voltage to turn off/on. This affect the I_D since the I_D is controlled by $G_m V_{gs}$. The I_D in return feedback to the V_s by $L_s dI_D/dt$. As a result, a negative feedback mechanism is thereby achieved.

The negative feedback can also be expressed analytically. During phase 1 of the turn-on transient and phase 4 of the turn-off transient, I_D can be expressed by:

$$I_D = G_m(V_{GS} - V_{th}) \quad (1)$$

Neglecting the dV_{DS}/dt , the gate current can be expressed as:

$$I_G = C_{iss} \frac{dV_{GS}}{dt} \quad (2)$$

Where C_{iss} is the input capacitance of the MOSFET.

In the gate loop, the following equation can thereby be obtained [10]:

$$V_{gg} = R_G I_G + V_{GS} + L_s \frac{dI_D}{dt} \quad (3)$$

Combining the (1-3), the dI_D/dt can be expressed as:

$$\frac{dI_D}{dt} = \frac{G_m(V_{gg} - V_{GS})}{R_G C_{iss} + G_m L_s} \quad (4)$$

The term $G_m L_s$ in the denominator reflects the influence of L_s on the dI_D/dt due to the negative feedback mechanism.

Fig. 9c shows the zoomed turn-off oscillation waveforms of I_D , V_{DS} , V_s and V_{GS} . During the oscillatory transient, the V_s and V_{GS} always has opposite phase shift. This shows the negative feedback mechanism presented in Fig. 10 also occurs during the turn-off oscillatory transient. Due to the negative feedback mechanism, the L_s has a significant damping effect on the turn-off oscillation. Therefore, the turn-off oscillation of 3-pin MOSFET has much more effective damping than that of 4-pin MOSFET.

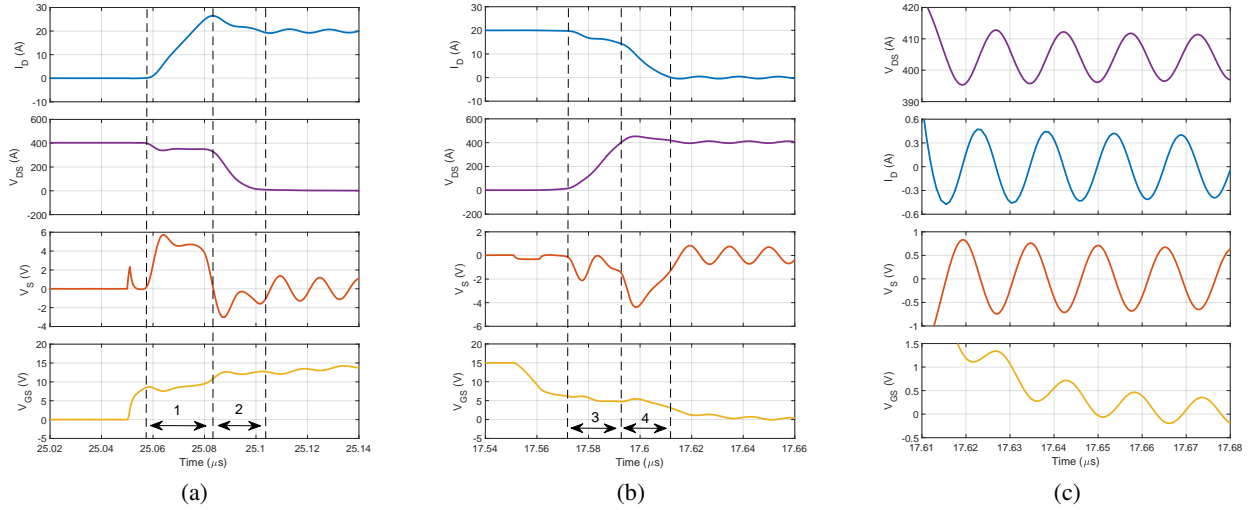


Fig. 9. Simulated I_D , V_{DS} , V_s and V_{GS} waveforms of (a) turn-on, (b) turn-off and (c) turn-off oscillation when $L_S = 4nH$.

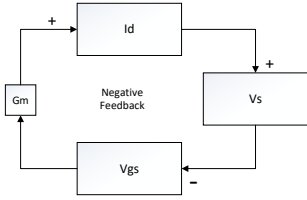


Fig. 10. The negative feedback mechanism.

IV. THE TRADE-OFF OF THE SWITCHING LOSSES AND EMI GENERATION FOR THE 4-PIN AND 3-PIN SiC MOSFET

In this section, the spectral magnitudes of V_{DS} and I_D waveforms are obtained using Fast Fourier transform (FFT). Figs. 11 and 12 show the spectral amplitudes of I_D and V_{DS} for 4-pin and 3-pin SiC MOSFET when R_G is 10Ω and 50Ω . The spectral envelopes are plotted in black for clarity.

In Fig. 11, the current spectra of 4-pin and 3-pin MOSFETs with 10Ω and 50Ω of R_G utilize. The current spectra indicate the levels of differential-mode noise generation. Due to the negative feedback induced by the L_S , the 3-pin MOSFET has a much lower dI_D/dt than that of the 4-pin MOSFET. As a result, when $R_G = 10\Omega$, the current spectral amplitude of 4-pin MOSFET is 1-14 dB higher compared to that of the 3-pin MOSFET at 10-90 MHz. A current spectrum peak also appears at 70-80 MHz for the 4-pin MOSFET due to the current oscillation. The spectrum peak is 14 dB higher than that of the 3-pin MOSFET. When $R_G = 50\Omega$, the current oscillation is suppressed. As a result, the spectrum peak of the 4-pin MOSFET greatly reduces and is only 7 dB

higher than that of the 3-pin MOSFET.

Fig. 12 shows the Fast Fourier Transform (FFT) computed V_{DS} spectral amplitudes of 4-pin and 3-pin MOSFETs when R_G is 10Ω and 50Ω . The voltage spectra indicate the levels of common-mode noise generation. As shown in Fig. 12a, the voltage spectral amplitude of 4-pin MOSFET is 1-14 dB higher than that of the 3-pin MOSFET at 30-100 MHz when R_G is 10Ω . A voltage spectrum peak also appears at 60-70 MHz for the 4-pin MOSFET due to the voltage oscillation at the turn-off transient. When the R_G increases to 50Ω , the spectrum peak of 4-pin MOSFET is mitigated since the large R_G greatly dampened the turn-off oscillation. The spectral amplitude of the 4-pin MOSFET becomes only 1-4 dB higher than that of the 3-pin MOSFET at 15-35 MHz.

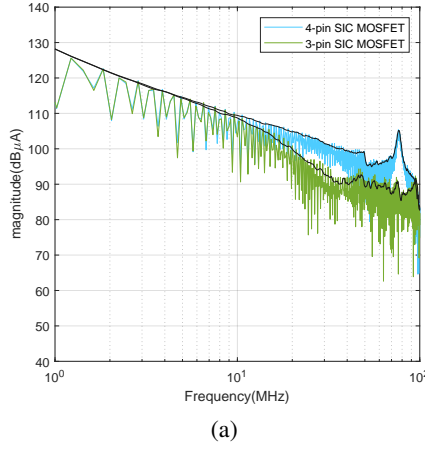
To qualitatively identify the high-frequency components V_{DS} and I_D waveforms, the power of high-frequency spectral content can be used as a metric [11], [12]. The power P_i (in decibel-milliwatt) dissipated by each current spectral amplitude component i (in decibel-microamps) on a load R_L can be calculated by:

$$P_i = i + 10\log_{10}(R_L) - 90 \quad (5)$$

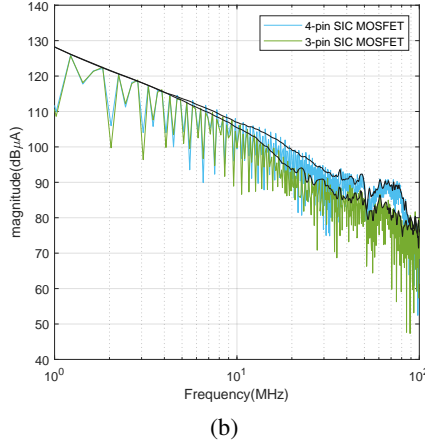
The power P_v (in decibel-milliwatt) dissipated by each voltage spectral amplitude component v (in decibel-microvolt) on a load R_L can be calculated by:

$$P_v = v - 10\log_{10}(R_L) - 90 \quad (6)$$

In this study, the average power P_{ai} and P_{av} within 10-100 MHz are used to reflect the high-frequency components on the spectra of V_{DS} and I_D . The P_{ai}



(a)

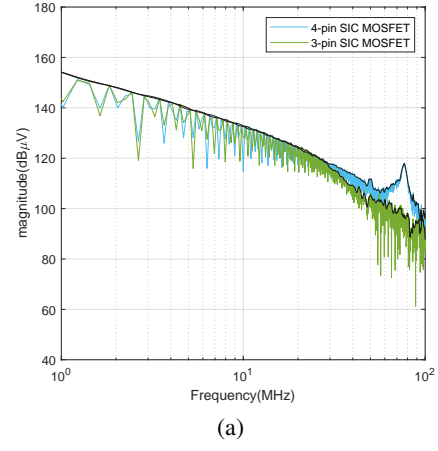


(b)

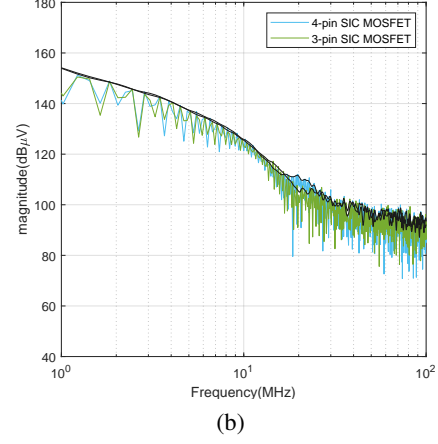
Fig. 11. Computed I_D spectral amplitudes of 4-pin and 3-pin SiC MOSFET using (a) $R_G = 10\Omega$ and (b) $R_G = 50\Omega$.

(P_{av}) is calculated by the mean of P_i (P_v) across 10-100 MHz utilizing a load $R_L = 50\Omega$. Fig. 13 shows the relationship between spectrum power and switching losses for the 3-pin and 4-pin MOSFETs at $V_{DC} = 400V$ and $I_L = 20A$ when R_G is 5 Ω , 10 Ω , 20 Ω , 30 Ω and 50 Ω . In Fig. 13, E_{on} is turn-on losses, E_{off} is turn-off losses and $E_{tot} = E_{on} + E_{off}$ is total power losses. With the increase of R_G , P_{ai} and P_{av} reduced at a cost of increased E_{on} , E_{off} and E_{tot} .

Compared to the 3-pin MOSFET, the 4-pin MOSFET always has a higher P_{ai} and P_{av} and lower E_{on} , E_{off} and E_{tot} at each R_G value. This gives rise to different trade-off relationships between spectrum power and switching losses for the 3-pin and 4-pin MOSFETs. As shown in Figs. 13a and 13b, the best trade-off between spectrum power (P_{ai} and P_{av}) and total power losses E_{tot} is achieved when R_G is 10 – 12 Ω for 3-pin MOSFET. For 4-pin MOSFET, the best trade-off of spectrum power and E_{tot} is achieved when R_G is 25 - 28 Ω . Figs. 13c - 13f also shows the trade-off of spectrum power (P_{ai} and P_{av}) and switching losses (E_{on} and E_{off}).



(a)



(b)

Fig. 12. Computed V_{DS} spectral amplitudes of 4-pin and 3-pin SiC MOSFET using (a) $R_G = 10\Omega$ and (b) $R_G = 50\Omega$.

Since the turn-on losses are the major part of the total power losses, the trade-off presented in Figs. 13a and 13b for the total power losses are mainly determined by the trade-off relationship of spectrum power and turn-on losses, as shown in Figs. 13c and 13d. For this case study, by looking at Figs. 13c - 13f, it would be also beneficial to select turn-on gate resistance $R_{G(on)}$ and turn-off gate resistance $R_{G(off)}$ differently to achieve an optimized trade-off between losses and voltage spectra power for 3-pin MOSFET.

V. CONCLUSION

The common source inductance induces negative feedback between the power loop and gate loop for the 3-pin MOSFET. The negative feedback action slows down the dI_D/dt , causing the reduction of dV_{DS}/dt at phase 1 and damps turn-off oscillation. Due to the negative feedback, the 3-pin and 4-pin MOSFETs have a different trade-off on switching loss and EMI noise generation. For 3-pin MOSFET under test, the best trade-off can be achieved when R_G is 10 - 20 Ω . For 4-pin MOSFET

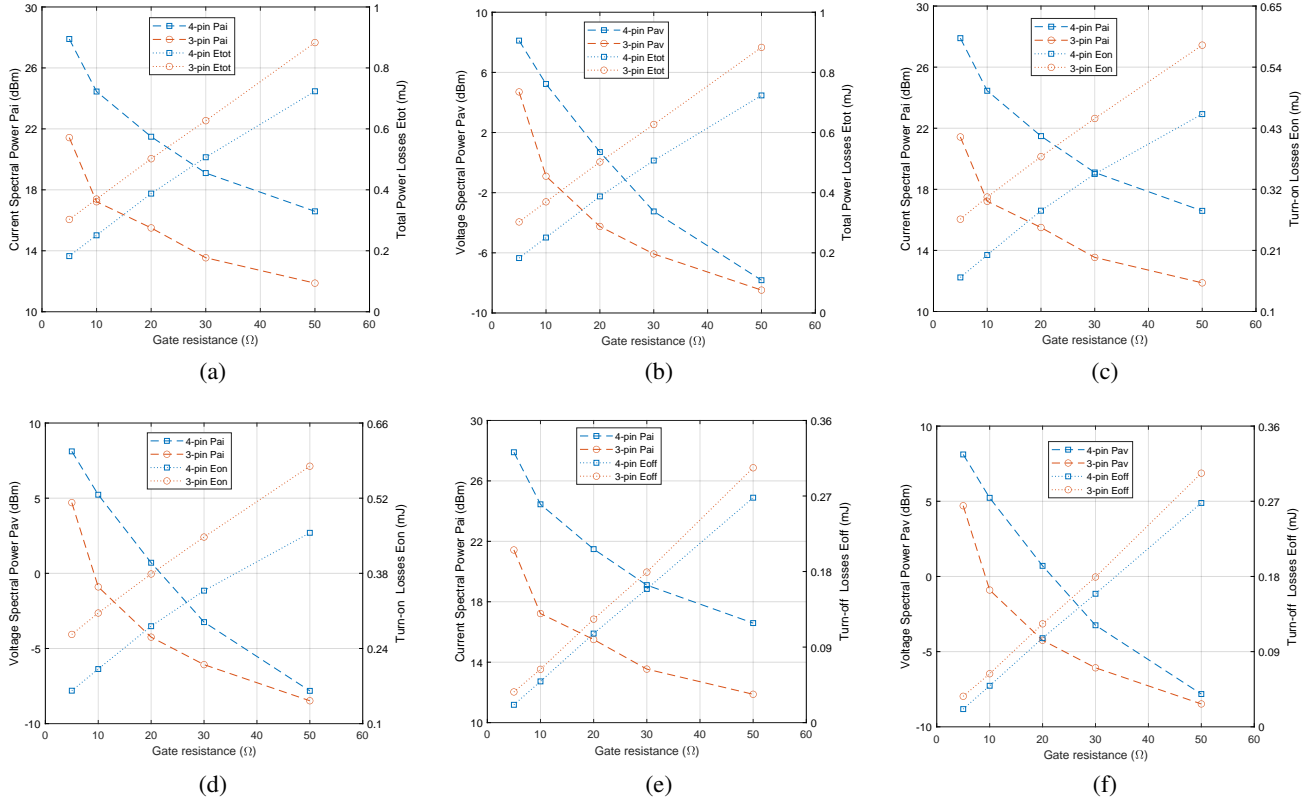


Fig. 13. Trade-off between spectrum power and switching losses at $V_{DC} = 400V$ and $I_L = 20A$ when R_G is 5 Ω , 10 Ω , 20 Ω , 30 Ω and 50 Ω : (a) P_{ai} vs E_{tot} . (b) P_{av} vs E_{tot} . (c) P_{ai} vs E_{on} . (d) P_{av} vs E_{on} . (e) P_{ai} vs E_{off} . (f) P_{av} vs E_{off} .

under test, the best trade-off can be achieved when R_G is 20 - 30 Ω .

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