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Ceramic baseplate-less 10 kV SiC MOSFET power module with integrated liquid cooling

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***Index Terms*—Packaging, SiC MOSFET, Additive manufacturing, Parasitic elements, Thermal management.**

***Abstract*—A 3D printed ceramic baseplate-less power module structure with integrated micro-channels for liquid cooling is presented. The main benefit is that parasitic capacitive couplings are removed in comparison with conventional power module packaging. Switching waveforms at 60 kV/us exhibit limited overshoot while good thermal performance is maintained.**

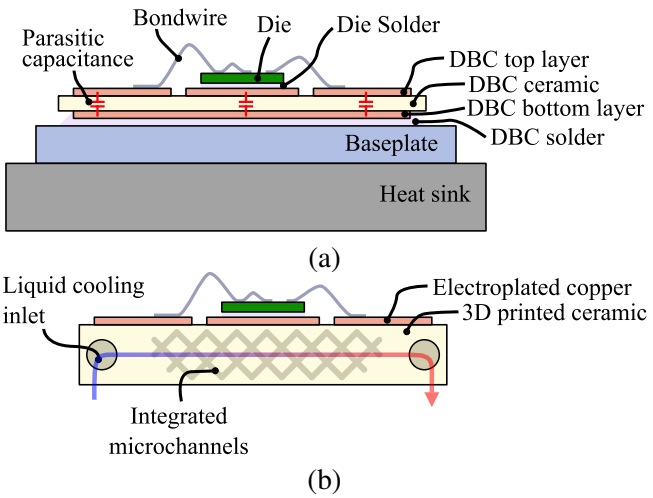


Fig. 1. Cross-sectional diagram of (a) conventional power module package and (b) the proposed ceramic power module package with integrated liquid cooling.

I. INTRODUCTION

The maturity of wide bandgap semiconductor materials, such as silicon carbide (SiC), offers benefits for power electronic converter designs. For medium voltage applications such as wind turbines, traction or distribution grid, the SiC metal-oxide-semiconductor field-effect transistors (MOSFET) are available at voltages of 10-15 kV. Their switching speed is faster when compared with silicon (Si) insulated gate bipolar transistor (IGBT), which is traditionally employed in such medium voltage applications, and therefore increases the system efficiency [1]. Alternatively, it also allows SiC MOSFETs to be operated at higher switching frequency without suffering too high losses, which may bring other system benefits such as reduced cooling requirements and more compact filters design [2]–[4].

Several research teams have demonstrated 10 kV SiC MOSFET power modules using a conventional power module packaging structure as shown in Fig. 1(a) [1], [5], [6]. A direct bonded copper (DBC) substrate is a sandwich structure with electrically insulating ceramic with copper on both sides. The semiconductor dies are soldered to the top copper layer, with wirebond interconnects. The bottom copper layer is soldered to a baseplate, which adds mechanical stability and is used to spread and transfer the dissipated power losses to a heat sink. While this DBC sandwich structure is an effective and proven way for low voltage operation and high power dissipation, it suffers from parasitic capacitance coupling between the copper traces on the top side and the bottom side copper [7]. This parasitic capacitance creates a common mode noise path which can limit robustness of the power converter [8], and impacts the achievable switching speed as more energy must be used to charge and discharge these parasitic capacitances during turn-on and turn-off [6]. The increased $\mathrm{d}v/\mathrm{d}t$ switching speed of medium voltage SiC MOSFETs introduce a larger

magnitude of the common mode current in the parasitic capacitances during switching, when compared with Si IGBTs.

A solution that reduces the parasitic capacitance is to use two stacked DBCs, by which the capacitances are connected in series [9]. Stacking of DBCs generally adds to the thermal resistance, as the heat has to be transferred through more layers of the electrically insulating ceramic layers. Additionally, while this solution reduces the parasitic capacitance the coupling still persists. If switching speed increases or copper areas get larger i.e. in multi-chip modules, it may still impact the full utilization of the medium voltage SiC MOSFET device potential.

A double sided ceramic liquid cooled heat sink with semiconductor dies was proposed in [10]. However, due to the double side cooling and the sintered silver planes being parallel to one another, this approach does not eliminate the parasitic capacitive coupling. To enable high voltage operation, in [11] a single-chip single-side liquid cooled 3D printed ceramic heatsink was demonstrated. The research focus was on the thermal flow simulation, thus neither the electrical switching performance or the influence of the parasitic capacitance was addressed.

In this paper, a 3D printed ceramic baseplate-less 10 kV SiC MOSFET power module is proposed, which eliminates the parasitic capacitance between the output copper trace and the heat sink. To maintain a good thermal performance liquid cooling is integrated directly into the 3D printed ceramic block which makes up the main part of the power module. The structure and assembly of the power module is presented in Section II. The electrical switching characteristics are experimentally measured in Section III, and the thermal performance is simulated in Section IV.

II. Power Module Structure and Assembly

For removal of the parasitic capacitance in power modules for medium voltage applications, while maintaining good thermal performance, we propose a 3D printed ceramic power module structure with the cross-section diagram shown in Fig. 1(b). Similar to [11] a 3D printed ceramic heat sink with integrated liquid cooling channels make up the main part of the power module to ensure good thermal performance. Copper traces are then electroplated onto only one side of the ceramic, to ensure no overlapping copper planes which otherwise would create the unwanted parasitic capacitance. The 10 kV SiC MOSFET semiconductor dies are then soldered to the copper and wirebonded similar to a conventional

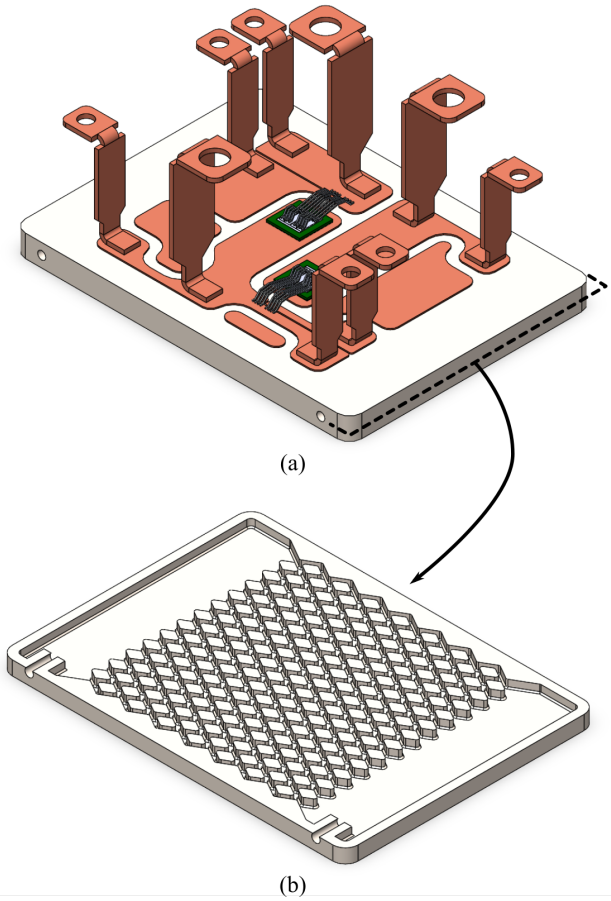
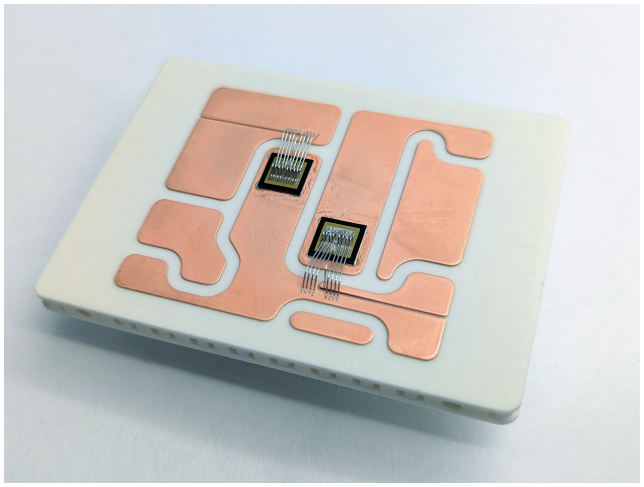


Fig. 2. 3D rendering of (a) the half-bridge power module structure with 10 kV SiC MOSFET dies and (b) cross-sectional view of the micro-channel structure inside the ceramic enabling liquid cooling.

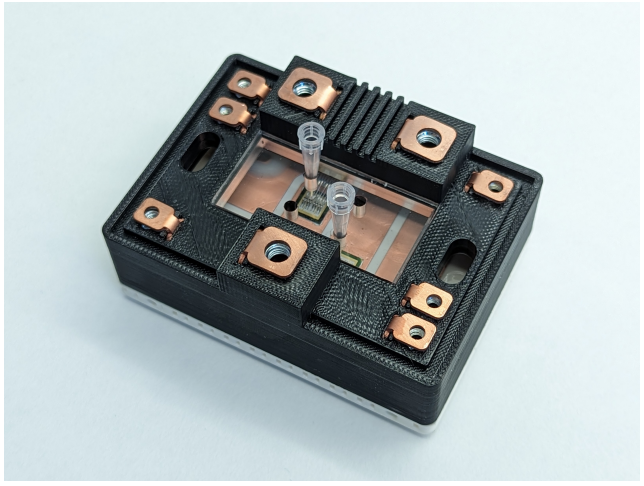
power module structure. The final assembly is potted in silicone gel to ensure high voltage compatibility.

A 3D rendering of the 10 kV SiC MOSFET half-bridge power module structure is shown in Fig. 2(a). The half-bridge power module copper trace layout is identical to a version manufactured using a conventional power module structure with baseplate [8]. The ceramic that also serves as the heat sink, has a size of 5.4 mm height, 82 mm width and 60 mm depth. It has two holes of 2 mm diameter used for inlet and outlet of the cooling liquid into the ceramic heat sink. A pattern of rectangular blocks of size 4 x 3 mm separated by channels of 1 mm width. A cross-sectional view of the internal structure of the cooling channels is shown in Fig. 2(b). The purpose of this is to increase the surface contact area and thereby heat transfer rate between the ceramic heat sink channels and the cooling liquid, and thereby decrease the thermal resistance seen by the SiC MOSFET dies.

For the assembly of the power module, the 3D



(a)



(b)

Fig. 3. Picture of the power module (a) with dies soldered and wirebonds (b) the housing mounted and silicone gel potted.

printed ceramic heat sink design is ordered in aluminium oxide (Al_2O_3) at Beijing TenDimensions Technology Co and the copper trace layout is electroplated to the top side. The 10 kV SiC MOSFET semiconductor dies are soldered using SAC305 solder paste in a vapor phase soldering oven. The SiC MOSFET semiconductor devices are wire bonded using 250 μm thick aluminium wire, as shown in Fig. 3(a). The copper terminals are soldered onto the power module, and a 3D printed plastic housing is mounted. Finally the power module is encapsulated in silicone gel, which concludes the final assembly of the power module shown in Fig. 3(b). The plastic funnels seen on top of the power module are added to allow for temperature monitoring of the semiconductor dies during continuous operation by using fiber optic temperature sensors [12].

III. Switching Characteristics

The manufactured power module is tested in a double pulse test to show its switching characteristics. It is tested at a DC-link voltage of 6000 V and the current is stepped up to 40 A using a 49 mH air coil inductor. The switching output voltage is measured using a Lecroy HVD3605A high voltage differential probe. Current is measured using a Lecroy CP150 current probe on a short wire connected between the DC-link busbar and the power module terminal as shown in Fig. 4, meaning insertion of some additional inductive elements in the circuit to enable the current measurement.

The switching waveforms during turn-on and turn-off are shown in Fig. 5. The voltage rise and fall times, defined as the time from 10 to 90 % of the switching output voltage, and vice versa, are read as 80 ns and 127 ns. This corresponds to voltage transients of 60 $\mathrm{kV}/\mu\mathrm{s}$ and 37.8 $\mathrm{kV}/\mu\mathrm{s}$, respectively.

The voltage transients are changing linearly with very limited overshoot and has no ringing. Likewise, the current waveforms measured do not exhibit ringing after the initial transition. This could suggest that the parasitic coupling between the copper output switch node, and other crucial copper traces i.e. low and high side gate traces have been successfully eliminated. In [6] and [8] the parasitic coupling between copper traces and a common heat sink is analyzed and shows how the circulating common mode currents can lead to sustained oscillations. These oscillations are not observed in the measured waveforms, which suggest a good performance at medium voltage operation at high $\mathrm{d}v/\mathrm{d}t$.

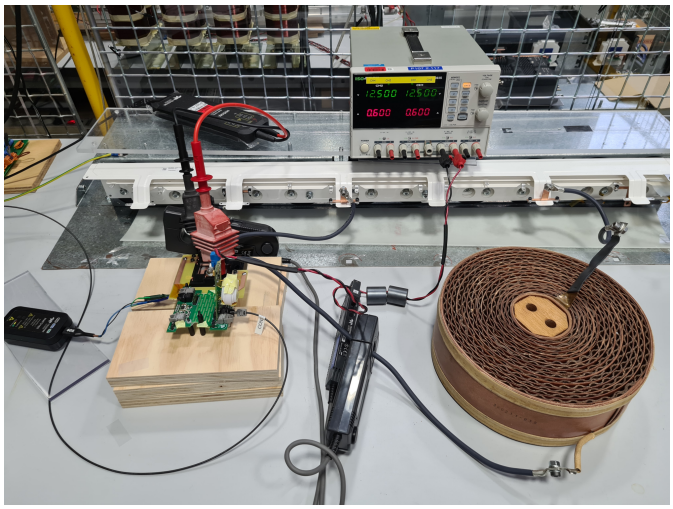
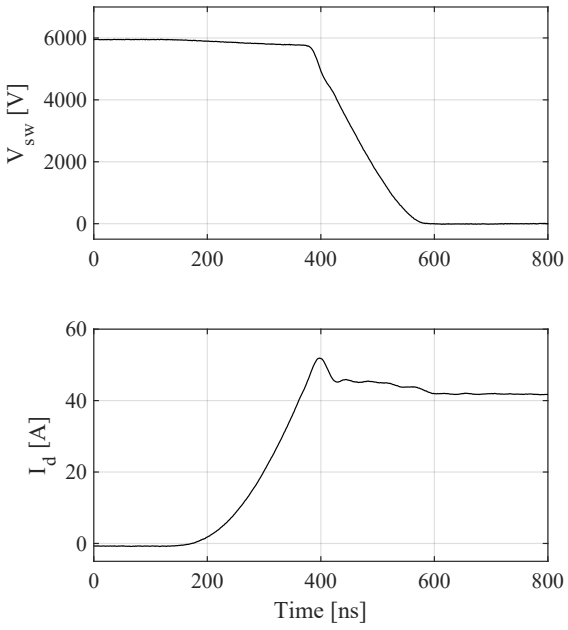
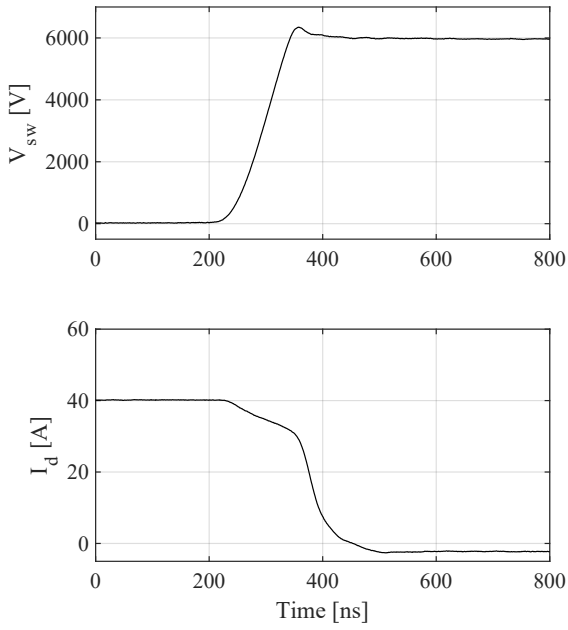


Fig. 4. Picture of double pulse test setup with wire attachments to enable current measurement.



(a)



(b)

Fig. 5. Measured switching voltage and drain-source current of low-side SiC MOSFET during (a) turn-on and (b) turn-off at 6000 V / 40 A operating conditions.

IV. Thermal performance

While the electrical characteristics have shown good compliance, for a power module packaging structure to be useful, its thermal performance must also be analyzed. Finite element analysis is used to evaluate the thermal performance of the power module. In COMSOL Multiphysics the 3D model from Fig. 2(a) is imported and both heat conduction in the solid material and laminar flow of the cooling liquid is simulated. The used material properties of the solids are listed in Table I. The viscosity, thermal conductivity, density and heat capacity of the cooling water are temperature dependent following the inbuilt equations available in COMSOL Multiphysics. In addition, for the cooling water it is defined as incompressible flow and there is no heat dissipation due to viscous effects.

For the boundary conditions a power loss of 50 W is injected into the active area of each SiC MOSFET chip. The inlet of the ceramic heat exchanger has an assigned flow rate in the range of 1 to 20 mL/s, while the outlet is set to 0 Pa pressure, which also provides a frame of reference for the fluid simulation. The ambient temperature and the inlet temperature of the cooling liquid are both set at 20°C.

The 3D model results for a flow rate of 2 mL/s are shown in Fig. 6, with both the surface temperature of the module and the temperature of the cooling water. Simulation results at flow rates lower than 1 mL/s are omitted, as the water temperature increases above 100°C and will result in a phase change. For future simulation and experimental tests, other cooling liquids with other boiling and freezing points could be taken into consideration [11].

The maximum recorded device temperature and the maximum cooling water temperature for different flow rates are shown in Fig. 7. For comparison with other publications, the temperatures are converted to thermal resistance by

$$R_{th} = \frac{T_{j,max} - T_A}{P} \tag{1}$$

where $T_{j,max}$ is the maximum temperature recorded on any of the devices, T_A is the ambient temperature of 20°C and P the power of 50 W per die. From Fig. 7 it can be read, that the thermal resistance starts

TABLE I
Material properties

Material	**Thermal cond.** $[\mathrm{W/(m \cdot K)}]$	**Specific heat** $[\mathrm{J/(kg \cdot K)}]$	**Density** $[\mathrm{kg/(m \cdot K)}]$
SiC	450	1200	3200
Cu	400	385	8960
Solder	50	150	9000
Al_2O_3	27	900	3900

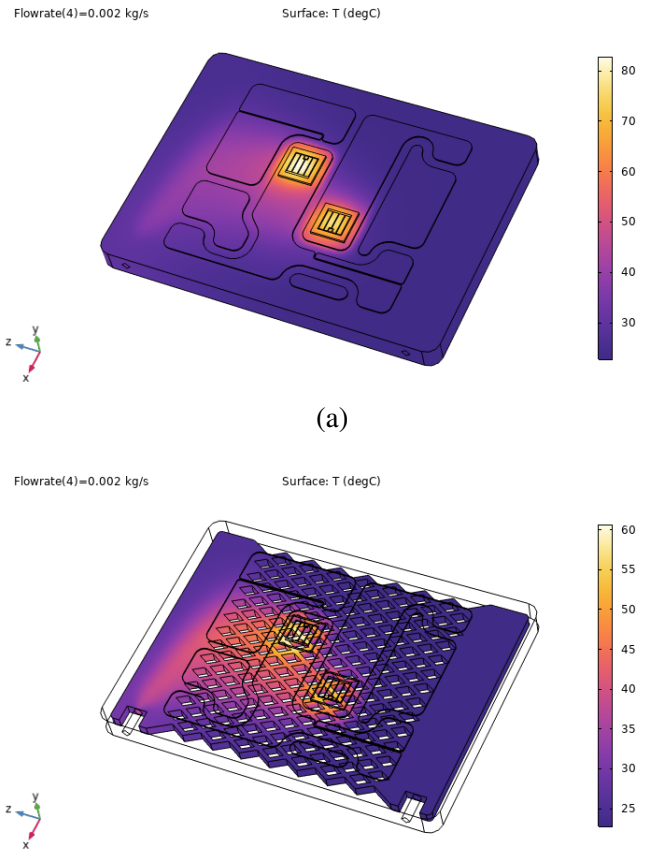


Fig. 6. COMSOL Multiphysics thermal simulation at power loss of 50 W per die and flow rate of 2 mL/s, showing (a) device surface temperatures and (b) temperature of the cooling liquid.

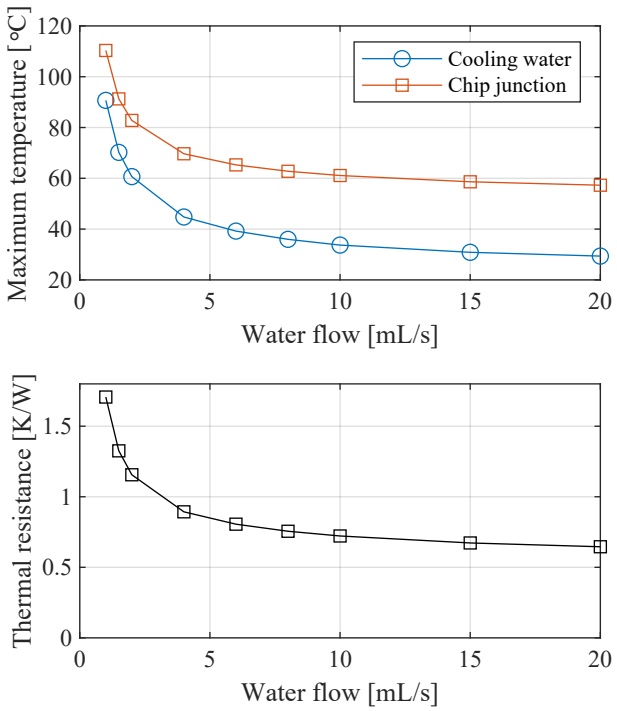


Fig. 7. Maximum temperatures of chip and cooling water (top) and the equivalent thermal resistance (bottom) as a function of inlet flow rate.

at 1.71 K/W for a flow rate of 1 mL/s, and drops to 0.65 K/W at 20 mL/s. The simulated pressure drop between inlet and outlet is in the range of 1 hPa to 343 hPa, when the flow rate is increased from 1 mL/s to 20 mL/s.

In comparison, the two-sided ceramic liquid cooling method presented in [10] achieved a thermal resistance of 0.26-0.46 K/W, which is less than half and shows the benefit of having two parallel heat paths from die to cooling reservoir. For the single-sided single-chip ceramic heat exchanger presented in [11], a thermal resistance of 0.38-0.6 K/W was experimentally verified. The heat exchanger was manufactured in aluminium nitride (AlN), which has a thermal conductivity of 170 $\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$ in comparison to 27 $\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$ of Al_2O_3 used for the ceramic heat sink in this paper. Based on this discussion, the simulation results presented in this paper are within reasonable range of what is expected. In future research, the 3D printed ceramic liquid cooling solution will be investigated in more detail and experimentally verified.

V. Conclusion

Full utilization of 10 kV SiC MOSFET devices in medium voltage applications might be impeded by parasitic capacitances from the power module packaging. This paper has presented a baseplate-less 3D printed ceramic power module structure, which eliminates the parasitic coupling to the baseplate found in conventional power module packaging. To maintain a good thermal performance of the power module, liquid cooling channels are integrated directly into the 3D printed ceramic. Following assembly of the power module, it achieves switching speed of 60 $\mathrm{kV}/\mu\mathrm{s}$ during a 6000 V, 40 A double pulse test, with very limited voltage overshoot and no sustained oscillations. Furthermore, the thermal performance of the module is evaluated using a finite element analysis in COMSOL Multiphysics, which provides a thermal resistance around 0.65-0.81 K/W for a flow rate in the range of 6-20 mL/s. The proposed power module structure is concluded as an effective way of eliminating the parasitic capacitive coupling otherwise present in other power module structures, while still maintaining good thermal performance. Future research will include a deeper analysis of the power module couplings versus die specific parasitics on the electrical

switching performance, as well as a more in-depth investigation on the thermal management and the possibilities within additive manufacturing for future medium voltage power module packaging.

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