Additional-Levels-based control method for modular multilevel converters with reduced DC-Link current ripple

Yu, Qiang; Deng, Fujin; Tang, Yi; Wang, Yanbo; Blaabjerg, Frede

Published in:
International Journal of Electrical Power & Energy Systems

DOI (link to publication from Publisher):
10.1016/j.ijepes.2023.109288

Publication date:
2023

Document Version
Publisher's PDF, also known as Version of record

Electrical Power and Energy Systems 153 (2023) 109288

Contents lists available at ScienceDirect

International Journal of Electrical Power and Energy Systems

journal homepage: www.elsevier.com/locate/ijepes

Additional-Levels-based control method for modular multilevel converters with reduced DC-Link current ripple

Qiang Yu [a,c], Fujin Deng [a,b,*], Yi Tang [c], Yanbo Wang [d], Frede Blaabjerg [d]

[a] Southeast University, Sipailou #2, Nanjing 210096, China
[b] Jiangsu Key Laboratory of Smart Grid Technology and Equipment, Nanjing 210096, China
[c] Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798, Singapore
[d] Aalborg University, Aalborg 9220, Denmark

ARTICLE INFO

Keywords:
Circulating current
Dc-link current ripple
model predictive control (MPC)
modular multilevel converter (MMC)

ABSTRACT

The high and low order dc-link current ripple can be caused under balanced and unbalanced ac grid/load conditions for three-phase modular multilevel converters (MMCs). To enhance the dc-link current quality, this paper proposes an additional-levels-based control (ALC) method, where the conventional modulation is employed to generate ac-side voltage levels and a model predictive control (MPC) algorithm with reduced calculation burden is developed to produce additional levels for dc-link current performance improvement. Through evaluating the cost function of MPC, the proposed method can reduce both high and low order dc-link current ripple for the MMC. Meanwhile, it avoids disturbing the quality of the ac-side voltage. Besides, the calculation burden of the proposed method is independent of the submodules' number per arm. The validity and effectiveness of the proposed method have been verified by simulation and experimental results.

1. Introduction

Modular multilevel converters (MMCs) have drawn extensive interests and become increasingly attractive in medium voltage high power industrial applications, such as dc distribution networks, motor drive, energy storage, etc. [1–3]. Consisting of many stacked submodules (SMs), the MMC can synthesize multilevel voltages in its ac side. It has a series of salient features such as modular structure, scalability, flexibility, and high efficiency [4–6].

The dc-link current distortion is one of the major concerns for the MMC, especially in some medium voltage applications with a relatively small number of submodules (SMs) and without large smoothing reactors. The unbalanced ac grid/load condition is one of the reasons that account for low order dc-link current ripple. In addition, due to the modulation schemes or the necessary second order circulating current suppression control (CCSC) methods, the total number of upper and lower arm inserted SMs no longer remain constant at N (where N is the number of SMs per arm). Instead, it become variable around N and asymmetric for three-phase system, which causes high order zero-sequence voltage. Accordingly, the zero-sequence circulating current is produced and further flows into the dc link of the MMC, leading to dc-link current ripple under balanced ac condition. It may result in dc-link power oscillation, deteriorate dc-link power quality, affect dc-link equipment, and lead to potential instability issues [7–12]. As a result, it is essential to improve the dc-link current performance of MMCs.

To date, some studies have been conducted to solve the low order dc-link current ripple of the MMC under unbalanced ac conditions. Reference [7] presents a supplementary dc current ripple suppressing control by compensating the second order zero-sequence voltages in three phase-legs, in which the second order dc-link current ripple of MMCs under unbalanced grid voltages can be removed. Reference [8] presents a proportional-resonant dc-link current controller, which can eliminate the second order dc-link current ripple of MMCs under unbalanced grid voltages. Reference [9] presents an MPC embedding the internally generated zero-sequence voltage into the three-phase predictive model, which can suppress most of the low order dc-link current ripple of MMCs under unbalanced ac currents. However, [7–9] ignore the fact that the dc-link current ripple can also be caused under balanced operation of the MMC.

Currently, a few research works have focused on the dc-link current ripple of MMCs under balanced operation conditions. A modified MMC topology is developed in [10] by replacing arm inductors with three-

* Corresponding author.
E-mail address: fdeng@seu.edu.cn (F. Deng).

https://doi.org/10.1016/j.ijepes.2023.109288
Received 22 August 2022; Received in revised form 21 April 2023; Accepted 2 June 2023
Available online 13 June 2023

winding transformers and employing a circulating current suppression inverter. The arm current harmonics are absorbed by SM capacitors, which can suppress both second order circulating current and high order dc-link current fluctuations. However, hardware cost and volume are increased unavoidably. Reference [11] presents a control based on regulating the phase-shifted angles of carrier waves, which can eliminate high frequency dc-link current ripple of the MMC introduced by the modified carrier phase shifted pulse width modulation (PWM) [12]. Reference [13] presents a method regulating three-phase arm inductor voltage pulses to be counteracted, which can suppress the dc-link current ripple for MMCs under $2N+1$ submodule unified PWM. References [14] and [15] present dc-link current ripple suppression strategies for MMCs based on two-group-carrier phase-disposition PWM. Through regulating the phase angles of three-phase carriers, the high frequency dc-link current ripple caused by CCSC can be eliminated. However, the methods in [11,13–15] are all implemented through precisely regulating PWM pulses and only applicable for PWM schemes. The dc-link current ripple under nearest level modulation (NLM) is more serious because the round error of CCSC reference voltage can further increase the dc-link current ripple [16]. In [16], a hybrid modulation is presented, where the fundamental frequency reference voltage is modulated by NLM and the CCSC reference voltage is modulated by PWM to remove the error. The dc-link current ripple of MMCs is reduced compared with conventional NLM. However, this method is not applicable for level-increased NLM [17], in which another modulation error is produced by the small offset combined in arm reference voltage and cannot be fully removed. Moreover, [11] and [13–16] are all open-loop control methods and cannot suppress the low order dc-link current ripple under unbalanced ac condition.

Recently, the MPC provides a promising solution for MMCs due to its good features like simple control structure, easy implementation for multiple objectives control, good dynamic response and easy handling of nonlinearities [18]. The finite-control-set MPC has been reported to coordinate the control of ac-side current, circulating current and/or capacitor voltages for MMCs [19–21]. Using one predefined cost function with some weighting factors, the MPC chooses one solution with the minimum cost function from limited number of switching combinations in each control period, which can achieve optimal control. Compared with linear controllers [7,8], the MPC does not extract the specific frequency information of dc-link current ripple and can suppress multiple frequency ripple components in one controller, which is simpler and easier and can achieve better dc-link current performance.

In this paper, the relationship between dc-link current and the total number of three-phase arm voltage levels is derived. An additional-levels-based control (ALC) method is proposed to reduce dc-link current ripple for MMCs. The modulation technique is employed to generate ac-side voltage levels, while an MPC algorithm with reduced calculation burden is developed to produce additional levels regulating the performance of dc-link current and three-phase circulating currents. The arm voltage levels are the sum of ac-side voltage levels and additional levels. The primary contributions of this paper are: 1) an ALC method is newly proposed, which can reduce high and low order dc-link current ripple under both balanced and unbalanced ac conditions, together with suppressing the low order circulating current for the MMC; 2) the proposed method does not disturb the ac-side voltage quality; 3) the calculation burden of the proposed method is independent of the number of SMs per arm.

The rest of this paper is organized as follows. Section 2 introduces the basic principle of MMCs. Section 3 proposes the ALC method to reduce dc-link current ripple as well as suppress second order circulating current for MMCs. Section 4 presents the discussion of proposed method. The simulation and experimental results are presented in Section 5 and 6, respectively, to show the effectiveness and validity of proposed method. Finally, Section 7 draws the conclusions.

2. Modular multilevel converters

Fig. 1 shows a three-phase MMC with six arms. The upper arm and lower arm in the same phase make up a phase-leg. Each arm is composed of N cascaded half-bridge SMs and an inductor L_s. Each SM contains a storage capacitor C_{SM} and two switches T_1, T_2. During its normal operation, each SM has two states. If the SM is "Inserted", its output voltage equals the capacitor voltage. If the SM is "Bypassed", its output voltage equals zero.

In Fig. 1, the ac-side mathematical model of phase j ($j = a, b, c$) for the MMC [22] is

$$u_j = u_{ej} - \frac{L_s}{2}\frac{di_j}{dt} \tag{1}$$

with

$$u_{ej} = (u_{lj} - u_{uj})/2 \tag{2}$$

where u_j and i_j are the ac-side voltage and current of phase j, respectively. u_{uj} and u_{lj} are the sum of the SM output voltages in the upper arm and lower arm of phase j, respectively. u_{ej} is the ac electromotive force (EMF) of the MMC.

In Fig. 1, the dc-link current of the MMC can be written as

$$i_{dc} = \sum_{j=a,b,c} i_{uj} = \sum_{j=a,b,c} i_{lj} \tag{3}$$

where i_{uj} and i_{lj} are the upper and lower arm current of phase j.

The dynamics of the circulating current in phase j of the MMC is [23]

$$\frac{di_{cirj}}{dt} = \frac{1}{2L_s}\left(U_{dc} - u_{uj} - u_{lj}\right) \tag{4}$$

with

$$i_{cirj} = (i_{uj} + i_{lj})/2 \tag{5}$$

where i_{cirj} is the circulating current in phase j. U_{dc} is the dc-link voltage of the MMC. During the normal operation, the rated average capacitor voltage of the SM is U_{dc}/N. Suppose that n_{uj} and n_{lj} are the number of upper and lower arm output voltage levels of phase j, u_{uj} and u_{lj} can be expressed as

$$\begin{cases} u_{uj} = n_{uj}U_{dc}/N \\ u_{lj} = n_{lj}U_{dc}/N \end{cases} \tag{6}$$

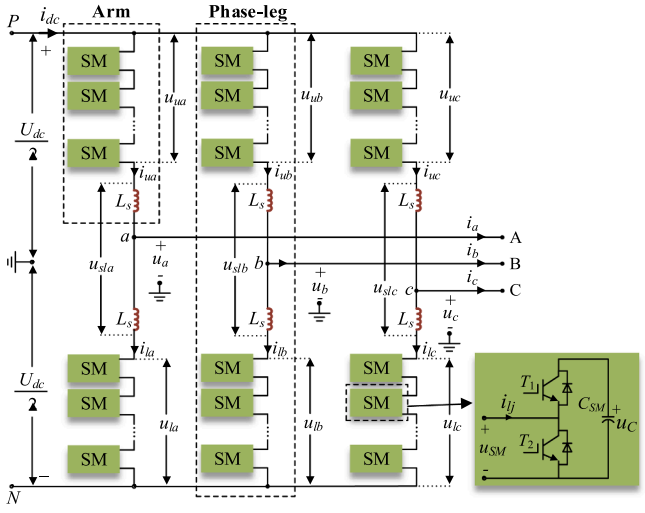

Fig. 1. Three-phase MMC with half-bridge SM.

3. Proposed ALC method for reduced dc-link current ripple

3.1. Relationship between dc-link current & circulating current

According to (3) and (5), the relationship between the dc-link current i_{dc} and three-phase circulating currents i_{cira}, i_{cirb}, and i_{circ} can be obtained as

$$i_{dc} = \sum_{j=a,b,c} i_{cirj} \tag{7}$$

The total number of upper and lower arm output voltage levels of phase j is denoted as n_{sumj}, which is expressed as

$$n_{sumj} = n_{uj} + n_{lj} \tag{8}$$

The circulating current of the MMC can be expressed based on (4), (6) and (8), as

$$i_{cirj} = \frac{U_{dc}}{2NL_s} \int (N - n_{sumj}) dt \tag{9}$$

The dc-link current of the MMC can be written based on (7) and (9), as

$$i_{dc} = \frac{U_{dc}}{2NL_s} \int (3N - \sum_{j=a,b,c} n_{sumj}) dt \tag{10}$$

Equation (9) shows that the three-phase circulating currents i_{cira}, i_{cirb}, and i_{circ} are affected by n_{suma}, n_{sumb}, and n_{sumc}. Equation (10) shows that the dc-link current i_{dc} is affected by the sum of n_{suma}, n_{sumb}, and n_{sumc}.

When the MMC works under balanced ac condition, n_{uj} and n_{lj} (and n_{sumj}) are mainly determined by modulation schemes and control strategies like CCSC [16,22,24]. Due to the common-mode control reference produced by CCSC, the references of upper and lower arms are not exactly symmetrical and the upper and lower arm output voltage levels are changed asynchronously [13–17]. As a result, n_{sumj} does not remain constant at N, but varies among N, $N \pm 1$, … This further lead to the variation of the sum of n_{suma}, n_{sumb}, and n_{sumc}. Fig. 2 shows the simulated waveforms of n_{suma}, n_{sumb}, n_{sumc} and their sum under the level-increased NLM [17] and conventional CCSC [24], which are derived from the simulation system in Section V. It clearly shows the variation of the sum of n_{suma}, n_{sumb}, n_{sumc}, which would cause high order dc-link current ripple and distort the dc-link current according to (10). On the other hand, when the MMC works under unbalanced ac condition, the second order dc-link current ripple will be generated [7,8,25].

3.2. Proposed ALC method for reduced dc-link current ripple

Despite different causes for dc-link current ripple, (10) shows that the dc-link current quality of the MMC can be improved by regulating the sum of n_{suma}, n_{sumb} and n_{sumc}. This paper proposes an ALC method to reduce dc-link current ripple of the MMC, as shown in Fig. 3. In each control period, the number of output voltage levels for upper and lower arms of phase j is firstly obtained, as

$$\begin{cases} n_{uj} = n_{uj0} + \eta_j \\ n_{lj} = n_{lj0} + \eta_j \end{cases} \tag{11}$$

where n_{uj0} and n_{lj0} are generated by modulation of fundamental reference voltages, as $U_{dc}/2 \mp u_{ej\_ref}$. u_{ej_ref} is the reference ac EMF of phase j. η_j is the number of additional levels obtained by the implementation of proposed MPC algorithm, which can coordinate the performance of circulating current and dc-link current. The final number of output voltage levels per arm is the sum of n_{uj0} (n_{lj0}) and η_j. The value of η_j could be 0, ±1, …, $\pm\eta_{max}$, where η_{max} is determined by MMC parameters to ensure the controllability of circulating current and dc-link current.

In Fig. 3, after n_{uj} (n_{lj}) is obtained, based on the arm current i_{uj} (i_{lj}) and the SMs capacitor voltages $u_{Cuj\_1} \sim u_{Cuj\_N}$ ($u_{Clj\_1} \sim u_{Clj\_N}$), the sorting-based capacitor voltage balancing (CVB) control [26] is applied to balance the capacitor voltages. Finally, the drive signals for SMs in the upper arm (lower arm) of the MMC are generated.

Combining (2), (6) and (11), the ac EMF of the MMC can be expressed as

$$u_{ej} = \frac{n_{lj} - n_{uj}}{2} \frac{U_{dc}}{N} = \frac{n_{lj0} - n_{uj0}}{2} \frac{U_{dc}}{N} \tag{12}$$

Equation (12) indicates that u_{ej} is not affected by η_j. Thus, the proposed method does not disturb the ac-side performance of the MMC.

Based on (8) and (11), the total number of upper and lower arm output voltage levels in phase j can be rewritten as.

$$n_{sumj} = n_{uj0} + n_{lj0} + 2\eta_j \tag{13}$$

From (13), n_{suma}, n_{sumb}, n_{sumc} in phases A, B and C can be regulated by η_j. Combining (9), (10) and (13), the additional levels number η_j can be used to reduce dc-link current ripple as well as suppress second order circulating current for MMCs.

3.3. Prediction model and cost function of MMCs

According to (4) and (11), the discrete mathematic model can be derived, and the predicted circulating current of phase j can be written as

$$i_{cirj}(k+1) = \frac{T_s}{2L_s}\left[U_{dc} - \left(n_{uj0}(k) + \eta_j(k)\right)\overline{u}_{Cuj}(k) - \left(n_{lj0}(k) + \eta_j(k)\right)\overline{u}_{Clj}(k)\right] + i_{cirj}(k) \tag{14}$$

where T_s is control period. $i_{cirj}(k)$ and $i_{cirj}(k+1)$ are the sampled circulating current at time step k and $k+1$, respectively. $\overline{u}_{Cuj}(k)$ and $\overline{u}_{Clj}(k)$ are the average upper arm and lower arm capacitor voltages at time step k, respectively, which can be obtained as

$$\begin{cases} \overline{u}_{Cuj}(k) = \dfrac{1}{N}\sum_{i=1}^{N} u_{Cuj\_i}(k) \\ \overline{u}_{Clj}(k) = \dfrac{1}{N}\sum_{i=1}^{N} u_{Clj\_i}(k) \end{cases} \tag{15}$$

where $u_{Cuj\_i}(k)$ and $u_{Clj\_i}(k)$ are the measured capacitor voltages of i-th SM in the upper arm and lower arm of phase j.

As mentioned above, both three-phase circulating currents and dc-link current are affected by η_j. To achieve reduced dc-link current ripple while ensure the necessary control of suppressing second order circulating current for the MMC, the control target is designed as the dc-link current and circulating currents of phases A, B, C for the MMC. Therefore, the cost function can be expressed as

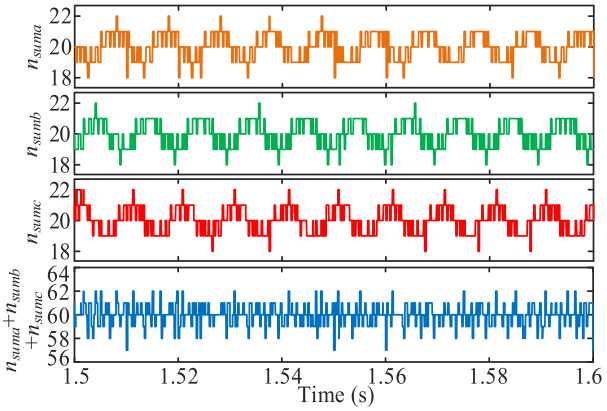

Fig. 2. Simulated waveforms of n_{suma}, n_{sumb}, n_{sumc} and their sum for MMCs.

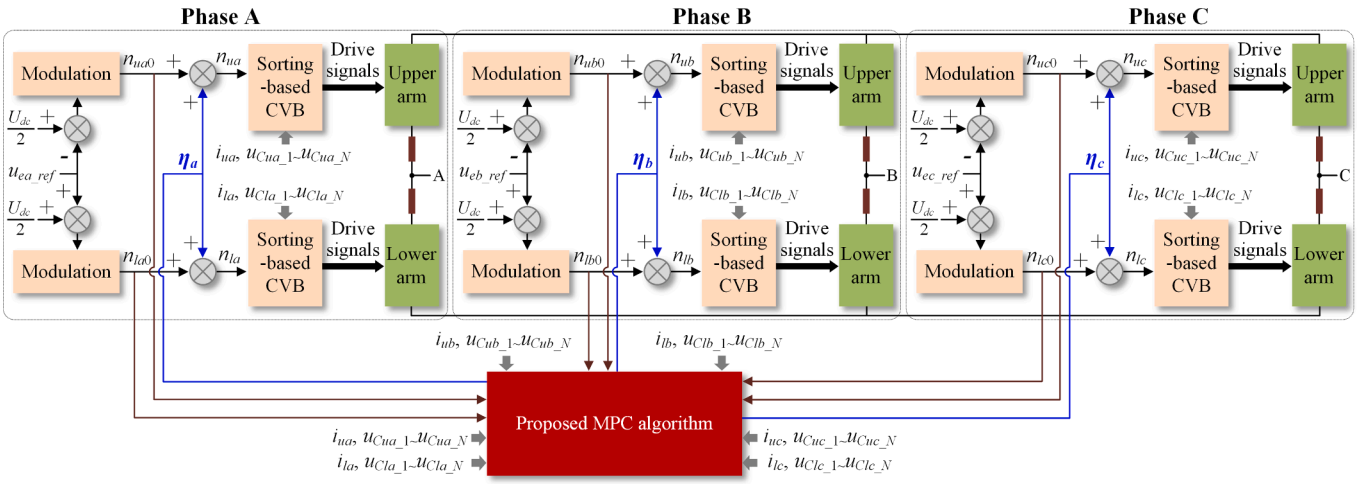

Fig. 3. Block diagram of the proposed ALC method for MMCs.

$$J = \lambda|i_{dc\_ref}(k+1) - \sum_{j=a,b,c} i_{cirj}(k+1)| + \sum_{j=a,b,c} |i_{cirj\_ref}(k+1) - i_{cirj}(k+1)| \tag{16}$$

where λ is the weighting factor. i_{dc_ref} and i_{cirj_ref} are the reference dc-link current and reference circulating current of phase j. The first term in (16) represents the tracking error of the dc-link current, which determines the performance of the dc-link current. The second term in (16) represents the tracking error of the circulating currents in three phases, which determines the performance of the circulating current. The tradeoff between the circulating current and dc-link current of the MMC can be achieved by regulating the value of λ. The aim is to select the values of η_a, η_b and η_c that minimizes (16) from a number of candidate combinations. By setting the value of λ appropriately, the dc-link current ripple can be reduced effectively, together with the second order circulating current.

The reference dc-link current at time step $k+1$ is the sum of reference circulating currents in phases A, B and C, as

$$i_{dc\_ref}(k+1) = \sum_{j=a,b,c} i_{cirj\_ref}(k+1) \tag{17}$$

where $i_{cirj\_ref}(k+1)$ is the reference circulating current of phase j at time step $k+1$. Using the third-order Lagrange extrapolation method [27], it can be expressed as

$$i_{cirj\_ref}(k+1) = 4i_{cirj\_ref}(k) - 6i_{cirj\_ref}(k-1) + 4i_{cirj\_ref}(k-2) - i_{cirj\_ref}(k-3) \tag{18}$$

3.4. Proposed candidate combinations generation

Generally, η_j in (13) has $2\eta_{max}+1$ possible values for phase j. η_a, η_b and η_c in three-phase MMC have $(2\eta_{max}+1)^3$ possible combinations in all. As a result, there are $(2\eta_{max}+1)^3$ predicted values of cost function J calculated in each control period. Apparently, the calculation burden of the algorithm will be greatly increased for the MMC system with a big value of η_{max}. To solve the issue, a candidate combinations generation (CCG) is proposed to keep the number of possible values of η_a, η_b and η_c in each control period unchanged, no matter what η_{max} is, which can prevent the growth of the calculation burden.

Owing to that the variation of n_{sumj} in (13) between two adjacent control periods is small during the normal operation of the MMC, three integer values around $n_{sumj}(k\text{-}1)$ are considered as possible values for $n_{sumj}(k)$, which correspond to three situations as $n_{sumj}(k) > n_{sumj}(k\text{-}1)$, $n_{sumj}(k) = n_{sumj}(k\text{-}1)$ and $n_{sumj}(k) < n_{sumj}(k\text{-}1)$. Accordingly, in the proposed CCG, based on (13), η_j has three possible values in each control period. Considering η_j is an integer, the possible values of η_j are given as.

$\eta_j \in [\eta'_{j(1)}, \eta'_{j(2)}, \eta'_{j(3)}]$,

with

$$\begin{cases} \eta'_{j(1)} = h_j - 1 \\ \eta'_{j(2)} = h_j \\ \eta'_{j(3)} = h_j + 1 \end{cases} \tag{19}$$

$$h_j = \mathrm{fix}\left[\frac{n_{uj0}(k-1) + n_{lj0}(k-1) - n_{uj0}(k) - n_{lj0}(k)}{2}\right] + \eta_j(k-1) \tag{20}$$

where the function fix(x) returns the integer part of x. It should be noted that the sum of $n_{uj0}(k)$ and $n_{lj0}(k)$ in (20) is not always equal to N, but can change among N-1, N and $N+1$ under some modulation schemes [17,22].

The possible values of η_a, η_b, and η_c for phases A, B, and C make up the candidate combinations V for the proposed ALC method. According to (19), the proposed CCG has 27 combinations in total in each control period for three-phase MMC, irrespective of N, as shown in Table 1. $J_1 \sim J_{27}$ are the calculated cost function values of these combinations.

3.5. Implementation of proposed MPC algorithm

An MPC algorithm is proposed for ALC method to determine the values of η_a, η_b, η_c that minimize the cost function in (16), so as to reduce the dc-link current ripple, as shown in Fig. 4.

Fig. 4(a) shows the generation of the reference circulating current i_{cirj_ref} [28]. The moving average filter (MAF) is adopted to obtain the mean value of the sum and difference of the upper and lower arm capacitor voltages. Δi_{cirj0_ref} is obtained to control the total capacitor voltages in phase j to follow the rated value $2U_{dc}$. Δi_{cirj1_ref} is obtained to control the upper and lower arm capacitor voltages equal. δ is the phase angle of the ac EMF in phase A. $V_jI_j\cos\varphi/(2U_{dc})$ is employed to achieve the power balance between the dc and ac side in phase j. V_j and I_j are, respectively, the amplitudes of the ac-side voltage u_j and current i_j in

Table 1
Candidate Combinations of Proposed Method.

Number	Combinations	Cost Function
1	$V(1, 1, 1) = [\eta'_{a(1)}, \eta'_{b(1)}, \eta'_{c(1)}]$	J_1
2	$V(1, 1, 2) = [\eta'_{a(1)}, \eta'_{b(1)}, \eta'_{c(2)}]$	J_2
3	$V(1, 1, 3) = [\eta'_{a(1)}, \eta'_{b(1)}, \eta'_{c(3)}]$	J_3
…	…	…
26	$V(3, 3, 2) = [\eta'_{a(3)}, \eta'_{b(3)}, \eta'_{c(2)}]$	J_{26}
27	$V(3, 3, 3) = [\eta'_{a(3)}, \eta'_{b(3)}, \eta'_{c(3)}]$	J_{27}

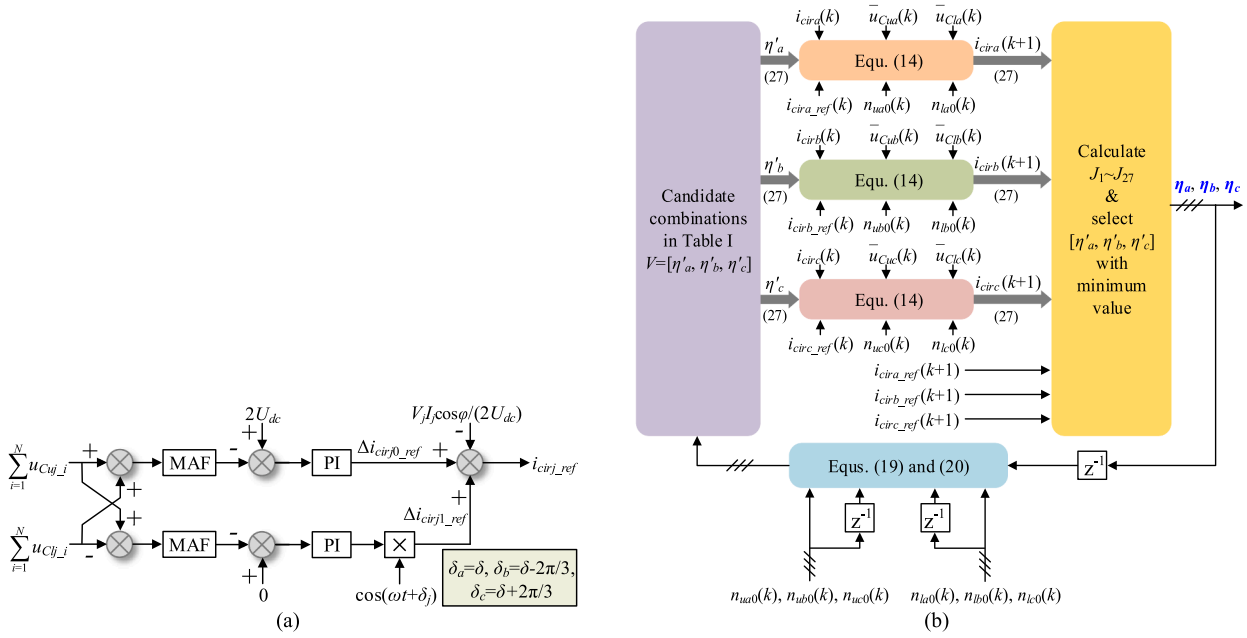

Fig. 4. Implementation of proposed algorithm. (a) Generation of the reference circulating current. (b) Diagram of proposed MPC algorithm.

phase j of the MMC. φ is the angle between u_j and i_j.

Fig. 4(b) shows the diagram of proposed MPC algorithm. In each control period, $n_{uj0}(k)$, $n_{lj0}(k)$, $n_{uj0}(k\text{-}1)$, $n_{lj0}(k\text{-}1)$ and $\eta_j(k\text{-}1)$ for phases A, B and C are firstly obtained. Here, $n_{uj0}(k)$ and $n_{lj0}(k)$ are obtained by the modulation of the fundamental reference voltages shown in Fig. 3. The values at time step k-1 can be obtained through z^{-1} block. Based on (19), (20) and Table 1, the candidate combinations with η'_a, η'_b and η'_c are generated. After then, according to η'_j, $i_{cirj}(k)$, $\bar{u}_{Cuj}(k)$, $\bar{u}_{Clj}(k)$, $i_{cirj\_ref}(k)$, $n_{uj0}(k)$, $n_{lj0}(k)$ for phases A, B, C and the predictive model in (14), all of the predicted circulating currents $i_{cira}(k+1)$, $i_{cirb}(k+1)$ and $i_{circ}(k+1)$ are obtained. Here, $\bar{u}_{Cuj}(k)$ and $\bar{u}_{Clj}(k)$ are obtained based on (15) and $i_{cirj\_ref}(k)$ is obtained through Fig. 4(a). According to all of the predicted circulating currents, their reference values $i_{cira\_ref}(k+1)$, $i_{cirb\_ref}(k+1)$, $i_{circ\_ref}(k+1)$ and (16), the cost functions $J_1 \sim J_{27}$ can be calculated, and the optimal combination with $\eta'_a(k)$, $\eta'_b(k)$ and $\eta'_c(k)$ that has minimum value in $J_1 \sim J_{27}$ can finally be determined. Consequently, η_a, η_b and η_c are obtained.

When the proposed algorithm is implemented in the digital controller, the issue of one-control-period delay is unavoidable. It can be compensated by applying the two-step prediction scheme [29]. Firstly, according to (14), $i_{cirj\_ref}(k+1)$ is predicted based on $i_{cirj\_ref}(k)$. Afterwards, the predictive algorithm is implemented again to obtain $i_{cirj\_ref}(k+2)$. The cost function is evaluated based on $i_{cirj\_ref}(k+2)$ to generate η_a, η_b and η_c.

4. Discussion of proposed ALC method

4.1. Range of η_{max}

According to [30], the amplitude of the MMC phase-leg difference voltage corresponding to circulating current under normal operation is

$$U_{cir} = \frac{S}{6\omega_0}\frac{1}{C_{SM}U_{dc}/N - U_{dc}/(8\omega_0^2 L_s)} \tag{21}$$

where S is apparent power, ω_0 is fundamental angular frequency.

In order to control circulating current, the total output voltages of the upper and lower arm should cover the range of maximum and minimum phase-leg difference voltage, which requires

$$\begin{cases} \max\left[(n_{uj0}+n_{lj0}+2\eta_j)U_{dc}/N\right] \geqslant U_{dc}+U_{cir} \\ \min\left[(n_{uj0}+n_{lj0}+2\eta_j)U_{dc}/N\right] \leqslant U_{dc}-U_{cir} \end{cases} \tag{22}$$

Usually, the sum of n_{uj0} and n_{lj0} varies among N-1, N and $N+1$ [13,17,21]. Therefore, η_{max} should meet

$$\eta_{\max} \geqslant \text{ceil}\left[\frac{1}{2}\left(\frac{NU_{cir}}{U_{dc}}+1\right)\right] \tag{23}$$

where ceil(x) returns the nearest integer that is no less than x.

Both n_{uj} and n_{lj} should be between 0 and N since each arm has N SMs, according to (11), η_{max} should also meet

$$\begin{cases} \eta_{\max} \leqslant N - \max(n_{uj0}, n_{lj0}) \\ \eta_{\max} \leqslant \min(n_{uj0}, n_{lj0}) \end{cases} \tag{24}$$

The maximum and minimum values of n_{uj0} and n_{lj0} in (24) are obtained by the modulation of the arm fundamental reference voltages $U_{dc}/2 \mp u_{ej\_ref}$, as shown in Fig. 2. Thus, (24) can be rewritten as

$$\begin{cases} \eta_{\max} \leqslant N - \text{ceil}\left[\max\left(N(U_{dc}/2 \mp u_{ej\_ref})/U_{dc}\right)\right] \\ \eta_{\max} \leqslant \text{floor}\left[\min\left(N(U_{dc}/2 \mp u_{ej\_ref})/U_{dc}\right)\right] \end{cases} \tag{25}$$

where floor(x) returns the nearest integer that is no more than x.

As a result, the range of η_{max} can be obtained with (23) and (25).

4.2. Selection of λ

The value of λ should be designed properly for best quality of dc-link current. Suppose that J_s and J_t are the cost function values of s-th and t-th ($1 \leq s, t \leq 27$ and $s \neq t$) combinations in Table 1, the difference between J_s and J_t is

$$J_t - J_s = \lambda D + E \tag{26}$$

with

$$D = |i_{dc\_ref}(k+1) - \sum_{j=a,b,c} i_{cirj\_t}(k+1)| - |i_{dc\_ref}(k+1) - \sum_{j=a,b,c} i_{cirj\_s}(k+1)| \tag{27}$$

$$E = \sum_{j=a,b,c} \left[\left| i_{cirj\_ref}(k+1) - i_{cirj\_t}(k+1) \right| - \left| i_{cirj\_ref}(k+1) - i_{cirj\_s}(k+1) \right| \right] \tag{28}$$

where i_{cirj_s} and i_{cirj_t} are the predicted circulating current of s-th and t-th combinations, respectively.

Ignoring the capacitor voltage ripple and based on (14), the predicted circulating current can be expressed as

$$i_{cirj}(k+1) = \frac{T_s}{2L_s}\left[U_{dc} - \frac{U_{dc}}{N} \times \left(n_{uj0}(k) + n_{lj0}(k)\right) - \frac{U_{dc}}{N} \times 2 \times \eta_j(k)\right] + i_{cirj}(k) \tag{29}$$

Based on (29), the values of $i_{cirj}(k+1)$ in each control period are determined by η_j. Fig. 5(a) shows an example about $i_{cirj}(k+1)$ with $\eta_j \in [\eta'_{j(1)}, \eta'_{j(2)}, \eta'_{j(3)}]$ and $i_{cirj\_ref}(k+1)$. The interval between $i_{cirj}(k+1)$ with $\eta'_{j(1)}$ and $\eta'_{j(2)}$ and the interval between $i_{cirj}(k+1)$ with $\eta'_{j(2)}$ and $\eta'_{j(3)}$ are both equal to $U_{dc}T_s/(NL_s)$, which is denoted as d. $e1 \sim e3$ denote the absolute errors between $i_{cirj\_ref}(k+1)$ and $i_{cirj}(k+1)$ with $\eta'_{j(1)}$, $\eta'_{j(2)}$, $\eta'_{j(3)}$. Based on Fig. 5(a), it can be derived that the maximum absolute difference between any two of $e1 \sim e3$ is smaller than $2d$. Combining (28), it can be obtained that

$$|E| < 6d. \tag{30}$$

Similarly, ignoring capacitor voltage ripple and based on (7) and (14), the predicted dc-link current (sum of three-phase circulating currents) can be expressed as

$$i_{dc}(k+1) = \frac{T_s}{2L_s}\left[3U_{dc} - \frac{U_{dc}}{N} \times \sum_{j=a,b,c}\left(n_{uj0}(k) + n_{lj0}(k)\right) + \frac{U_{dc}}{N} \times 2 \times \sum_{j=a,b,c}\eta_j(k)\right] + \sum_{j=a,b,c} i_{cirj}(k) \tag{31}$$

It shows that $i_{dc}(k+1)$ is determined by $\eta'_a + \eta'_b + \eta'_c$. According to different values of $\eta'_a + \eta'_b + \eta'_c$, the 27 candidate combinations in Table 1 can be divided into 7 groups, as shown in Table 2.

Based on (31), in Table 2, the combinations in the same group have nearly identical values of $i_{dc}(k+1)$, while the combinations in the different groups have big differences of $i_{dc}(k+1)$. Fig. 5(b) shows an example about $i_{dc}(k+1)$ of groups (1) ~ 7 and $i_{dc\_ref}(k+1)$. The interval of $i_{dc}(k+1)$ between adjacent groups is d. $g1 \sim g7$ are absolute errors between $i_{dc\_ref}(k+1)$ and $i_{dc}(k+1)$ of groups (1) ~ 7. The bigger the error is, the higher the dc-link current ripple is.

In Fig. 5(b), g3 and g4 are the two smallest errors among $g1 \sim g7$. In this case, it is desired to select the combination from group (3) and (4) for reduced dc-link current ripple. It can be observed that the minimum absolute difference between the two errors ($g3$ and $g4$) and the other errors ($g1$, $g2$, $g5 \sim g7$) is greater than d. Supposing that $i_{cirj\_s}(k+1)$ in (27) is the predicted current of the combination in groups with small errors (like group 3 or 4 in Fig. 5(b)) and $i_{cirj\_t}(k+1)$ in (27) is the predicted current of the combination in other groups, it can be obtained that

$$|D| \geq d. \tag{32}$$

Table 2
Values of $\eta'_a + \eta'_b + \eta'_c$ for Candidate Combinations.

Group	$\eta'_a + \eta'_b + \eta'_c$	Combinations
1	$h_a + h_b + h_c$-3	$V(1, 1, 1)$
2	$h_a + h_b + h_c$-2	$V(1, 1, 2)$, $V(1, 2, 1)$, $V(2, 1, 1)$
3	$h_a + h_b + h_c$-1	$V(1, 2, 2)$, $V(2, 1, 2)$, $V(2, 2, 1)$, $V(1, 3, 1)$, $V(1, 1, 3)$, $V(3, 1, 1)$,
4	$h_a + h_b + h_c$	$V(2, 2, 2)$, $V(1, 3, 2)$, $V(1, 2, 3)$, $V(2, 1, 3)$, $V(2, 3, 1)$, $V(3, 2, 1)$, $V(3, 1, 2)$
5	$h_a + h_b + h_c + 1$	$V(3, 2, 2)$, $V(2, 3, 2)$, $V(2, 2, 3)$, $V(3, 1, 3)$, $V(3, 3, 1)$, $V(1, 3, 3)$
6	$h_a + h_b + h_c + 2$	$V(3, 3, 2)$, $V(3, 2, 3)$, $V(2, 3, 3)$
7	$h_a + h_b + h_c + 3$	$V(3, 3, 3)$

To minimize the dc-link current ripple by the proposed MPC algorithm, it is desired that $J_s < J_t$, which means that (26) should be greater than zero. Combining (26), (30) and (32), the value of λ should meet

$$\lambda \geq 6. \tag{33}$$

Equation (33) can ensure that the combinations in groups with small dc-link current tracking errors have smaller cost functions than those combinations in other groups, so that the proposed ALC method has minimal dc-link current ripple. And these combinations in groups with small dc-link current tracking errors have nearly same dc-link current performance, while they may have different circulating current performance, because their three-phase circulating current tracking errors are different. The combination with smallest cost function will be finally selected. Therefore, (33) can make sure that not only the dc-link current ripple of the MMC can be reduced, but also the three-phase circulating currents are controlled to track their references. It is worth noting that the dc-link current ripple can also be reduced when $\lambda < 6$. When (33) is satisfied, the best dc-link current quality can be achieved, which is independent of MMC system parameters.

4.3. Comparison studies

Table 3 shows the comparison of proposed method with existing MPC methods [9,31,32] that reduce dc-link current ripple for the MMC.

In [9], [31] and [32], the cost function of the MPC algorithms all include ac-side current. Their dc-link current and ac-side current are

Table 3
Comparisons of Dc-link Current Ripple Suppression Methods Using MPC.

Methods	Having effect on ac-side performance	Computational burden (three-phase)	Dc-link current reduction capability	
			Low order	High order
[9]	Yes	$2^{3\times 2N}$	Yes	No
[31]	Yes	$3(N+1)^2$	–	Yes
Method A in [32]	Yes	$2(2N+1)\times 3^3$	No	Yes
Method B in [32]	Yes	27	No	Yes
Proposed method	No	27	Yes	Yes

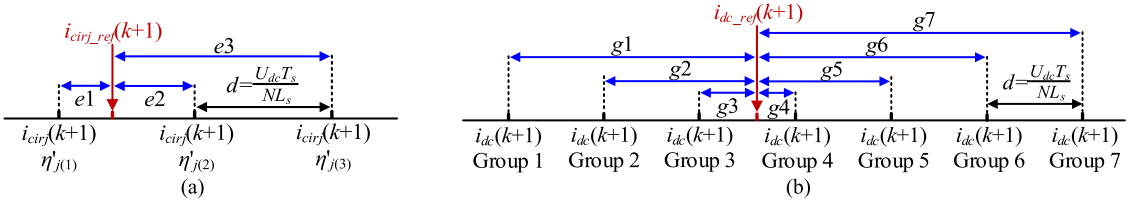

Fig. 5. Predicted current tracking errors. (a) $i_{cirj}(k+1)$ with $\eta_j \in [\eta'_{j(1)}, \eta'_{j(2)}, \eta'_{j(3)}]$ and $i_{cirj\_ref}(k+1)$. (b) $i_{dc}(k+1)$ of groups (1) ~ 7 and $i_{dc\_ref}(k+1)$.

both controlled by cost function with weighting factors. Therefore, the regulation of dc-link current can affect the ac-side current performance. In contrast, the proposed method does not affect ac-side performance, because the cost function of the developed MPC algorithm does not have ac-side current, and the ac EMF is only determined by ac-side voltage levels generated by conventional modulation and not affected by the additional levels generated by MPC. The proposed method has the same ac-side performance as conventional MMC control method.

The combinations in [9,31] and method A in [32] are increased along with N. The combinations in method B in [32] and proposed method are independent of N, which have lower computational burden.

The methods in [9] can reduce low order dc-link current ripple but cannot reduce high order dc-link current ripple. In [31], only high order dc-link current reduction results are presented. In [32], both methods A and B can reduce high-order dc-link current ripple but cannot reduce low order dc-link current ripple. The proposed method can reduce both low order and high order dc-link current ripple for the MMC.

5. Simulation

To confirm the effectiveness of the proposed method, a three-phase MMC with series connected R-L load is simulated through PSCAD/EMTDC. The simulated system parameters are shown in Table 4. The level-increased NLM [17] is applied in the simulation. To better demonstrate the performance of the proposed method, the simulated results of the typical CCSC strategy [24] are also shown for comparison.

5.1. Operation under balanced load conditions

Fig. 6 shows MMC performance with CCSC. Fig. 6(a) shows the capacitor voltages of phase A, which are well balanced. Fig. 6(b) shows waveforms of upper arm current, lower arm current and circulating current of phase A. The second order components of circulating current i_{cira} is suppressed. The peak-to-peak value of circulating current Δi_{cira} is 60 A (36% of the rated value). Fig. 6(c) shows the waveforms of i_{dc}. The peak-to-peak value of dc-link current Δi_{dc} reaches to 95 A (19% of the rated value). Fig. 6(d) shows the spectrum of i_{dc}. Apart from the dc-component, there are also other harmonic components, which ac-counts for the dc-link current ripple. Fig. 6(e) shows the ac-side currents of the MMC. The total harmonics distortion (THD) of the ac-side currents is 1.2%.

Fig. 7 shows MMC performance with the proposed method. Fig. 7(a) shows the capacitor voltages of phase A, which are well balanced. Fig. 7 (b) shows the waveforms of the upper arm current, lower arm current and circulating current of phase A. It shows that the second order circulating current is suppressed. The peak-to-peak value of circulating current Δi_{cira} is 66 A (39.6% of the rated value), which is only a little higher than that in Fig. 6(b). Fig. 7(c) shows the waveform of i_{dc}. The peak-to-peak value of i_{dc} is 43 A (8.6% of the rated value), which is reduced to 43% of that in Fig. 6(c). Fig. 7(d) shows the spectrum of i_{dc}. Compared with Fig. 6(d), most of the harmonic components are suppressed. Fig. 7(e) shows the ac-side currents of the MMC. The THD of the ac-side currents is 1.0%, which is smaller than that in Fig. 6(e). The proposed method does not deteriorate the ac-side performance. From Figs. 6 and 7, the proposed method can reduce dc-link current ripple dramatically.

Fig. 8 shows MMC performance with the proposed method, where λ is tuned at 1. Fig. 8(a) shows the waveforms of the upper arm current, lower arm current and circulating current of phase A. It shows that the second order circulating current is suppressed. The peak-to-peak value of circulating current Δi_{cira} is 60 A (36% of the rated value), which is the same as that with CCSC in Fig. 6(b). Fig. 8(b) shows the waveform of i_{dc}. The peak-to-peak value of i_{dc} is 65 A (13% of the rated value), which is reduced to 68.4% of that with CCSC in Fig. 6(c). Fig. 8(c) shows the ac-side currents of the MMC. The THD of the ac-side currents is 1.0%, which is smaller than that in Fig. 6(e) and identical as that in Fig. 7(e). The proposed method has better ac-side current performance compared with CCSC.

5.2. Operation under unbalanced load conditions

Fig. 9 shows MMC performance without and with proposed method under unbalanced ac loads operation, where the active power is 8 MW. The load resistance in phase A is changed to 15 Ω, while the load resistances in phases B and C are 10 Ω. The controller in [33] is applied to suppress the negative sequence ac-side currents. The proposed method is enabled at $t = 1.5$ s. Fig. 9(a) shows the ac-side currents of the MMC. The waveforms of i_a, i_b and i_c are controlled to be symmetric. The proposed method does not affect the ac-side current performance. Fig. 9(b) shows the waveforms of i_{ua}, i_{la} and circulating current i_{cira}. Before $t = 1.5$ s, i_{cira} has low order ripples. After the proposed method is enabled at $t = 1.5$ s, the low order components of i_{cira} is suppressed. Fig. 9(c) shows the dc-link current of the MMC. Before $t = 1.5$ s, i_{dc} has low order ripples. After the proposed method is enabled, the low order current ripple of i_{dc} is suppressed effectively.

6. Experimental studies

A downscaled three-phase MMC is built to verify the effectiveness of proposed method, as shown in Fig. 10. The dc side of the MMC is connected to a dc power supply. The ac side of the MMC is connected to a three-phase inductor and resistors in star connection. The control algorithm is implemented by digital signal processor (DSP) and the drive signals are transferred to the driving panel of each SM by optical fibers. The level-increased NLM [17] is applied. The system parameters are shown in Table 5. The experimental results with the CCSC [24] are also shown for comparison.

6.1. Operation under balanced load conditions

Fig. 11 ~ 13 show the performance of the MMC under balanced operation conditions. Fig. 11 shows the performance of the MMC when the CCSC is applied. Fig. 11(a) shows the waveforms of i_{dc}, i_{ua}, i_{la} and $2i_{cira}$. It can be seen that the second order circulating current harmonics in phase A is suppressed. In Fig. 11(a), the peak-to-peak value of $2i_{cira}$ is 5.0 A. The peak-to-peak value of the dc-link current Δi_{dc} is 4.0 A. Fig. 11 (b) shows the ac-side current of the MMC, where the THD of the current is 3.3%. Fig. 11(c) shows the upper arm and lower arm output voltages u_{ua}, u_{la}, as well as the $2u_{ea}$. The high frequency pulses of u_{ua}, u_{la} and $2u_{ea}$ in the waveforms are produced because the CCSC changes the number of upper and lower arm output voltage levels of the MMC.

Fig. 12 shows the performance of MMCs with the proposed method. Fig. 12(a) shows the waveforms of i_{dc}, i_{ua}, i_{la} and $2i_{cira}$. The second order harmonics of the circulating current is suppressed. The peak-to-peak value of $2i_{cira}$ is 5.2 A, which is only a little higher than that in Fig. 11 (a). By contrast, the peak-to-peak value of the dc-link current is 1.6 A, which is only about 40% of that in Fig. 11(a). Fig. 12(b) shows the ac-side current of the MMC. The THD of the current is 2.3%. Fig. 12(c) shows the upper arm and lower arm output voltage u_{ua}, u_{la}, as well as the $2u_{ea}$. The high frequency pulses of u_{ua} and u_{la} are produced by the

Table 4
Simulation System Parameters.

Parameter	Value
Active power P (MW)	10
DC-link voltage U_{dc} (kV)	20
Fundamental frequency (Hz)	50
Number of SMs per arm N	20
SM capacitance C_{sm} (mF)	7
Arm inductance L_s (mH)	6
Load inductance (mH)	2
Load resistance (Ω)	10

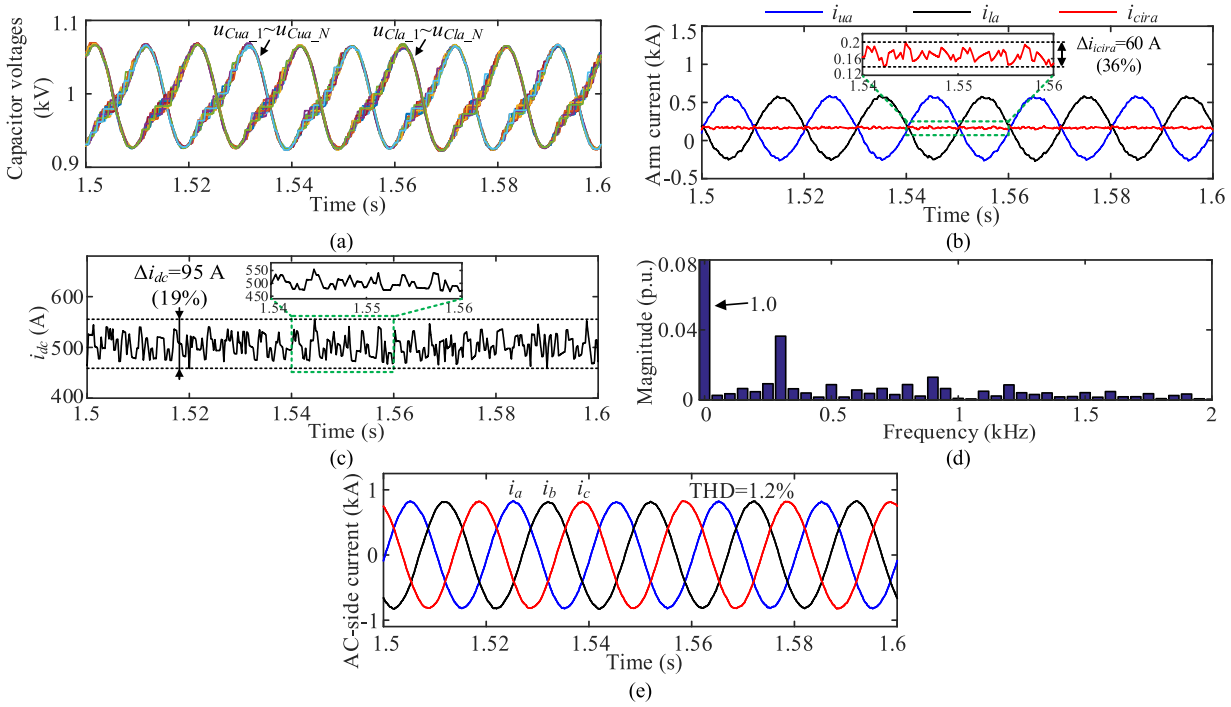

Fig. 6. Simulated waveforms with CCSC. (a) Capacitor voltages. (b) i_{ua}, i_{la} and i_{cira}. (c) i_{dc}. (d) Spectrum of i_{dc}. (e) i_a, i_b and i_c.

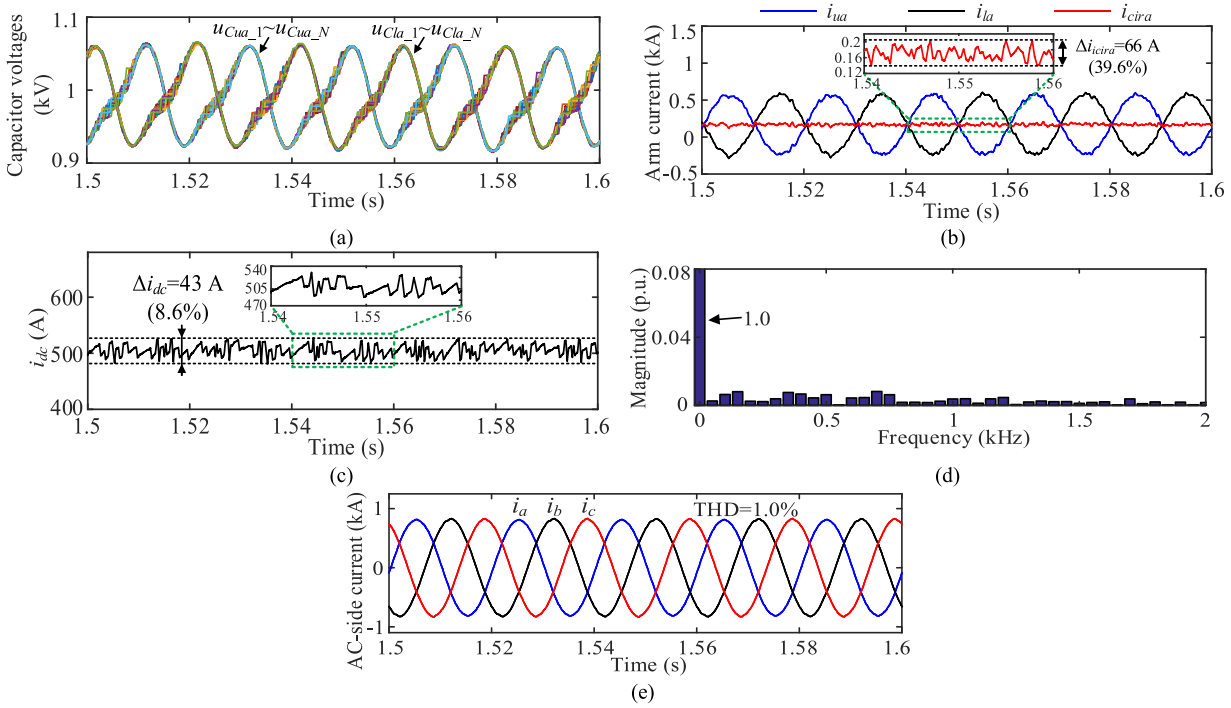

Fig. 7. Simulated waveforms with proposed method ($\lambda = 6$). (a) Capacitor voltages. (b) i_{ua}, i_{la}, i_{cira}. (c) i_{dc}. (d) Spectrum of i_{dc}. (e) i_a, i_b, i_c.

proposed method and always appear at the same time, so that the ac EMF u_{ea} does not have high frequency pulses. Therefore, the ac-side performance of the MMC is not affected by the proposed method.

Fig. 13 shows the performance of MMCs with the proposed method, where λ is tuned at 1. Fig. 13(a) shows the waveforms of i_{dc}, i_{ua}, i_{la} and $2i_{cira}$. The second order harmonics of the circulating current is suppressed. The peak-to-peak value of $2i_{cira}$ is 5 A, which is the same as that in Fig. 11(a). The peak-to-peak value of the dc-link current is 2.2 A, which is 55% of that in Fig. 11(a). Fig. 13(b) shows the ac-side current of the MMC. The THD of the current is 2.3%, which is lower than that in Fig. 11(b) and identical as that in Fig. 12(b). It shows that the proposed method has better ac-side current performance.

6.2. Operation under unbalanced load conditions

Figs. 14 and 15 show the performance of the MMC under unbalanced

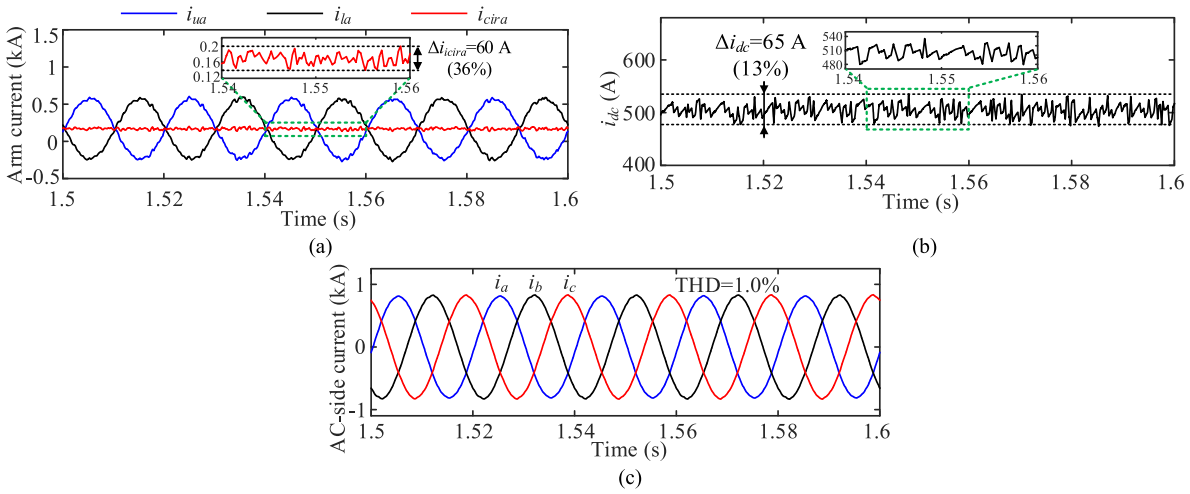

Fig. 8. Simulated waveforms with proposed method ($\lambda = 1$). (a) i_{ua}, i_{la}, i_{cira}. (b) i_{dc}. (c) i_a, i_b, i_c.

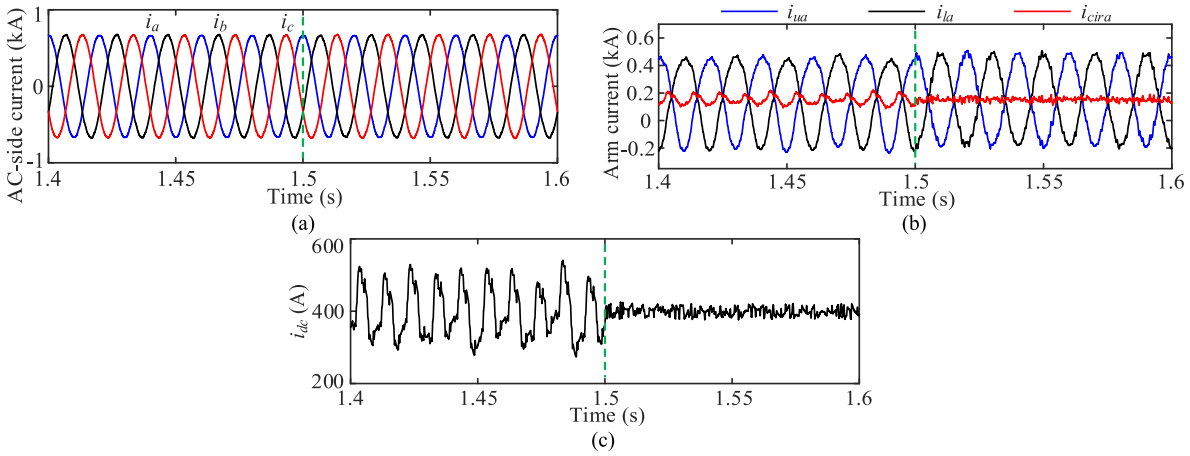

Fig. 9. Simulated waveforms under unbalanced load conditions. (a) i_a, i_b, i_c. (b) i_{ua}, i_{la}, i_{cira}. (c) i_{dc}.

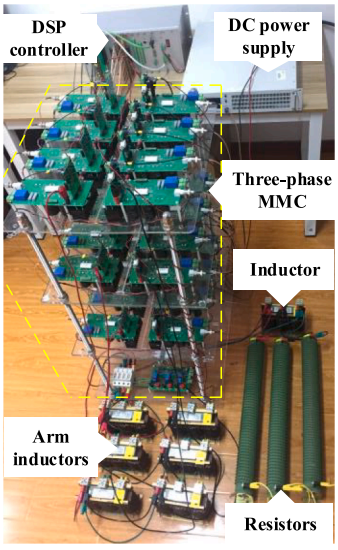

Fig. 10. Photograph of the MMC experimental setup.

Table 5
Experimental System Parameters.

Parameter	Value
Active power P (W)	300
DC-link voltage U_{dc} (V)	100
Fundamental frequency (Hz)	50
Number of SMs per arm N	4
SM capacitance C_{sm} (mF)	2.35
Arm inductance L_s (mH)	5
Load inductance (mH)	5
Load resistance (Ω)	2.5

load conditions. The load resistance in phase A is 5 Ω, while the load resistances in phases B and C are 2.5 Ω. The controller in [33] is applied to suppress the negative sequence current. Fig. 14 shows waveforms without proposed method. In Fig. 14(a), both circulating current and dc-link current have considerable low order fluctuations. The peak-to-peak value of the dc-link current Δi_{dc} is 4.2 A. The peak-to-peak value of $2i_{cira}$ is 13.5 A. Fig. 14(b) shows waveforms of i_a, i_b and i_c, which are controlled to be symmetric. Fig. 15 shows the waveforms when the proposed method is enabled. In Fig. 15(a), the peak-to-peak value of dc-link current Δi_{dc} is 1.8 A, which is greatly reduced. The low order circulating current harmonics in phase A are also suppressed. The waveforms of arm currents become sinusoidal. The peak-to-peak value of $2i_{cira}$ is 4.5 A. Fig. 15(b) shows ac-side currents, which are not affected

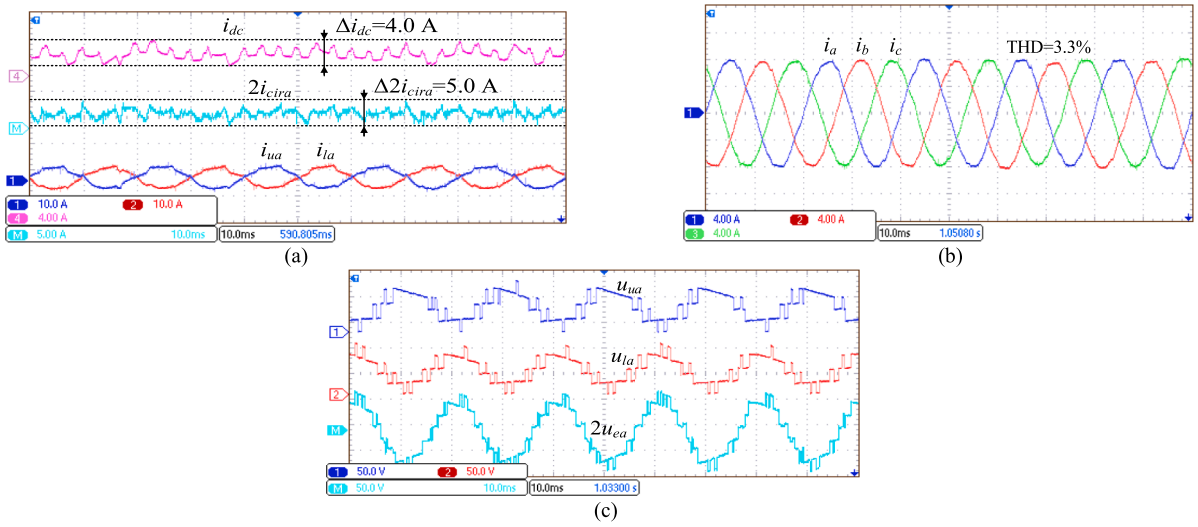

Fig. 11. Experimental waveforms with the CCSC. (a) i_{dc} (4 A/div), i_{ua}, i_{la} (10 A/div), and $2i_{cira}$ (5 A/div). Time base is 10 ms. (b) i_a, i_b, and i_c (4 A/div). Time base is 10 ms. (c) u_{ua}, u_{la}, and $2u_{ea}$ (50 V/div). Time base is 10 ms.

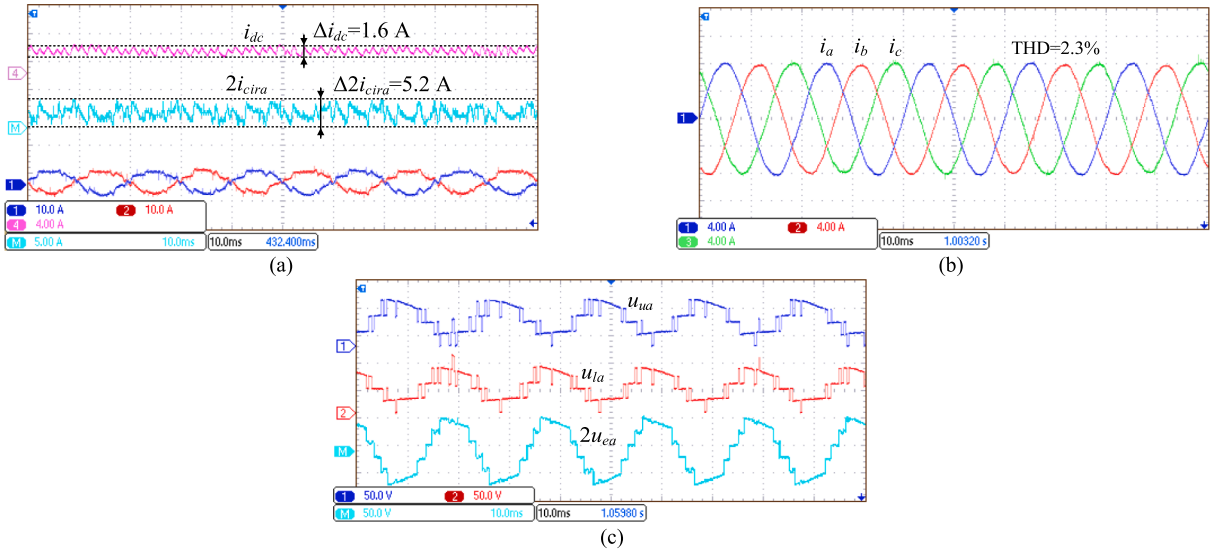

Fig. 12. Experimental waveforms with proposed method ($\lambda = 6$). (a) i_{dc} (4 A/div), i_{ua}, i_{la} (10 A/div), $2i_{cira}$ (5 A/div). Time base is 10 ms. (b) i_a, i_b, and i_c (4 A/div). Time base is 10 ms. (c) u_{ua}, u_{la} and $2u_{ea}$ (50 V/div). Time base is 10 ms.

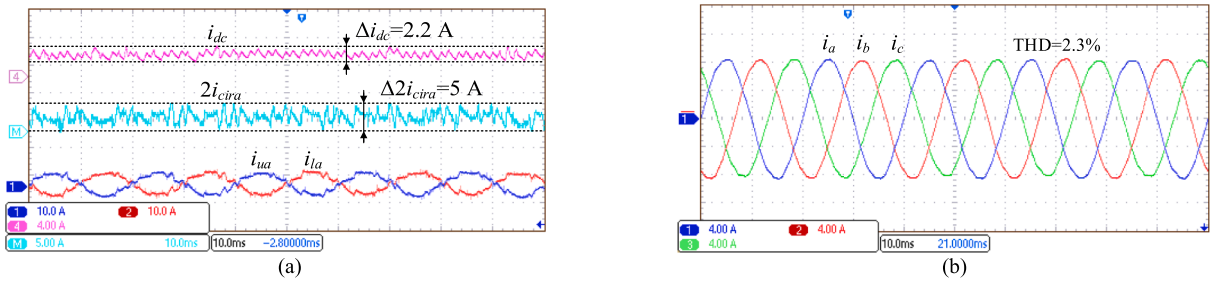

Fig. 13. Experimental waveforms with proposed method ($\lambda = 1$). (a) i_{dc} (4 A/div), i_{ua}, i_{la} (10 A/div), $2i_{cira}$ (5 A/div). Time base is 10 ms. (b) i_a, i_b, and i_c (4 A/div). Time base is 10 ms.

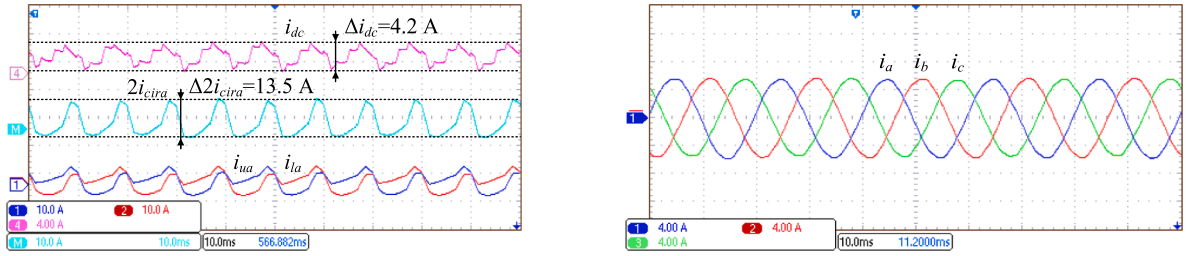

Fig. 14. Experimental waveforms under unbalanced ac loads without proposed method. (a) i_{dc} (4 A/div), i_{ua}, i_{la} (10 A/div), and $2i_{cira}$ (10 A/div). Time base is 10 ms. (b) i_a, i_b, and i_c (4 A/div). Time base is 10 ms.

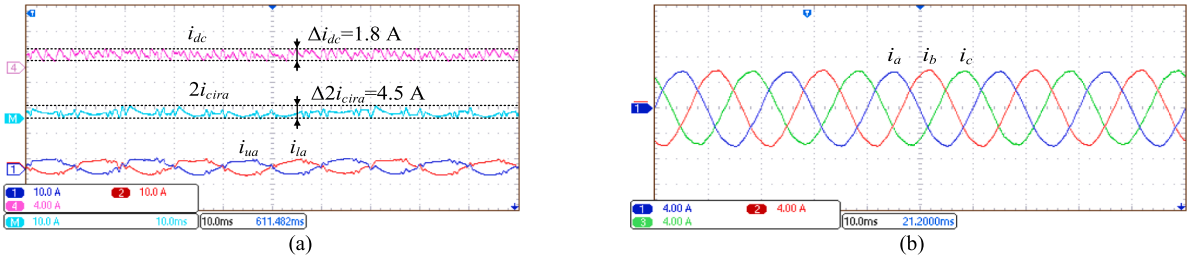

Fig. 15. Experimental waveforms under unbalanced ac loads with proposed method. (a) i_{dc} (4 A/div), i_{ua}, i_{la} (10 A/div), and $2i_{cira}$ (10 A/div). Time base is 10 ms. (b) i_a, i_b, and i_c (4 A/div). Time base is 10 ms.

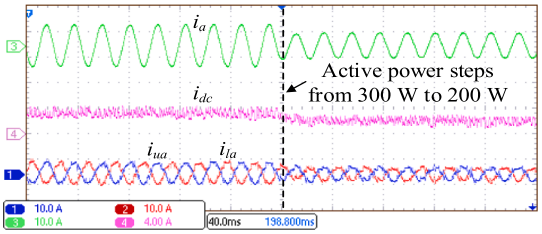

Fig. 16. Experimental waveforms with proposed method including i_{dc} (4 A/div), i_{ua}, i_{la}, i_a (10 A/div). Time base is 10 ms. The active power is dropped from 300 W to 200 W.

by the proposed method.

6.3. Dynamic performance

Fig. 16 shows the dynamic performance of proposed method, where the active power is dropped from 300 W to 200 W. The waveforms of i_{ua}, i_{la}, i_{dc} and i_a are shown in Fig. 16. It can be observed that the MMC works well under the proposed method.

7. Conclusions

This paper proposes an ALC method to reduce both high and low order dc-link current ripple and improve the dc-link current quality for MMCs. In the proposed method, the conventional modulation techniques are employed to generate ac-side voltage levels for necessary ac-side current control, and an MPC algorithm is developed to generate additional levels to control the dc-link current as well as circulating current. Through regulating the additional levels in each control period based on the optimal control combination in MPC, the proposed method can reduce both high and low order dc-link current ripple for the MMC under balanced and unbalanced ac load conditions. The proposed method does not deteriorate the ac-side performance of the MMC. The calculation burden of the proposed method is independent of the number of SMs per arm. Simulations and experimental studies are both conducted, which show that the proposed method can improve the dc-link current performance significantly without affect the ac-side performance.

CRediT authorship contribution statement

Qiang Yu: Conceptualization, Methodology, Software, Validation, Writing – original draft, Writing – review & editing. **Fujin Deng:** Conceptualization, Writing – review & editing, Supervision. **Yi Tang:** Writing – review & editing, Supervision. **Yanbo Wang:** Writing – review & editing. **Frede Blaabjerg:** Writing – review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

References

[1] Qin X, Hu W, Tang Y, Huang Q, Chen Z, Blaabjerg F. An improved modulation method for modular multilevel converters based on particle swarm optimization. Int J Electr Power Energy Syst Apr. 2023;151:109136.
[2] Li H, Deng F, Zhao J, Tian J, Lu Y, Li G. Variable sampling frequency based SM power losses balancing control for MMCs with bypassed faulty SMs. *IEEE Trans Power Electron*, early access 2023.
[3] Li Q, et al. A novel design of circulating current control target to minimize SM capacitance in MMC. Int J Electr Power Energy Syst Dec. 2022;143:108432.
[4] Luo Y, Jia Z, Xu L, Li Q, Song Y. A reduced switching frequency capacitor voltage balancing control for modular multilevel converters. Int J Electr Power Energy Syst Nov. 2022;142:108272.
[5] Deng F, Zhao J, Liu C, Wang Z, Cai X, Blaabjerg F. Temperature-balancing control for modular multilevel converters under unbalanced grid voltages. IEEE Trans Power Electron Apr. 2022;37(4):4614–25.
[6] Xin Y, Chen C, Sun L, Zhou L, Xiong J, Zhang K. Module selection method with improved capacitor voltage balance for MMC using (2*N*+1) SHEPWM. Int J Electr Power Energy Syst Dec. 2021;133:107294.
[7] Tu Q, Xu Z, Chang Y, Guan L. Suppressing dc voltage ripples of MMC-HVDC under unbalanced grid conditions. IEEE Trans Power Del Jul. 2012;27(3):1332–8.

[8] Y. Ma L. Fan Circulating current and DC current ripple control in MMC under unbalanced grid voltage Proc. North American Power Symposium (NAPS) 2015 Charlotte, NC, USA 1 6.
[9] Dekka A, Wu B, Zargari NR. Minimization of dc-bus current ripple in modular multilevel converter under unbalanced conditions. IEEE Trans Power Electron Jun. 2017;32(6):4125–31.
[10] Li K, Liao Y, Lin H, Lin R, Zhang J. Circulating current suppression with improved dc-link power quality for modular multilevel converter. IET Gener Transm & Distrib Apr. 2018;12(10):2220–30.
[11] Deng F, Chen Z. Elimination of dc-link current ripple for modular multilevel converters with capacitor voltage balancing pulse-shifted carrier PWM. IEEE Trans Power Electron Jan. 2015;30(1):284–96.
[12] Deng F, Chen Z. A control method for voltage balancing in modular multilevel converters. IEEE Trans Power Electron Jan. 2014;29(1):66–76.
[13] Yu Q, Deng F, Liu C, Wang Z, Li B, Blaabjerg F. Advanced 2N+1 submodule unified PWM with reduced dc-link current ripple for modular multilevel converters. IEEE Trans Power Electron Apr. 2022;37(4):4261–74.
[14] Deng F, Yu Q, Wang Q, Zhu R, Cai X, Chen Z. Suppression of dc-link current ripple for modular multilevel converters under phase-disposition PWM. IEEE Trans Power Electron Mar. 2020;35(3):3310–24.
[15] Yu Q, et al. DC-link high-frequency current ripple elimination strategy for MMCs using phase-shifted double-group multicarrier based phase-disposition PWM. IEEE Trans Power Electron Aug. 2021;36(8):8872–86.
[16] B. He K. Ma X. Xin W. Wang Hybrid modulation method for nearest-level-control-based MMC to suppress dc power fluctuation when enabling circulating current suppression Proc. IEEE Energy Convers. Congr. Expo. (ECCE) 2020 Detroit, MI, USA 6232 6237.
[17] Lin L, Lin Y, He Z, Chen Y, Hu J, Li W. Improved nearest-level modulation for a modular multilevel converter with a lower submodule number. IEEE Trans Power Electron Aug. 2016;31(8):5369–77.
[18] Dekka A, Wu B, Yaramasu V, Fuentes RL, Zargari NR. "Model predictive control of high-power modular multilevel converters-an overview". IEEE J Emerg Sel Topics Power Electron Mar. 2019;7(1):168–83.
[19] Qin J, Saeedifard M. Predictive control of a modular multilevel converter for a back-to-back HVDC system. IEEE Trans Power Del Jul. 2012;27(3):1538–47.
[20] Yin J, et al. Variable rounding level control method for modular multilevel converters. IEEE Trans Power Electron Apr. 2021;36(4):4791–801.
[21] Vatani M, Bahrani B, Saeedifard M, Hovd M. Indirect finite control set model predictive control of modular multilevel converters. IEEE Trans Smart Grid May 2015;6(3):1520–9.
[22] Hu P, Jiang D. A level-increased nearest level modulation method for modular multilevel converters. IEEE Trans Power Electron Apr. 2015;30(4):1836–42.
[23] Qiu H, Wang J, Tu P, Tang Y. Device-level loss balancing control for modular multilevel converters. IEEE Trans Power Electron Apr. 2021;36(4):4778–90.
[24] Li S, Wang X, Yao Z, Li T, Peng Z. Circulating current suppressing strategy for MMC-HVDC based on nonideal proportional resonant controllers under unbalanced grid conditions. IEEE Trans Power Electron Jan. 2015;30(1):387–97.
[25] Li M, Chang X, Dong N, Liu S, Yang H, Zhao R. "Arm-current-based model predictive control for modular multilevel converter under unbalanced grid condition". IEEE J Emerg Sel Topics Power Electron Jun. 2022;10(3):3195–206.
[26] Li Z, et al. Power module capacitor voltage balancing method for a ±350-kV/1000-MW modular multilevel converter. IEEE Trans Power Electron Jun. 2016;31(6):3977–84.
[27] Wang J, Liu X, Xiao Q, Zhou D, Qiu H, Tang Y. Modulated model predictive control for modular multilevel converters with easy implementation and enhanced steady-state performance. IEEE Trans Power Electron Sept. 2020;35(9):9107–18.
[28] Wang S, Adam GP, Massoud AM, Holliday D, Williams BW. "Analysis and assessment of modular multilevel converter internal control schemes". IEEE J Emerg Sel Topics Power Electron Mar. 2020;8(1):697–719.
[29] Cortes P, Rodriguez J, Silva C, Flores A. Delay compensation in model predictive current control of a three-phase inverter. IEEE Trans Ind Electron Feb. 2012;59(2):1323–5.
[30] Tu Q, Xu Z, Huang H, Zhang J. "Parameter design principle of the arm inductor in modular multilevel converter based HVDC", in *Proc*. Int. Conf. Power Syst. Technol.: Hangzhou, China; 2010. p. 1–6.
[31] Gao X, Tian W, Pang Y, Kennel R. Model-predictive control for modular multilevel converters operating at wide frequency range with a novel cost function. IEEE Trans Ind Electron Jun. 2022;69(6):5569–80.
[32] Chai N, Tian W, Gao X, Rodriguez J, Heldwein ML, Kennel R. "Three-phase model-based predictive control methods with reduced calculation burden for modular multilevel converters". IEEE J Emerg Sel Topics Power Electron Dec. 2022;10(6):7037–48.
[33] Guan M, Xu Z. Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions. IEEE Trans Power Electron Dec. 2012;27(12):4858–67.