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Output Power Control in Class-E Power Amplifiers

Daniel Sira, Pia Thomsen and Torben Larsen, Senior member, IEEE

Abstract—A technique is presented to facilitate power control of cascode class-E power amplifiers (PAs). It is shown that by controlling the signal applied to the gate of the cascode transistor, the transmit power is changed. The main advantage of the proposed technique is a high 36 dB output power control range (PCR) compared to 20 dB for the traditional approach. This fulfills the requirements of the GSM standard on the PCR at all power levels and all frequency bands (for GMSK modulation). The concept of the cascode power control of class-E RF PA operating at 2.2 GHz with 18 dBm output power was implemented in a 0.18 μm CMOS technology, and the performance has been verified by measurements. The PA has been tested by a single tone, and by a GMSK modulated input signal.

Index Terms—Cascode, class-E, CMOS power amplifier, dynamic range, power control.

I. INTRODUCTION

Generally, switch mode PAs are well suited to constant envelope modulation schemes such as Gaussian minimum-shift keying (GMSK) or Gaussian frequency-shift keying (GFSK). In addition, wireless communication standards are employing power control techniques to reduce interference (congestion) in the network, and power consumption of the mobile device.

There have been several fully integrated implementations of class-E PAs in CMOS reported — see e.g. [1], [2], [3], [4]. The conventional power control of a switch mode PA is implemented by adjusting the supply voltage [5]. The conventional technique offers a limited output power control range, especially at low supply voltage [2]. The PCR can be increased by adjusting the input power, but that is generally not desirable in a switch mode class-E PA.

An alternative to the traditional power control scheme is presented in this paper where a cascode voltage controls the output power of the PA. The main advantage of the proposed technique compared to a conventional supply voltage power control technique is increased output power control range.

II. POWER CONTROL TECHNIQUES

Power control techniques for a constant envelope modulation schemes can be used to improve the efficiency of the PA. For a switch mode PA, the input power is expected to be constant, and therefore a supply voltage power control technique (SVPCT) is traditionally employed.

A. Supply voltage power control technique (SVPCT)

The supply voltage power control technique is depicted in Fig. 1(a). The output power is controlled by a power controller.

The output power control range is the maximum range over which the PA output power can be controlled. The GSM900 standard (GMSK modulation) for a mobile station specified by European Telecommunications Standards Institute (ETSI) requires the power control range of 24 dB (class 5) to 34 dB (class 2). In the DCS1800 and PCS1900 frequency bands, the standard requires 24 dB to 36 dB power control range. The power control range can be written as

$$PCR[dB] = P_{out, max} - P_{out, min} = 20 \log_{10} \frac{V_{dd, max}}{V_{dd, min}}$$

where $P_{out, max}$ and $P_{out, min}$ are maximum and minimum average output power in dBm. It is assumed the load impedance is constant. A low voltage class-E PA with a constant input power has a very limited PCR. For a supply voltage range of 0.2 V to 1.8 V the PCR is 19.1 dB.

The main drawbacks of SVPCT are limited output power control range, high sensitivity to load variations, and that the switch mode power controller is placed in the high power path [6]. Since the supply voltage power controller pulls a high current to the PA, the placement in the high power path (in series with the RF choke) makes the efficiency the most important parameter. The efficiency of state-of-the-art power converters is up to 90 % at the maximum output power [5].

It is important to note, that if the supply voltage drops to zero, there is still some output voltage. This is due to feedthrough from the input to the output. In order to maximize the output power control range, the supply voltage controller must be able to reach the positive battery supply rail and also to provide close to zero output voltage. The maximum supply voltage is limited by the reliability of the CMOS PA [1].

B. Cascode power control technique (CPCT)

The proposed alternative power control technique is shown in Fig. 1(b). The power control signal is applied to the gate
of the cascode transistor M3.

In the CPCT the input voltage on the gate of the cascode transistor M3 is divided between $V_{gs,M3}$ and $V_{ds,M2}$ (see Fig. 2). By decreasing the input voltage, $V_{ds,M2}$ also decreases until $V_{CASC} \approx V_{th,M3}$ when $V_{ds,M2}$ drops close to zero ($V_{th,M3}$ is the threshold voltage of the transistor M3). For the SVPCT, the supply voltage can be decreased almost to zero. Therefore, the input dynamic range of the CPCT is approximately one threshold voltage lower than in the SVPCT.

In the technology used for the experimental work in Section III, the threshold voltage is $0.55\,\text{V}$. By taking into consideration the subthreshold region of the transistor, $V_{CASC}$ can be decreased approximately to $0.3\,\text{V}$.

The CPCT also provides higher output power control range than the SVPCT. This is because the capacitive coupling between the input (gate of M2) and the output (drain M3) is reduced, provided the cascode transistor M3 is in saturation. In the CPCT this is fulfilled for the whole $V_{CASC}$ range.

The PAE of the CPCT is higher than of the SVPCT due to the lower power losses associated with parasitic capacitances charging/discharging. The voltage across M2 is limited by the cascode M3. By decreasing the supply voltage in the SVPCT, the transistor M3 goes into the linear region. This increases the voltage swing across M3. Therefore, the dissipated power due to the charging/discharging of parasitic capacitances at the common node of M2 and M3 is also increased. On the other hand, by decreasing the $V_{CASC}$ voltage in the CPCT M3 stays in saturation and M2 stays in the linear region. The voltage swing across M3 is limited and the CPCT has lower power loss than SVPCT.

In the proposed design, the finite RF choke (RFC) technique was used and the maximum drain voltage peak is reduced to $2.5\,V_{dd}$ [3].

III. MEASUREMENTS

Fig. 2 shows the proposed two-stage PA where the class-E output stage (M2 & M3) is driven by a class-E driver stage (M1). A microphotograph of the implemented power amplifier is shown in Fig. 3. The area of the PA is $1.2 \times 1.0\,\text{mm}^2$. Supply voltages are filtered on the PCB (capacitors C3 and C7 in Fig. 2). Inductors L4 and L5 are realized by bond-wires. The adaptive power control circuit was not implemented in the prototype, and therefore the performance is evaluated for specific values of $V_{CASC}$ and $V_{DD2}$ voltages.

The measured AM-AM characteristic is depicted in Fig. 4. The input dynamic range of the CPCT is 14.5 dB (from 0.3 V to 1.6 V) whereas SVPCT offers 24 dB (from 0.1 V to 1.6 V). The available input power was 3.5 dBm at a frequency of 2.2 GHz.

The measured AM-PM distortion for a fixed input power. The phase distortion of the CPCT is larger than that of the
Fig. 5. Measured average in-band power of the PA ($P_{OUT}$) delivered to a 50Ω load versus $V_{DD2}$ ($V_{CASC} = 1.6\,V$) and $V_{CASC}$ ($V_{DD2} = 1.6\,V$). The input signal is a GMSK modulated signal (BT=0.3) at a carrier frequency of 2.2GHz with 3.5dBm available average input power. The measurement bandwidth is 200kHz around the carrier.

SVPCT. This is due to the parasitic drain capacitance variation of the cascode transistor (M3) on the $V_{CASC}$ voltage, and due to the Miller drain-gate capacitance of the switching power transistor (M2). The high AM-PM doesn’t deteriorate the phase error (or EVM) in the transmitting signal because the power control signal has a very low frequency (for GSM/EDGE it is approximately 16.6 Hz) and its value can be considered constant during the frame period.

The performance comparison between the proposed PA and a published CMOS PAs is shown in Table. I.

IV. CONCLUSION

This letter presents a power control technique of a cascode class-E PA. The proposed cascode power control technique provides a high 36dB output power control range. This is about a 16dB larger control range compared to a conventional supply voltage power control technique. It also provides a slightly higher PAE at high output power than supply voltage power control technique. The cascode power control technique appears attractive because of elimination of the switch mode power switch needed in the supply voltage power control technique. A single tone and GMSK modulated input signals were used to characterize the PA performance. The measurements have been performed on a 0.18μm CMOS implemented power amplifier capable of delivering 18dBm output power to a 50Ω load at 2.2GHz.

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REFERENCES


TABLE I

<table>
<thead>
<tr>
<th>Technology</th>
<th>Frequency</th>
<th>VDD</th>
<th>Peak $P_{out}$</th>
<th>Peak PAE</th>
<th>$P_{out}$ Dynamic Range</th>
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<td></td>
<td>[μm]</td>
<td>[GHz]</td>
<td>[V]</td>
<td>[dBm]</td>
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