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Dynamic Current Sharing Optimization of Asymmetric SiC Power Module

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***Abstract*—The dynamic current imbalance in the power modules with paralleled Silicon Carbide (SiC) MOSFETs appears due to the die parameter variations and layout asymmetry. This can force the derating of a power module and decrease reliability, potentially leading to a thermal runaway. In this work, an optimization scheme, compensating for the layout asymmetry using the individual gate and drive source resistances is presented. The results are verified experimentally in a Double Pulse Test setup.**

***Index Terms*—SiC paralleling, current sharing, gate resistance, optimization**

I. Introduction

Recently, Silicon Carbide (SiC) devices experienced widespread adaptation due to the higher breakdown voltage and higher switching speed compared to silicon devices [1]. Unfortunately, the current carrying capacity of SiC MOSFET dies can be too low for high-power applications, forcing die paralleling in power modules targeting such implementations [2].

The main challenge in paralleling is ensuring balanced current sharing between the SiC dies. The balance can be affected by the on-state resistance (R_{dson}) and threshold voltage (V_{th}) spread between the chips, and by layout asymmetry. The current sharing issue is typically divided into static and dynamic current sharing, associated with gate and power loops respectfully [3].

Dynamic current balancing is dependent on V_{th}, the responses of gate and power loops, and couplings within the system. It is the main concern for SiC MOSFET paralleling, due to the negative temperature coefficient of V_{th} causing the most loaded chips to further increase the share of current they conduct. This can result in a thermal runaway and forces derating of modules with paralleled SiC dies [4]. Moreover, with the increase of paralleled die number, achieving layout symmetry becomes more and more challenging limits the achievable SiC power module current ratings [3].

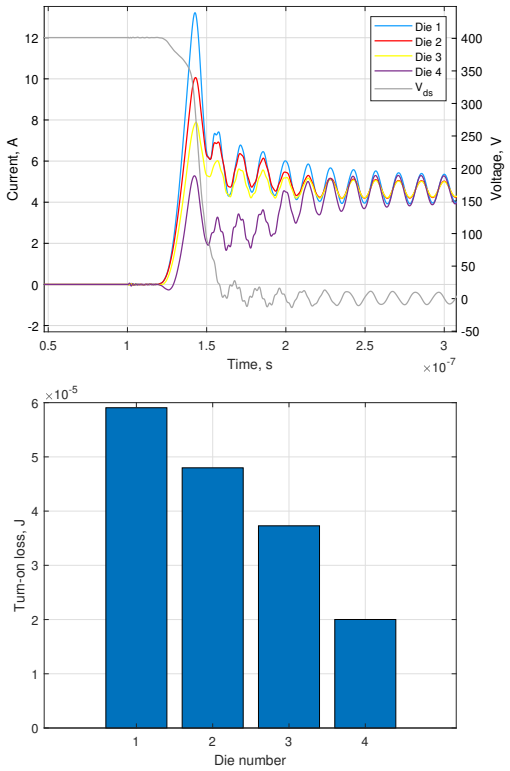

Fig. 1. Switching waveform example with high dynamic current imbalance (Top) and energy loss for each die (Bottom).

In order to solve the problem of dynamic current imbalance, multiple approaches have been proposed. Sorting has been used for minimizing the die parameter variation [5], bondwire placement [6] has been adjusted compensating imbalances, and additional components have been inserted into power and gate loops in order to improve the current sharing [7]. Finally,

active gate driving techniques have been deployed [8].
In this paper, a digital twin-based optimization scheme for improving current sharing by the selection of internal gate and gate source resistances is presented.

II. Dynamic Current Imbalance Mitigation

The previous section introduced the problem of dynamic current sharing in paralleled SiC MOSFET. Starting from die level, solutions proposed in the literature are described in this section.

A. Die screening methods

The die sorting have been described in [5]. They require acquiring IV curves and transfer characteristics of all the available dies and performing clustering in order to find the most similar groups of dies. The process itself can easily cause die damage, as authors reported 2 out of 30 screened die have been damaged during the screening. An improved approach has been presented in [9], where die data is directly linked to the potential current imbalance. This allows bypassing the preparation of custom MOSFET models. Those methods, even though not sufficient to fully mitigate imbalance, are quite effective in limiting it. Unfortunately, their effectiveness relies on having a large number of dies with clusters suitable for the type of layout necessary. The difficulty in finding matching dies increases sharply with the number of paralleled dies, requiring a significant die population to choose from.

B. Layout methods

In [6] bond wire number and placement are varied in order to improve current sharing, [10] combines this with layout design for improved current sharing. It is an effective strategy with a limited compensation range. For this reason, it will likely be insufficient in larger paralleled structures.
Module layout is an important factor for current sharing and has been used for improving the balance [1], however individual adaptation to each die set is hard to deploy in large-scale manufacturing. On the other hand, generally good layouts are still unable to eliminate die variation and begin to introduce additional imbalance when a larger amount of dies has to be paralleled [3].

C. Active gate driving

Active gate driving has been used to mitigate the current imbalance in [8]. Combining a differential current sensor for detecting the imbalance, and a variable gate delay circuit in each MOSFETs, the turn-on losses have been matched between two devices with significant threshold voltage spread. While this solution provides good results, it requires differential current measurement in order to be efficient. Additionally, access to separate gate terminals for each die is required in order to vary the delays. Both of those requirements scale badly with the amount of parallel dies.

D. Balancing component

Differential choke is proposed in [7]. All of the power loops are led around the magnetic core, providing good coupling between them, which leads to improved current sharing. This also forces a significant constraint on module layout, especially in the case of a high number of parallel dies. The space consumption by the choke also can become a potential issue.

III. Optimization scheme

This work improves the current sharing by adjusting drive source and gate resistances using genetic algorithm optimization, targeting highly asymmetric power module layout with four parallel dies.

The target of the optimization scheme presented in this section is a highly asymmetric half-bridge module layout presented in Fig.2.

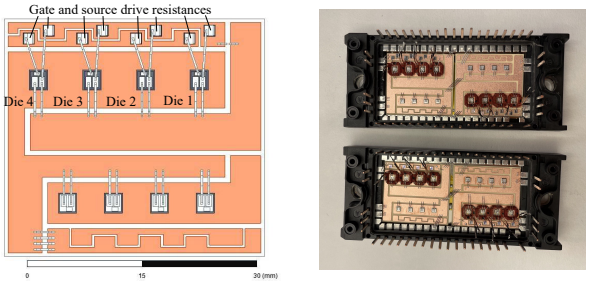

Fig. 2. Layout used in Q3D rendering (left) and manufactured modules (right).

A. Case modelling

The optimization has been conducted on a Double Pulse Test (DPT) setup. The power module geometry has been modelled using SolidWorks and used for RLGC parasitic matrix extraction with Ansys Q3D. The full parasitic model of the module has been then exported as a SPICE subcircuit. The DPT setup has been modeled in MATLAB using the LTSM interface to LTSpice. The schematic has been depicted in the figure below, with unnamed elements being a simplified parasitic model.

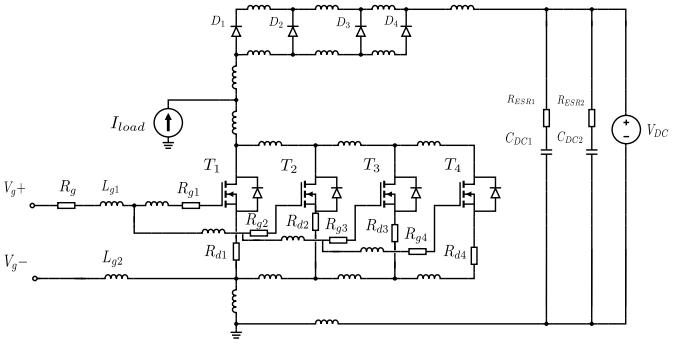

Fig. 3. Simplified model schematic

The load has been modeled as a current source, as no specific application is assumed. The named circuit parameters have been described in the table below.

TABLE I
MODEL DATA

Parameter	Value	Unit
Rg	43	Ohm
I_{load}	15	Amp
V_{DC}	400	V
R_{g1-4}	0, 1.8, 3, 5, 10, 15	Ohm
R_{d1-4}	0, 1.8, 3, 5, 10, 15	Ohm
C_{DC1}	0.02	uF
C_{DC2}	47	uF
MOSFET model	CPM2-1200-0160B	-
Diode model	CPW41200S010B	-

The manufacturer-provided models have been used for diodes and MOSFETs. Due to this approach, a potential risk of die parameter imbalance is introduced. The gate driver has been modelled as a PWL voltage source of with a fixed transition slope. The model is publicly available in the CoDE project Git Hub repository.

B. Defining a cost function

Selecting the cost function for switching waveform optimization is not a trivial problem. Incorrect definitions can lead to significant issues, even when the cost function has been based on widely-used metrics, such as rise time or overshoot.

Had a rise time matching been chosen, all the conditions below 10% and above 90% of steady-state current value are ignored. In some cases, this can encourage introducing high oscillations and overshoots that allow to achieve both lower and more matched rise times. High oscillations negatively affect electromagnetic compatibility. Therefore, a metric promoting an upper bound on the signal can be preferred, encouraging a choice of overshoot matching. This approach is much better than the rise time matching. However, it promotes a very conservative switching, as the differences between overshoots are much smaller when the overshoot is minimal, leading to a slow switching and excessive losses.

Finally, as loss balance is the main issue so switching loss matching would be a good metric to address the issue directly. However, it does have a potentially fatal flaw when applied to a switching waveform optimization problem. Minimal, and perfectly matching switching loss can be achieved by avoiding switching at all, and this will certainly be exploited by the optimization algorithm as long as optimization variables have states allowing to prevent switching. For this reason, a more robust approach to cost function definition is desired.

This paper proposes a solution to the above-mentioned issue, by introducing the perfect waveform approach. First, a perfect current waveform is defined based on the ideal gate driver waveform. As in the most desired case for switching, the perfect current waveform would have no delay in relation to the gate signal. The slope of a perfect waveform would tend to infinity, to minimize the switching loss or to the current derivative limit required by application. Therefore a perfect current waveform for our application can be depicted as below.

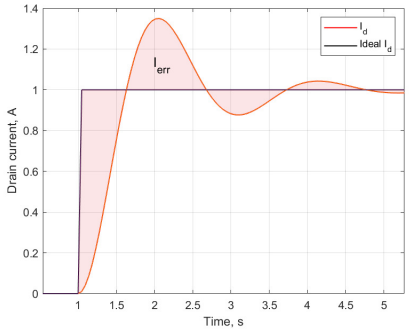

Fig. 4. Cost function visualisation

The proposed cost function value equals the area between the actual and perfect current waveform for the single switch case. For improving the current sharing in multiple parallel switches, the difference between those areas for each die is to be minimized. This cost function is robust against no-switching exploitation while still leading toward matched losses.

C. Optimization results

The results of optimization scheme are presented below.

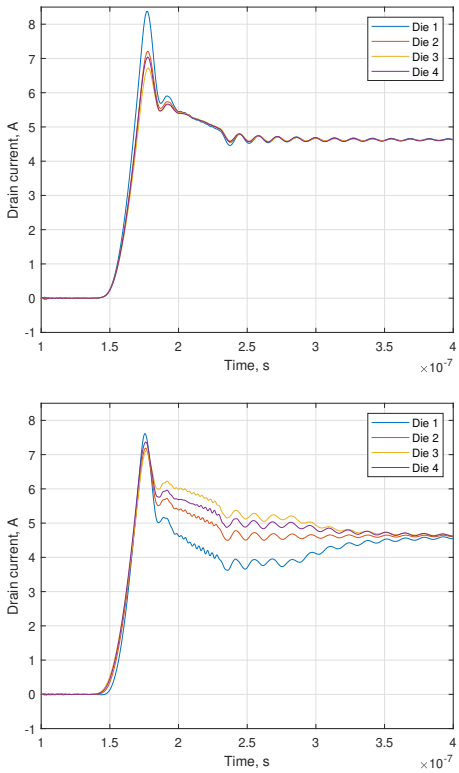

Fig. 5. Simulated die currents of unoptimized (Top) and optimized (Bottom) power module.

As it can be seen in the Fig 5, the balancing has been improved in terms of overshoot matching. The current imbalance has been shifted to the later phase of switching, past the voltage fall, which can reduce the loss mismatch.

IV. Experimental validation

In order to validate the optimization results experimentally, a DPT setup has been prepared. The current measurements have been taken as described in the figure below.

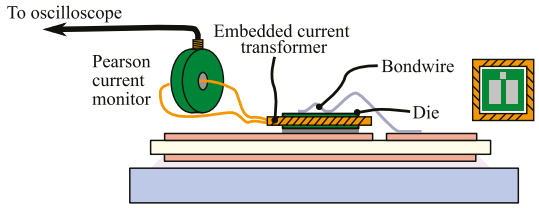

Fig. 6. Current measurement visualisation, adapted from [12]

The rest of the setup consisted of a load inductor of 103μH has been used, along with an external driver board.

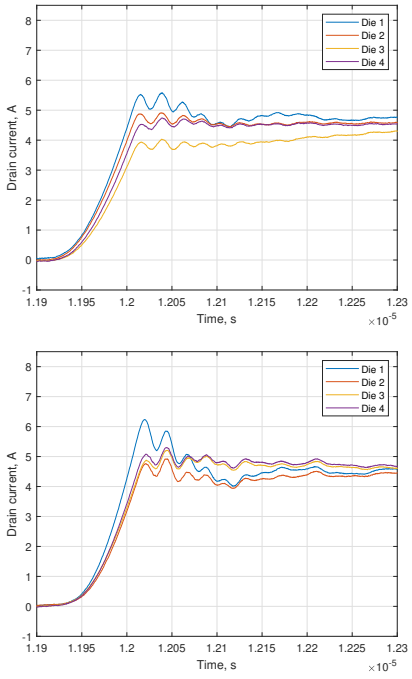

Fig. 7. Experimental die current switching waveforms at 18.3A total module current for unoptimized (Top) and optimized (Bottom) module.

As can be seen in Fig. 7, improved overshoot matching has been achieved. The maximum current imbalance has decreased in the optimized module and shifted to a later part of the transient. Compared to the simulation results, a significantly slower switching speed has been observed.

V. Error analysis

In this section, the significant mismatch between simulation and experiment is investigated. Additional measurements have been conducted at different current and voltage levels. The simulation model has first been altered by introducing additional inductance of 50 nH in the gate loop, potentially introduced by the external gate driver board. Next, a less steep gate driver voltage slope is introduced.

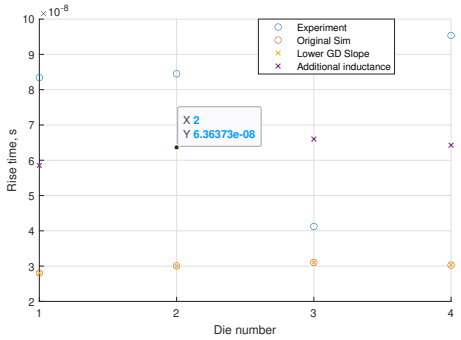

Fig. 8. Rise time error analysis at 200V DC-link voltage and 9.3A load

Based on Fig. 8, gate loop inductance underestimation might be the reason behind the simulation and experiment mismatch.

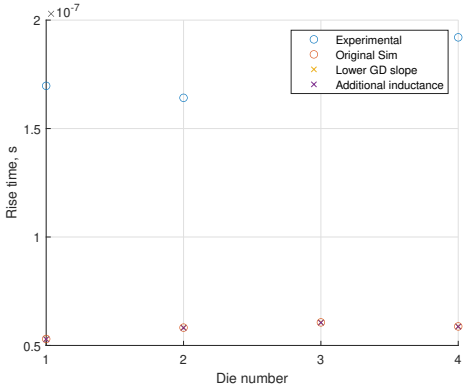

Fig. 9. Rise time error analysis at 400V DC-link voltage and 41A load

Fig. 9 depicts the investigation results at higher load and increased DC-link voltage. At this current and voltage level, introducing extra gate loop inductance did not have such a significant effect as in the previous case.

VI. Conclusion

In this paper, an optimization scheme for compensating layout imbalance in power modules with paralleled SiC MOSFETs using gate resistances was presented and verified experimentally.

The current imbalance has been decreased and shifted to the less crucial part of the switching transient, as the contribution to the loss difference will be smaller due to the lower voltage present in this phase of the switching transient.

Even though a mismatch between simulation and experimental results has been found, the optimization has been effective. The error has been investigated and can be attributed to an underestimation of inductance in the gate loop, combined with

the die parameter variation that was unaccounted for.
In future works, a higher resistance resolution can be used to further improve the current balance. Including current and temperature variation in the optimisation scheme may also be worth exploring.
The models and MATLAB code used for this optimization case is publicly available at the CoDE project GitHub repository [11].

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