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A Novel Common-Ground-Type Nine-Level Dynamic Boost Inverter

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***Abstract*– Recently, inverters with a common ac and dc ground are gaining significant interests due to their zero common-mode voltage that made them particularly attractive for the solar photovoltaic (PV) application. However, the dc source current of the existing topologies is discontinuous, and their voltage gains are limited. This paper proposes a novel common-ground-type boost inverter that achieves continuous dc source current with significantly enhanced dynamic voltage gain. It consists of one boost inductor, four capacitors, nine power MOSFETs and two power diodes. Voltage-boosting and generation of 9-level ac voltage are achieved concurrently within a single-stage operation. The operation of the proposed CGT-9L-BI inverter is analyzed. Simulation and experimental results are presented for validation.**

***Index Terms*– Boost inverter, common ground, multilevel inverter, nine level, single-stage.**

I. Introduction

HIGH penetration of photovoltaic (PV) energy in modern power systems expedites the tremendous development of various power electronic converters [1]–[3]. The transformerless inverters, in particular, are steadily rising to become one of the prominent enabling technologies in integrating PV energy into power systems [4], [5]. These transformerless inverters does not require a bulky transformer and thereby enhances their compactness and power conversion efficiency. The absence of transformer in the configurations, however, unfavorably gives rise to insufficient voltage isolation between the PV source and the ac output. The resulting high-frequency common mode voltage (CMV) across the stray capacitor of PV modules will therefore induce the risk of leakage current [6].

The high-frequency CMV issue can be effectively counteracted in a neutral-point-clamped (NPC) inverter configuration. With the ac neutral grounded to the midpoint of dc-link, the stray capacitor of PV modules is clamped across the dc-link capacitor and thus preventing leakage current [7]. Nonetheless, the limited voltage gain and voltage levels are two main downsides of the classical NPC inverter [8]. With the maximum attainable voltage level of only half the dc-link voltage, high dc-link (dc source) voltage of at least twice the ac peak voltage is always mandatory. While high dc voltage requirement is mostly accompanied by an indispensable front-end boost dc-dc converter, there has been a tendency in reducing the magnitude of dc source voltage in transformerless topologies.

In an attempt to realize a single-stage structure, significant efforts have been devoted on developing topologies based on H-bridge inverter which features unity gain, three levels generation, and a maximum voltage level equal to dc source voltage. As the neutral of ac output in a H-bridge inverter is connected to a half-bridge, some structural modifications are required to provide galvanic isolation between the PV source and ac output. For instance, it might requires the incorporation of either an additional dc-bypass circuit into its dc side or an additional ac-bypass circuit into its ac side, where either circuit consists of power switches and diodes [9]. Noting that high-frequency CMV remains an issue in H-bridge based topologies and therefore the establishment of complex modulation technique is essential [10].

A new class of transformerless inverter with a common ac and dc ground has recently garnered increasing popularity. Effective CMV mitigation is achieved with its ac neutral grounded to the negative terminal of PV source [11]. To make the common ac and dc ground possible, [12] uses an electrolytic capacitor to establish the concept of virtual dc-bus, as shown in Fig. 1(a). The virtual dc-bus is charged to dc source voltage during the positive and zero voltage levels. Negative voltage level can be generated by reversing the polarity of the virtual dc-bus across the ac load. Note that the dc source is not utilized to supply the load during negative voltage level and hence its negative terminal can remain connected to the neutral of ac output. Similar concept is extended in [13] (Fig. 1(b)) where two capacitors are adopted to ensure sufficient energy storage to supply the load during negative voltage level and reduce the magnitude of voltage ripple. The various common-ground-type inverters which are capable of 3-level generation are summarized in [14]. Fig. 1(c) presented in [14] requires only one diode to be inserted into the second leg of an H-bridge that makes it the most compact 3-level topology.

An attempt to increase the number of levels generation from 3 to 5 is made in [15], as depicted in Fig. 1(d). It is a hybrid topology that replaces the first H-bridge leg of Fig. 1(c) with a flying capacitor inverter. In a separate attempt, voltage-

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boosting is made possible by utilizing two SCs to realize a twofold voltage gain in Fig. 1(e) [16]. One of the SCs is charged to twice the dc source voltage magnitude so that the maximum voltage level is twice the dc source voltage. However, the number of ac voltage levels remains 3 despite the use of two capacitors.

In recent literature, the common-ground-type inverters have seen evolution in terms of their simultaneous achievement of 5-level voltage generation and double voltage gain [17]–[19]. Further enhancement in the voltage levels generation, such as 7-level and 9-level topology is also presented in [20] (Fig. 1(i)) and [21] (Fig. 1(j)), respectively.

All the aforementioned common-ground-type inverters exhibit a common characteristic such that their dc sources are not fully exploited during some or all the negative voltage levels. A simulation study of Fig. 1(h) is conducted to investigate the consequence of disconnecting the dc source during some voltage levels. As shown in Fig. 2, the dc source current is discontinuous. This is a tradeoff of the common-ground structure that hinders their application for PV system. Aiming to resolve this drawback, a novel topology is proposed in this paper and its key contributions can be summarized as follows:

(a) A distinctive topological structure in accomplishing common ac and dc ground to enable leakage current mitigation.
(b) Capability of nine symmetric voltage level generation with low number of power semiconductor devices.
(c) Enhanced voltage boost capability for a single-stage dc-ac power conversion.
(d) The provision of continuous dc source current to accommodate the PV source.

The remainder of this paper is organized as follows. In Section II, the steady-state analysis of the proposed topology is presented. Section III compares the proposed topology with the state-of-the-art common-ground-type inverters. Simulations and experimental results are discussed in Section IV. Finally, Section V concludes the article.

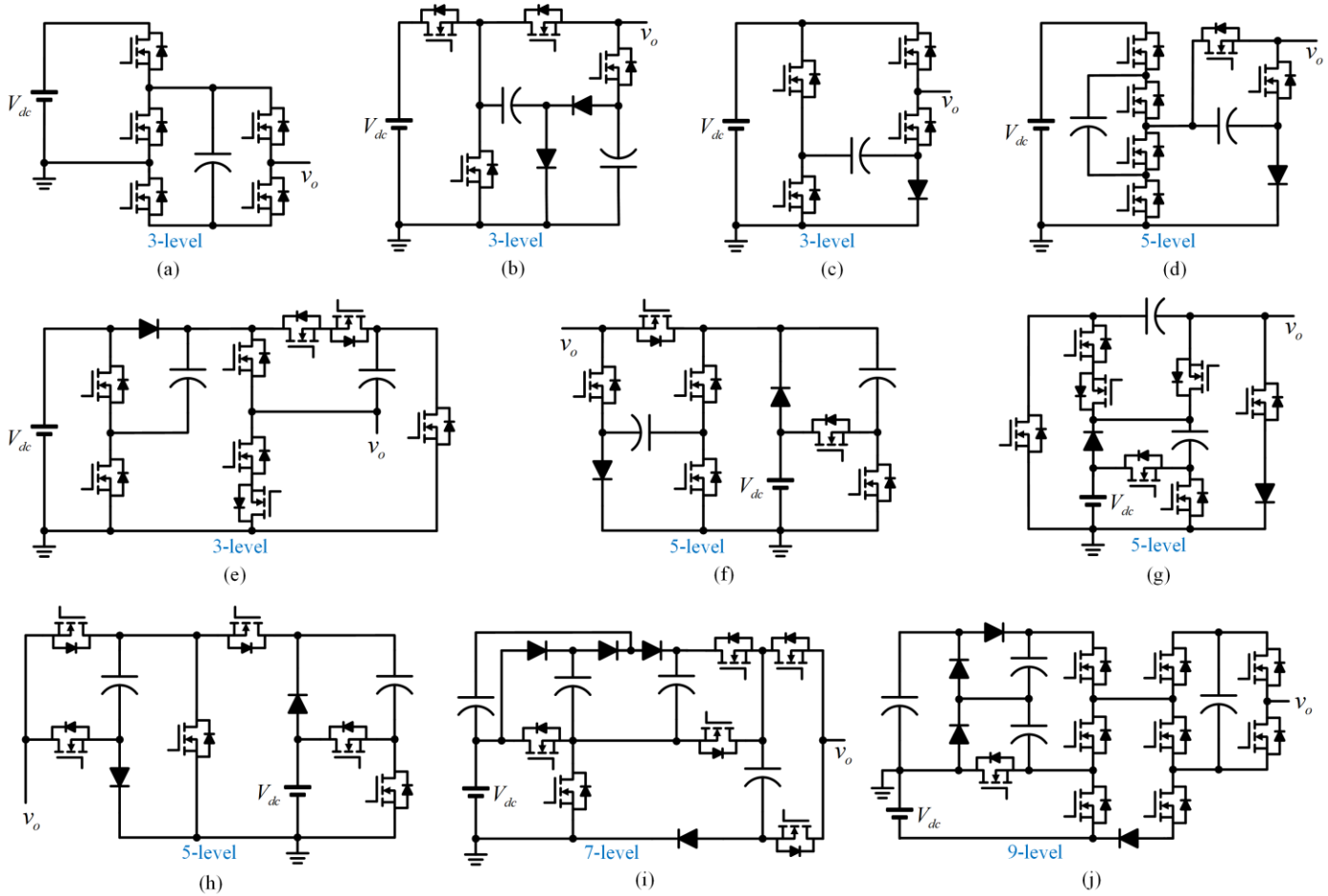

Fig. 1. Existing multilevel inverter with common ac and dc ground presented in: (a) [12], (b) [13], (c) [14], (d) [15], (e) [16], (f) [17], (g) [18], (h) [19], (i) [20], and (j) [21] (the common ac and dc ground is located at dc source positive terminal instead of negative terminal in all other topologies).

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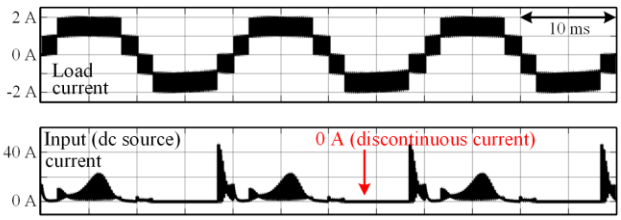

Fig. 2. Simulation results of Fig. 1(h) showing discontinuous input (dc source) current.

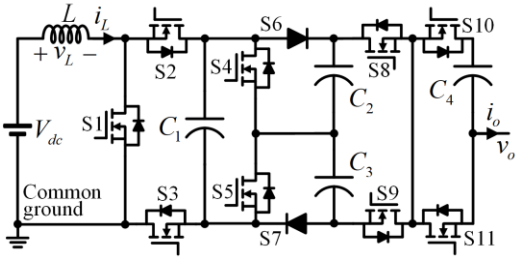

Fig. 3. Proposed common-ground-type nine-level boost inverter (CGT-9L-BI).

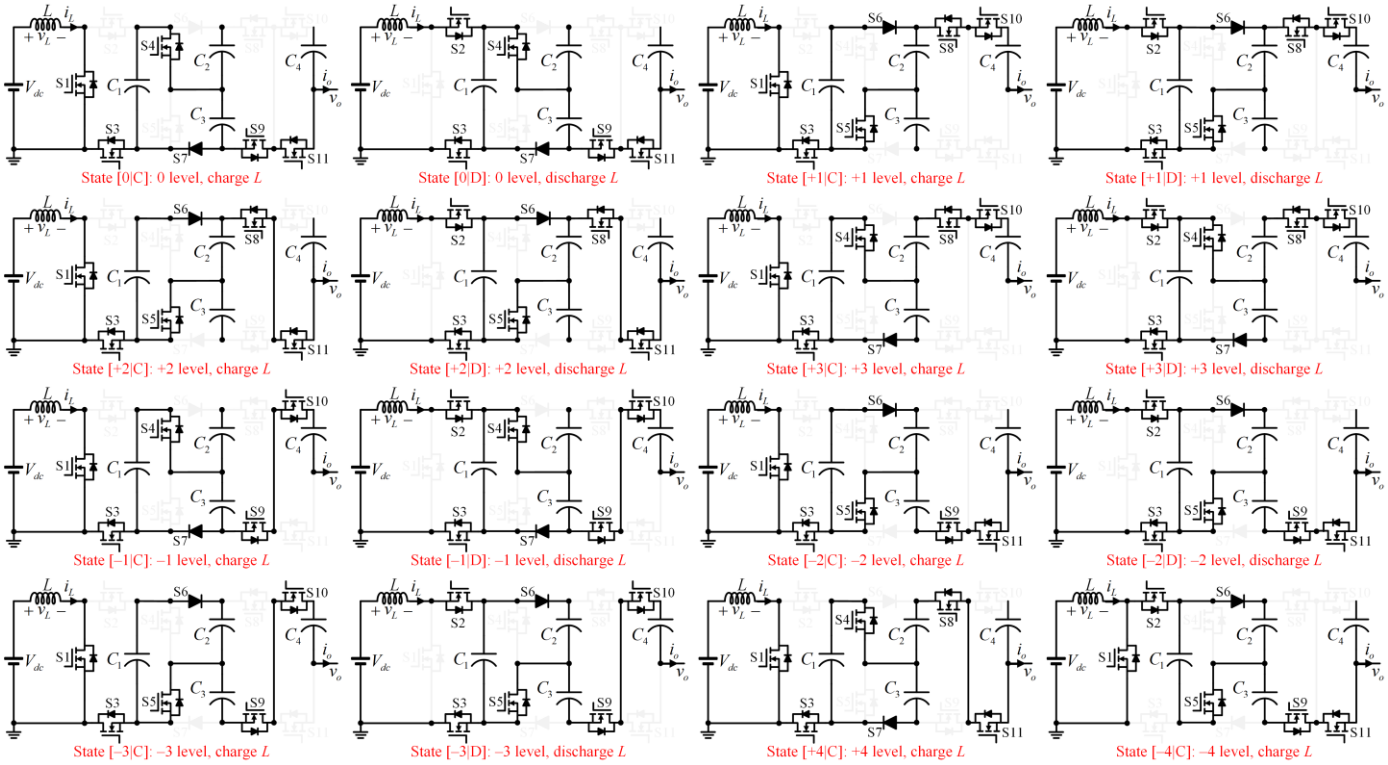

Fig. 4. Switching states of the proposed CGT-9L-BI.

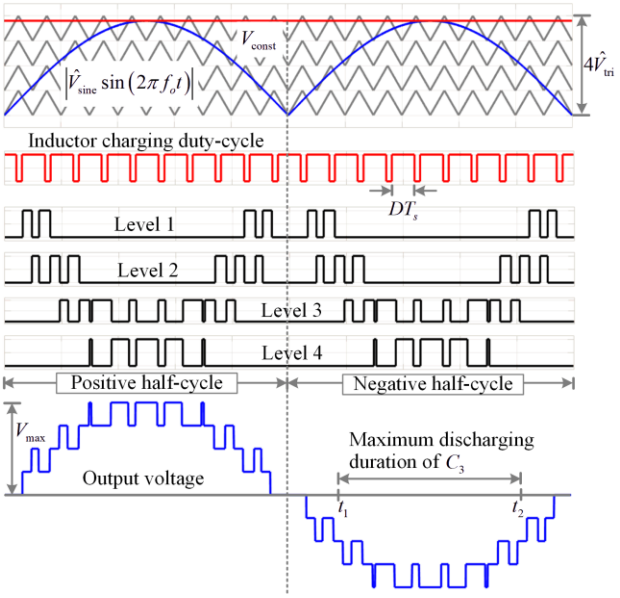

Fig. 5. Multicarrier PWM for the proposed CGT-9L-BI.

TABLE I.
SUMMARY OF SWITCHING STATES

State	S1 – S11	Inductor	Voltage level
[0|C]	10110010101	charging	0
[0|D]	01110010101	discharging	
[+1|C]	10101101010	charging	$+0.25V_{max}$
[+1|D]	01101101010	discharging	
[+2|C]	10101101001	charging	$+0.5V_{max}$
[+2|D]	01101101001	discharging	
[+3|C]	10110011010	charging	$+0.75V_{max}$
[+3|D]	01110011010	discharging	
[+4|C]	10110011001	charging	$+V_{max}$
[–4|C]	11001100101	charging	$-V_{max}$
[–3|C]	10101100110	charging	$-0.75V_{max}$
[–3|D]	01101100110	discharging	
[–2|C]	10101100101	charging	$-0.5V_{max}$
[–2|D]	01101100101	discharging	
[–1|C]	10110010110	charging	$-0.25V_{max}$
[–1|D]	01110010110	discharging	

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II. Proposed CGT-9L-BI

Fig. 3 shows the circuit diagram of the proposed topology that consists of a boost inductor, four capacitors, nine power MOSFETs, and two power diodes. Note that the power diodes can also be replaced with power MOSFETs operating in synchronous rectification mode. This topology is uniquely designed to provide a common ground for dc source and ac output.

A. Switching States

The equivalent circuit of each switching state is shown in Fig. 4 and summarized in Table I. The proposed CGT-9L-BI is capable of generating nine symmetrical voltage levels. While generating ac voltage, the boost inductor can be simultaneously charged by the dc source to boost the voltages across capacitors C_1, C_2 and C_3. The voltages of all the capacitors are naturally balanced.

B. Multicarrier Pulse-Width Modulation (PWM)

Multicarrier PWM as shown in Fig. 5 is developed to control the proposed CGT-9L-BI. By charging the boost inductor L with a constant duty-cycle D, the voltage of capacitors $C_1 - C_3$ can be boosted to

$$V_{C_1} = V_{C_2} = V_{C_3} = \frac{1}{1-D} V_{dc} . \tag{1}$$

Compared to these three capacitors, the voltage of C_4 is halved. Referring to Fig. 4, the maximum voltage level $V_{\max}$ is

$$V_{\max} = \frac{2}{1-D} V_{dc} . \tag{2}$$

The peak of fundamental ac voltage $\hat{V}_{o,1}$ can be controlled by the modulation index M,

$$\hat{V}_{o,1} = MV_{\max} = \frac{2M}{1-D} V_{dc} . \tag{3}$$

Therefore, the voltage gain of the proposed topology can be written as

$$G = \frac{\hat{V}_{o,1}}{V_{dc}} = \frac{2M}{1-D} . \tag{4}$$

C. Design of Passive Components

Passive components can be calculated based on their ripple magnitude. Four capacitors with the same capacitance C are considered. Considering the maximum discharging duration of C_3 depicted in Fig. 5, the capacitor voltage ripple can be derived by solving

$$\left| \int_{t_1}^{t_2} \hat{I}_{o,1} \sin(\omega t)\, dt \right| = C\Delta V_C \tag{5}$$

that gives

$$\Delta V_C = \left| \frac{2\hat{I}_{o,1}}{\omega C} \cos(\omega t_1) \right| \tag{6}$$

where ΔV_C is capacitor voltage ripple and $\hat{I}_{o,1}$ is the peak of load current at unity power factor.

The current ripple of boost inductor consists of low-frequency and high-frequency components due to the single-phase load and PWM, respectively. Assuming that the capacitor voltage ripple is sinusoidal and the dc source is ideal without low-frequency ripple, the low-frequency voltage across the inductor can be obtained for calculating its current ripple:

$$\Delta I_{L,LF} = \frac{(1-D)\Delta V_C}{\omega L} \tag{7}$$

where $\Delta I_{L,LF}$ is the low-frequency current ripple of boost inductor. Considering volt-second balance of the inductor for each triangular carrier period, the high-frequency current ripple is

$$\Delta I_{L,HF} = \frac{DV_{dc}}{f_s L} \tag{8}$$

where f_s denotes the frequency of triangular carrier.

III. Comparison with Existing Common-Ground-Type Multilevel Inverters

Table II summarizes the comparison of the proposed topology with the state-of-the-art common-ground-type inverters. Observations shows that the proposed CGT-9L-BI outperforms others such that it demonstrates the greatest number of voltage level generation (9 levels) and highest voltage boosting gain. Moreover, it exhibits the highest utilization ratio of power semiconductor devices, as can be seen from its lowest $(N_{S+D})/N_L$ ratio of only 1.2. This indicates that the proposed topology requires the least number of power semiconductor devices to generate each level. The most noteworthy advantage of the proposed topology is that it has overcome the problem associated with discontinuous input current in the existing common-ground-type inverters. Continuous dc source current is guaranteed in the proposed topology, this implies that it is the best common-ground-type inverter for PV application.

TABLE II
COMPARISON BETWEEN THE PROPOSED CGT-9L-BI AND THE EXISTING COMMON-GROUND-TYPE INVERTERS

Topology	N_L	N_S	N_D	N_C	$(N_{S+D})/N_L$	G	CIC
Fig. 1(a)	3	5	–	1	1.7	M	No
Fig. 1(b)	3	4	2	2	2.0	M	No
Fig. 1(c)	3	4	1	1	1.7	M	No
Fig. 1(d)	5	6	1	2	1.4	M	No
Fig. 1(e)	3	8	1	2	3.0	$2M$	No
Fig. 1(f)	5	6	2	2	1.6	$2M$	No
Fig. 1(g)	5	7	2	2	1.8	$2M$	No
Fig. 1(h)	5	6	2	2	1.6	$2M$	No
Fig. 1(i)	7	6	4	4	1.4	$3M$	No
Fig. 1(j)	9	9	4	4	1.4	$4M$	No
CGT-9L-BI	**9**	**9**	**2**	**4**	**1.2**	$\mathbf{2M/(1-D)}$	**Yes**

N_L = number of levels, N_S = number of switches, N_D = number of diodes, N_C = number of capacitors, $N_{S+D} = N_s + N_D$ (total number of switches and diodes), G = voltage gain, M = modulation index, D = duty-cycle, CIC = continuous input current.

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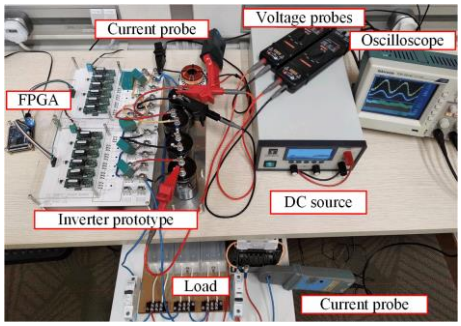

Fig. 6. Experimental setup.

TABLE III.
PARAMETERS OF THE EXPERIMENTAL SETUP

Component	Value
DC source V_{dc}	18 V
Boost inductor L	2 mH
Capacitor C	1000 μF
Carrier frequency f_s	5 kHz
Output frequency f_o	50 Hz
Load resistor	100 Ω
Load inductor	100 mH

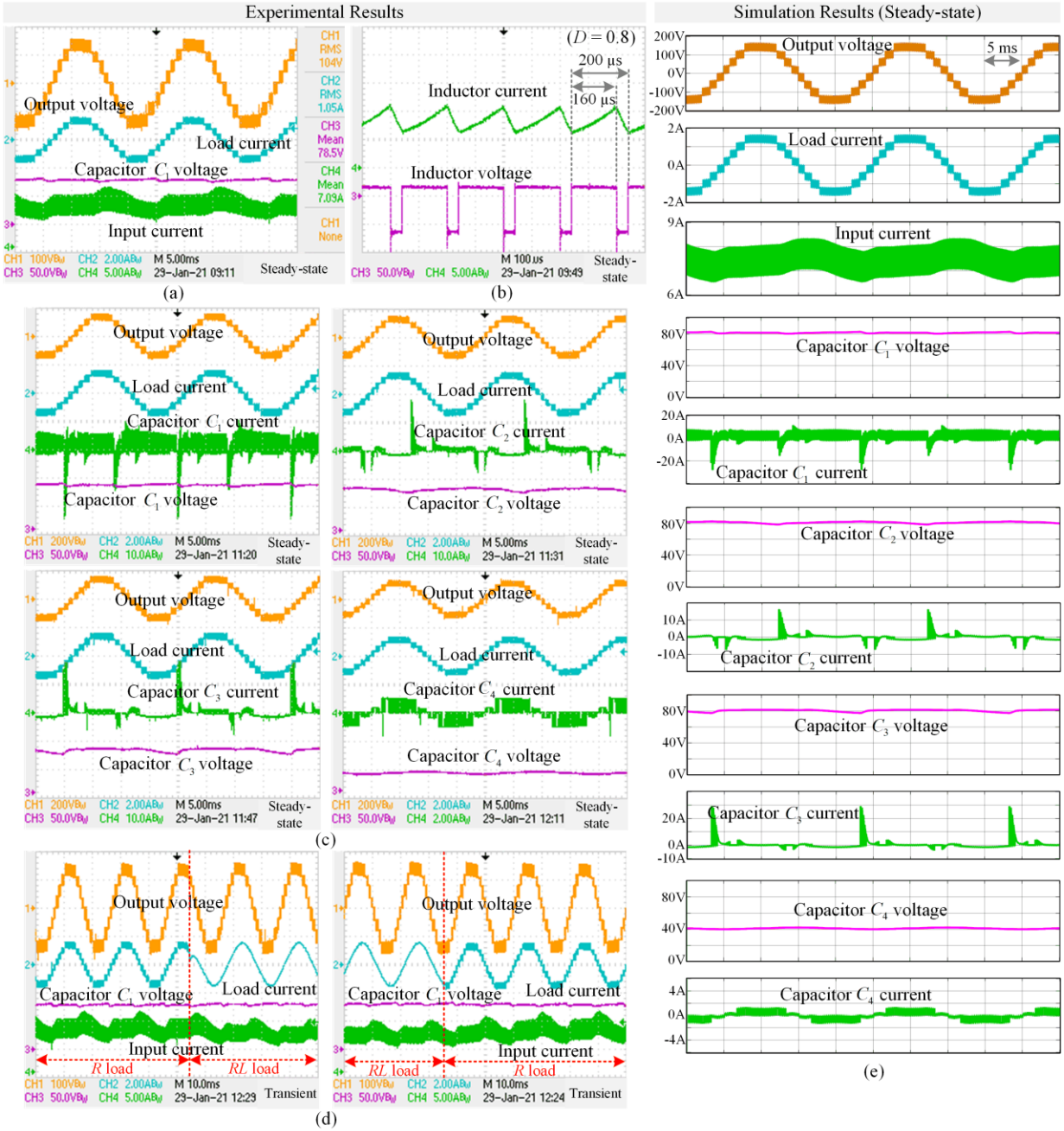

Fig. 7. Simulation and experimental results at M = 0.95: (a) output voltage, load current, capacitor C_1 voltage and input current, (b) inductor voltage and current, (c) voltage and current of each capacitor, (d) output voltage, load current, capacitor C_1 voltage and input current during transient response, and (e) simulation results for comparison with the experimental results.

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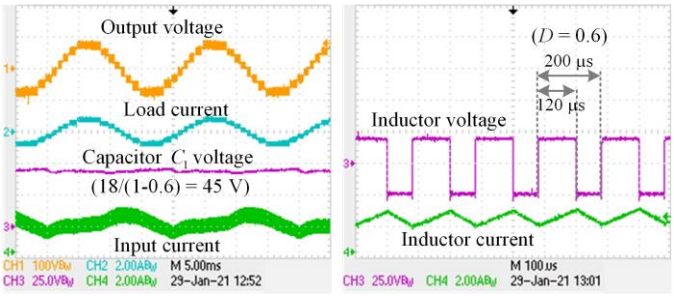
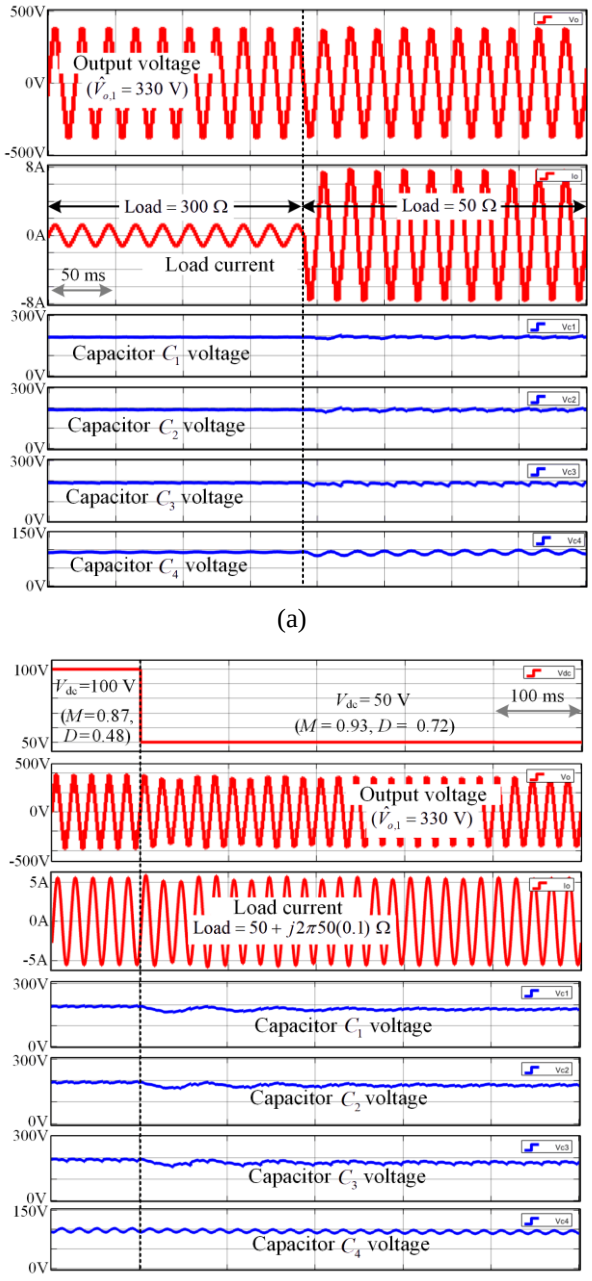


Fig. 8. Experimental results at M = 0.9.



(a)

(b)

Fig. 9. Dynamic response of the proposed CGT-9L-BI illustrating the self voltage balancing ability of the capacitors: (a) step change in load current, and (b) step change in dc source voltage and modulation index.

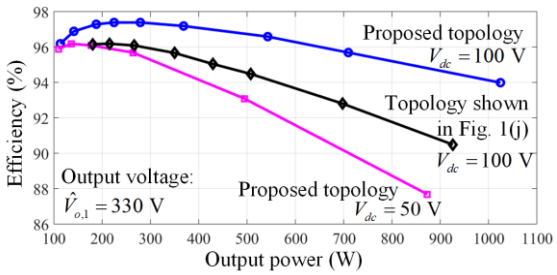


Fig. 10. Simulated efficiency of the proposed topology and comparison with the latest counterpart shown in Fig. 1(j) [21].

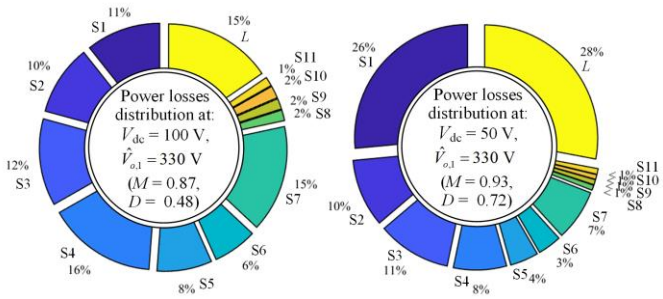


Fig. 11. Power losses distribution of the proposed topology at different input voltage.

IV. Simulation and Experimental Results

To validate the operation of the proposed CGT-9L-BI, an experimental prototype as depicted in Fig. 6 was tested. The parameters are summarized in Table III. Practical results measured from experimental tests are compared with simulation results in Fig. 7.

It can be seen that the boost inductor is charged with D = 0.8 and the voltages across capacitors C_1, C_2 and C_3 are boosted to approximately 80 V from the 18-V dc source. Nine symmetrical levels are clearly observed between 160 V to –160 V. Measurement shows that the RMS value of ac voltage is 104 V, which implies that the peak of ac voltage is 147 V. A voltage gain that exceeds 8 confirms the high voltage-boosting capability of the proposed CGT-9L-BI that enables its single-stage dc-ac inversion. All the measured waveforms are in good agreement with the simulated waveforms, thus validating the operation of the proposed topology.

Transient response of the experimental prototype was also tested. As illustrated in Fig. 7(d), the load current changes instantly when the load is switched from purely resistive R to series resistive-inductive RL load and vice-versa. The 9-level waveform of the ac output voltage is maintained without any deterioration during the load transient. Fig. 8 shows the measured waveforms at different modulation index, i.e. M = 0.9. It is worth emphasized that continuous dc source current is assured in all modulation indexes because the boost inductor is charged by the dc source with constant duty-cycle. Due to single-phase load, low-frequency current ripple can be observed at the dc source side. Power decoupling control schemes for mitigating this low-frequency ripple can be referred to comprehensive studies presented in [22]–[24].

Although the experimental prototype is tested at low power, the dc source current has reached to the 10 A limit of the dc power supply, as shown in Fig. 7. Therefore, results for higher power level are obtained by simulations. Fig. 9(a) shows the transient response of the proposed topology during step load changes from 300 **Ω** to 50 **Ω**. At output voltage of approximately 230 V (RMS), the amplitude of load current increases 6 times from 1.28 A to 7.7 A without deteriorating the waveform of ac voltage. When load current is increased, higher voltage ripple is observed in all capacitors. However, their average voltage is naturally balanced. By charging the boost inductor L at a constant duty-cycle of 0.48, the average voltage of each C_1, C_2 and C_3 is boosted to approximately 192 V (100/(1-0.48)). The capacitor C_4 is a flying capacitor that achieves naturally balancing for its voltage via load current. Step change in dc source voltage from 100 V to 50 V is also simulated, as shown in Fig. 9(b). To maintain the output voltage at rated value, twofold voltage gain can be achieved by increasing M to 0.93. Therefore, D is increased to 0.72 that generates 179 V across C_1, C_2 and C_3.

Fig. 10 continues to investigate the efficiency of the proposed topology by modeling the experimental prototype in simulation. Considering a peak ac output voltage of 330 V and dc source voltages of 100 V and 50 V, peak efficiency exceeding 96% can be achieved from the proposed topology. To compare the efficiency of the proposed CGT-9L-BI with the latest counterpart, the 9-level topology in the same family of common-ground-type inverters depicted in Fig. 1(j) [21] is also simulated. For fair comparison, power devices with the same characteristic as that used in the proposed topology are considered. As the voltage gain of Fig. 1(j) [21] is limited to 4, it cannot generate 330 V (peak) from a 50-V dc source. Therefore, only 100-V dc source is simulated with M = 0.825 (peak ac voltage of Fig. 1(j) = $4MV_{dc}$ = 330 V). The efficiency comparison at V_{dc} = 100 V in Fig. 10 clearly shows the advantage of the proposed CGT-9L-BI. In addition, the proposed topology also achieves higher voltage gain and continuous dc source current that is more attractive for PV application.

The power losses distribution of the proposed topology is also analyzed, as shown in Fig. 11. At lower dc source voltage, higher voltage gain is achieved by increasing the constant duty-cycle D that charges the boost inductor L. Due to higher dc source current, the power losses of inductor and S1 are more significant at lower dc source voltage.

V. Conclusion

A novel common-ground-type nine-level boost inverter has been proposed in this paper. As compared to other existing common-ground-type inverters, the proposed topology demonstrates significant improvement from three aspects, i.e. greater voltage level generation (9-level) with minimal power switch count, higher voltage-boosting gain, and continuous input current to cater for PV application. The drawback of discontinuous dc source current in the existing topologies has been resolved. The operation of the proposed topology has been analyzed and validated through simulations and experimental tests. Good agreement can be found among the theoretical analysis, simulations, and experimental results.

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