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New Switching Patterns Based on Current Space-Vector Diagram Viewpoint to Reduce Input Current Ripple for Three-Level Inverters

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***Abstract*—From the current space-vector diagram viewpoint, this paper proposes new switching patterns which reduce the input current ripple in DC link capacitors by considering the three-level inverter as a special case of a matrix converter. Several modulation concepts of the matrix converter are applied to the three-level inverter. Comparison among several modulation methods reveals that the lowest input current ripple can be achieved by the proposed PWM method without loss of neutral-point voltage balancing and limitation on the modulation index.**

Keywords—three-level inverters, matrix converters, space-vector diagram, current ripple, carrier-based PWM

I. Introduction

PWM methods for a three-level inverter, which can be viewed as a special case of a matrix converter as shown in Fig. 1, have been extensively investigated [1]. There are numerous research works which develop some specific modulation methods to achieve the desired modulation characteristics for the three-level inverters [2]-[10]. These modulation methods may be classified as space-vector modulation (SVM) and carrier-based modulation (CBM). The space-vector PWM methods for three-level inverters are popular and widely used [2]-[5]. In [2], the nearest-three vectors (NVT) are used to generate the required output voltage. This modulation gives not only low output voltage ripple but also low switching losses. A symmetric SVM is also proposed in [4] to obtain some improvement in the behavior of the switching sequence along with the control of neutral-point voltage balancing. However, both the NTV and symmetric SVM cannot eliminate the neutral-point voltage fluctuation completely. The nearest-virtual-space-vector (NVT^2) [3] is thus proposed to assure the neutral-point voltage balancing with no limitation, but its switching losses are higher than the NVT method. On the other hand, the CBM [6]-[10] is also widely used for three-level inverters because it requires fewer computations. As shown in [8], most SVM methods can be realized by CBM if the corresponding zero voltages are known. The limitation on the neutral-point voltage balancing in [4] is eliminated in [9] and [10], and the number of branch switch overs (BSOs) in [10] is only 6.

In all of the aforementioned research, attention has been paid mainly to the output voltage generation along with the neutral-point voltage balancing, while the input current ripple in DC link capacitors is rarely considered and may be of a high level. The current ripple is a significant factor affecting the lifetime and reliability of capacitors [11], [12]. Research works in [13]-[16] have proposed methods to reduce the ripple of the input current. In [14], space-vectors are selected to give a low current ripple but the neutral-point voltage fluctuation still remains. Another SVM method in [15] is proposed by considering the combination of space vectors which gives the instantaneous input current closest to its average value. Though the current ripple in the high-frequency range is low and it is effective for a wide range of load power factor, the neutral-point voltage balancing is not achieved. In [16], the optimal three space-vectors are proposed to reduce the current ripple, but similar to [15], simultaneous switching occurs in any two phases which results in 6 BSOs, and the neutral-point voltage for high modulation index is still not balanced.

This paper presents new switching patterns with 6 BSOs to solve the high input current ripple and the neutral-point voltage balancing problems together for three-level inverters by considering the three-level inverter as a matrix converter and applying several concepts of the matrix converter [17], [18] to analyze the input current of the three-level inverter. Comparison of input current spectra among several PWM methods will be shown to verify the effectiveness of the proposed PWM.

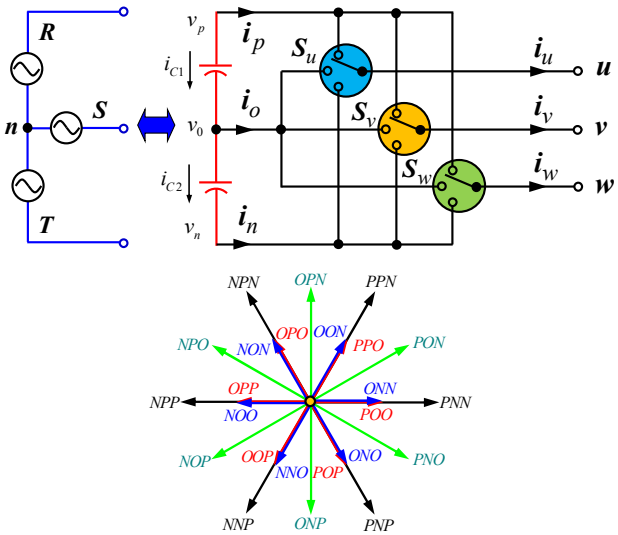

Fig. 1 Structure of a three-level inverter viewed as a matrix converter and its output voltage space vectors.

II. Structure and Basic Equations of Three-Level Inverters

By considering the three-level inverter shown in Fig. 1 as a special case of a matrix converter, the equations of the

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output voltages u,v,w and the input currents i_p,i_o,i_n can be described by (1)-(3).

$$\begin{bmatrix} u \\ v \\ w \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \begin{bmatrix} v_p \\ v_o \\ v_n \end{bmatrix} = \begin{bmatrix} u^*+v_Z \\ v^*+v_Z \\ w^*+v_Z \end{bmatrix} \Leftrightarrow \boldsymbol{v}_o = \mathbf{M}\boldsymbol{v}_i \quad (1)$$

$$\begin{bmatrix} i_p \\ i_0 \\ i_n \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix}^T \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} \Leftrightarrow \boldsymbol{i}_i = \mathbf{M}^{\mathrm{T}}\boldsymbol{i}_o \quad (2)$$

$$0 \le m_{ij} \le 1, \quad \sum_{j=1}^{3} m_{ij} = 1, \quad i = \{1,2,3\}, j = \{1,2,3\} \quad (3)$$

where v_p, v_o, v_n are the instantaneous input voltages. u^*,v^*,w^* and i_u, i_v, i_w are commanded output voltages and output currents, respectively. v_z is the zero voltage and $\mathbf{M}$ is the modulation matrix.

III. Analysis of Neutral Point Voltage Balancing and The Input Current Ripple by Using Current Space-Vector Diagram

In general, analysis of the neutral-point voltage balancing from the viewpoint of output-voltage space-vector utilization is not easy. However, when the three-level inverter is considered as a matrix converter, the dc-bus current at the input side is related to the output current by (2). Therefore, a better approach to investigate the neutral-point current is by using the input current space-vector diagram as shown in Fig. 2, where the current space vector is defined by (4).

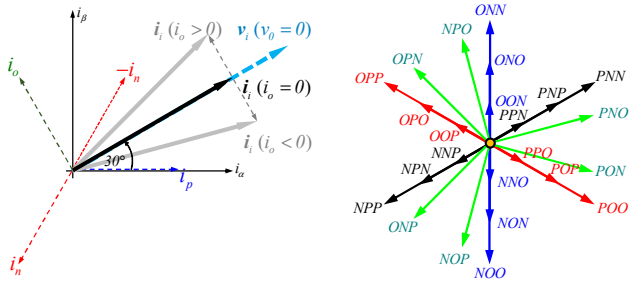
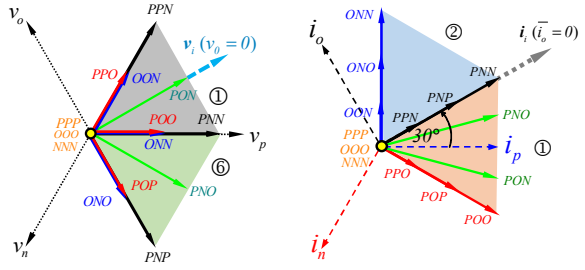


Fig. 2 The input current space-vector diagram based on a matrix converter.

$$\boldsymbol{i}_i = \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_p \\ i_o \\ i_n \end{bmatrix} \quad (4)$$



(a) Output voltage vector (b) Input current vector

Fig. 3 Space-vector diagram and the corresponding switching state.

As shown in Fig. 2, the input current vector as calculated by (4) points at 30° direction when the neutral-point current is zero $(i_o = 0)$, and in this case, the dc-bus voltages are balanced. If the phase of the input current vector is more or less than 30°, the neutral-point current i_o will not be zero (positive or negative) and causes the unbalanced dc-bus voltages. Moreover, the RMS value of the input current will also be increased.

Figure 3 shows the space-vector diagram of the output voltage and input current together. The input current vector of Fig. 2 and the current space-vector diagram in Fig. 3(b) can be used to evaluate the neutral-point current by considering the space-vectors selected by each PWM method. The 30° line is used as a reference for the condition of zero average neutral-point current. Considering the switching states of the voltage space vectors in Fig. 1, it is found that the input current space vectors in Fig. 3(b) can be classified into 4 groups: 1) the blue line corresponding to the small space-vectors which give a phase angle of the input current larger than 30°, 2) the red and green lines corresponding to the small (red) and medium (green) space-vectors whose phase angle is less than 30°, 3) the black line corresponding to the large space-vectors which lies exactly on the 30° line, and 4) the yellow points at the origin corresponding to the zero space-vectors which do not generate an input current. Consequently, for the average neutral-point current to be zero to maintain the neutral-point voltage balancing, the space-vectors in each group must be chosen properly. The black line in Fig. 3 related to the large space-vectors, gives zero neutral-point current because for these switching stages the three-level inverter behaves like a two-level one with the neutral point disconnected. Also from Fig. 3(b), when the small space-vectors in the first group are not used in the PWM pattern, e.g. [PNP]-[PNO]-[PON] or [OOO]-[POO]-[PON]-[PNN], the dc-bus voltages cannot be balanced. This is because the corresponding space-vectors lie on the right-hand side of the 30° line and thus cannot create the average input current vector to be on the 30° line. To achieve a zero neutral-point current, the current space vectors on the blue line are necessary in the PWM pattern, e.g. [ONO]-[PNN]-[PON] or [OOO]-[OON]-[PON]-[PNN]. In this case, for the neutral-point voltage to be balanced, the average neutral-point current must satisfy the condition (5). In general, the neutral-point voltage balancing may be unattainable under, e.g., a high modulation index or a low load power factor, and also with the PWM which uses only three space-vectors.

$$\left.\begin{aligned} i_o = {} & \left(m_{ONN}i_u + m_{ONO}(-i_v) + m_{OON}(-i_w)\right) + \left(m_{PON}i_v + m_{PNO}i_w\right) \\ & + \left(m_{POO}(-i_u) + m_{POP}i_v + m_{PPO}i_w\right) = 0 \end{aligned}\right\} \quad (5)$$

The distances from the utilized space-vectors to the 30° line can be considered to represent the ripple in the input current. For example, the distance to the 30° line for the space-vectors [OON] and [PPO] is small, so the corresponding neutral-point current ripple is low too. On the contrary, the neutral-point current ripple is high for the space vectors [ONN], and [POO] because their distances to the 30° line are large. Also, since the neutral-point current and the capacitor currents are related by (6), the smaller the ripple in the neutral-point current, the less the dc-capacitor current ripple.

$$i_{C1} = -i_{C2} = i_o / 2 . \quad (6)$$

Therefore, to achieve a small current ripple in the capacitors, the space-vectors close to the 30° line should be utilized as much as possible. In addition, the current ripple also depends on the dwell time of each space-vector that is generally determined by the commanded output voltages.

IV. New Switching Patterns for Simultaneous Control of Neutral-Point Voltage and Input Current

A. <2u1b> PWM for Three-Level Inverters

From the result in [17], the general modulation matrix **M** to the three-level inverter can be described as

$$\mathbf{M}=\left[m'_{ij}\right]+\mathbf{M}_0=\mathbf{M}_U+\mathbf{M}_I+\mathbf{M}_N+\mathbf{M}_0 \tag{7}$$

where

$$\mathbf{M}_U=\frac{1}{\left(v_p^2+v_0^2+v_n^2\right)}\begin{bmatrix}u^*\\ v^*\\ w^*\end{bmatrix}\begin{bmatrix}v_p\\ v_0\\ v_n\end{bmatrix}^T,\ \mathbf{M}_I=\frac{k_1}{\sqrt{3}\left(v_p^2+v_0^2+v_n^2\right)}\begin{bmatrix}i_u\\ i_v\\ i_w\end{bmatrix}\begin{bmatrix}v_n-v_0\\ v_p-v_n\\ v_0-v_p\end{bmatrix}^T$$

$$\mathbf{M}_N=\frac{k_2}{3\left(v_p^2+v_0^2+v_n^2\right)}\begin{bmatrix}i_w-i_v\\ i_u-i_w\\ i_v-i_u\end{bmatrix}\begin{bmatrix}v_n-v_0\\ v_p-v_n\\ v_0-v_p\end{bmatrix}^T,\ \mathbf{M}_0=\begin{bmatrix}1\\ 1\\ 1\end{bmatrix}\begin{bmatrix}X & Y & Z\end{bmatrix}.$$

The PWM switching pattern for each output phase can be either non-switching, unipolar, dipolar, or bipolar. Here, an integer and a letter "n" "u" "d" or "b" are used to represent a three-phase PWM mode. For example, <1n2d> PWM means that one phase is clamped (not switched), and the other two phases are in dipolar mode.

In order to achieve a minimum switching loss, only the PWM methods with 6 BSOs will be considered in the following. For the three-level inverter, the possible PWM modes with 6 BSOs are <3u>, <1n1u1d>, and <2u1b> only. Detail explanation of the <3u> and <1n1u1d> PWM can be found in [10]. So, only the <2u1b> PWM under which two phases are in unipolar mode, and one phase is in bipolar mode, will be discussed using Fig. 4.

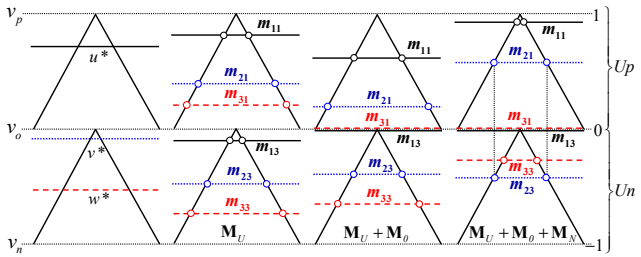


Fig. 4 Steps of CB dipolar modulation for generating <2u1b> PWM mode.

The simple steps of <2u1b> PWM begin with <3d> mode as shown in Fig 4(b), which results from using the modulation matrix $\mathbf{M}_U$ and arbitrary zero-voltage matrix $\mathbf{M}_0$. However, for a particular zero-voltage matrix $\mathbf{M}_0$ according to (8), the <3d> PWM mode changes to <2u1d> mode as shown in Fig. 4(c). In this case, dipolar modes in the maximum and minimum phases are changed to unipolar modes. Finally, the matrix $\mathbf{M}_N$ is added to get the <2u1b> PWM with 6 BSOs as shown in Fig 4(d).

$$[X,Y,Z]=\left[-\min(m'_{11},m'_{21},m'_{31}),1-X-Z,-\min(m'_{13},m'_{23},m'_{33})\right] \tag{8}$$

$$\left.\begin{aligned} m_{11}&=\frac{(u-w)v_p+k_2i_v(v_o-v_n)}{v_p^2+v_o^2+v_n^2},\ m_{13}=0\\ m_{21}&=\frac{(v-w)v_p-k_2i_u(v_o-v_n)}{v_p^2+v_o^2+v_n^2},\ m_{23}=\frac{(v-u)v_n+k_2i_w(v_p-v_o)}{v_p^2+v_o^2+v_n^2}\\ m_{31}&=0,\qquad\qquad m_{33}=\frac{(w-u)v_n-k_2i_v(v_p-v_o)}{v_p^2+v_o^2+v_n^2}\end{aligned}\right\}. \tag{9}$$

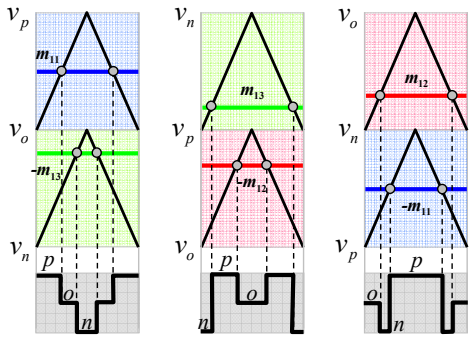
From the steps in Fig. 4, the algorithm to determine <2u1b> PWM with neutral-point voltage balancing is as follows:

1. Calculate modulation matrix $\mathbf{M}_U$ in (6) and add the zero voltage matrix $[X,Y,Z]$ by (8) to get the output "u" and "w" phases in the unipolar mode and the "v" phase in the dipolar mode <2u1d>PWM.
2. Calculate k_2, which satisfies $m_{21}+m_{23}=1$ to change "v" phase from dipolar to bipolar mode, and then calculate modulation functions m_{ij} with (9).
3. Check whether (10) is satisfied. If it is not true, the neutral-point voltage balancing cannot be achieved, and the <1n1u1d> PWM shall be used instead,

$$i_o^*=m_{12}i_u+m_{32}i_w=0. \tag{10}$$

B. Switching Sequence for <2u1b> PWM

The values inside the modulation matrix $\mathbf{M}=\left[m_{ij}\right]$ have already been determined from the previous calculation in Part A. The final step is to generate the PWM signals from the modulation matrix. Similar to the switching sequence arrangement of a matrix converter studied in [18], there are three choices, depending on which of the input phase is chosen as a reference. When the mid-point bus voltage v_o is selected as the reference, the reference signals U_p and U_n for the double-carrier modulation are given by (11) as shown in Fig. 5(a). On the other hand, if the positive-bus voltage v_p is chosen as the reference, U_p and U_n in (12) must be used. And finally, if the negative-bus voltage v_n is selected as the reference, U_p and U_n in (13) will be used.



(a) v_o-bus reference (b) v_p-bus reference (c) v_n-bus reference

Fig. 5 Switching sequence when choosing different dc-bus voltage as a reference

$$[U_p]=\begin{bmatrix}m_{11} & m_{21} & m_{31}\end{bmatrix}^T\geq 0,\quad [U_n]=-\begin{bmatrix}m_{13} & m_{23} & m_{33}\end{bmatrix}^T\leq 0 \tag{11}$$

$$[U_p]=\begin{bmatrix}m_{13} & m_{23} & m_{33}\end{bmatrix}^T\geq 0,\quad [U_n]=-\begin{bmatrix}m_{12} & m_{22} & m_{32}\end{bmatrix}^T\leq 0 \tag{12}$$

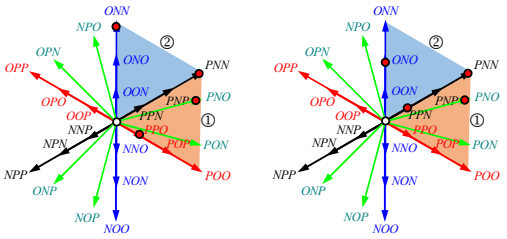
$$[U_p]=\begin{bmatrix}m_{12} & m_{22} & m_{32}\end{bmatrix}^T\geq 0,\quad [U_n]=-\begin{bmatrix}m_{11} & m_{21} & m_{31}\end{bmatrix}^T\leq 0. \tag{13}$$

TABLE I. Switching Patterns of <2u1d>, <3u>, <1n1u1d>, <2u1b> PWM with different reference (Modulation Index M=0.8-1.0).

PWM modes												
<2u1d>			<3u>			<1n1u1d>			<2u1b>(new)			
Bus Ref.			Bus Ref.			Bus Ref.			Bus Ref.			
v_p	v_o[3]	v_n	v_p	v_o[4]	v_n[5]	v_p	v_o[10]	v_n	v_p	v_o	v_n
Modulation index m=0.8											
pnn	ppo	ooo	pnn	poo	ooo	nnn	pon	oon	pnn	ppo	ono
ppn	poo	pnn	pon	pon	oon	pnn	pnn	non	pno	pno	pno
ooo	pon	ppn	oon	pnn	pon	pon	onn	nnn	ppo	pnn	pnn
	pnn		ooo	onn	pnn	oon	nnn	pnn	opo	onn	ppn
	onn										
Modulation index m=0.9											
pnn	ppo	ooo	pnn	pon	oon	pnn	ppn	oon	pnn	ppo	ono
ppn	poo	pnn	pon	pnn	pon	ppn	pon	pon	ppn	ppn	pno
ooo	pon	ppn	oon	onn	pnn	pon	pnn	pnn	ppo	pnn	pnn
	pnn					oon	onn	ppn	opo	onn	ppn
	onn										
Modulation index m=1.0											
pnn	ppo	ooo	pnn	pon	oon	pnn	ppn	oon	pnn	ppo	ono
ppn	poo	pnn	pon	pnn	pon	ppn	pon	pon	ppn	ppn	pno
ooo	pon	ppn	oon	onn	pnn	pon	pnn	pnn	ppo	pnn	pnn
	pnn					oon	onn	ppn	opo	onn	ppn
	onn										

Switching patterns of the <2u1d> PWM [3], <3u> PWM [4], <1n1u1d> PWM [10], and <2u1b> PWM are given for comparison in Table I.

Comparison of the space-vector utilization between <2u1b> PWM with v_o-bus reference and v_n-bus reference is shown in Fig. 6, wherein the utilized vectors are marked by red dots. It is seen that the utilized space-vectors of <2u1b> PWM with v_n-bus reference are nearer the 30° line than those of the <2u1b> PWM with v_o-bus reference.



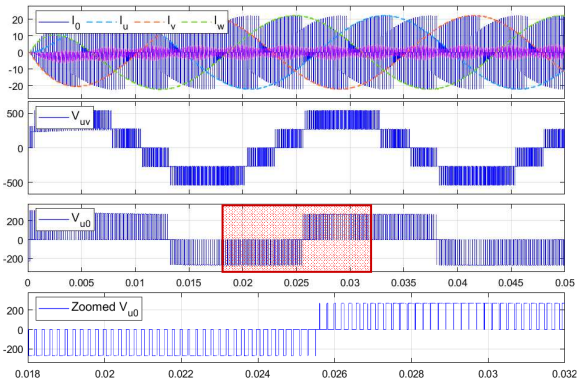
(a) v_o-bus reference (b) v_n-bus reference

Fig. 6 Space-vector utilization of <2u1b>PWM with m=0.8.

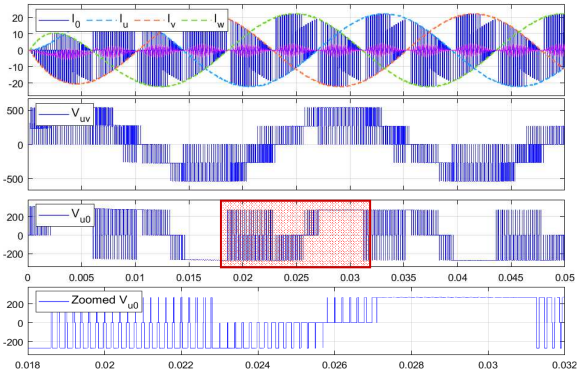
V. Simulation Results

Simulation is done to compare the input current ripple, the neutral-point voltage balancing, and the output PWM voltage of the proposed <2u1b> PWM with other PWMs. Simulation conditions are shown in Table II. Figs. 7 to 9 show the simulation results for various PWM methods.

As shown in Figs. 7(a)-(c), it is seen that three PWM methods with v_o-bus voltage reference have a high input current ripple because the maximum or minimum output current appears in the neutral-point current for a long duration. On the contrary, when using the v_n-bus reference, Figs. 7(d)-(f) reveal that the maximum or minimum output currents in the neutral-point current are reduced, and therefore, the ripple is reduced. Considering the zoomed voltage, the detailed pulse patterns of voltages are quite different for different PWM methods.



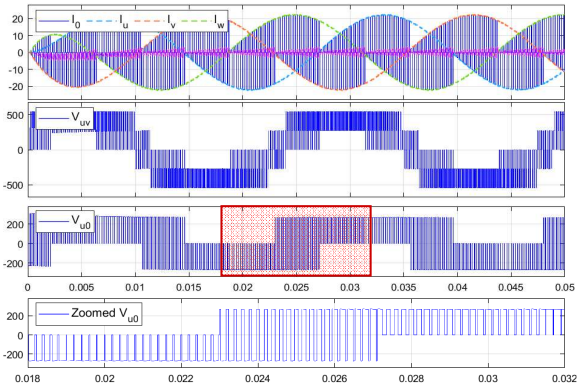
(a) <3u>PWM with v_o-bus reference (equivalent to SVM in [4])



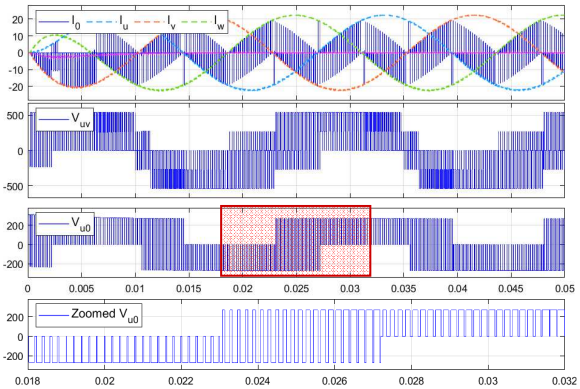
(b) <1n1u1d> PWM with v_o-bus reference (equivalent to CBM in [10])

TABLE II. Simulation Conditions

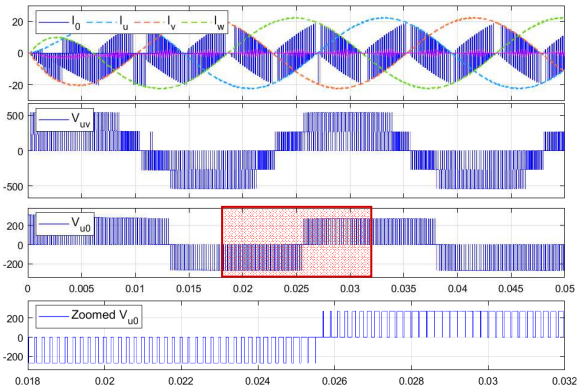
DC-bus capacitors: $C_1 = C_2 = 220\mu F$	Loads: $R_L = 10\Omega$, $L = 20mH$
Switching frequency: 5 kHz	Modulation index: m=0.8-1.0
DC-bus voltage: 540V, output voltage: m*380V, m*50Hz (V/f constant)	



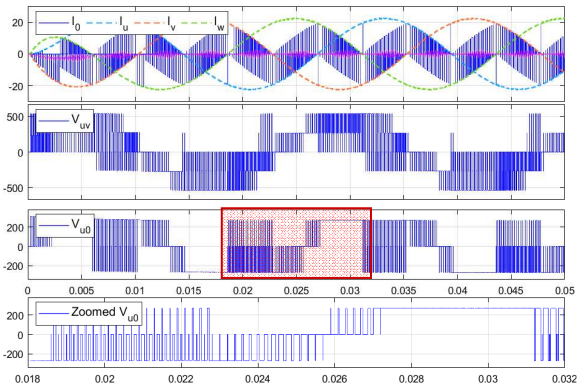
(c) <2u1b> PWM with v_o-bus reference (new)



(d) <2u1b> PWM with v_n-bus reference (new)



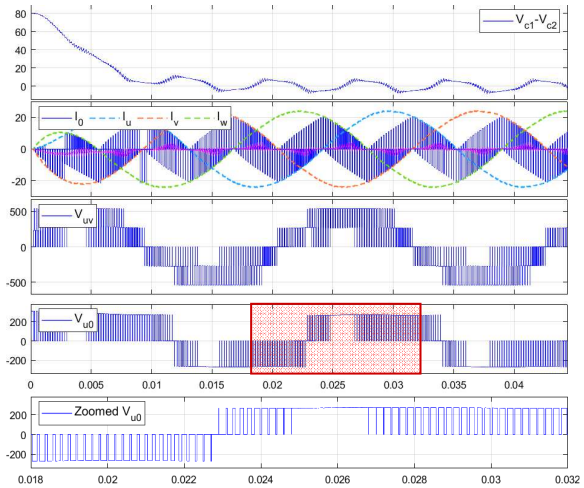
(e) <3u>PWM with v_n-bus reference (equivalent to SVM in [5])



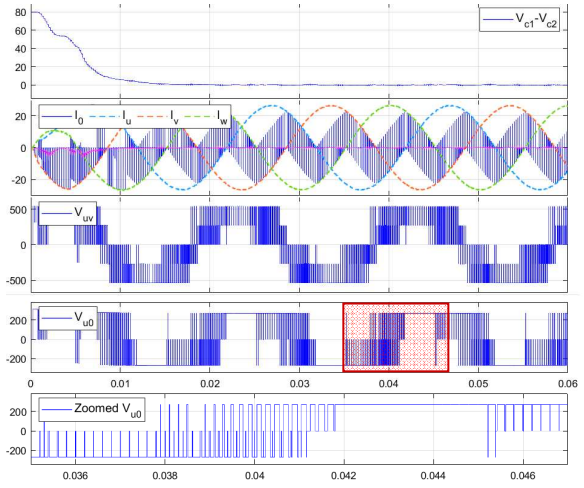
(f) <1n1u1d> PWM with v_p-bus reference (new)

Fig. 7. Voltage and current waveforms for various PWM methods at m=0.8

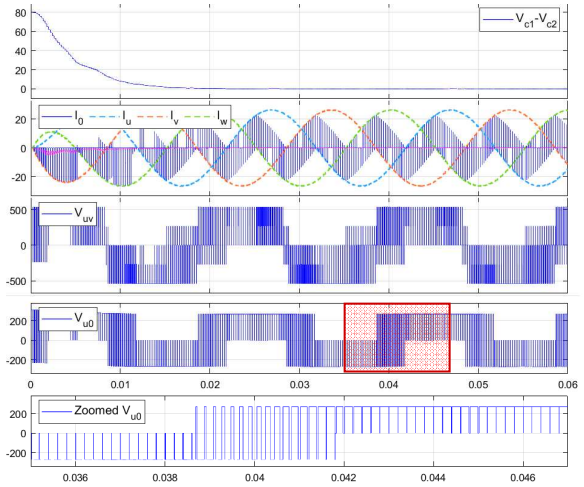
From Fig. 8(a), it is seen that overmodulation appears in the <3u>PWM with m=0.9, which makes the neutral-point voltage oscillation, so the RMS capacitor current may be increased especially by the low-frequency component. On the contrary, at m=1.0 the neutral-point voltage balancing can still be achieved by the <1n1u1d>, and <2u1b> PWM as shown in Figs. 8(b)-(c). Observing waveforms of <2u1d> PWM with v_n-bus voltage reference using three space-vectors [OOO], [PNN], and [PPN] as shown in Fig. 8(d), the average neutral-point current in the steady state is zero, and the neutral-point voltage is balanced as expected.



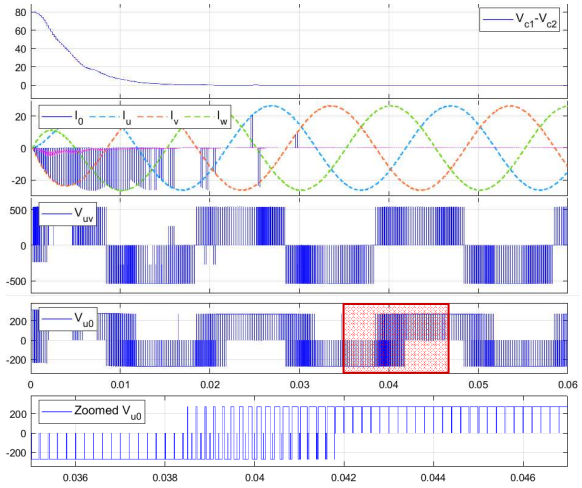
(a) <3u>PWM with v_n-bus reference and m=0.9



(b) <1n1u1d> PWM with v_n-bus reference and m=1.0



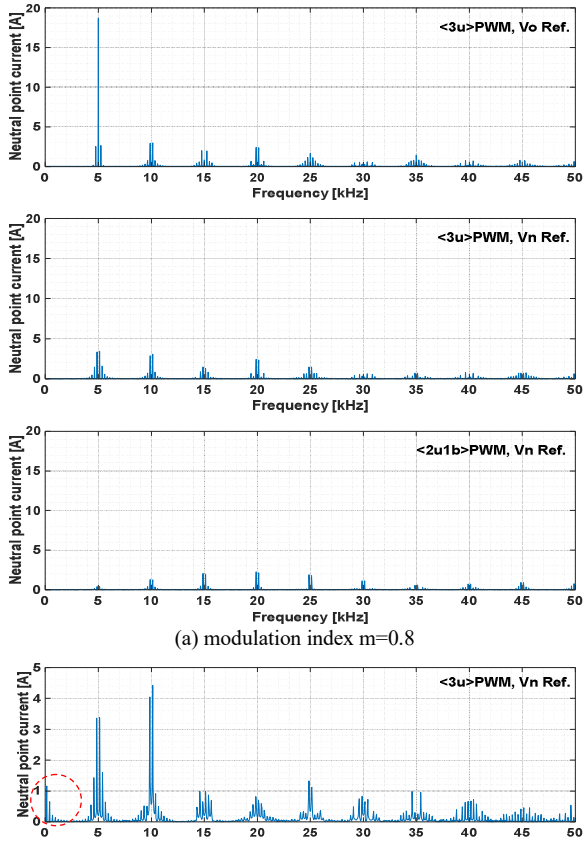
(c) <2u1b> PWM with v_n-bus reference and m=1.0



(d) <2u1d> PWM with v_n-bus reference and m=1.0

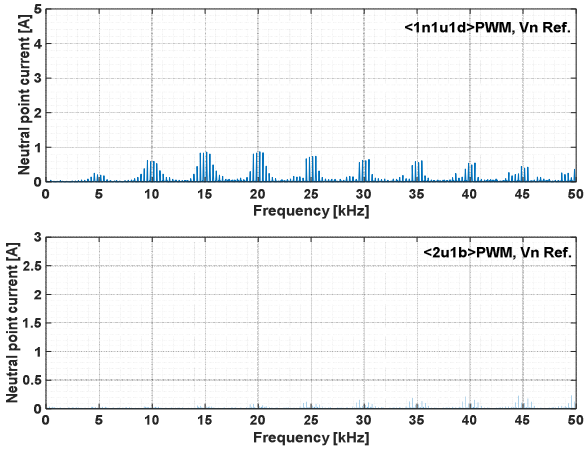
Fig. 8. Voltage and current waveforms for various PWM methods at high modulation index.

Figure 9 shows neutral-point current spectrum of some PWM methods compared with the proposed method. The conventional <3u> PWM (with v_0 as the reference) has a high current at the switching frequency of 5kHz, while <3u> PWM with v_n-bus voltage reference gives a lower current at 5kHz. When the modulation index increases from 0.8 to 0.9, the average neutral-point current with <3u> PWM becomes no more zero, so ripple currents in the low-frequency range appear as shown in Fig 9(b). As a consequence, the RMS value of the neutral-point current is increased. Fig. 9(c) shows that <1n1u1d> and <2u1b> PWM have no problems at a high modulation index. The characteristics of each PWM method can be summarized as shown in Table III.



(a) modulation index m=0.8

(b) modulation index m=0.9



(c) modulation index m=1.0

Fig. 9. Spectrum of the neutral-point current for various PWM methods at modulation index m=0.8-1.0.

TABLE III. SUMMARIZED CHARACTERISTICS OF EACH PWM METHOD

PWM Modes	Bus Ref.	Mod. Index	RMS value of input currents			i_u %THD	v_{uv} %THD
			I_o	I_p	I_n		
3u[4]	vo	0.8	14.84A	16.25A	16.24A	0.4	38.45
3u	vp	0.8	6.787A	16.24A	16.24A	0.89	59.37
3u[5]	vn	0.8	6.780A	16.24A	16.24A	0.90	59.33
1n1u1d[10]	vo	0.8	11.11A	16.26A	16.27A	0.99	53.09
1n1u1d	vp	0.8	7.210A	16.52A	16.21A	0.97	62.30
1n1u1d	vn	0.8	7.214A	16.21A	16.52A	0.91	62.69
2u1b	vo	0.8	10.78A	16.20A	16.20A	0.77	62.39
2u1b	vp	0.8	4.971A	16.25A	16.20A	1.25	83.66
2u1b	vn	0.8	4.960A	16.21A	16.25A	1.24	83.22
3u	vn	0.9	7.757A	17.93A	17.93A	1.28	48.15
1n1u1d	vp	0.9	6.738A	18.59A	18.51A	0.74	52.66
2u1b	vn	0.9	4.095A	18.51A	18.52A	1.0	67.95
1n1u1d	vp	1	4.081A	20.29A	20.10A	0.74	49.25
2u1b	vn	1	2.217A	20.64A	20.65A	0.8	53.54

Considering the RMS value of the neutral-point currents at the modulation index m=0.8 for each PWM method in Table III, it is clear that the <3u> PWM with v_o-bus voltage reference (which is equivalent to the conventional SVPWM) has a higher RMS value of the neutral-point current than those of the <1n1u1d> and <2u1b> PWM. However, when the v_p- or v_n-bus voltage is chosen as the reference, the RMS values for all PWM methods are reduced, and the RMS value of the <3u> PWM becomes less than those of the <1n1u1d> PWM. It should be noted that in all cases at the modulation index m=0.8, the neutral-point voltage balancing can be maintained. However, at m=0.9 the <3u> PWM cannot completely control the neutral-point voltage balancing. Hence, the current RMS value is higher than those of the <1n1u1d> PWM. And at m=1.0, it is confirmed that the <2u1b> PWM with v_n-bus reference gives the lowest RMS, and similar to the <1n1u1d> PWM it does not have a problem regulating the neutral-point voltage balancing. Although, the <2u1b> PWM gives the lowest input current ripple, the <3u> PWM gives the lowest THD of the output voltage.

VI. CONCLUSION

This paper proposed new switching patterns to reduce the input current ripple for three-level inverters, and thereby reduce power loss in the dc-link capacitors. Considering the three-level inverter as a matrix converter, the current space-vector diagram viewpoint and switching sequence arrangement of a matrix converter can be applied to the three-level inverter. It is proposed to use the viewpoint of the current space-vector diagram to analyze the neutral-point voltage balancing and the input current ripple. Furthermore, it is shown that different switching sequence can be generated in corresponding to the reference bus used. The research results reveal that the lowest input current ripple and the neutral-point voltage balancing can be achieved by the proposed switching patterns without any modulation index limitation and with only 6 BSOs.

REFERENCES

[1] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[2] L. Helle, S. Munk-Nielsen, and P. Enjeti, "Generalized Discontinuous DC-Link Balancing Modulation Strategy for Three-Level Inverters," in *Proc. of the Power Conversion Conference (PCC)*, 2002, pp. 359-366.

[3] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The Nearest Three Virtual Space Vector PWM-A Modulation for the Comprehensive Neutral-Point Balancing in the Three-Level NPC Inverter," *IEEE Power Electronics Letters*, vol. 2, no. 1, pp. 11-15, Mar. 2004.

[4] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Evaluation of the Low-Frequency Neutral-Point Voltage Oscillations in the Three-Level Inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1582-1588, Dec. 2005.

[5] X. Xing, X. Li, F.Gao, C.Qin, and C. Zhang, "Improved space vector modulation technique for neutral-point voltage oscillation and common-mode voltage reduction in three-level inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8697–8714, Sep. 2019.

[6] T. Bruckner and D. G. Holmes, "Optimal pulse-width modulation for three-level inverters," *IEEE Trans. Power Electron.*, vol. 20, pp. 82-89, Jan. 2005.

[7] J. Pou, J. Zaragoza, P. Rodriguez, S. Ceballos, V. M. Sala, R. P. Burgos, "Fast-Processing Modulation Strategy for the Neutral-Point-Clamped Converter With Total Elimination of Low-Frequency Voltage Oscillations in the Neutral Point," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2288-2294, Aug. 2007.

[8] S. Sangwongwanich and S. Paiboon, "Carrier-Based Realization of Arbitrary Space-Vector PWM Methods for Three-Level Inverters," *in Proc. of International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018, pp. 1642-1648.

[9] A. Saengseethong, S. Sangwongwanich, "A new modulation strategy for capacitor voltage balancing in three-level NPC inverters based on matrix converter theory," in *Proc. of International Power Electronics Conference (IPEC-Sapporo 2010 -ECCE Asia) 2010*, pp. 2358-2365.

[10] S. Sangwongwanich, "Double-carrier-based modulation theory of three-level inverters and a new discontinuous PWM for neutral-point voltage balancing," in *Proc. of IECON 2012*, pp. 4961- 4966.

[11] M. A. Vogelsberger, T. Wiesinger, and H. Ertl, "Life-cycle monitoring and voltage-managing unit for dc-link electrolytic capacitors in PWM converters," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 493–503, Feb. 2011.

[12] A. Sangwongwanich, M. Novak, S. Sangwongwanich and F. Blaabjerg, "Reliability of DC-link capacitors in three-level NPC inverters under different PWM methods," *in Proc. of Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1804-1811.

[13] L. Kai, L. Mengshu, L. Zhengfeng, D. Zhenghua, and T. Shaoju, "Analytical closed-form expressions of dc current ripple for three-level neutral point clamped inverters with space-vector pulse-width modulation," *IET Power Electron.*, vol. 9, no. 5, pp. 930–937, Apr. 2016.

[14] S.-M. Kim, J.I. Won, J. Kim, and K.-B. Lee, "DC-link ripple current reduction for three-level inverters with optimal switching pattern," *IEEE Trans. Ind. Electron.*, vol. 65, no. 12, pp. 9204-9214, Dec. 2018.

[15] K. Nishizawa, J. Itoh, A. Odaka, A. Toba, and H. Umida, "Input current harmonic reduction based on space vector PWM for three-level inverter operating over a wide range power factor," *IEEJ Journal IA. Japan*, vol. 9, pp. 208-218, Oct. 2019.

[16] S.-W. An, S.-M. Kim, and K.-B. Lee, "Optimized space-vector modulation to reduce neutral point current for extending capacitor lifetime in three-level inverters," *IEEE Access*, vol. 8, pp. 97689–97697, Jun. 2020.

[17] P. Kiatsookkanatorn and S. Sangwongwanich, "A unified PWM strategy to reduce minimum switching number for matrix converters," in *Proc. of International Power Electronics Conference (IPEC-Himeji 2022 -ECCE Asia)*, 2022, pp. 83-88.

[18] P. Kiatsookkanatorn and S. Sangwongwanich, "A unified PWM method for matrix converters and its carrier-based realization using dipolar modulation technique," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 80-92, Jan. 2012.