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Design of Common DC-Link Capacitor in Multiple-Drive System Based on Reduced DC-Link Current Harmonics Modulation

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***Abstract*—Many industrial applications are recently utilizing the advantages of common DC-bus-based multiple-drive (multidrive) system such as low installation cost, space savings as well as improved reliability, and flexibility. One of the main drawbacks of such systems is the requirement for a bulky DC-capacitor due to the presence of large DC-link current ripples from the harmonic interaction between these multidrive and pulse width modulation (PWM) switching. This problem not only increases the cost and volume of the DC-link capacitors, but also decreases its lifetime, which must be considered in the design from the industrial aspect. This article proposes a new DC-bus capacitor design method for a multidrive system, focused on the capacitor sizing, cost-reduction, and lifetime improvements. First, an analytical model to obtain the DC-link capacitor-current in a multidrive system is proposed, which would aid the designers to configure the DC-capacitor current in systems having numerous multiple drives. Next, using the developed analytical model, the DC-link current harmonics are reduced through optimal interleaving of the fundamental output currents in addition to the phase-shifting of the carrier waves of the parallel-connected inverters. Finally, new capacitor sizing/design is proposed considering the lifetime, power-loss, cost, and volume of the DC-link capacitor bank. The proposed approach reduced the volume and cost of DC-cap bank by 50%, and increased the lifetime by four years (∼35000 hours), considering the worst-case scenarios. Experimental and analytical results are given for validation of the proposed method. The results could serve as a guideline for designing the DC-link capacitor in multidrive applications in a low-cost manner.**

***Index Terms*—DC-bus connected multidrive, DC-link capacitor interleaving, industrial power systems, integrated motor drive, pulse width modulation inverters.**

I. Introduction

MULTIDRIVE system concept has become an attractive approach in various commercial, industrial, and residential applications to scale up the power generation capacity [1] or when several drives form part of a single process [2]. A few examples of their applications include textiles, paper, oil-pumping, pumps, dairy farm processes, and sugar productions, etc [1]–[5]. Recently, in various industrial application, distributed DC-link system is being advocated as a possibility for the future integrated motor drive systems [2], [5]–[7]. In such a system, as shown in Fig. 1(a), industrial drive modules that are connected to a common DC-bus bar or a centralized rectifier [8] which is used to supply the drive modules with DC-power, and each module then inverts the DC to AC and powers an individual motor [2]. A prototype of such an integrated motor drive (IMD) system is shown in Fig. 1(b). The first generation of the IMD encountered some difficulties, such as the electronics placed on the motor experiencing heating effects and vibrations [7]. However, the DC-grid connected multidrive system promises several user benefits. This kind of construction simplifies the total installation and maintenance costs and enables savings in cabling [4], [8]. It also reduces the component count, thus improving the space savings and increasing the reliability as now a centralized rectifier or common DC-bus is used instead of each inverter having its rectifier and [8]–[10]. The common supply of the multidrive enables each module to be controlled to operate at its optimized power rating, which can improve system performance [11]–[13]. Furthermore, the system can be more flexible and scalable as the system capacity can be increased by simply adding more inverter modules without removing existing inverters [2], [5], [14]. Additionally, the common DC-bus topology enhances the ability to meet the demands of mass production at a low cost [15], [16], and enables the integration of renewable energy sources [8], [9], [17].

Despite these benefits, one main limitation of the multidrive system is the presence of large DC-link current ripple

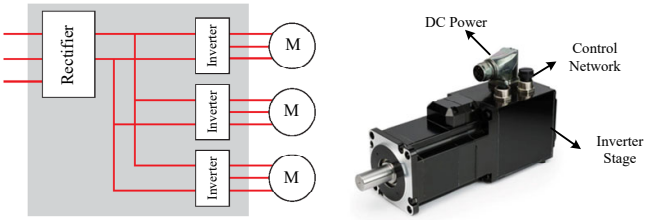

Fig. 1. (a) Schematic of the multidrive system [2] (b) A prototype of an integrated motor drive [6], [7].

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(harmonics) from the harmonic interaction between these parallel-connected inverters [1], [3], [14], and from pulse width modulation (PWM) switching. As a result, the DC-capacitance requirements in multidrive system is linear increasing with the number of drives connected with the DC-link by using the existing design method. A common practical solution in the market to suppress the DC-link harmonics is to use a large DC-link capacitor, but the total volume, weight, and cost of the overall system will significantly increase [9]. It is also a known fact that high capacitor ripple currents (i.e. root-mean-square (RMS) value of capacitor-current) increase the hot-spot temperature due to internal self-heating, and increase the capacitor equivalent series resistor (ESR) over time, thereby degrading the lifetime of DC-link capacitors. Furthermore, the DC-link capacitor is one of the highest failure rate components in power electronic systems and contributes to more than 30% of failures in certain applications [8], [18]. Hence, considered the weakest component and bottleneck of the power electronic systems. Concerning this, proper designing of the DC-link capacitor in a multiple-drive system, which is not discussed in the available literature, is an essential aspect that needs to be investigated. Because not designing the DC-link capacitor properly, could result in possible catastrophic failures of the multidrive system. In this paper, a new design approach for the DC-link capacitor in a multidrive system is discussed, which focuses on the capacitor size, cost reduction, and lifetime improvements by reducing the DC-capacitor-current harmonics.

The reliability design of DC-link capacitors has been discussed in [11], [18]–[20]. A comprehensive analysis of the lifetime estimation, and comparison between aluminum electrolytic capacitors (El-caps) and slim capacitor DC-link in grid-connected adjustable speed drives (ASDs), under grid voltage balanced, and unbalanced conditions are detailed in [11]. A review [18] of the state-of-the-art research in the area of reliability of capacitors for DC-link applications in power electronic converters, including the identification of the corresponding challenges, and future research directions is presented from the capacitor user's viewpoint. It also briefly discusses the failure modes, failure mechanisms, and reliability-oriented design approach of the three types of DC-link capacitors. However, the estimated results are for applications of DC-link capacitors in a single drive that cannot be extended to multidrive drives because the large amount of harmonic distortion (produced by nonlinearity drives) in the DC-link may change the stresses of the DC-link filters. A time-efficient equivalent model to obtain the electro-thermal stress of individual capacitors in the multidrive system along with an investigation on the impact of the number of drives under grid voltage unbalance on the capacitor lifetime is proposed by [19]. Reference [20] provides an analytical model to obtain the DC-link continuous current in a multidrive system consisting of El-caps as well as multidrive having slim capacitors. The aforementioned articles [11], [19], [20] have comprehensively analyzed DC-link capacitor reliability in multiple parallel-inverters from the view of harmonic distribution and electro-thermal stress. However, multiple standard drives systems used in these articles have their own individual rectifier, and the rectifiers are connected to a common AC source. The available literature has not so far addressed the design of the DC-link capacitors in a multidrive system connected to a common DC-source.

A few other researchers [21]–[24] have focused on DC-link capacitor size reduction by mitigation of harmonics in the grid-connected multiple-inverters-based system. References [21], [22] focus on the interleaving (i.e., phase-shifting) control scheme to reduce the RMS value of DC-current, and thereby, to reduce the size of DC-link capacitor size independent of the loading condition. Specifically, [22] mentions that for a multidrive system consisting of a few parallel-drive units, the resultant total-harmonic-distortion (THD) of the grid current will vary in a wide range (15% to 28%), and unequal loading will affect the harmonic cancellation performance at the DC-link, which should be addressed properly. The following paper thus focuses on a multidrive system with two parallel-drive units. A coordinated PCC voltage harmonics mitigation strategy is discussed in [23] for parallel-inverters by properly shaping inverter output impedance to minimize the DC-capacitor size. Similarly, in [24], a harmonic damping approach using a point of common coupling (PCC) voltage control for multi-parallel-inverters is discussed, which can effectively attenuate the harmonic level of PCC voltage caused by non-linear loads. The common point regarding the above-mentioned articles is that they focus on methods for attenuating harmonics and, thereby, reducing the DC-link capacitor size by using various control techniques. Even though these techniques seem as promising solutions in terms of effectiveness in harmonic mitigation, the total cost and complexity have become the main obstacle for these harmonic elimination approaches in multidrive systems.

The existing research regarding the DC-link capacitors in multidrive system either focuses on the reliability of DC-caps from harmonic distribution, and electro-thermal stress point of view or uses complex control techniques to reduce the RMS value of DC-link current. One of the most significant design criteria of industrial drives is to improve the lifetime of its wearing parts such as DC-capacitors in the demanding industrial market in a low-cost manner. To the best of the authors' knowledge, there is no prior literature available that discusses the design of DC-capacitor focussing on lifetime improvements while reducing the size and cost in a multidrive system connected to a common DC-source through centralized rectifier, which makes this worth studying. The contributions of this article are shown as follows:

1) First, an analytical model to obtain the DC-link capacitor-current in a multidrive is proposed, which would help the designers to reduce the simulation time for a system with large number of multiple drives.
2) Next, using the developed analytical model, the DC-link current harmonics are reduced through optimal interleaving of the fundamental output currents in addition to the phase-shifting of the carrier waves of the parallel-connected inverters. Using this analytical method helps to completely cancel out the double-fundamental frequency harmonics and switching frequency harmonics at the DC-link. This method of reducing the DC-link

harmonics is not discussed in any available literature and is more cost-efficient and convenient to use, due to no hardware change is needed.

3) Finally, new capacitor sizing/design is proposed considering the lifetime, power-loss, cost, and volume of the DC-capacitor based on the proposed reduced DC-capacitor current.

The proposed general design method could serve as a guideline for practically designing the DC-link capacitor in multidrive applications. The rest of this article is organized as follows. An overview of the multidrive systems is described in Section II. The proposed design method, to reduce the DC-capacitor current is explained in Section III, and considering the design of DC-capacitor with lifetime, cost, and volume constrains is explained in Section IV. The experimental results and discussions to verify the effectiveness of the proposed design solution are presented in Section V. Finally, Section VI concludes this article.

II. OVERVIEW OF THE MULTIDRIVE SYSTEM

The multidrive system proposed in this paper is shown in Fig. 2. It consists of two parallel-inverters connected to a common DC-bus, powered by a DC-grid. The parallel-inverters in the proposed system (specifications given in Table I) are assumed to be synchronized, and have the same phase, same output power ratings, and the same output waveforms, as it is considered being used for a single application process. For example, in applications such as the air conditioning and cooling systems in a dairy factory or for connecting parallel-operating motors (which usually have the same ratings such as same power, and same speed) used in rolling mills [9]. The common DC-link capacitor-bank $C_{DC-bank}$, consists of individual capacitors C_{dc}, which are connected in parallel to ensure the equal distribution of the total DC-link capacitor ripple current $I_{capbank}$. The ripple current flowing through a single capacitor is denoted by I_{cap}. In this study, El-caps are used as DC-link capacitors, due to their advantage of providing a high capacitance per unit volume at low costs compared to other types of capacitors [8]. The system can also be connected to an AC source using a centralized rectifier (sized according to the overall power rating and the total number of parallel-inverters), as shown in Fig. 1(a). The DC-source current is denoted by $I_{DC-source}$, and the I_{dc} represents the total DC-current drawn by the two parallel-inverters.

The proposed system uses the unipolar-sinusoidal PWM technique, explained in detail in [25] to control the four switches Q_{x1}, Q_{x2}, Q_{x3}, Q_{x4} (where x= U or L), of the voltage-source inverter units (VSIs). The output filter of each inverter is designed according to [26], and its specification is given in Table II. A Proportional-Resonant (PR) controller (designed according to [26], [27]) is used to maintain a rated output voltage of 230 V (RMS value) for each inverter unit. The control algorithm for the inverter is shown in Fig. 3. As both VSIs are synchronized, and have the same system ratings, the parameters for the controller of each inverter unit have the same value. The DC-capacitor is designed according to [28], [29] and the chosen capacitor's data [30] is shown in Table III and Table IV.

TABLE I
SPECIFICATIONS OF THE MULTIDRIVE SYSTEM SHOWN IN FIG. 2.

Parameter	Symbol	Value
Rated power (kW)	P_{o_1}, P_{o_2}	2.5
Load (Ω)	R_{o_1}, R_{o_2}	20
Rated RMS load voltage (V)	$V_{sine-ref}$	230
Load frequency (Hz)	f_o	50
Rated DC-link voltage (V)	V_{dc-ref}	400
Switching frequency (kHz)	f_{sw}	20
Modulation amplitude index	M_A	0.8

TABLE II
SPECIFICATIONS OF THE INVERTER OUTPUT FILTER SHOWN IN FIG. 2.

Parameter	Symbol	Value
Inductor-filter ripple current limit	I_{f_ripple}	20%
Inductor (mH)	L_{f_1}, L_{f_2}	2
Filter cutoff frequency (kHz)	f_{cutoff} (f_{cutoff}<f_{sw}/10)	2
Filter capacitor (μF)	C_{f_1}, C_{f_2}	6

TABLE III
DESIGN CRITERIA FOR DC-LINK CAPACITOR SHOWN IN FIG. 2.

Parameter	Symbol	Value
Ripple DC-link voltage (V) peak to peak (p−p) value (V)	V_{p-p}	20
Hold-up time (ms)	$t_{hold}(=1/f_o)$	20
Minimum required capacitor value (mF)	C_{min}	3.3

TABLE IV
DATASHEET [30] OF THE CHOSEN DC-CAPACITOR (KEMET−ALS8(1)(2)392NF500) IN FIG. 2.

Parameter	Symbol	Value
Single capacitance (μF)	C_{dc}	3900
Equivalent series resistance ($m\Omega$)	ESR	61 (at 100 Hz), and 46 (at 10 kHz)
Thermal resistance (°C/W)	R_{th}	3.8
Rated lifetime (hours)	L_o	9000 (at T_{rated} & I_{rated})
Rated upper category temperature (°C)	T_{rated}	105
Rated ripple current (A)	I_{rated}	12.2 (at 100 Hz), and 19.0 (10 kHz)
Rated voltage (V)	V_{rated}	500
Operating temperature (°C)	T_a	45

III. PROPOSED METHOD TO REDUCE THE DC-LINK CAPACITOR CURRENT IN A MULTIDRIVE SYSTEM

The design of DC-link capacitors in a multidrive system is restricted by its large size and cost, due to a large amount of DC-link harmonics present. To tackle this issue, one of the effective methods is to reduce the DC-link harmonics, which will reduce the RMS-capacitor-current, thereby reducing the size and cost of the DC-capacitor required. In this paper, a new cost-effective DC-link capacitor design procedure is explained for the multidrive system (depicted in Fig. 2), with unipolar

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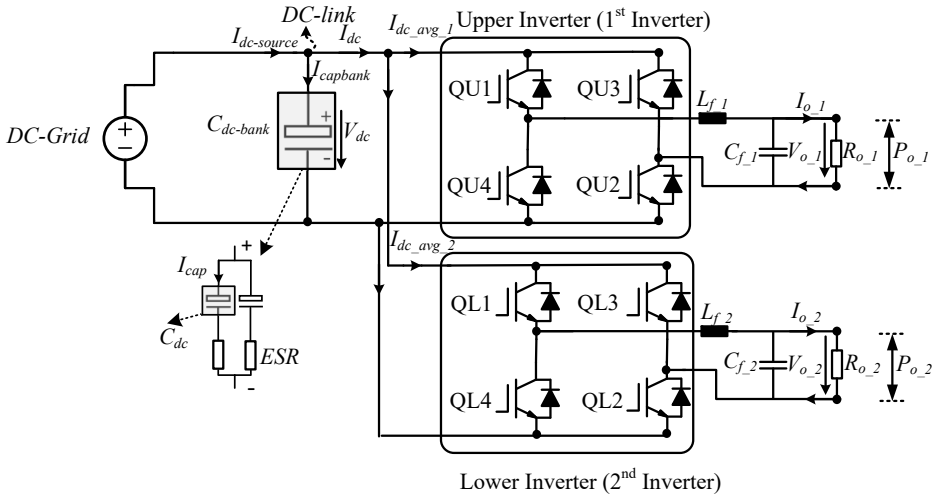

Fig. 2. Schematic of the proposed multidrive system.

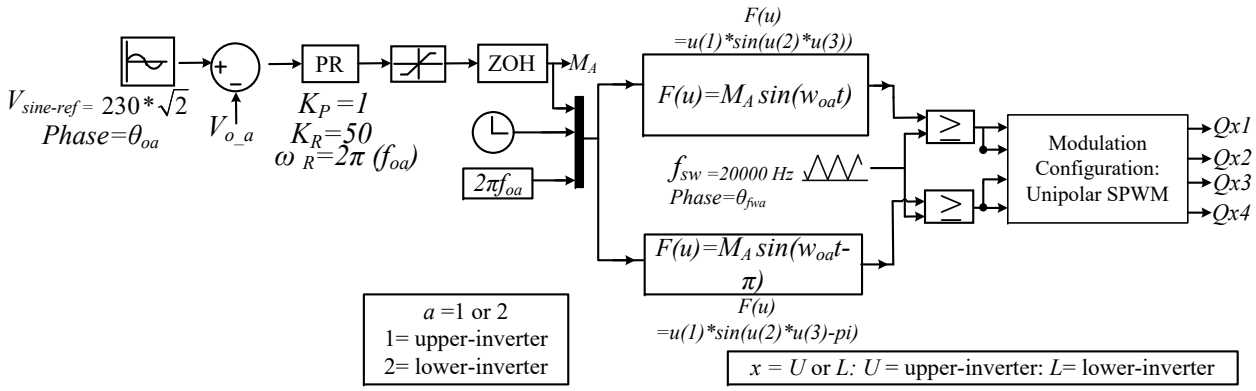

Fig. 3. Control algorithm for inverter unit (K_P−Proportional parameter, K_I−Integral parameter, K_R−Resonant coefficient, ω_R-Resonant frequency, ω_{oa}=2πf_{oa}).

SPWM, by applying a phase-shift to both the fundamental output current, and to the carrier wave of the lower inverter, as shown in the Fig. 4.

A. Analytical Modelling of DC-Capacitor-Current

To apply the proposed DC-link capacitor design method, the total current flowing through the DC-capacitor is analytically modeled. First, the capacitor-current harmonic contribution by the individual inverter is analyzed using (1)-(9). The capacitor-bank current for the upper-inverter, denoted by, $I_{capbank\_1}$ is found using (1)-(4), while (5)-(8) is used to find the lower-inverter capacitor-current, expressed by $I_{capbank\_2}$. The general analytical equation (1) to find the output voltage of an inverter using unipolar SPWM is explained in detail in [31].

$$V_{o\_1} = M_A V_{dc} \sin(\omega_{o1} t + \boldsymbol{\theta_{o1}}) + \frac{4V_{dc}}{\pi} \sum_{m=2,4,6\ldots}^{\infty} \sum_{n=\pm1,\pm3,\pm5\ldots}^{\pm\infty} \left(\frac{J_n(mM_A\pi/2)}{m} cos(\frac{m\pi}{2}) \sin(n(\omega_{o1} t + \boldsymbol{\theta_{o1}}) + m(\omega_{c1} t + \boldsymbol{\theta_{fsw1}})) \right) \quad (1)$$

$$I_{o\_1} = I_{o\_peak\_1} \times \sin(\omega_{o1} t + \boldsymbol{\theta_{o1}}) \quad (2)$$

$$I_{dc\_1} = I_{o\_1} \times \underbrace{(\frac{V_{o\_1}}{V_{dc}})}_{SwitchingFunction} \quad (3)$$

$$I_{capbank\_1} = I_{dc\_1} - I_{dc\_avg\_1} \quad (4)$$

$$V_{o\_2} = M_A V_{dc} \sin(\omega_{o2} t + \boldsymbol{\theta_{o2}}) + \frac{4V_{dc}}{\pi} \sum_{m=2,4,6\ldots}^{\infty} \sum_{n=\pm1,\pm3,\pm5\ldots}^{\pm\infty} \left(\frac{J_n(mM_A\pi/2)}{m} cos(\frac{m\pi}{2}) \sin(n(\omega_{o2} t + \boldsymbol{\theta_{o2}}) + m(\omega_{c2} t + \boldsymbol{\theta_{fsw2}})) \right) \quad (5)$$

$$I_{o\_2} = I_{o\_peak\_2} \times \sin(\omega_{o2} t + \boldsymbol{\theta_{o2}}) \quad (6)$$

$$I_{dc\_2} = I_{o\_2} \times \underbrace{(\frac{V_{o\_2}}{V_{dc}})}_{SwitchingFunction} \quad (7)$$

$$I_{capbank\_2} = I_{dc\_2} - I_{dc\_avg\_2} \quad (8)$$

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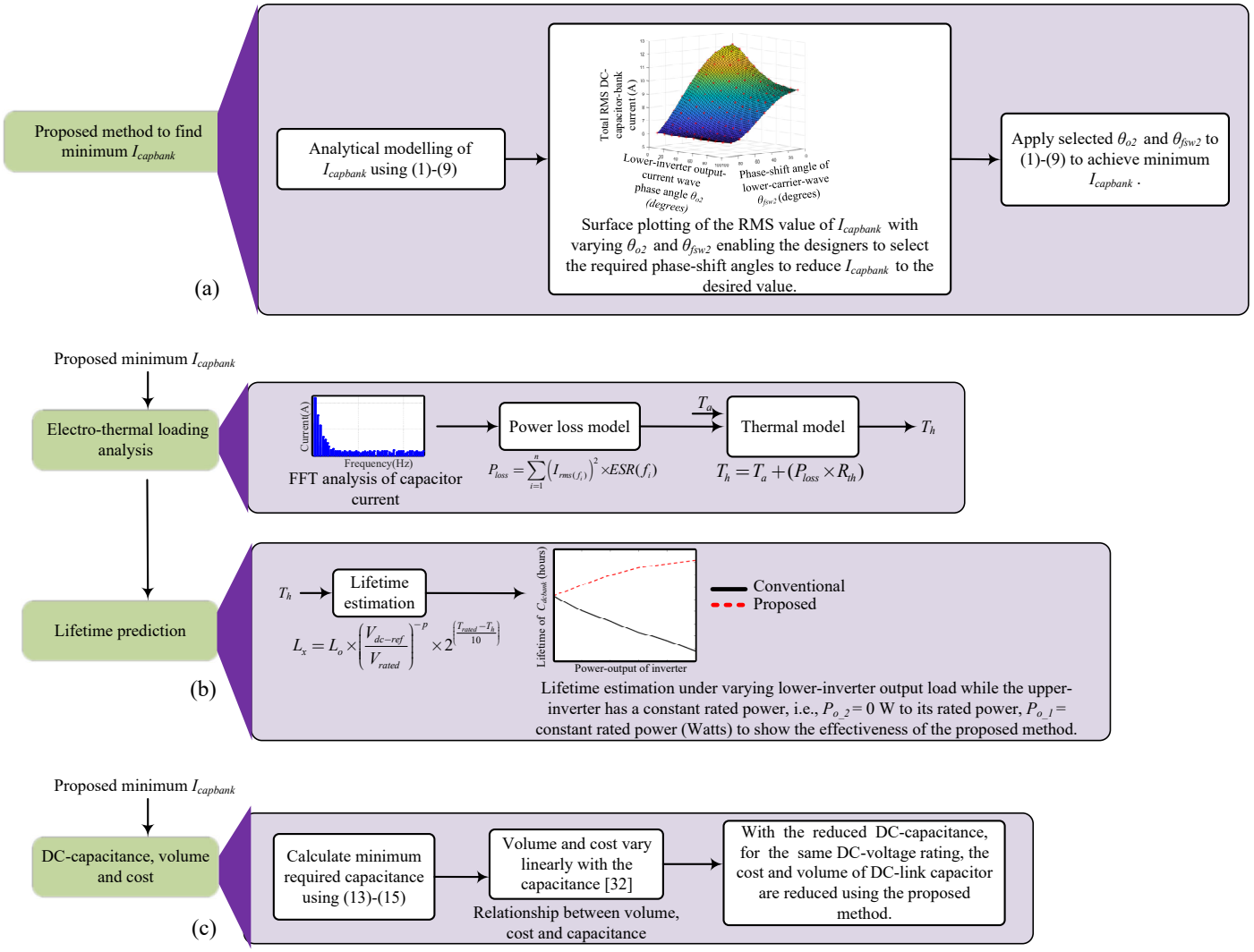

Fig. 4. (a) Flowchart of the proposed method to obtain minimum DC-capacitor current in a multidrive system, (b) lifetime prediction method using the proposed minimum $I_{capbank}$, and (c) DC-capacitance, cost and volume estimation procedure using the proposed minimum $I_{capbank}$.

In the above equations (1) - (8), θ_{o1} is the phase-angle for the upper-inverter fundamental output current, and θ_{fsw1} is the interleaving angle for the upper-carrier-wave. Likewise, θ_{o2} and θ_{fsw2} are the phase-angles for the lower-inverter fundamental output current, and the lower-carrier-wave.

$V_{o\_1}, V_{o\_2}, I_{o\_1}, I_{o\_2}$, in the above equations (1) - (8), present upper and lower inverter output voltages, and output currents. $I_{o\_peak\_1}$ and $I_{o\_peak\_2}$ are the peak values of output currents of upper and lower inverters. $I_{dc\_1}, I_{dc\_2}, I_{dc\_avg\_1}, I_{dc\_avg\_2}$ represent the individual DC-current drawn by the upper and lower inverters, and their average value. Finally, the fundamental angular frequency, and angular switching-frequency of the upper inverter are symbolized by ω_{o1}, ω_{c1}, and that of the lower inverter is designated by ω_{o2}, ω_{c2}. The power balance equation (neglecting the loss of the inverter), which states that the input power on the DC-side $(P_{dc} = V_{dc} \times I_{dc})$ of the converter relates to the output apparent power on the AC-side, $(P_{ac} = V_o \times I_o)$ is used to derive (3) and (7).

Nevertheless, the total DC-link capacitor-current $I_{capbank}$ in Fig. 2 can be expressed by summing up all harmonic capacitor-currents in (4) and (8) as

$$I_{capbank} = I_{capbank\_1} + I_{capbank\_2} \tag{9}$$

indicating the possibility to cancel out the double-fundamental $(2 \times f_o)$ harmonic component and switching-frequency harmonic (f_{sw_h}) component of the total DC-capacitor-current, if the two inverters' output currents and carrier waves are phase-shifted by the optimal angle. Subsequently, helping to achieve the desired minimum $I_{capbank}$. It is important to note that it is possible to completely cancel $2 \times f_o$ and f_{sw_h} switching-frequency harmonic component of $I_{capbank}$ occurs, when the two inverters have the same operating conditions, as per (9).

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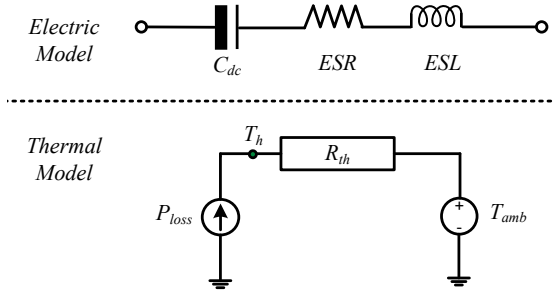

Fig. 5. Equivalent electrical and thermal model of the DC-link capacitor [8].

B. Surface Plotting to Find the Minimum $I_{capbank}$

The design requirements to reduce the $I_{capbank}$ value differs from one application to another. Hence, one practical method is to obtain the surface plot of the $I_{capbank}$, with varying θ_{o2} and θ_{fsw2} using (1)-(9) for the system shown in Fig. 2. This plotting enables the designers to select the required phase-shift angles to reduce $I_{capbank}$ to the desired value. This is a key step, because, selection of these optimal phase-shift angles θ_{o2}, and θ_{fsw2} from the plotted graph determines how much DC-link harmonic cancellation occurs, according to which the capacitor size, along with its power-losses and expected lifetime changes. In this paper, the optimal angles are considered to be the ones, which results in the minimum $I_{capbank}$ value. The optimally phase-shifted switching cycles lead to variations of the output current ripples, and the double-fundamental frequency ripples of the output current are also phase-shifted, both of which when summed together, as explained in (9), results in the minimization of ripples in DC-link current as shown in Fig. 9(d). Increasing or decreasing the phase-shift angles beyond this point will increase the $I_{capbank}$ as there will not be as much harmonic cancellations as in the scenario where $I_{capbank}$ is minimum.

IV. Design of DC-Link Capacitor in Multidrive System Based on the Proposed Minimum DC-capacitor current

In this section, using the proposed minimum DC-capacitor current, the DC-link capacitor in a multidrive system (shown in Fig. 2) can be designed based on the following criteria: (1) lifetime, (2) capacitance, volume and cost.

A. Design Criteria: Lifetime of DC-Capacitor

Based on the proposed minimum $I_{capbank}$ achieved by applying θ_{o2} and θ_{fsw2} to (1)-(9), the expected lifetime of the DC-link capacitor can be analyzed using the (10)-(12) [9]. The equivalent circuit model consisting of the electrical and thermal model of the capacitor used in this paper is illustrated in Fig. 5. The electro-thermal analysis of the DC-capacitor can be analyzed using (11) - (12). These parameters are of adequate importance, as an increase in the electro-thermal stress decreases the lifetime of the DC-capacitor. Reducing the harmonics ripples in the DC-capacitor current helps to improve the expected lifetime L_x of the DC-capacitor, as the overall electrical and thermal stress in the capacitor significantly decreases [8]. The equivalent series inductance (ESL) is not considered in this paper for calculations because the simulations are operated below the resonance frequency of the capacitor, where the inductive resistance of the winding and its terminals ($X_L = \omega \times$ESL) is considered to be very small and constant. Similarly, for the selected capacitor $I_{leakage}$ is very small (in values of μA) [30], and not considered into calculations.

$$L_x = L_o \times (\frac{V_{dc-ref}}{V_{rated}})^{-p} \times 2^{\frac{T_{rated}-T_h}{10}} \tag{10}$$

$$T_h = T_a + (P_{loss} \times R_{th}) \tag{11}$$

$$P_{loss} = \sum_{i=1}^{n} (I_{rms(f_i)})^2 \times ESR(f_i), \tag{12}$$

where the value of the exponent p is between 3 to 5 for El-caps [8]. $I_{rms(f_i)}$ is the RMS value of the harmonic ripple current at frequency f_i, obtained from the harmonic spectrum of the capacitor current, and $ESR(f_i)$ is the ESR at the i^{th} frequency f_i. The hot-spot temperature T_h of the DC-capacitor, estimated by (11), and the power-loss P_{loss} of the capacitor (which is a function of ripple current and ESR) is calculated using (12).

The above equations (10) - (12) show that an increase in the capacitor-current (i.e., capacitor-current harmonic ripples) increases both the power-losses and capacitor core temperature (T_h) within the capacitor, which will eventually result in a decreased lifetime for the DC-link capacitor. Therefore, reducing the DC-link capacitor current using the proposed method will help to reduce the power-losses P_{loss} and hot-spot temperature T_h of the DC-capacitor, thereby improving its lifetime as per (10).

B. Design Criteria: DC-link Capacitance, Volume and Cost

The required minimum DC-link capacitor $C_{DC-bank}$ can be calculated using (13)-(15). To meet the hold-up time (t_{hold}) and voltage ripple requirements, the capacitor is selected to have the larger value of the (13) and (14) below.

$$C_{DC-bank1} \geq \frac{2 \times P_{o-total} \times t_{hold}}{V_{dc-ref}^2 - V_{dc-ref-min}^2} \tag{13}$$

$$C_{DC-bank2} \geq \frac{P_{o-total}}{2\pi f_o \times V_{p-p} \times V_{dc-ref}} \tag{14}$$

$$C_{DC-bank} = max(C_{DC-bank1}, C_{DC-bank2}) \tag{15}$$

where $P_{o-total}$ is the total output power of the multidrive system. For the system shown in Fig. 2, the $P_{o-total}$ = P_{o_1}+ P_{o_2}. $V_{dc-ref-min} \cong 90\% \times V_{dc-ref}$ is the minimum amount of DC-link voltage required to make sure that in case of disruption in the power supply, the output power remains stable for an t_{hold} amount of time [29]. Furthermore, it is a known fact that the required capacitance value is linearly varying with the amount of current flowing through the capacitor. Therefore, the proposed minimum $I_{capbank}$ will reduce the amount of required capacitance. Additionally, the volume and cost of capacitors are also linear with the energy storage, which

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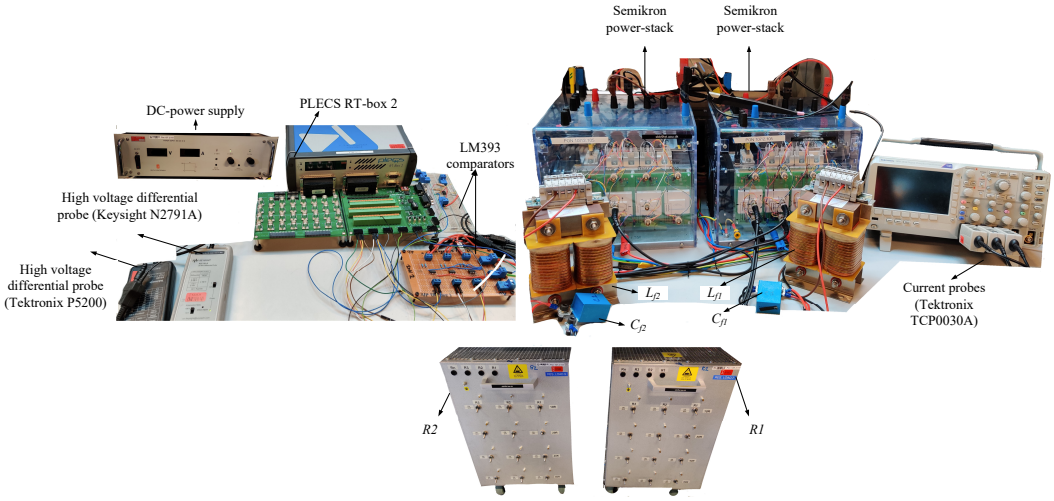

Fig. 6. Experimental prototype of the multi-converter system (shown in Fig. 2) having two parallel inverters.

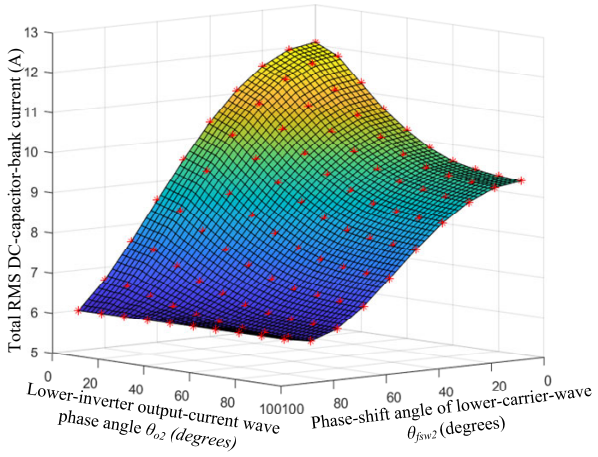

Fig. 7. Surface plotting of the total DC-link capacitor-current with varying θ_{o2}, and θ_{fsw2} for the multidrive system (shown in Fig. 2).

is $E_{capbank}$= $\frac{1}{2}C_{DC-bank}$ $\times {V_{dc-ref}}^2$, which depends upon the required DC- capacitance and voltage, respectively [20]. Hence, with the reduced DC-capacitance value, for the same DC-voltage rating, the cost and volume of DC-link capacitor are reduced.

V. Experimental Validation of the Proposed Method

To validate the proposed method, a downscale experimental platform (referring to Fig. 2) is built as shown in Fig. 6. Resistor banks are used as the loads for the inverters, and the operating conditions listed in Table V, and main system specifications listed in Table VI, are scaled down to enable lab-scale experimentation. The operating conditions of the two parallel-inverters (SEMIKRON power stacks) are kept the same throughout the experiment. The SEMIKRON power stacks are connected to a common DC-bus supplied with a constant DC-voltage source of 50 V, and the PLECS-RT box 2 is used to control the unipolar PWM signals for each of these are inverters. The LM393 comparators are used to shift this voltage level of the RT-box PWM signals have from 5V to 15V (the minimum requirement for gate drivers to operate).

TABLE V
Experimental System Specifications for Fig. 6

Module	Part Number/Parameter	Symbol
SEMITEACH IGBT module stack	SEMIKRON 08753450	-
AC-filter inductors	4 mH, 20 A rated current	L_{f1},L_{f2}
AC-filter capacitors	1 μF, 1600 V, 19.1 A @ 40°C	C_{f1},C_{f2}
Voltage comparators	LM393	-
PLECS controller box	RT-box 2	-
Resistor Banks	10 Ω–80 Ω	R_1,R_2

TABLE VI
Scaled-down Operating Conditions for Experimental Analysis.

Parameter	Symbol	Value
Rated power (W)	P_{o_1}, P_{o_2}	50
Upper-inverter load (Ω)	R_{o_1}	20
Lower-inverter load (Ω)	R_{o_2},	20, 35, 52
Rated RMS load voltage (V)	$V_{sine-ref}$	32
Load frequency (Hz)	f_o	50
Rated DC-link voltage (V)	V_{dc-ref}	50
Switching frequency (kHz)	f_{sw}	5
Modulation amplitude index	M_A	0.8

A. Verification of the Proposed DC-Capacitor Current Reduction Method

1) Case 1: Multidrive System with Same Output Power and Same Frequency: Referring to example case study (in Fig. 2), using (1)-(9) and applying the specifications mentioned in Table I-Table IV, Fig. 7 is plotted. It can be observed that the RMS DC-capacitor current attains a minimum value when θ_{o2} = 90° and θ_{fsw2} = 90° for this particular case study. Increasing or decreasing the phase-shift angles beyond this point will

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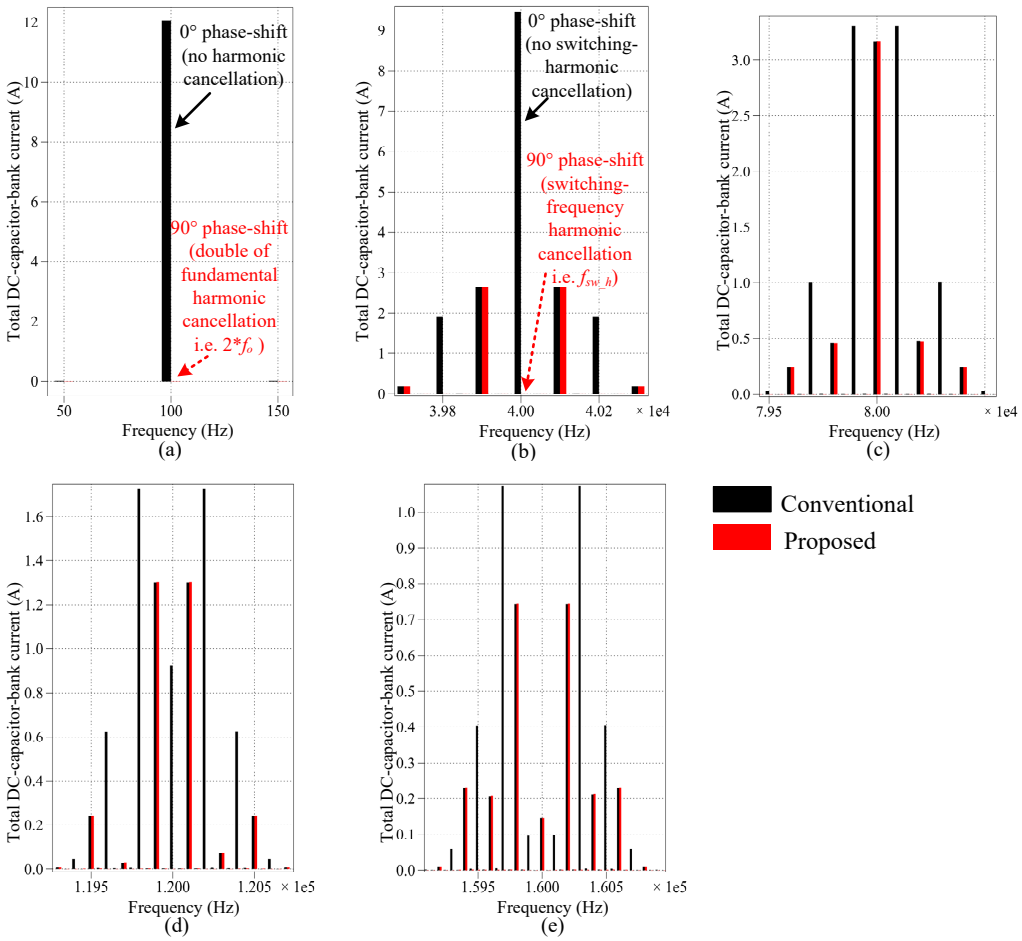

Fig. 8. Harmonic characteristics of the total DC-link capacitor-current for the multidrive system, (illustrated in Fig. 2) presenting the following harmonic components: (a) $2 \times f_o$, i.e. 100 Hz, (b) first switching-frequency harmonic component f_{sw_h} = 40 kHz (c) second f_{sw_h} = 80 kHz, (d) third f_{sw_h} = 120 kHz, (e) fourth f_{sw_h} = 160 kHz. (Since a unipolar SPWM is implemented with f_{sw_h} = 20 kHz, f_{sw_h} will appear at multiples of two times the switching frequency).

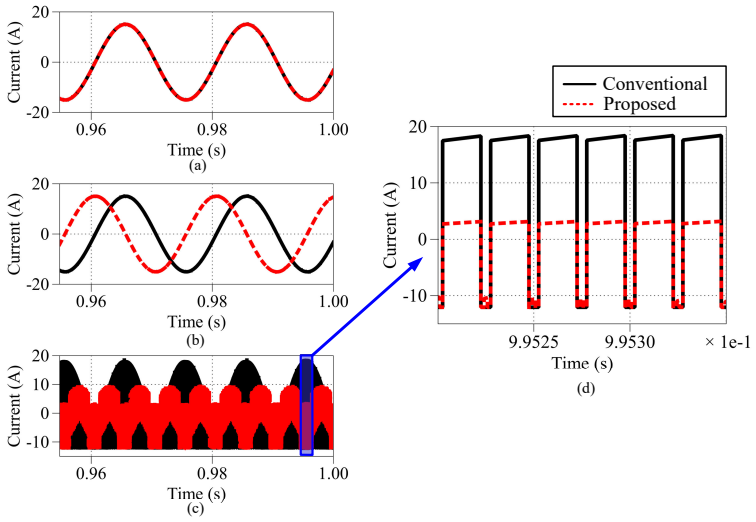

Fig. 9. Time-domain waveforms (red lines indicating the proposed method with optimal phase-shift, and black lines indicating system without any phase-shift) of: (a) upper-inverter output current wave, (b) lower-inverter output current wave, (c) total DC-capacitor current waveform, (d) zoomed in version showing $I_{capbank}$ ripples.

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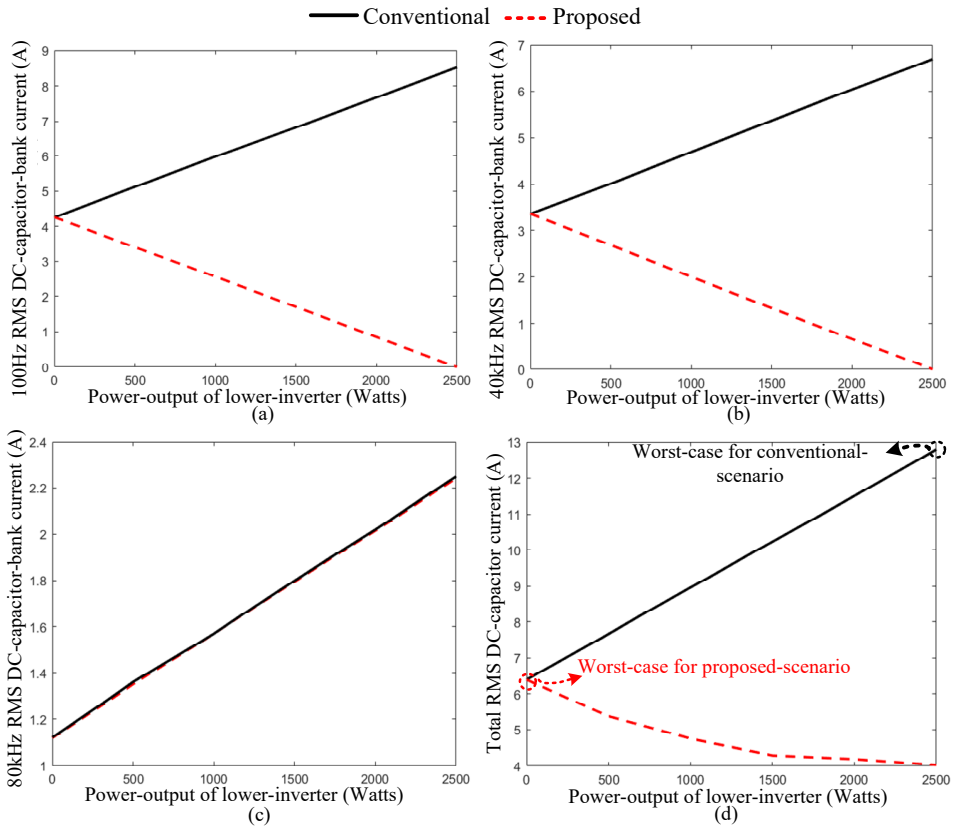

Fig. 10. Plots of the harmonic components of $I_{capbank}$, and the total DC-link capacitor-bank current, when P_{o_2} is varied between 0 W to 2500 W (rated power), while P_{o_1} has a constant rated power of 2500 W, and θ_{o2} = θ_{fsw2} = 0° (conventional method shown in black colour line), and θ_{o2} = θ_{fsw2} = 90° (proposed method in red colour line) showing: (a) 2 × f_o = 100 Hz, (b) f_{sw_h} = 40 kHz, (c) f_{sw_h} = 80 kHz, and (d) $I_{capbank}$.

increase the $I_{capbank}$ as there will not be as much harmonic cancellations as in the scenario where $I_{capbank}$ is minimum. Thus, the optimal phase-shift angle in this example case study is considered to be 90°, for the inverter output currents, as well as carrier waves. Applying these interleaving angles in (1)-(9), the harmonic spectrum of $I_{capbank}$ is plotted in Fig. 8(a-e), which exemplifies the effectiveness of the proposed method. It can be seen that in the conventional method (black color), i.e. when no phase-shift is applied, there are no harmonic cancellations, whereas using the proposed method (red color), there are complete cancellations of $2\times f_o$ and f_{sw_h} harmonics. The time-domain waves from the PLECS simulations in Fig. 9, of the multidrive system (in Fig. 2), further demonstrate the usefulness of the proposed method in reducing the DC-link capacitor current ripple. Moreover, it can be seen in Fig. 9(d) that the $I_{capbank}$ ripple is reduced by almost 50% (red color) by implementing the proposed technique, compared to the conventional case (black color) when no interleaving is applied. Significantly, using the proposed method helps to achieve the minimum value of $I_{capbank}$, which reduces the electro-thermal stress and hot-spot temperature at the DC-link capacitor.

The plots in Fig. 10(a-b) confirm the impact of the proposed method and demonstrates that even in scenarios when parallel-inverters are partially loaded, there is still some amount of $2 \times f_o$ and f_{sw_h} harmonic components' cancellation, which eventually reduces the total RMS $I_{capbank}$, as shown in Fig. 10(d). This demonstrates the feasibility to practical implementation of the proposed method. Particularly, this is an interesting result to the industrial applications, as the proposed method is effective in reducing the DC-link current even in the case when parallel units do not have the same power. When P_{o_2} = 0 W, the scenario where the lower inverter is not operating, as there is no interleaving (phase-shifting) occurring, there is no harmonic ripple cancellation. In Fig. 10(c), there is no impact of the optimal phase-shift observed. This is because, when a 90° phase-shift (the optimal phase-shift angle in this case study example) is applied to carrier waves, the first harmonic component, i.e. f_{sw_h} = 40 kHz of the lower-inverter is phase-shifted by 180° concerning that of the upper-inverter and cancels off with each other, whereas, the second harmonic component lower-inverter, i.e. f_{sw_h} = 80 kHz is phase-shifted by 360°, and doesn't cancel with that of the upper-inverter. Hence, the effect of the proposed phase-shift is not seen in the 80kHz harmonic component of $I_{capbank}$.

The key idea is to show, for instance, how the designers can implement the proposed method explained above to design DC-capacitor in a multidrive system with reduced RMS DC-capacitor current, lowered power- loss, and improved lifetime. Looking at Fig. 10(d), it is observed that even in the worst-case scenario, the proposed method can reduce the RMS value of $I_{capbank}$ by 50% compared to that of the conventional method.

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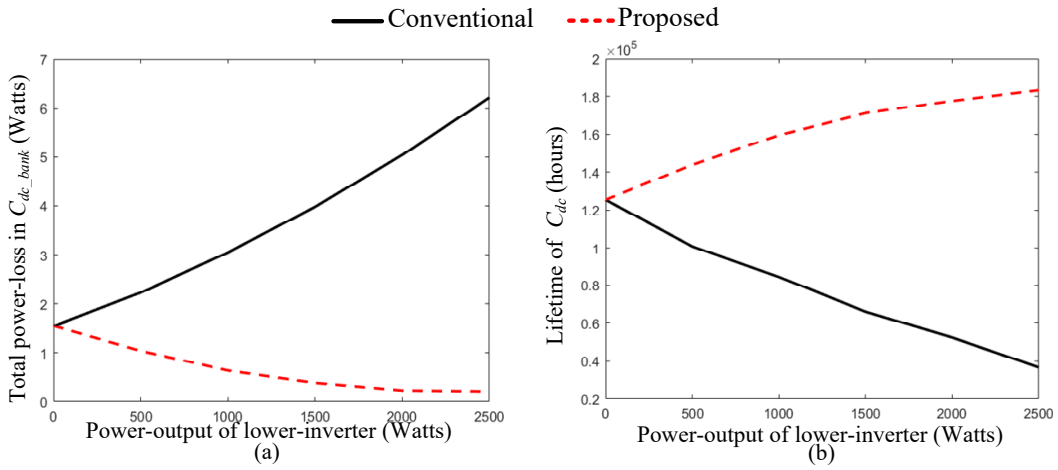

Fig. 11. Plots showing the impact of the proposed method (red color) compared to the conventional method (black color) in the (a) total power-loss in DC-capacitor, (b) lifetime of DC-capacitor (calculated as per [9])-with varying lower-inverter having output power (0 W - 2500 W), and P_{o_1} = 2500 W.

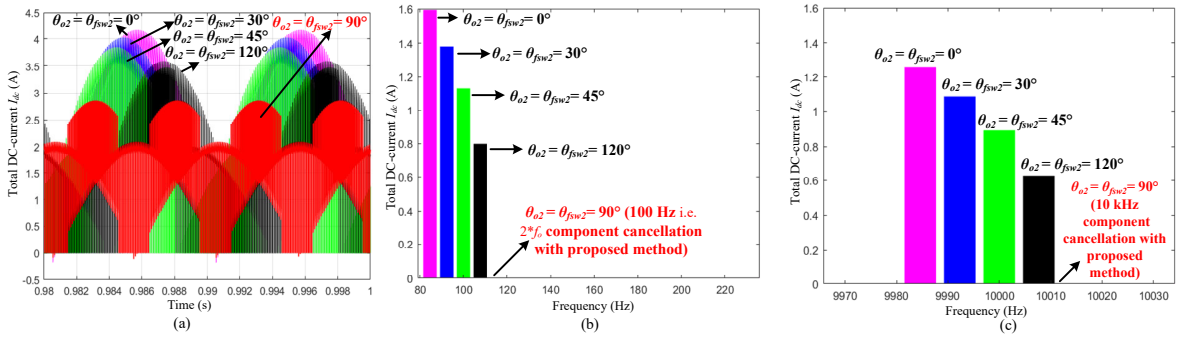

Fig. 12. Experimental data (using the scaled-down operating conditions, given in Table VI) of case-1 plotted in MATLAB showing: (a) the time-domain waveforms when various phase-shift angles are applied, and the corresponding harmonic spectrum components, (b) $2 \times f_o$ = 100 Hz, and θ_{fsw2} = 10 kHz: demonstrating the effectiveness of the proposed method in cancellation of the main harmonic components of I_{dc}.

This helps to improve the overall reliability and is of particular interest to industry as the lifetime of DC-capacitors can be increased at a lower-cost. Designers focussing to reducing the power-loss within capacitor of a multidrive system can refer to Fig. 11(a), which highlights that, for example, when both drives are operated at same loading condition, the power-loss is reduced to more than 80% when the proposed method is applied. On the other hand, those intending to improve the DC-capacitor lifetime can understand from Fig. 11(b) that the proposed method helps to improve the DC-capacitor lifetime. For instance, in Fig. 11(b), it can be observed that implementing the proposed method on a multidrive system with drives having same output loading conditions, the lifetime of DC-capacitor increased by four years (∼35000 hours). Applying the proposed method will thus, help to reduce the harmonic content of DC-link, reducing the overall RMS DC-capacitor current in the multidrive system, thereby improving its lifetime.

One among the methods to experimentally verify the proposed method is to apply various phase-shift angles (such as $\theta_{o2} = \theta_{fsw2} = 0°$, $\theta_{o2} = \theta_{fsw2} = 30°$, $\theta_{o2} = \theta_{fsw2} = 45°$, $\theta_{o2} = \theta_{fsw2} = 120°$, and $\theta_{o2} = \theta_{fsw2} = 90°$) to the lower-power stack of the experiment setup. The upper-inverter output power is P_{o_1} = 50 W, R_{o_1} = 20 Ω, and the lower-inverter has output power P_{o_2} = 50 W, R_{o_2} = 20 Ω. Both inverters have same fundamenatl frequency of 50 Hz. Then the main harmonic spectrum components ($2 \times f_o$ = 100 Hz and f_{sw_h} = 10 kHz) of the DC-current I_{dc} are observed. Due to the presence of a large DC-capacitor in the power stack, it is difficult to obtain this waveform directly as all higher harmonics are absorbed by the DC-capacitor, and only low harmonics of I_{dc} can be measured. Hence, the $I_{dc-source}$ and the $I_{capbank}$ are measured first, using current-probes, and their CSV data is obtained from the oscilloscope measurements. This is used to plot the time-domain waveforms of I_{dc} and their respective harmonic spectrum in MATLAB, as shown in Fig. 12. It can be seen that the $2 \times f_o$ = 100 Hz and f_{sw_h} = 10 kHz is completely cancelled when the proposed method, i.e. phase-shift angles of $\theta_{o2} = \theta_{fsw2} = 90°$ are applied to the multidrive system, thus making it the optimal phase-shift angle. More importantly, the total DC-current ripple is reduced by 50% if compared to the conventional case, i.e. when no phase-shift is applied, $\theta_{o2} = \theta_{fsw2} = 0°$, meaning that required DC-link capacitance is reduced. Overall, test results agree with the proposed method explained in the Section III and Section IV. For completeness, the output voltage and current

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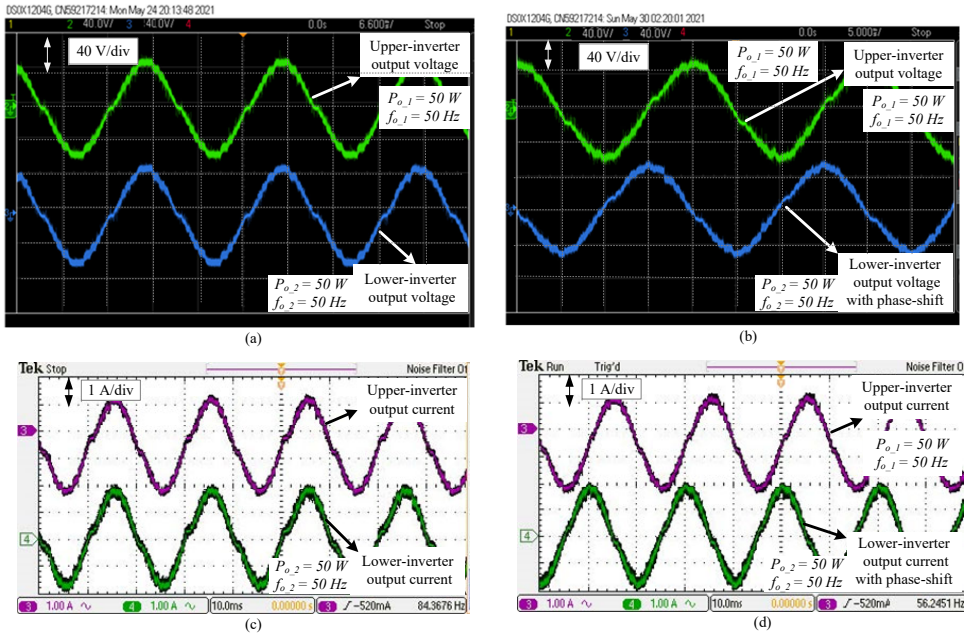

Fig. 13. Measured waveforms of the multidrive system (using the parameters in Table V) for case-1 showing: (a) output voltages with no interleaving, (b) output voltages with $\theta_{o2} = \theta_{fsw2} = 90°$, (c) output currents with no interleaving, and (d) output currents with $\theta_{fsw2} = 90°$.

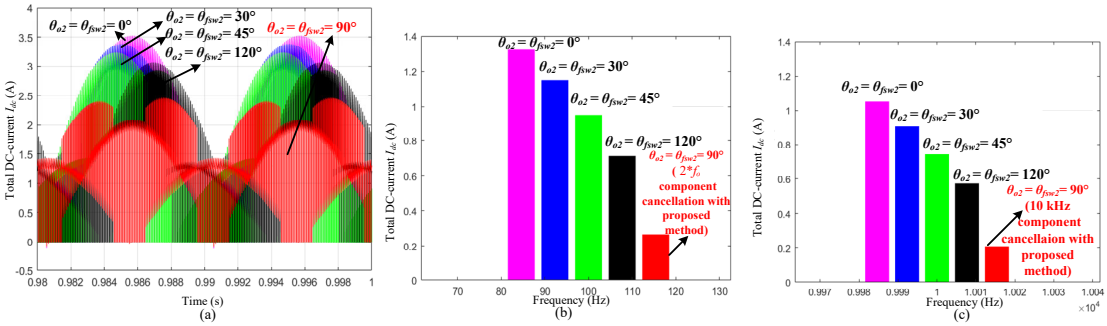

Fig. 14. Experimental data of I_{dc} for case-2 plotted in MATLAB showing: (a) the time-domain waveforms when various phase-shift angles are applied, and the corresponding harmonic spectrum components, (b) $2 \times f_o$ = 100 Hz, and θ_{fsw2} = 10 kHz: demonstrating the effectiveness of the proposed method in cancellation of the main harmonic components of I_{dc}.

waveforms of the multidrive system at $\theta_{o2} = \theta_{fsw2} = 0°$, and $\theta_{o2} = \theta_{fsw2} = 90°$, are shown in Fig. 13.

To further verify the proposed method, the following experiments have been conducted, which involve implementing parallel-inverters with different loading conditions, and with different output frequencies. All experiments below are using the setup parameters, and the operating conditions given in Table V and Table VI, except the rated power and the load frequency of the upper and lower inverter, which changes in each of the following cases. The same procedure as mentioned above in Section V.A is followed for the following additional experiment analysis.

2) Case 2: Multidrive System with Different Output Power but Same Frequency: In this case, the output frequencies of the two parallel inverters are kept the same, while their output powers are different, and various phase-shift angles are applied to the lower-inverter of the experimental setup to measure its effect on the I_{dc}. The upper-inverter output power is P_{o_1} = 50 W, R_{o_1} = 20 Ω, and the lower-inverter has output power P_{o_2} = 30 W, R_{o_2} = 35 Ω. Both parallel-inverters have the same output frequency of 50 Hz. The obtained results are shown in Figs. 14 and 15, respectively. As expected, when the drives do not have the same output powers, the harmonic components, i.e. $2 \times f_o$ = 100 Hz, and f_{sw_h} = 10 kHz cancellation is less (as shown in Fig. 14) than in the proposed situation (with two drives having the same output power), shown in Fig. 12(b-c). However, it is to be noted that the lowest harmonic ripple is till when $\theta_{o2} = \theta_{fsw2} = 90°$, proving that the proposed method can be utilized in such scenarios to reduce the DC-link current.

3) Case 3: Multidrive System with Same Output Power but Different Frequency: The parallel-drives in the multidrive system may not have the same output frequencies, and this point needs to be considered while designing the DC-capacitor from the DC-link harmonics point of view. Therefore, in this

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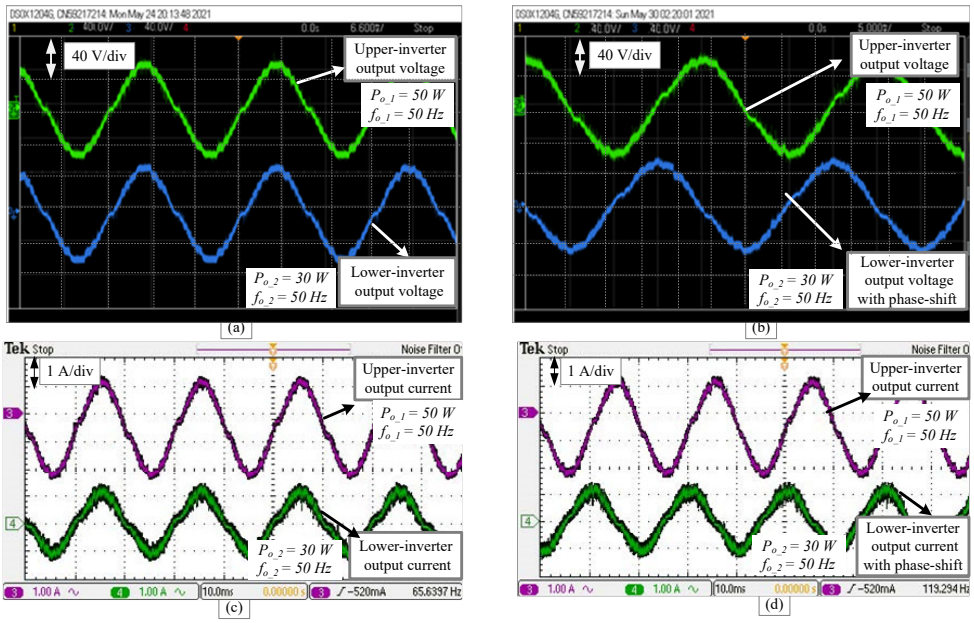

Fig. 15. Measured waveforms of the multidrive system for case-2 showing: (a) output voltages with no interleaving, (b) output voltages with θ_{o2} = θ_{fsw2} = 90°, (c) output currents with no interleaving, and (d) output currents with θ_{fsw2} = 90°.

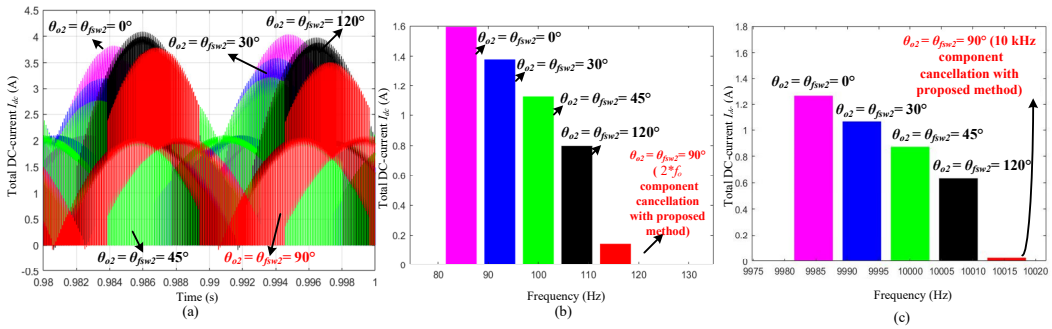

Fig. 16. Experimental data of I_{dc} for case-3 plotted in MATLAB showing: (a) the time-domain waveforms when various phase-shift angles are applied, and the corresponding harmonic spectrum components, (b) $2 \times f_o$, and θ_{fsw2} = 10 kHz: demonstrating the effectiveness of the proposed method in cancellation of the main harmonic components of I_{dc}.

case-3, the output frequencies of the two parallel inverters are different, i.e. the upper-inverter has an output fundamental frequency f_{o_1} = 45 Hz, while the lower-inverter has an output fundamental frequency f_{o_2} = 50 Hz. The output powers are assumed to be the same P_{o_1} = P_{o_2} = 50 W, R_{o_1} = R_{o_2} = 20 Ω and various phase-shift angles are applied to the lower-inverter of the experimental setup to measure its effect on the I_{dc}. It is observed from Figs. 16 and 17, that even though the drives have the same output powers, there are no complete harmonic cancellation of components, i.e. $2 \times f_o$, and f_{sw_h} = 10 kHz compared to Fig. 12. This is because of the different inverter output frequencies. Remarkably, the lowest harmonic ripple is still achieved by using the optimal θ_{o2} and θ_{fsw2}, proving that the proposed method can be utilized in such scenarios to reduce the DC-link current.

4) Case 4: Multidrive System with Different Output Power and Frequency: The final test conducted is on parallel-drives in a multidrive system may be having different output frequencies, and different output powers, i.e., the upper-inverter has an output fundamental frequency f_{o_1} = 45 Hz, output power P_{o_1} = 50 W while the lower-inverter has output fundamental frequency f_{o_2} = 50 Hz, and output power P_{o_2} = 20 W. The upper-inverter has R_{o_1} = 20 Ω, and the lower-inverter has R_{o_2} = 52 Ω. Both inverters have same fundamenatl frequency of 50 Hz. Various phase-shift angles are applied to the lower-inverter of the experimental setup to measure its effect on I_{dc}, and the obtained results are shown in Figs. 18 and 19. It is observed from Fig. 18(b-c) that, unlike the previous case study results, the harmonic components, i.e. $2 \times f_o$, and f_{sw_h} = 10 kHz are not mitigated. However, implementing the proposed method (i.e. using the optimal θ_{o2} and θ_{fsw2}), the harmonic ripple, and the overall I_{dc} is reduced by more than 50% compared to the conventional operating condition where there is no phase-shift applied i.e. when θ_{o2} = θ_{fsw2} = 0°. This is because of the different inverter output frequencies and output powers, due to which the $2 \times f_o$, and f_{sw_h} ripples don't cancel

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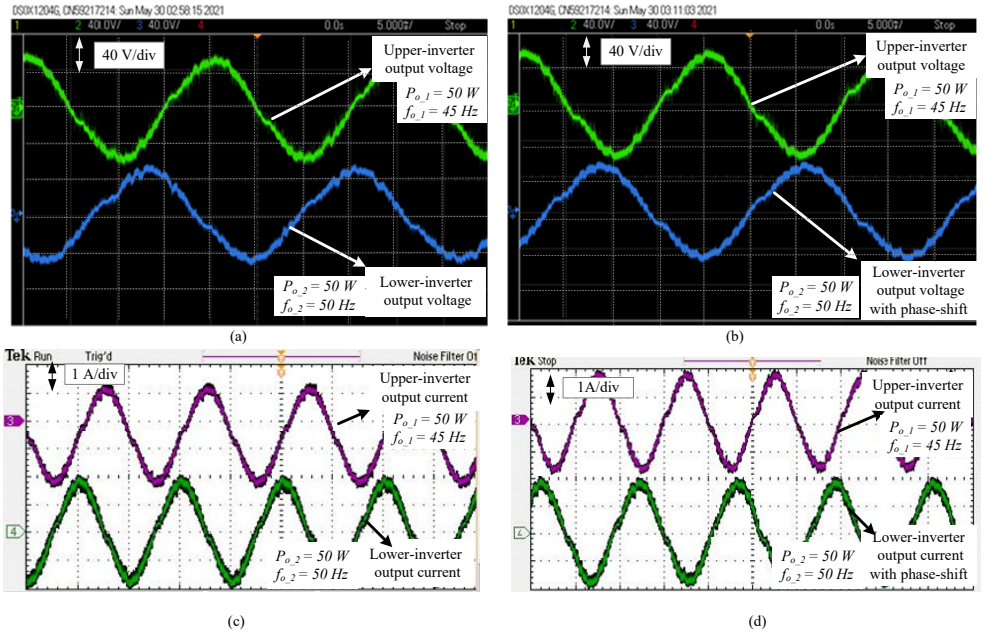

Fig. 17. Measured waveforms of the multidrive system for case-3 showing: (a) output voltages with no interleaving, (b) output voltages with θ_{o2} = θ_{fsw2} = 90°, (c) output currents with no interleaving, and (d) output currents with θ_{fsw2} = 90°.

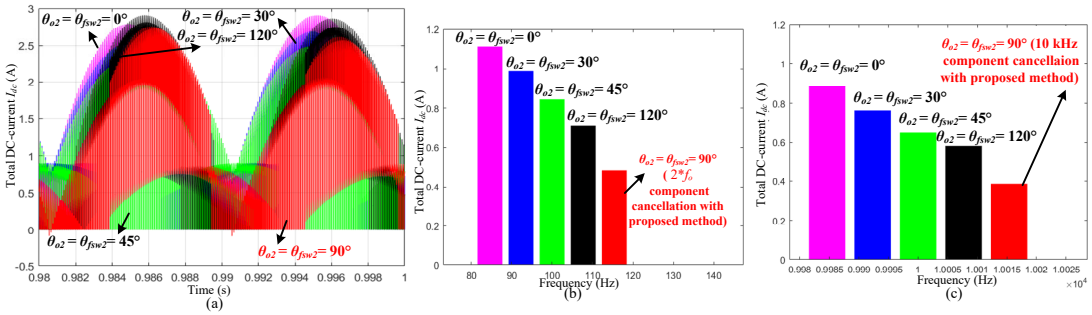

Fig. 18. Experimental data of I_{dc} for case-4 plotted in MATLAB showing: (a) the time-domain waveforms when various phase-shift angles are applied, and the corresponding harmonic spectrum components, (b) 2 × f_o, and θ_{fsw2} = 10 kHz: demonstrating the effectiveness of the proposed method in cancellation of the main harmonic components of I_{dc}.

each other as per (9) at the common DC-bus.

B. Verification of the Design of DC-Capacitor Based on the Proposed Capacitor Current Reduction Method

Using the minimum $I_{capbank}$, the new capacitor can be designed for Case-1. Notably, from a practical application standpoint, the design of any component, especially the DC-link capacitor is better, if the worst-case scenario is taken into consideration. Also, from (9), it can be inferred that the complete cancellation of the 2 × f_o and f_{sw_h} harmonic components of $I_{capbank}$ occurs, when the two inverters have the same output-power ratings and same operating conditions. This is one of the challenges in multidrive systems, because the parallel units do not necessarily always operate at the same rated power. To address this scenario, and design a DC-capacitor fulfilling the aforementioned criteria, the following steps are applied to the multidrive topology (in Fig. 2). In this case study, since the phase shift is applied to only the lower-inverter output current, and lower-inverter carrier signal, θ_{o1}=0°, θ_{fsw1}=0°, whereas θ_{o2}, θ_{fsw2} take the optimal phase-shift angle value, found as per the explanation in the above Subsubsection. V-A1. Firstly, P_{o_2} is varied between 0 W to 2500 W (rated power), while P_{o_1} has a constant rated power of 2500 W. Then, in each case, the 2 × f_o, first and second switching frequency harmonic component, as well as $I_{capbank}$ is observed from Fig. 10(a-c), when no phase-shift is applied (considered as the conventional method), and when the chosen optimal phase-shift angles (considered as the proposed method) is applied. Secondly, the worst case scenario, i.e., when $I_{capbank}$ RMS is the highest, is noted for both conventional and the proposed method from Fig. 10(d). Finally, the DC-capacitor is designed to operate under these worst case scenarios, and compared in terms of the minimum required capacitance value, its volume, and cost. The comparison of DC-capacitance, volume, and cost for case-1 designed using the proposed method and the conventional method is shown Fig. 20. Overall, it can be inferred that when the proposed method is applied to a multidrive system: (1) the

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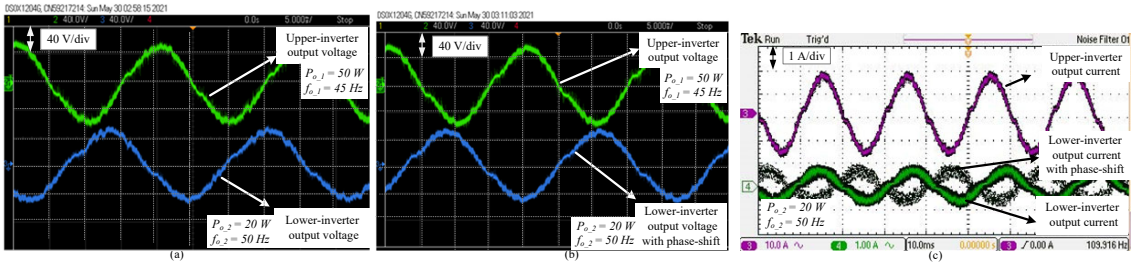

Fig. 19. Measured waveforms of the multidrive system for case-4 showing: (a) output voltages with no interleaving, (b) output voltages with θ_{o2} = θ_{fsw2} = 90°, (c) output currents with no interleaving, and output currents with θ_{fsw2} = 90°.

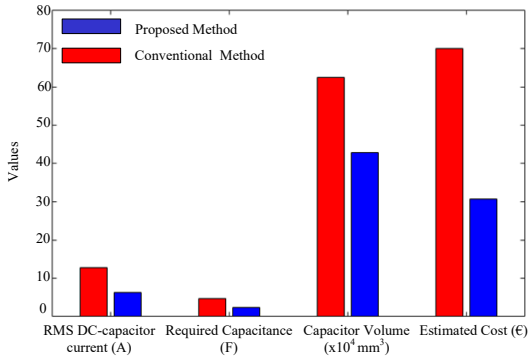

Fig. 20. Comparison of the DC-capacitor design using conventional and proposed method.

overall $I_{capbank}$ RMS value decreases (for case-1, $I_{capbank}$ reduces by 50%), (2) consequently lowers the required DC-link capacitance value (only half the value of the DC-capacitor is needed in case-1), which means that the overall capacitor volume, and cost reduces (by half in this example case-1).

All the above experimental results are in agreement with Section III and Section IV. Hence, it is fair to say that the proposed method is a feasible option to reduce the DC-link current and thereby reduce the bulkiness of the DC-link capacitor as well as increase its lifetime in a multidrive system cost-effectively. While it should be noted that in multidrive systems with more than two drives operating at various power levels, the proposed method needs further investigation. In such scenarios, one possible way is to group the drives having the same power together, forming an equivalent "two-drive" system, and apply the proposed method. However, if the number of inverters is 3, 5, etc then the following solution is a possibility. For example, if it is a system having 3 inverters, this can be done by adding the DC-link capacitor currents of two inverters together-$I_{capbank12}$ and then implementing a phase-shift between this $I_{capbank12}$ and the 3rd capacitor current $I_{capbank3}$. A detailed research about this scenario needs to be done in one of our future works. Another future work could involve optimizing the phase-shift angles when two inverters have different switching frequency waves, as well as different output frequencies.

VI. Conclusion

In this paper, a cost-effective design of the DC-link capacitor has been introduced for a multidrive system, focused on the DC-capacitor-current reduction, capacitor-size reduction, and lifetime improvements, without the need for additional hardware. The low-cost design is achieved by reducing DC-link current harmonics through optimal interleaving of the fundamental output currents in addition to the phase-shifting of the carrier waves of the parallel-connected inverters. Experimental results from four different case-studies have confirmed the effectiveness of the proposed method, and the following conclusions can be drawn:

1) Applying the proposed method results in the mitigation of the double-fundamental as well as switching frequency harmonics in the DC-current of the multidrive systems having same output loading conditions, i.e. same output load and frequency.
2) Consequently, the RMS value of capacitor current reduces by almost by 50%, which means that the required volume of DC-link capacitor, and the cost is reduced by 50%.
3) Mean-while, the power-loss within the DC-link capacitor is reduced by more than 80%, and the lifetime is increased by almost four years due to reduced electro-thermal stress.
4) Notably, the proposed method is also effective for practical industrial applications, where the parallel units do not necessarily run at the same power or same speed, and this has been exemplified through experimental and simulation results.

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