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A Review of Multi-Sampling Techniques in Power Electronics Applications

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***Abstract*—Due to the increasing performance and decreasing price of microcontrollers in recent years, applying a high sampling frequency becomes more feasible in modern control that is known as multi-sampling technology. The first motivation to use multi-sampling is emulating the analog control, and thereby reducing the control delay and improving the stability of power electronics controllers. On the other hand, more information can be acquired from the multi-sampled current/voltage, which helps to save the cost and improve the reliability. In this paper, a review of the multi-sampling application in power electronics converters is provided. Starting from the control delay analysis in single/double-sampling control, the modelling, implementation and related control strategies are given when using multi-sampling pulse width modulation (PWM). Then, based on the multi-sampled data, the applications in condition monitoring and parameter estimation are discussed. Lastly, perspectives on challenges and future trends are discussed.**

***Index Terms*—Multi-sampling PWM, multi-sampling control strategies, practical implementation, condition monitoring, parameter estimation.**

I. INTRODUCTION

NOWADAYS, digital control is the most commonly used technology in power electronic converters due to its flexibility, adaptability and insensitivity [1]. Nevertheless, for the regular single/double-sampling control, a control delay always exists in the control loop. Moreover, the control delay will affect the control bandwidth, dynamic performance and stability of digital controllers, especially in high-power converters with a low switching frequency [2]. Therefore, several control delay compensation methods are proposed, which are mainly divided into two categories. The first is the digital-filter-based delay compensation such as high-pass filter, Smith predictor and linear predictor, etc., but the compensation effect in high frequency range is limited and the high frequency noise may even be amplified [3-4]. The second is to shift the sampling instant or the update instant of the PWM, and the control delay can be reduced physically [5-7]. Specifically, shifting the sampling instant can minimize the computation delay but will introduce the aliased low-order harmonics. In addition, the output duty cycle is limited by the code processing time when shifting the update instant. To summarize the prior art, the control delay still cannot be reduced to one quarter of switching period, which is a critical stability boundary according to the passivity based theory [8].

With the gradually decreasing cost of high-performance microprocessors, multi-sampling control is a potential candidate to overcome the bandwidth limits, where the state variable is sampled and the duty cycle is updated multiple times within one switching period [9-10]. Consequently, multi-sampling control delay is inversely proportional to the sampling rate, which can make it close to the analog control if the sampling rate is high enough [11]. Therefore, the multi-sampling has been widely used to improve the control bandwidth of power electronic converters including DC-AC converters, DC-DC converters and motor drives [12].

Besides the average value, the switching ripple is introduced in the control loop when using multi-sampling, which is the main difference compared with the single/double-sampling [13]. Based on the voltage-second balance principle, the multi-sampling PWM is equivalent to a double-sampling PWM with the sampling instant and the update instant shift. Therefore, the equivalent Nyquist frequency is switching frequency, and the low-order aliased harmonics will appear in the output voltage/current [14-15]. In order to suppress the aliasing, various repetitive filters are proposed in DC-DC and DC-AC converters, where the introduced phase lag is the main optimization goal [13-16]. Another switching ripple suppression method is to change the sampling process or the carrier, but the feasibility should be further investigated [17-20]. For the multi-level converter, there will be no sampled switching ripple if using an optimum sampling rate. This is because the apparent switching frequency is higher than the preset switching frequency [21-23]. In addition, the multi-sampling can help to achieve a more accurate digital derivative and faster large-signal response [24-25].

However, there are a set of nonlinearities that need to be considered when employing the multi-sampling PWM. The first is the multi-switching within one switching period, which will cause higher switching loss compared with the regular PWM [26-27]. Second, the modulation signal may intersect with the carrier vertically, where the small-signal modulation gain is reduced and the stability margin is jeopardized [28-29]. Third, when the modulation signal and the carrier are in-phase operation, there will be an "increased gain" zone in the modulator trans-characteristic [30]. Fourth, limit cycle oscillations may happen if the PWM clock frequency and the sampling rate are not selected properly [25, 31]. Aiming for the above issues, some related solutions are discussed in this paper.

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Apart from the reduced control delay and the improved stability from the multi-sampling control, some new state variables and parameters can be estimated based on the multi-sampled voltage/current data. The main principle is to utilize the sampled switching ripple instead of the suppression. First, for a three-phase two-level inverter, the current slope can be estimated during the zero/active voltage vectors. Then the estimated current slope can be used to estimate the motor speed [32], the motor inductance [33], the grid voltage [34], etc. Moreover, the estimated current slope can be also used to diagnose the converter fault [35], compensate the dead-time [36], and reduce the magnitude of high frequency injected voltage signal [37]. In order to improve the dc-link reliability, the dc-link parameters can be estimated by multi-sampling the dc-link voltage/current [38]. In addition, the grid impedance can be estimated by multi-sampling the voltage/current at the point of common coupling (PCC) [39, 40, 95].

The subsequent content is organized as follows. The control delay analysis of the single/double/multi-sampling PWM is presented in Section II. The aliasing suppression, the control of multi-cell converters, the multi-sampled digital controllers, as well as the practical implementation are discussed in Section III. This is followed by the condition monitoring and the parameter estimation in Section IV. Finally, the challenges and future trends are outlined in Section V, and Section VI concludes the paper.

II. Control Delay Analysis of Single/Double-Sampling PWM and Multi-Sampling PWM

Control delay plays an important role in the digital control of power electronic converters, which affects the system stability and the control bandwidth. Considering the current control of a three-phase grid-connected inverter, as shown in Fig. 1(a), where U_{ga}-U_{gc} are the grid voltage, U_{pcca}-U_{pccc} are the PCC voltage, i_{inv} is the inverter-side current, L_f is the filter inductance, L_g and C_g are the grid impedance, respectively. The dc-link voltage is controlled to generate i^*_{invd}, and the PCC voltage is measured to obtain the grid phase angle through a phase-locked loop (PLL). Fig. 1(b) illustrates the block diagram of the used dq-frame current control loop and $G_i(s)$ is the proportional-integral (PI) current controller. By substituting $s \rightarrow s+j\omega_1$, the plant model $G_p(s)$ and the control delay $G_d(s)$ (the computation delay and the PWM delay) in the dq-frame are given in (2) and (3), where ω_1 is the grid angle frequency [41].

$$G_i(s) = K_p + \frac{K_i}{s} \tag{1}$$

$$G_p(s) = \frac{1}{(s + j\omega_1)L_f} \tag{2}$$

$$G_d(s) = e^{-(s+j\omega_1)T_d} \tag{3}$$

Based on Fig. 1(b), the inverter-side current is

$$i_{inv}(s) = G_{cl}(s)i^*_{inv}(s) - Y_o(s)U_{pcc}(s) \tag{4}$$

$$G_{cl}(s) = \frac{G_i(s)G_d(s)G_p(s)}{1+G_i(s)G_d(s)G_p(s)} \tag{5}$$

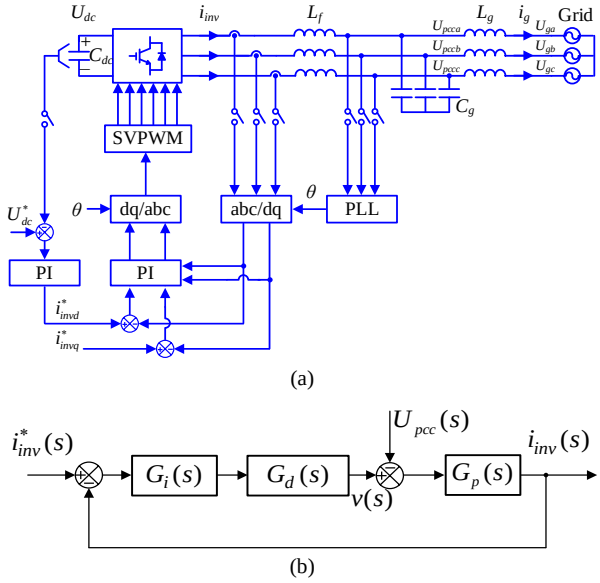


Fig. 1. Single current loop control of a three-phase grid-connected inverter. (a) System diagram, (b) Current control model.

$$Y_o(s) = \frac{G_p(s)}{1+G_i(s)G_d(s)G_p(s)} \tag{6}$$

where $G_{cl}(s)$ is the current control closed-loop transfer function and $Y_o(s)$ is the output admittance. Based on the passivity theory [8], the terminal response of a grid-connected inverter can be stabilized if the following two constraints are satisfied. First, the closed-loop transfer function $G_{cl}(s)$ should be stable. Second, the phase of $Y_o(s)$ should be within [−90°, 90°] or the real part of $Y_o(j\omega)$ should be non-negative [41] at all frequencies. Therefore, a positive real part of the converter admittance represents a dissipative behavior, whereas a negative resistance implies amplification of any oscillation at the respective frequency [50]. A network, consisting of resistive, inductive, and capacitive elements, results in passive $Y_{eq}(s)$. Passivity of both $Y_o(s)$ and $Y_{eq}(s)$ provides a sufficient condition for stable operation of the closed-loop current controller [96]. Note that the pure passivity is impossible to obtain, and the upper boundary of the dissipative region is set to the Nyquist frequency [97].

In terms of the first constraint, the maximum bandwidth r_b under a given phase margin is given in (7) [42].

$$r_b = \frac{\omega_c}{\omega_{sw}} = \frac{0.5\pi - \varphi_m}{T_d\omega_{sw}} = \frac{0.5\pi - \varphi_m}{2\pi h} \tag{7}$$

The control delay is expressed as $T_d = hT_{sw}$, where T_{sw} is the switching period. φ_m is the phase margin, ω_c is the crossover angle frequency, ω_{sw} is the switching angle frequency. For the conventional single-sampling PWM (h=1.5) and double-sampling PWM (h=0.75), based on (7), the bandwidth can be set to 0.08 and 0.16 when φ_m is set to 0.25π [43]. Hence, the inner stability in (5) can be easily secured.

Since the control delay mainly affects the passivity in the high-frequency range, the I current controller and the coupled term $j\omega_1 L_f$ can be neglected. By substituting '$s=j\omega$' into (6), Re{$Y_o(j\omega)$} can be simplified as (8). It can be seen that the sign of $Re\{Y_o(j\omega)\}$ is determined by the numerator, and the

dissipative region (i.e., the frequency range when $Re\{Y_o(j\omega)\}\geq 0$ below Nyquist frequency) is given in (9) where $f_{dissipative}$ is the dissipative frequency. Hence, the dissipative region can be lifted up to the switching frequency only if the control delay T_d is $0.25T_{sw}$. To illustrate the advantage of the multi-sampling PWM in the control delay reduction, the regular single/double-sampling PWM and their variants are reviewed.

$$\begin{aligned}\mathrm{Re}\{Y_o(j\omega)\} &= \mathrm{Re}\left\{\frac{1}{j(\omega+\omega_1)L_f + K_p e^{-j(\omega+\omega_1)T_d} + \frac{K_i}{j\omega}e^{-j(\omega+\omega_1)T_d}}\right\} \\ &\approx \mathrm{Re}\left\{\frac{1}{j\omega L_f + K_p e^{-j\omega T_d}}\right\} \\ &\approx \mathrm{Re}\left\{\frac{K_p\cos(\omega T_d)}{(K_p\cos(\omega T_d))^2 + (\omega L_f - K_p\sin(\omega T_d))^2}\right\}\end{aligned} \tag{8}$$

$$f_{dissipative} \in (0, \frac{1}{4T_d}) \tag{9}$$

A. Control Delay Using Single/Double-Sampling PWM

1) Without Sampling Instant and Update Instant Shift

The timing diagram of the single-sampling single-update (SSSU) PWM is shown in Fig. 2(a), the state variables are sampled in the valley of the carrier, and the modulation signal is updated after one switching period. Since the computation delay is T_{sw} and the PWM delay is $0.5T_{sw}$, the total control delay is given in (10) where T_{sw} and T_{sa} are the switching period and the sampling period, respectively [44-45]. Substituting (10) into (9), the dissipative region for SSSU PWM is given in (11).

$$T_{d\_SSSU} = \underbrace{T_{sw}}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} = 1.5T_{sw} \tag{10}$$

$$f_{dissipative\_SSSU} = (0, \frac{1}{6} f_{sw}) \tag{11}$$

Another conventional digital PWM method is double-sampling double-update (DSDU) PWM (see Fig. 2(b)), and the sampling instant and the update instant are located at the peak and the valley of the carrier. The control delay and the dissipative region are given in (12) and (13). Compared with the SSSU PWM, the DSDU PWM can effectively reduce the control delay and improve the stability. In addition, both the PWM methods have the same sampling instant and the update instant, which is convenient for the practical implementation, and the switching noise is not introduced.

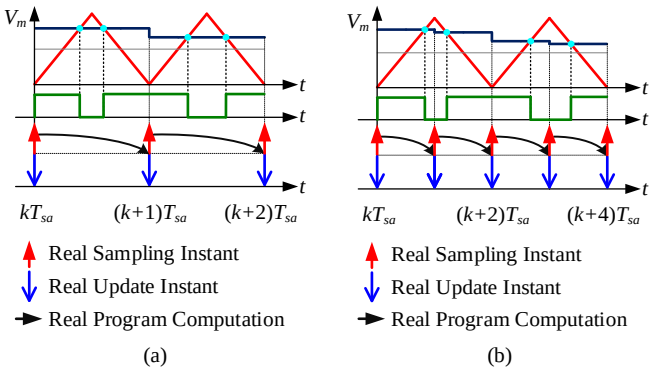


Fig. 2. Conventional digital PWM with the same sampling instant and update instant. (a) Single-update PWM with one-step computation delay, (b) Double-update PWM with one-step computation delay.

$$T_{d\_DSDU} = \underbrace{0.5T_{sw}}_{\text{computation delay}} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} = 0.75T_{sw} \tag{12}$$

$$f_{dissipative\_DSDU} = (0, \frac{1}{3} f_{sw}) \tag{13}$$

2) With Sampling Instant Shift

The SSSU PWM and the DSDU PWM control delay can be smaller by shifting the sampling instant, which can be defined as SSSU_SIS and DSDU_SIS (see Fig. 3) [46]. Therein, T_{cp} is the practical code implementation time that is set to mT_{sw}, the control delay, and the dissipative region for the SSSU_SIS PWM and DSDU_SIS PWM are given as follows.

$$T_{d\_SSSU\_SIS} = \underbrace{T_{cp}}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} = (m+0.5)T_{sw} \tag{14}$$

$$f_{dissipative\_SSSU\_SIS} = (0, \frac{1}{4m+2} f_{sw}) \tag{15}$$

$$T_{d\_DSDU\_SIS} = \underbrace{T_{cp}}_{\text{computation delay}} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} = (m+0.25)T_{sw} \tag{16}$$

$$f_{dissipative\_DSDU\_SIS} = (0, \frac{1}{4m+1} f_{sw}) \tag{17}$$

Note that the SSSU_SIS PWM and the DSDU_SIS PWM depend on the code implementation time T_{cp}. If m is small enough, the critical frequency for the SSSU_SIS PWM and the DSDU_SIS PWM will be close to $0.5f_{sw}$ and f_{sw}, respectively. However, there is a trade-off between the control delay reduction and the aliasing suppression. Because the non-average value is sampled and the low-order aliased harmonics will be introduced in the grid-side current [5, 47-48]. When m is set to 0.25, the aliased harmonics are minimized and the dissipative region for the DSDU_SIS is in the interval of $(0, \frac{1}{2}f_{sw})$. In addition, when m is set to 0.5 for the SSSU_SIS PWM, the computation delay is reduced from T_{sw} to $0.5T_{sw}$. As a result, the dissipative region is in the interval of $(0, \frac{1}{4} f_{sw})$ and no switching noise is introduced.

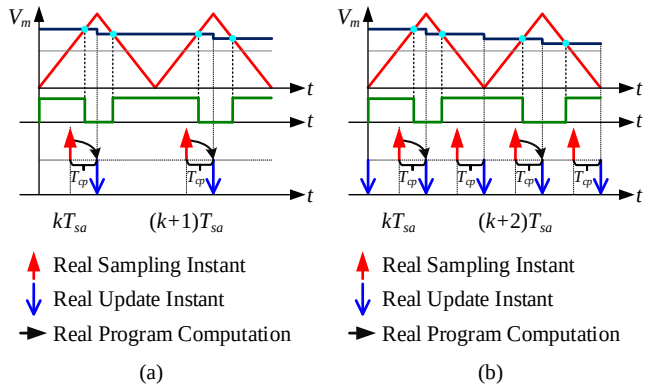


Fig. 3. Conventional digital PWM with the sampling instant shift. (a) Single-update PWM with the sampling instant shift, (b) Double-update PWM with the sampling instant shift.

3) With Update Instant Shift

In addition to shifting the sampling instant, shifting the update instant is an alternative option to reduce the control

delay [49]. As shown in Fig. 4(a), the sampling instant is located at the valley of the carrier, and the duty cycle is updated immediately when the calculation is finished. Based on the voltage-second balance principle, the equivalent update instant is located at the valley of the carrier. Hence, the computation delay is zero and only the PWM delay is left. However, when the duty cycle is close to zero, the updated duty cycle cannot produce an effective voltage pulse. It can be seen from Fig. 4(b) that the equivalent update instant is located at the peak of the carrier, and the computation delay changes from zero to $0.5T_{sw}$.

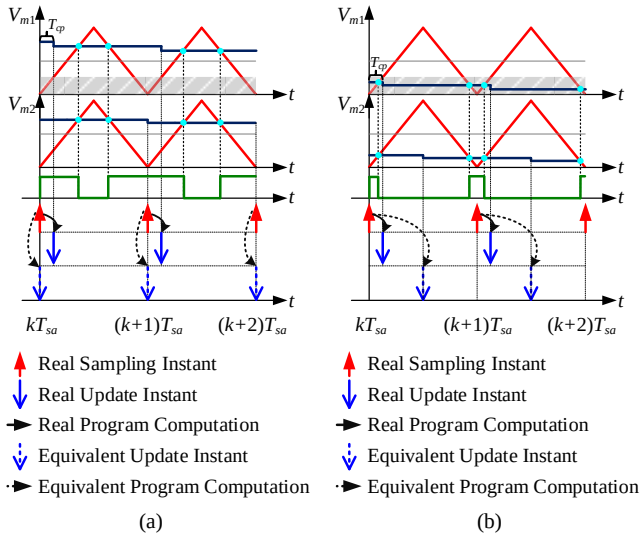


Fig. 4. Single-valley-sampling digital PWM with the update instant shift. (a) Without the duty cycle limitation, (b) With the duty cycle limitation.

According to the property of the similar triangles, the critical duty cycle considering the code implementation time is given in (18).

$$d_{cri} = \frac{2T_{cp}}{T_{sw}} \tag{18}$$

The control delay and the dissipative region for single-valley sampling PWM with the update instant shift (SVS_UIS) are given in (19)-(20). The control delay for the SVS_UIS PWM is a piecewise function, which jeopardizes the system stability when the duty cycle is smaller than the critical duty cycle. The solution can be reducing the code implementation time, improving the dc-link voltage and limiting the minimum output duty cycle, which increases the overall cost and constraints the application range.

$$\begin{cases} T_{d\_SVS\_UIS} = \underset{\text{computation delay}}{0} + \underset{\text{PWM delay}}{0.5T_{sw}} = 0.5T_{sw} & d \ge d_{cri} \\ T_{d\_SVS\_UIS} = \underset{\text{computation delay}}{0.5T_{sw}} + \underset{\text{PWM delay}}{0.5T_{sw}} = T_{sw} & d < d_{cri} \end{cases} \tag{19}$$

$$\begin{cases} f_{dissipative\_SVS\_UIS} = (0, \frac{1}{2} f_{sw}) & d \ge d_{cri} \\ f_{dissipative\_SVS\_UIS} = (0, \frac{1}{4} f_{sw}) & d < d_{cri} \end{cases} \tag{20}$$

Similarly, when using the single-peak-sampling with the update instant considering the code implementation time is given in (21). When the duty cycle is larger than the critical duty cycle, the control delay increases twice and the dissipative

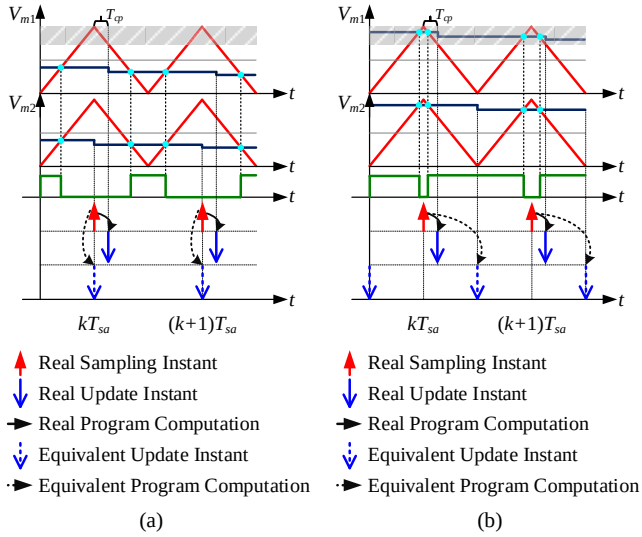


Fig. 5. Single-peak-sampling digital PWM with the update instant shift. (a) Without the duty cycle limitation, (b) With the duty cycle limitation.

region shrinks a half as given in (22) and (23). For both the SVS_UIS PWM and the SPS_UIS PWM, no switching noise is introduced.

$$d_{cri} = 1 - \frac{2T_{cp}}{T_{sw}} \tag{21}$$

$$\begin{cases} T_{d\_SPS\_UIS} = \underset{\text{computation delay}}{0} + \underset{\text{PWM delay}}{0.5T_{sw}} = 0.5T_{sw} & d \le d_{cri} \\ T_{d\_SPS\_UIS} = \underset{\text{computation delay}}{0.5T_{sw}} + \underset{\text{PWM delay}}{0.5T_{sw}} = T_{sw} & d > d_{cri} \end{cases} \tag{22}$$

$$\begin{cases} f_{dissipative\_SPS\_UIS} = (0, \frac{1}{2} f_{sw}) & d \le d_{cri} \\ f_{dissipative\_SPS\_UIS} = (0, \frac{1}{4} f_{sw}) & d > d_{cri} \end{cases} \tag{23}$$

Combining the PWM methods in Fig. 4(a) and Fig. 5(a), the duty cycle limitation can be removed by switching the sampling point [50]. As shown in Fig. 6, the sampling instant is located at the valley of the carrier when the modulation signal is in the positive half cycle, while it is shifted to the peak of the carrier when the modulation signal is in the negative half cycle. Consequently, the control delay and the dissipative region for the single-sampling without the duty cycle limitation (SS_WDCL) are given in (24) and (25). Compared with the DSDU_SIS in [5], the SS_WDCL has the same control delay and no aliased low-order harmonics exist. Based on the area equivalence and single-sampling, the control delay can also be reduced to $0.5T_{sw}$ but the output duty cycle is still limited [51-52].

$$T_{d\_SS\_WDRL} = \underset{\text{computation delay}}{0} + \underset{\text{PWM delay}}{0.5T_{sw}} = 0.5T_{sw} \tag{24}$$

$$f_{dissipative\_SS\_WDRL} = (0, \frac{1}{2} f_{sw}) \tag{25}$$

Shifting the update instant can be used in the DSDU PWM as well [6-7]. As shown in Fig. 7(a), when the duty cycle is not limited, the equivalent update instant is located at the same position with the sampling point. As a result, the computation

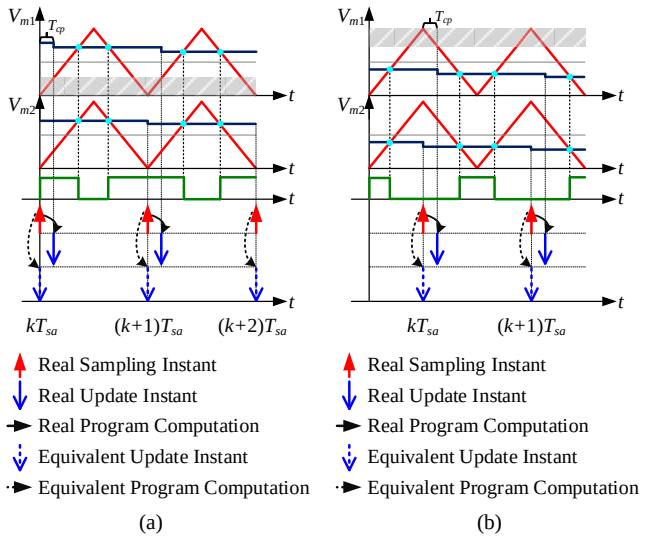


Fig. 6. Single-sampling digital PWM without duty cycle limitation. (a) Positive half cycle, (b) Negative half cycle.

delay is zero and only the PWM delay is left. On the other hand, when the duty cycle is limited (see Fig. 7(b)), it changes back to SPS_UIS in the positive half cycle and to SVS_UIS in the negative half cycle. The control delay and the dissipative region for the double-sampling PWM with the update instant shift (DS_UIS) are given in (26) and (27).

$$\begin{cases} T_{d\_DS\_UIS} = \underbrace{0}_{\text{computation delay}} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} = 0.25T_{sw} & \dfrac{2T_{cp}}{T_{sw}} \le d \le 1-\dfrac{2T_{cp}}{T_{sw}} \\ T_{d\_DS\_UIS} = \underbrace{0}_{\text{computation delay}} + \underbrace{0.5T_{sw}}_{\text{PWM delay}} = 0.5T_{sw} & others \end{cases} \tag{26}$$

$$\begin{cases} f_{dissipative\_DS\_UIS} = (0,\ f_{sw}) & \dfrac{2T_{cp}}{T_{sw}} \le d \le 1-\dfrac{2T_{cp}}{T_{sw}} \\ f_{dissipative\_DS\_UIS} = (0,\ \dfrac{1}{2} f_{sw}) & others \end{cases} \tag{27}$$

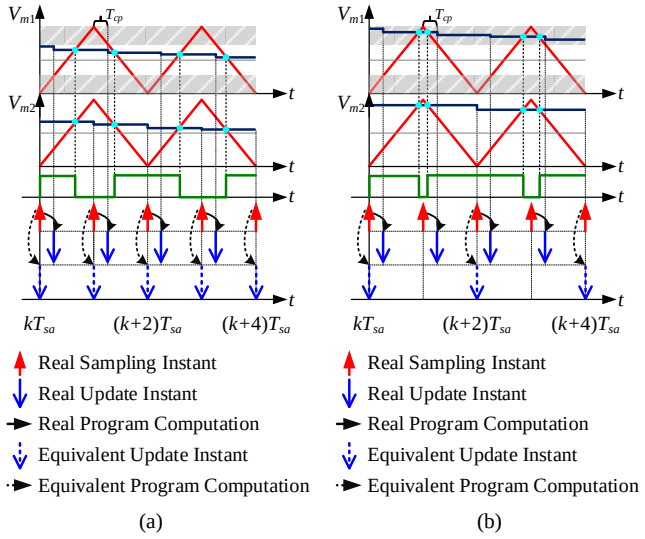


Fig. 7. Double-sampling digital PWM with the update instant shift. (a) Without the duty cycle limitation, (b) With the duty cycle limitation.

In terms of the aliasing and the control delay, the DS_UIS PWM is the best choice among conventional single/double-sampling methods when the computation time is short enough. Based on (26), the allowed output duty cycle can be up to 0.98 only if T_{cp} is $0.005T_{sw}$. Especially, if T_{cp} is equal to $0.25T_{sw}$, the DS_UIS is the same as the SS_WDCL.

B. Control Delay Using Multi-Sampling PWM

1) General Multi-Sampling PWM

The multi-sampling multi-update (MSMU) PWM is a potential candidate to reduce the control delay, and the state variable is sampled and the duty cycle is updated multiple times within a switching period. The control delay is inversely proportional to the sampling rate N [11, 53] and it is given as

$$T_{d\_MSMU} = \frac{1.5T_{sw}}{N} \tag{28}$$

Taking four-sampling four-update PWM as an example, as shown in Fig. 8, not every duty cycle will intersect with the carrier and produce an effective pulse pattern.

In the positive half cycle (see Fig. 8(a)), D_2 and D_3 are the effective duty cycle. Based on the voltage-second balance principle, the duration time of the effective duty cycle can be extended to half of one switching period. As a result, the four-sampling PWM can be transformed into a DSDU PWM with the sampling instant shift and the update instant shift. The equivalent computation delay for D_2 is zero, and the equivalent update instant is the same as the sampling instant [14]. Besides, there is a $0.25T_{sw}$ equivalent computational delay for the duty cycle D_3. The average computational delay in one switching period is $(0.25+0)/2=0.125T_{sw}$. Considering the double-sampled PWM delay of $0.25T_{sw}$, the total control delay is $0.375T_{sw}$, which is consistent with the multi-sampling delay $1.5T_{sw}/4$. Similarly, the effective duty cycles in the negative half cycle are D_1 and D_4, as shown in Fig. 8(b). The equivalent computation delay for D_1 and D_4 are $0.25T_{sw}$ and zero, respectively, and the total control delay is equal to $1.5T_{sw}/4$.

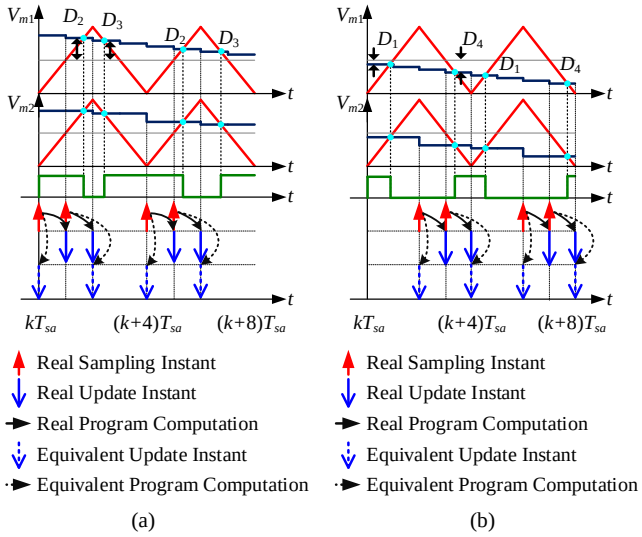


Fig. 8. General multi-sampling digital PWM with the same sampling instant and update instant. (a) Positive half cycle, (b) Negative half cycle.

Similarly, when the sampling rate is higher, e.g., N=8, the eight-sampling PWM can be transformed into a DSDU PWM with the sampling instant shift and the update instant shift [14]. The core principle for the MSMU PWM in reducing control delay is the smaller computation delay, and the PWM delay is always equal to $0.25T_{sw}$. Therefore, a more specific control delay expression for the MSMU PWM is

$$T_{d\_MSMU} = \underbrace{\frac{6-N}{4N}T_{sw}}_{\text{computation delay}} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} = \frac{1.5T_{sw}}{N} \tag{29}$$

It can be seen from (29) that when the sampling rate N is larger than six, the computation delay will be negative, which leads to a phase-leading. For example, the computation delay is $-0.0625T_{sw}$ when the sampling rate is eight and a detailed analysis can be found in [14]. Substituting (29) into (9), the dissipative region for the MSMU PWM is given in (30). Moreover, the dissipative region can be extended to switching frequency when the sampling rate N is equal to or larger than six.

$$f_{dissipative\_MSMU} = (0, \frac{N}{6} f_{sw}) \tag{30}$$

In addition, the multi-sampling single-update (MSSU) PWM and the multi-sampling double-update (MSDU) PWM are also a kind of alternatives, and the multiple intersections between the modulation signal and the carrier can be avoided [54-56]. As a result, the control delay is the same with the SSSU_SIS and the DSDU_SIS. However, the switching noise will be introduced when using the multi-sampling, as the average value can only be sampled at the peak/valley point of the carrier for a two-level inverter or a DC-DC converter. One typical method is to use an anti-aliasing filter but the extra delay will be introduced, which will be discussed in Section III.A.

2) Multi-Sampling PWM for Multi-Level Converters

Multi-level converter with phase-shifted PWM modulation is a good application, and no switching noise is introduced if selecting the multi-sampling rate properly. For a single-phase H-bridge inverter, the carriers are interleaved with 180°, respectively. As shown in Fig. 9, the apparent switching frequency is twice larger than the preset switching frequency. Hence, it is natural to sample four times within one switching period including the peak/valley points and the intersection points of the carriers [21]. In particular, four-sampling four-update control for a single-phase H-bridge inverter can also be regarded as a double-sampling control with a double preset switching frequency. Hence, the control delay is given in (29) where T_{sw_ap} is the apparent switching period.

$$\begin{aligned} T_{d\_4S4U} &= \underbrace{\frac{T_{sw}}{4}}_{\text{computation delay}} + \underbrace{\frac{T_{sw}}{8}}_{\text{PWM delay}} = \frac{1.5T_{sw}}{4} \\ &= \underbrace{\frac{T_{sw\_ap}}{2}}_{\text{computation delay}} + \underbrace{\frac{T_{sw\_ap}}{4}}_{\text{PWM delay}} = \frac{1.5T_{sw\_ap}}{2} \end{aligned} \tag{31}$$

More generally, for a cascaded H-bridge (CHB) inverter, the apparent switching frequency is $2Mf_{sw}$ where M is the number of cascaded cells. The optimum multi-sampling rate is $4M$ without introducing switching noise, and the control delay is given in (32).

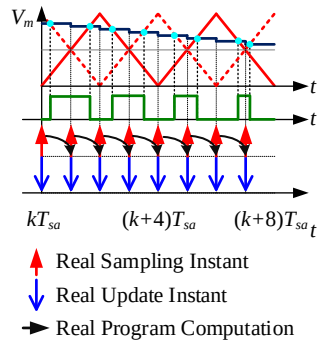


Fig. 9. Multi-level converter based multi-sampling digital PWM with the same sampling instant and update instant.

$$\begin{aligned} T_{d\_MSMU\_CHB} &= \underbrace{\frac{T_{sw}}{4M}}_{\text{computation delay}} + \underbrace{\frac{T_{sw}}{8M}}_{\text{PWM delay}} = \frac{1.5T_{sw}}{4M} \\ &= \underbrace{\frac{T_{sw\_ap}}{2}}_{\text{computation delay}} + \underbrace{\frac{T_{sw\_ap}}{4}}_{\text{PWM delay}} = \frac{1.5T_{sw\_ap}}{2} \end{aligned} \tag{32}$$

Recalling (29), multi-sampling control of the CHB inverter and the HB inverter can reduce the computation delay and the PWM delay at the same time instead of reducing the computation delay only [22, 57]. Again, if seen from the apparent switching period perspective, the control delay is the same with DSDU PWM. Substituting (32) into (9), the dissipative region in terms of the cascaded cells is given in (33). The region below the switching frequency can be made dissipative when the number of cascaded cells is equal to or larger than two, but the dissipative region cannot be extended based on the apparent switching frequency f_{sw_ap}.

$$\begin{aligned} f_{dissipative\_MSMU\_CHB} &= (0, \frac{2M}{3} f_{sw}) \\ &= (0, \frac{1}{3} f_{sw\_ap}) \end{aligned} \tag{33}$$

Similar to the DS_UIS PWM in Fig. 7, the update instant can be also shifted for the multi-sampling PWM to further reduce the control delay [58]. For a single-phase HB inverter, the average current can be sampled at the peak/valley points and the intersection points of the phase-shifted carriers, and two control modes are switched based on the amplitude of the duty cycle. As shown in Fig. 10(a), when the duty cycle is in the interval of $[\frac{2T_{cp}}{T_{sw}}, 1-\frac{2T_{cp}}{T_{sw}}]$, the sampling point is located at the peak/valley points of the carriers, and the duty cycle is updated immediately after the calculation is finished. Similarly, when the duty cycle is not in the interval, the sampling point is switched to the intersection points of the carriers (see Fig. 10(b)). As a result, the computation delay is zero and only the PWM delay is left. The control delay for the multi-sampling PWM with the update instant shift (MS_UIS) is $T_{sw}/4$, and no switching noise is introduced.

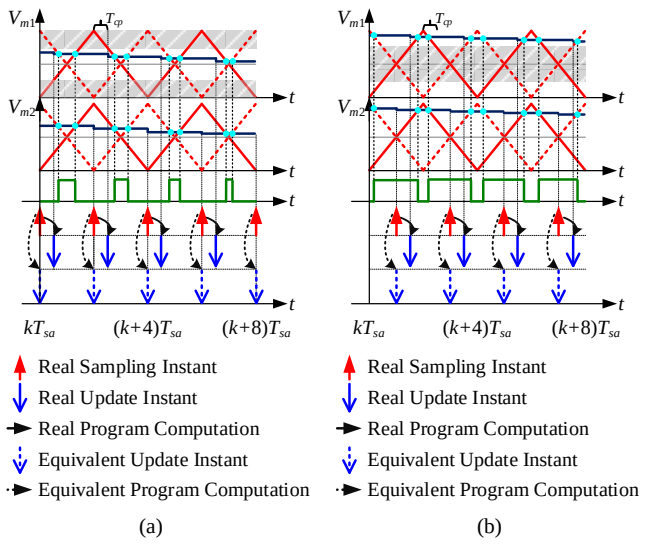


Fig. 10. Multi-sampling digital PWM with the update instant shift. (a) Sampling at the peak/valley points of the carriers, (b) Sampling at the intersection points of the carriers.

However, the computation time for the MS_UIS should be lower than $T_{sw}/8$ according to the geometric relationship in Fig. 10, which presents a higher demand for the microprocessors compared with the four-sampling four-update control. Generally, for a CHB inverter with M cells, there will be $2M$ control modes [59]. The control delay and the dissipative region are given in (34) and (35). Similarly, seen from an apparent switching period perspective, the control delay for MS_UIS for HB inverter and MS_UIS for CHB inverter is the same with SS_WDCL PWM. Hence, the sampling rate selction for multi-level converters should be further researched.

$$\begin{aligned} T_{d\_MS\_UIS\_CHB} &= \underbrace{0}_{\text{computation delay}} + \underbrace{\frac{T_{sw}}{4M}}_{\text{PWM delay}} = \frac{T_{sw}}{4M} \\ &= \underbrace{0}_{\text{computation delay}} + \underbrace{\frac{T_{sw\_ap}}{2}}_{\text{PWM delay}} = \frac{T_{sw\_ap}}{2} \end{aligned} \tag{34}$$

$$\begin{aligned} f_{dissipative\_MS\_UIS\_CHB} &= (0, Mf_{sw}) \\ &= (0, \frac{1}{2} f_{sw\_ap}) \end{aligned} \tag{35}$$

C. Comparison

To evaluate the performance of the prior art, several indexes are used, i.e., control delay, dissipative region, aliasing, duty cycle limitation, and maximum allowed computation time. As shown in Table I, SS_WDCL PWM is the best one among single-sampling PWM methods. Specifically, by combining the update instant shift and the sampling instant shift, the control delay can be reduced to $0.5T_{sw}$. Moreover, not only the aliasing and the duty cycle limitation are removed, but also the maximum allowed computation time is acceptable (T_{cp}=$0.25T_{sw}$).

When using double-sampling, as shown in Table II, the control delay for the DSDU_SIS PWM (m=0.25) can be also reduced to $0.5T_{sw}$, but the extra aliasing is introduced compared with the SS_WDCL PWM. By shifting the update instant for double-sampling PWM, the control delay can be further reduced to $0.25T_{sw}$, which is a big advantage compared with SS_WDCL PWM. However, the duty cycle is limited otherwise the computation time is small enough to be ignored.

Considering the multi-sampling PWM in Table III, an anti-aliasing filter is required to remove the sampled switching harmonics, i.e., MSMU PWM with an anti-aliasing filter. Although an extra control delay $0.25T_{sw}$ is introduced compared with MSMU PWM, the total control delay is still lower than SS_WDCL PWM when the sampling rate is larger than six. Seen from an apparent switching frequency perspective, the control delay for 4S4U for HB inverter and MSMU for CHB inverter is the same as the DSDU PWM. Similarly, the control delay for MS_UIS for HB inverter and MS_UIS for CHB inverter is the same with SS_WDCL PWM.

To summarize, SS_WDCL PWM, DS_UIS PWM, and MSMU PWM with an anti-aliasing filter are possible candidates. Then the selection principle based on the computation time is given as follows.

1) If T_{cp}≤$0.005T_{sw}$, choose DS_UIS PWM where T_d=$0.25T_{sw}$ and d∈(0.01, 0.99);
2) If $0.005T_{sw}$<T_{cp}<$T_{sw}/6$, choose MSMU with an anti-aliasing filter where $0.25T_{sw}$<T_d<$0.5T_{sw}$ and d∈(0, 1);
3) If $T_{sw}/6$≤T_{cp}≤$0.25T_{sw}$, choose SS_WDCL PWM where T_d=$0.5T_{sw}$ and d∈(0, 1).

TABLE I
COMPARISON AMONG VARIOUS SINGLE-SAMPLING PWM

Modulation methods / Index	SSSU[44-45] (see Fig. 2(a))	SSSU_SIS[46-48] (see Fig. 3(a))			SVS_UIS[49] (see Fig. 4)	SPS_UIS[49] (see Fig. 5)	SS_WDCL[50] (see Fig. 6)
Control delay	$\frac{3}{2}T_{sw}$	$(m+\frac{1}{2})T_{sw}$	$T_{sw}(m=\frac{1}{2})$	$\frac{3}{4}T_{sw}(m=\frac{1}{4})$	$\frac{1}{2}T_{sw}$	$\frac{1}{2}T_{sw}$	$\frac{1}{2}T_{sw}$
Dissipative region	$(0, \frac{1}{6} f_{sw})$	$(0, \frac{1}{4m+2} f_{sw})$	$(0, \frac{1}{4} f_{sw})$	$(0, \frac{1}{3} f_{sw})$	$(0, \frac{1}{2} f_{sw})$	$(0, \frac{1}{2} f_{sw})$	$(0, \frac{1}{2} f_{sw})$
Aliasing	No	Large when $m\neq \frac{1}{2}$ or $\frac{1}{4}$	No	Small	No	No	No
Duty cycle limitation	No	No	No	No	Yes	Yes	No
Maximum allowed computation time	T_{sw}	mT_{sw}	$\frac{1}{2}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$

SSSU: single-sampling single-update, SSSU_SIS: single-sampling single-update with the sampling instant shift, SVS_UIS: single-valley-sampling with the update instant shift, SPS_UIS: single-peak-sampling with the update instant shift, SS_WDCL: single-sampling without the duty cycle limitation.

TABLE II
COMPARISON AMONG VARIOUS DOUBLE-SAMPLING PWM

Modulation methods / Index	DSDU[44-45] (see Fig. 2(b))	DSDU_SIS[5] (see Fig. 3(b))		DS_UIS[6-7] (see Fig. 7)
Control delay	$\frac{3}{4}T_{sw}$	$(m+\frac{1}{4})T_{sw}$	$\frac{1}{2}T_{sw}(m=\frac{1}{4})$	$\frac{1}{4}T_{sw}$
Dissipative region	$(0, \frac{1}{3}f_{sw})$	$(0, \frac{1}{4m+1}f_{sw})$	$(0, \frac{1}{2}f_{sw})$	$(0, f_{sw})$
Aliasing	No	Large when $m\neq\frac{1}{4}$	Small	No
Duty cycle limitation	No	No	No	Yes
Maximum allowed computation time	$\frac{1}{2}T_{sw}$	mT_{sw}	$\frac{1}{4}T_{sw}$	$\frac{1}{8}T_{sw}$

DSDU: double-sampling double-update, DSDU_SIS: double-sampling double-update with the sampling instant shift, DS_UIS: double-sampling with the update instant shift.

TABLE III
COMPARISON AMONG VARIOUS MULTI-SAMPLING PWM

Modulation methods / Index	MSMU[11, 53] (see Fig. 8)	MSMU with an anti-aliasing filter[14, 34] (see Fig. 12)	MSSU[55] (same with Fig. 3(a))	MSDU[56] (same with Fig. 3(b))	4S4U for HB inverter [21] (see Fig. 9)	MSMU for CHB inverter [22] (similar with Fig. 9)	MS_UIS for HB inverter [58] (see Fig. 10)	MS_UIS for CHB inverter [59] (similar with Fig. 10)
Control delay	$\frac{1.5}{N}T_{sw}$	$(\frac{1.5}{N}+\frac{1}{4})T_{sw}$	$(\frac{1}{N}+\frac{1}{2})T_{sw}$	$(\frac{1}{N}+\frac{1}{4})T_{sw}$	$\frac{1.5}{4}T_{sw}$ ⇕ $\frac{1.5}{2}T_{sw\_eq}$	$\frac{1.5}{4M}T_{sw}$ ⇕ $\frac{1.5}{2}T_{sw\_eq}$	$\frac{1}{4}T_{sw}$ ⇕ $\frac{1}{2}T_{sw\_eq}$	$\frac{1}{4M}T_{sw}$ ⇕ $\frac{1}{2}T_{sw\_eq}$
Dissipative region	$(0, \frac{N}{6}f_{sw})$	$(0, \frac{N}{6+N}f_{sw})$	$(0, \frac{N}{4+2N}f_{sw})$	$(0, \frac{N}{4+N}f_{sw})$	$(0, \frac{2}{3}f_{sw})$ ⇕ $(0, \frac{1}{3}f_{sw\_ap})$	$(0, \frac{2M}{3}f_{sw})$ ⇕ $(0, \frac{1}{3}f_{sw\_ap})$	$(0, f_{sw})$ ⇕ $(0, \frac{1}{2}f_{sw\_ap})$	$(0, Mf_{sw})$ ⇕ $(0, \frac{1}{2}f_{sw\_ap})$
Aliasing	Yes	No	Yes	Yes	No	No	No	No
Duty cycle limitation	No	No	No	No	No	No	No	No
Maximum allowed computation time	$\frac{1}{N}T_{sw}$	$\frac{1}{N}T_{sw}$	$\frac{1}{N}T_{sw}$	$\frac{1}{N}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4M}T_{sw}$	$\frac{1}{8}T_{sw}$	$\frac{1}{8M}T_{sw}$

MSMU: multi-sampling multi-update, IRF: improved repetitive filter, MRF: modified repetitive filter, MSSU: multi-sampling single-update, MSDU: multi-sampling double-update, HB: H-bridge, CHB: cascaded H-bridge, MS_UIS: multi-sampling with the update instant shift.

III. MULTI-SAMPLING CONTROL STRATEGIES AND PRACTICAL IMPLEMENTATION

A. Aliasing Suppression

1) With Anti-Aliasing Filters

In the past decades, linear controllers based on the PWM have been the most popular control methods due to their simpleness in the implementation, the parameter design, and the stability analysis [60-62]. Moreover, the multi-sampling PWM is an extension of the conventional PWM, and the linear controllers can be easily updated using a higher sampling frequency.

When using a multi-sampled linear controller with the PWM, however, the switching harmonics are introduced which affects the control performance. Specifically, the multi-sampling PWM is equivalent to a double-sampling PWM with the sampling instant shift and the update instant shift, and the equivalent Nyquist frequency is equal to the switching frequency. According to Fig. 8, the non-average value is sampled at least once within one switching period, which causes the aliased low-order harmonics. Besides the four-sampling PWM, a same conclusion can be acquired using a higher samping rate. For example, eight-sampling PWM analysis can be found in [14], and the aliasing is still severe due to the sampled switching harmonics. The frequency domain based aliasing analysis method in the DSDU_SIS PWM can be used directly for the MSMU PWM, where the aliased harmonics is regarded as an additional aliasing disturbing source in the control loop [48]. For example, for the current control of LCL-filtered inverters, the aliased disturbance can be added after the multi-sampled feedback variables such as the inverter-side current, grid-side current, filter capacitor voltage, etc. Similarly, the low-order aliasing phenomenon also exists in the multi-sampled voltage control of DC-DC converters. Hence, using an anti-aliasing filter to remove the sampled switching harmonics is necessary, which can suppress the aliasing and make the analytical modelling match with the simulation results [14, 15, 63]. In order to remove the sampled high frequency switching harmonics, various repetitive filters (RFs) are proposed based on internal model principle. The most effective RF is the moving average filter (MAF) with a window equal to one switching period [64], as shown in (36).

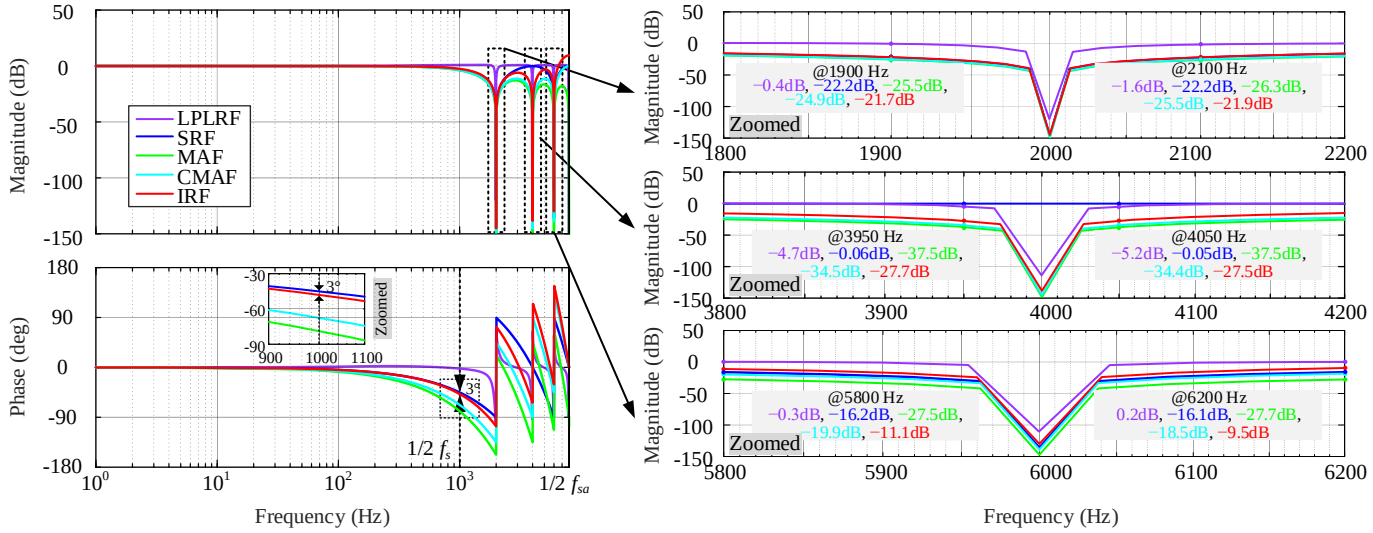


Fig. 11. Bode diagram of the repetitive filters based on eight-sampling (LPLRF: low-phase-lag repetitive filter, SRF: simplified repetitive filter, MAF: moving average filter, CMAF: compromised moving averaging filter, IRF: improved repetitive filter).

But the MAF introduces a delay equal to $T_{sw}/2$, thus losing the advantage on the phase boost. Since the sampled switching harmonics for a DC-DC converter are at the integral switching frequency, a low-phase-lag RF (LPLRF) is proposed which is given in (37) [13]. To reduce the calculation complexity, a simplified RF (SRF) is proposed, as shown in (38) [16]. For a two-level three-phase inverter, the multi-sampled switching harmonics are at the side switching frequency. As shown in Fig. 11, the LPLRF cannot remove the sampled even-order and odd-order switching harmonics, and the SRF cannot remove the sampled odd-order switching harmonics.

Therefore, a compromised moving average filter (CMAF) is proposed, and the size of the window reduces from one to half of the switching period, as shown in (39). However, there is still a delay from the CMAF compared with the SRF, hence a linear delay compensation block is inserted after the CMAF, i.e., improved repetitive filter (IRF), as shown in (40) [14]. The IRF can remove the even-order and odd-order switching harmonics, but also has a similar phase lag with the SRF. Moreover, when the sampling rate is higher, e.g., N=50, IRF will amplify the sampled high-frequency harmonics [34]. As shown in (41), a modified repetitive filter (MRF) should be used where r is the attenuation factor.

$$MAF(z)=\frac{1}{N}\sum_{k=0}^{N-1}z^{-k} \tag{36}$$

$$LPLRF(z)=\frac{(1+0.25)(1-(z^{-N}-\frac{1}{N}\sum_{n=1}^{N}z^{-n}))}{1-(z^{-N}-\frac{1}{N}\sum_{n=1}^{N}z^{-n})+0.25}\approx 1 \tag{37}$$

$$SRF(z)=\frac{1}{2}(1+z^{-N/2})\approx z^{-N/4} \tag{38}$$

$$CMAF(z)=\frac{2}{N}(1+z^{-2}+z^{-4}+\cdots z^{-(N-2)}) \tag{39}$$

$$IRF(z)=\frac{2}{N}(1+z^{-2}+z^{-4}+\ldots z^{-(N-2)})\times(3\log_2 N-7-(3\log_2 N-8)z^{-1}) \tag{40}$$

$$MRF(z)=\frac{2}{N}(1+z^{-2}+z^{-4}+\ldots z^{-(N-2)})\times\frac{(1-r^8)}{(1-r^2)}\frac{(1-r^2z^{-2})}{(1-r^8z^{-8})} \tag{41}$$

On the other hand, the IRF has a similar control delay with the SRF that is equal to one quarter of switching period, the total control delay including the computation delay, PWM delay and IRF delay is

$$T_{d\_MS\_IRF/MRF}=\underbrace{\frac{6-N}{4N}T_{sw}}_{\text{computation delay}}+\underbrace{0.25T_{sw}}_{\text{PWM delay}}+\underbrace{0.25T_{sw}}_{\text{IRF/MRF delay}}=\frac{6+N}{4N}T_{sw} \tag{42}$$

When the sampling rate N is infinite, the control delay is close to $1/4T_{sw}$ and the dissipative region is

$$f_{dissipative\_MS\_IRF/MRF}=(0,\frac{N}{6+N}f_{sw}) \tag{43}$$

Consequently, the dissipative region and the loop delay using the multi-sampling control strongly depend on the inserted digital filter. Therefore, in order to fully take advantage of the multi-sampling control, how to remove the sampled switching harmonics with less phase lag becomes an important issue.

2) With Changed Carrier or Sampling Process

Based on the single-edge modulator, the multi-sampled SHs can be compensated through an offline pre-distorted carrier. As shown in Fig. 12(a), the switching harmonics are produced from the comparison process between the modulation signal and the carrier, which can be compensated through the feedforward of the carrier. Moreover, Fig. 12(a) can be equivalently transformed into Fig. 12(b), where a series combination of $G_i(s)$ and the plant model is inserted after the carrier. As a result, a new carrier can be done offline, which is stored in a look-up table [17-18]. However, the double-edge modulator is more general, and the compensation strategy for the single-edge modulator cannot be used directly.

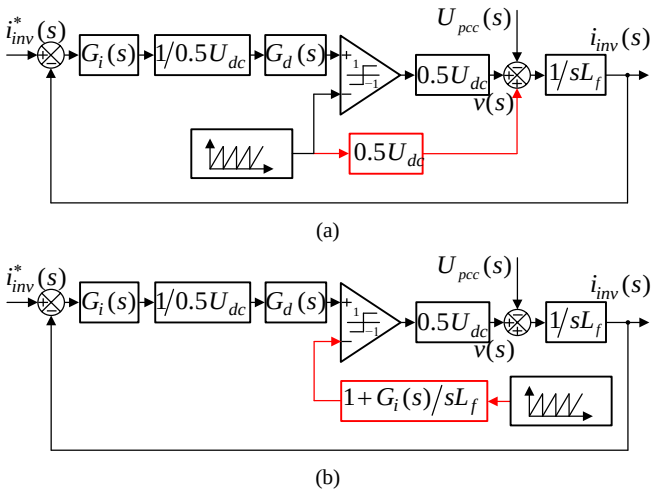


Fig. 12. Single edge modulator with ripple compensation. (a) Carrier feedforward, (b) Equivalent transformation.

By replacing the zero-order hold (ZOH) with the first-order hold (FOH) in the sampling process, the modulation signal is more like a continuous signal using the MSMU PWM. The arbitrary sampling rate can be used with the improved harmonic performance, linearity, and phase delay compared with the ZOH sampler [19-20]. The transfer functions of the FOH and the ZOH are

$$FOH(s) = \left(\frac{1-e^{-sT_{sa}}}{sT_{sa}}\right)^2 (1+sT_{sa}) \tag{44}$$

$$ZOH(s) = \frac{1-e^{-sT_{sa}}}{sT_{sa}} \tag{45}$$

It can be seen from Fig. 13 that the FOH has a larger amplitude response at high frequency compared with the ZOH, which may affect the small-signal stability and amplify the high-frequency noise. Hence, the analysis and controller design using first-order hold sampled still need to be further studied.

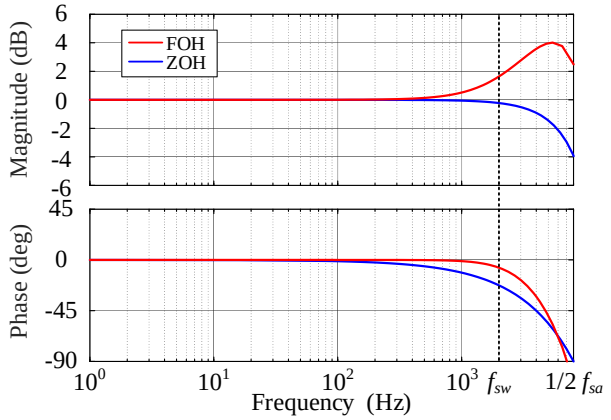


Fig. 13. Bode diagram of the zero-order hold and the first-order hold.

B. *Control of Multi-Cell Converters*

In addition, noise-free sampling can be achieved for the multi-parallel/series multi-cell converters with the phase-shifted modulation. For the cascaded H-bridge inverter and modular multi-level converter, the sampling rate can be four times higher than the number of cells, i.e., the sampling point is

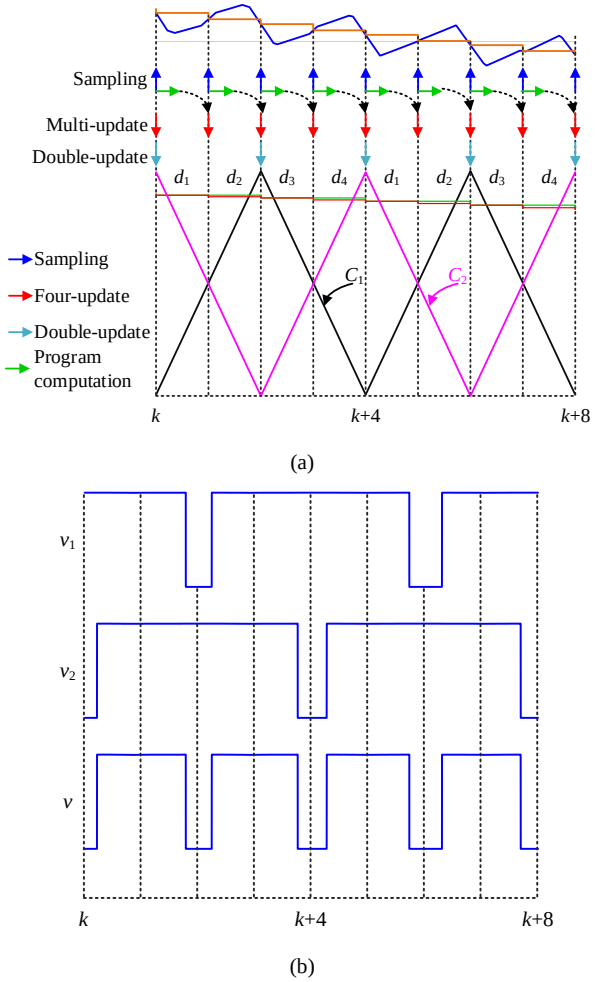


Fig. 14. Multi-sampling control principle of two-cell interleaved three-phase inverters. (a) Sampling process and modulation, (b) Pulse pattern.

located at the intersection point and the peak/valley point of the carrier [22, 54, 57, 67]. On the other hand, for a multi-cell interleaved converter, the sampling rate and the update rate cannot be the same. This is because the average output voltage for every single cell is different, which leads to the circulating current among cells [23]. Taking a two-cell interleaved inverter as an example, the sampling rate can be set to four when sampling the PCC current, as shown in Fig. 14 [68].

If updating four times within one switching period, the average output voltage in the positive half cycle is

$$\begin{cases} i_{inv1}(k+4) - i_{inv1}(k) = L_{c1}(d_2+d_3)\dfrac{u_{dc}}{2} \\ i_{inv2}(k+4) - i_{inv2}(k) = L_{c2}(d_1+d_4)\dfrac{u_{dc}}{2} \end{cases} \tag{46}$$

where i_{inv1}~i_{inv2}, L_{c1}~L_{c2}, d_1~d_4, u_{dc} are single-phase inverter-side current for the first- and second-cell, inverter-side inductance for the first- and second-cell, four updated duty cycles within a switching period, dc-link voltage, respectively. As a result, a low frequency circulating component appears in the inverter-side currents for every single cell if the non-ideal factors such as filter-inductance variation and dead-time effect are ignored. If updating twice within one switching period, the average output

voltage for every single cell is same, as shown in (47). Hence, the four-sampling double-update mode is recommended.

$$\begin{cases} i_{inv1}(k+4)-i_{inv1}(k)=L_{c1}(d_1+d_3)\dfrac{u_{dc}}{2} \\ i_{inv2}(k+4)-i_{inv2}(k)=L_{c2}(d_1+d_3)\dfrac{u_{dc}}{2} \end{cases} \tag{47}$$

The control delay and dissipative region for the two-cell interleaved inverter is

$$T_{d\_MS\_interleaved}=\underbrace{0.25T_{sw}}_{\text{computation delay}}+\underbrace{0.25T_{sw}}_{\text{PWM delay}}=0.5T_{sw} \tag{48}$$

$$f_{dissipative\_MS\_interleaved}=(0,\,0.5f_{sw}) \tag{49}$$

It can be seen from (48) and (49) that the stability is weakened compared with the single-phase H-bridge inverter in (33). Moreover, when the number of interleaved cells improves, the configuration of the sampling rate and the update rate will be more complicated.

C. Multi-Sampled Digital Controller

The digital derivative is often required in the control of power electronic converters, and the first-order and second-order forms are given in (50)-(51) [69]. The bode plot using double-sampling is given in Fig. 16(a). However, compared with the ideal ''s'' function, there is a large deviation for the amplitude-frequency characteristic and the phase-frequency characteristic close to the switching frequency. Multi-sampling

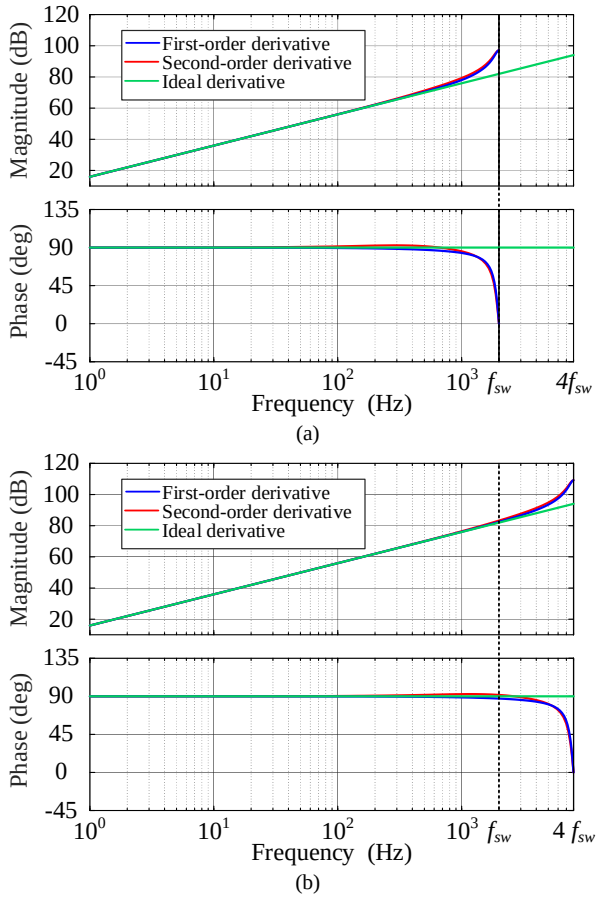


Fig. 15. Comparison between double-sampling derivative and multi-sampling derivative. (a) Double-sampling derivative, (b) Multi-sampling derivative.

can effectively reduce the phase lag and make the digital derivative more accurate [24]. For example, when the sampling frequency is eight times higher than the switching frequency, as shown in Fig. 16(b), the multi-sampling derivative can emulate the characteristic of the ideal derivative accurately below the switching frequency.

$$G_{first-order}(z)=\frac{1.8}{T_{sa}}\frac{z-1}{z+0.8} \tag{50}$$

$$G_{second-order}(z)=\frac{3}{T_{sa}}\frac{(2z-1)(z-1)}{3z^2+z-1} \tag{51}$$

For the PI controller design, there is always a trade-off between the bandwidth and the overshoot, which weakens the advantage of multi-sampling PWM [65]. The pseudo-derivative-feedback (PDF) controller can be used in order to suppress the overshoot and improve the dynamic response at the same time [66], as shown in Fig. 12. Specifically, the PDF controller can be transformed into a PI controller, and a low-pass filter is inserted after the reference current. Moreover, the inserted low-pass filter will not affect the system stability. It can be seen from Fig. 12(b) that the delay from the low-pass filter is K_p/K_i, and increasing K_i can improve the response speed with the same open-loop bandwidth.

In addition, some non-linear controllers are combined with multi-sampling to further improve the control performance such as the hysteresis controller [70-71], the sliding mode controller [72], and the model predictive controller [73-74]. The performance comparison among the multi-sampled PI controller, the multi-sampled deadbeat controller, and the multi-sampled hysteresis controller is provided in [75]. When setting the same control bandwidth, the multi-sampled hysteresis controller has a minor control delay, where a higher sampling frequency is required. The analytical model is hard to be derived and the digital implementation is complicated instead. The model predictive controller has a similar performance to the multi-sampled PI controller for the current THD and step response [76]. Hence, the linear controller with

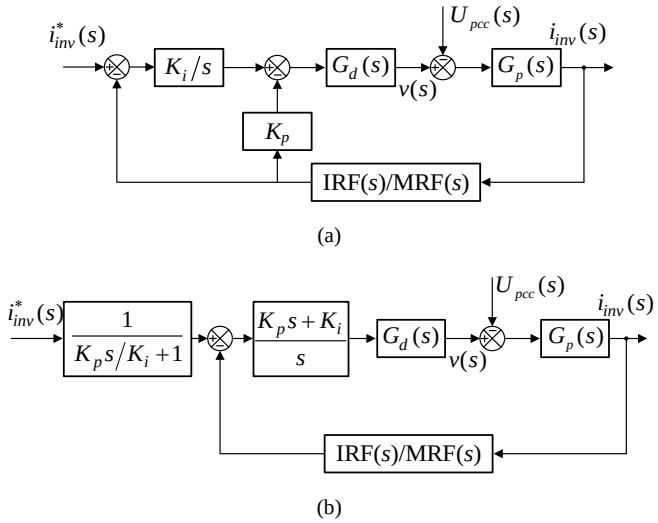


Fig. 16. Relationship between the PI and PDF controller. (a) PDF controller, (b) Equivalent transformation.

with PWM modulator is still the most common controller due to its clear model in the frequency domain, which simplifies the stability analysis and parameter design. However, the non-linear controller should inevitably earn more concerns because of the gradual development of powerful microprocessors [62-63].

Besides the small-signal response, the multi-sampling can help to improve the large-signal response. When the control error derivative between the reference value and the feedback value is larger than the threshold value, the output duty cycle will be 0 or 1 within one multi-sampling period instead of half of the switching period [25]. Consequently, the controller saturation can be triggered faster, and the settling time under a large-signal disturbance can be shorter than the double-sampling control.

D. Practical Implementation

As aforementioned, using multi-sampling PWM can provide several, however, the multi-sampling PWM also introduces a set of nonlinearities in the practical implementation. First, when the duty cycle is updated more than twice within one switching period, the switch may be triggered more than twice and the switching loss will increase compared with the double-sampling PWM [77]. The multi-switching diagram using multi-sampling PWM is given in Fig. 17.

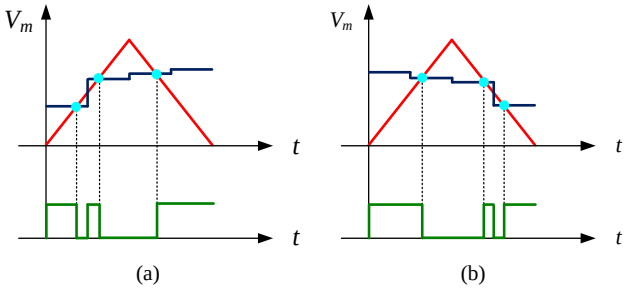


Fig. 17. Multi-switching diagram using multi-sampling PWM. (a) Rising edge, (b) Falling edge.

In order to avoid multi-switching, the maximum rate of change of the reference should not equal or exceed that of the carrier [26]. For the current control of a two-level inverter using the PI controller, the constraint in (52) should be satisfied. Moreover, a ‘‘self-lock’’ logic should be used in the microprocessors, where a single turn-off occurs during the first half of the switching period and a single turn-on occurs during the second half [27].

$$K_p \frac{0.5U_{dc}}{L_f} < 2U_{dc} f_{sw} \tag{52}$$

Moreover, the modulation signal may intersect with the carrier vertically, i.e., dead-band, where a variation in the modulating signal is no longer able to produce a change in the duty cycle [28]. This phenomenon depends on the considered modulation scheme and more precisely on the number of modulated edges. As shown in Fig. 18, the small-signal modulation gain will be halved or nulled under the single vertical crossing or double vertical crossing, respectively. Moreover, reduced gain regions can potentially lower the stability margins of the system, leading to oscillating behaviors.

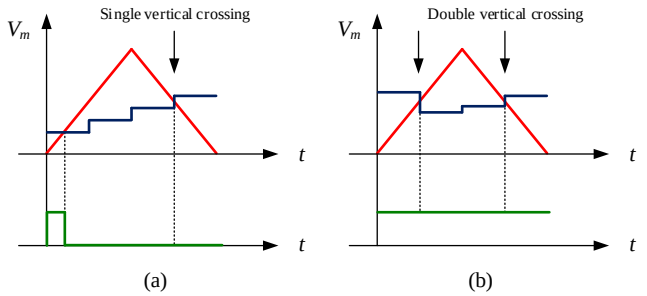


Fig. 18. Vertical crossing in multi-sampling PWM. (a) Single vertical crossing, (b) Double vertical crossing.

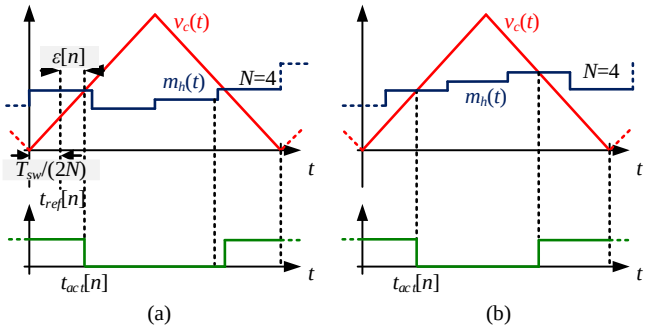


Fig. 19. Modulation diagrams before (a) and after, (b) correction in multi-sampling PWM.

Through the detection of vertical crossing, the dead-band can be avoided by forcing PWM to output pull-up and pull-down [29]. An alternative method is to make the modulation signal intersect with the carrier in the midpoint of two consecutive sampling events [28]. Consequently, the modulator operating point is equally distant from the two neighboring sampling instants and thus to the respective dead-bands. For example in Fig. 19(a), $\varepsilon[n]$ is the error between the actual turn-off instant $t_{act}[n]$ and a reference turn-off instant $t_{ref}[n]$ in the n-th switching cycle:

$$\varepsilon[n] = t_{act}[n] - t_{ref}[n] \tag{53}$$

The PLL correction algorithm will force $\varepsilon[n]$ to become zero by properly modulating the sampling period, as shown in Fig. 19(b), when the correction is achieved, ε=0, and thus T_{sa}=T_{sw}/N. This property means that no provisions have to be taken to ensure stabilization of the sampling frequency.

It is worth noting that the dead-band happens when the modulation signal and the carrier are in counter-phase operation. On the contrary, another nonlinear phenomenon called the jitter amplification will happen when the modulation signal and the carrier are in-phase operation [30]. As shown in Fig. 20, for a four-sampling PWM, switching action occurs near the instant at which m_h(t) is updated. With a small-signal change of the controller output, such a higher duty cycle is required, and the up-count effective duty cycle changes from D_1 to D_2. As a result, there will be an “increased gain” zone in the modulator trans-characteristic. The solution is to block the second duty cycle when the jitter is detected.

In order to prevent the limit cycle oscillations as any controller driving in a digital PWM, two conditions should be satisfied: i) sufficient resolution of digital PWM; ii) correct

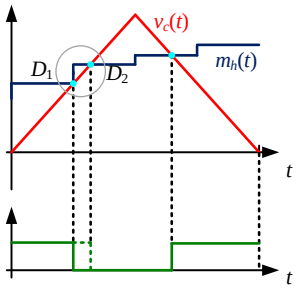


Fig. 20. Jitter amplification operating condition under four-sampling PWM.

selection of the controller multi-sampling rate [25, 31, 60]. Assuming the digital PWM resolution is *M*, varying the duty cycle by 1/*M* determines an average current variation after half of the switching period, whose amplitude can be compared with the current error least significant bit value, i.e., q_{ADC}. Then the clock frequency constraint for an inverter is

$$f_{clock} \geq \frac{U_{dc}}{L_f}\frac{2^{nbit}}{|i_{\max}|} \tag{54}$$

where *nbit* is analog-to-digital converter (ADC) resolution and i_{max} is the full-scale range of current sensor. In addition, the sampling process should be synchronized with the carrier, and an even number of current error samples are taken in each switching period. Only if these necessary conditions are met in the steady-state, all zero crossings of the current error signal will be aligned with the average current sampling instants, and undesired transients will be avoided.

IV. Condition Monitoring and Parameter Estimation

Improving sampling rate can not only reduce the control delay and improve the stability of power electronics controllers, but also provide more information from the multi-sampled data. The main difference with the multi-sampled current/voltage controllers is that the switching ripple is utilized rather than suppressed. Up till now, there are three kinds of applications, i.e., i) current slope estimation within zero/active voltage, ii) dc-link capacitor monitoring, iii) grid impedance estimation. The difference among these three applications only lies in the used multi-sampled variables and the related converters. Specifically, the current slope estimation only employs the sampled current ripple in the three-phase inverters. DC-link capacitor monitoring employs both the sampled current and the sampled voltage at the same time. Grid impedance estimation employs the sampled current and the sampled voltage for the two-level three-phase inverters, and only the sampled voltage is used in the single-phase H-bridge inverter and the interleaved two-cell three-phase inverters. Consequently, some new system state variables and parameters are estimated, which can help to save the cost and improve the reliability.

A. Current Slope Estimation

A three-phase PWM value can be transformed into two active vectors (U_{11} and U_{12}) and two zero vectors (U_{01} and U_{02}) within one switching period (see Fig. 21). The current slope within specific voltage vectors is widely used to estimate the position and the speed in the motor drive [32].

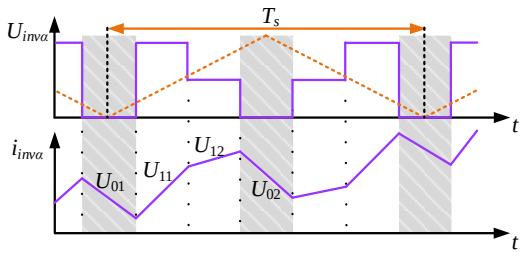


Fig. 21. Diagram of PWM voltage and current.

The current slope measurement can be achieved in two ways. One uses three low-cost current slope (*di*/*dt*) sensors to measure the current derivative directly; the other uses the motor line current samples to estimate the current slope [78]. The latter is more cost-effective in practical applications since no additional sensors and ADC channels are required. Based on numerous current-time pairs from multi-sampling, the least square based linear regression is used to calculate the current slope [79-82]. Assuming that the current evolves linearly during active/zero voltage vectors, a first-order function is used to fit the current data and it is given as

$$i(t) = a_1 t + a_0 \tag{55}$$

where $i(t)$, t, a_1, a_0 are the current, time, the current slope and intercept, respectively.

$$\begin{cases} a_1 = \dfrac{\overline{it} - \bar{i}\bar{t}}{\overline{t^2} - \bar{t}^2} = \dfrac{\frac{1}{n}\sum_{k=1}^{n} i(t_k)t_k - \frac{1}{n^2}\sum_{k=1}^{n} i(t_k)\sum_{k=1}^{n} t_k}{\frac{1}{n}\sum_{k=1}^{n} t_k^2 - \frac{1}{n^2}(\sum_{k=1}^{n} t_k)^2} \\ a_0 = \bar{i} - a_1\bar{t} = \dfrac{1}{n}\sum_{k=1}^{n} i(t_k) - a_1\dfrac{1}{n}\sum_{k=1}^{n} t_k \end{cases} \tag{56}$$

where $\overline{it}$, $\bar{i}$, $\bar{t}$ and $\overline{t^2}$ are the average product of current and time, average current, average time, and average time square during the active/zero voltage vectors. In order to mitigate the computational effort in the practical implementation, the four average values $\overline{it}$, $\bar{i}$, $\bar{t}$ and $\overline{t^2}$ can be calculated recursively and the computational effort remains the same for each sampling interval.

In addition, except a high-performance FPGA-based platform, the current slope fitting method can also be achieved in a low-cost microprocessor based platform. The ADC can be triggered by an internal timer block, and the direct memory access (DMA) engine is used to store the sampled currents in the software buffer after every ADC sampling is completed. The DMA engine is now common in most of the processors used in the automotive and aerospace industry [33].

During the switching transients, there will be some short-time current oscillations due to the parasitic parameters. The solution is to delay the start point of regression window [37]. The estimation accuracy highly depends on the number of sampled data. Narrow voltage vectors should be extended to a minimum duration time, which is longer than the oscillation time of the phase current. The extension of the narrow voltage vector changes the fundamental PWM sequence, thus leading to additional current distortion and acoustic noise.

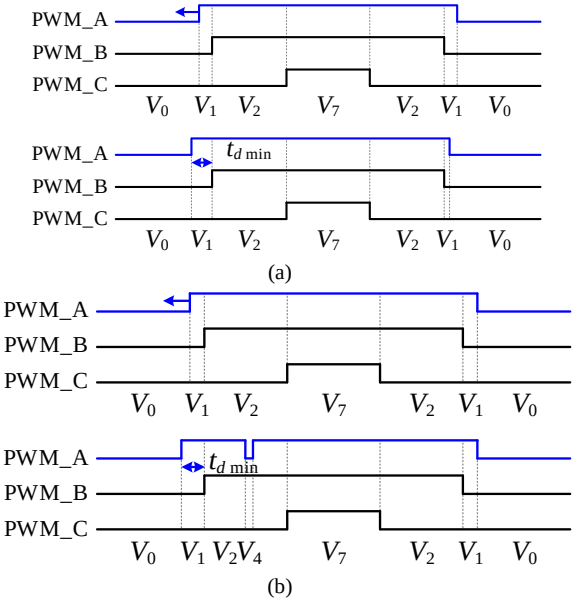


Fig. 22. Narrow voltage vector extension and compensation. (a) Shifting the double switching edge, (b) Opposite voltage pulse injection.

The first compensation method is shifting the double switching edge based on the voltage second balance [32], as shown in Fig. 22(a). However, modifying the standard PWM sequence can still cause additional current distortion. Another compensation method is injecting an opposite voltage pulse, as shown in Fig. 22(b), and a better current THD can be achieved [78]. Based on the artificial neural network, the minimum duration time requirement can be further relieved [83-84]. The experimental current data is used as training data, and the target data is generated by fitting the steady-state data and propagating backwards the beginning of the sample window. Moreover, the inverter nonlinearity is also included in the training process.

Besides estimating the motor position and speed, the fitted current slope can also be used to detect the open-circuit fault of three-phase two-level inverters [35]. The current slope difference during two consecutive zero voltage vectors is approximately the same in normal condition, however, in fault condition, the fault index is

$$\begin{cases} \varepsilon_{a01}-\varepsilon_{a02} \approx -2(\varepsilon_{b01}-\varepsilon_{b02}) \approx -2(\varepsilon_{c01}-\varepsilon_{c02}) \, Fault\ a \\ \varepsilon_{b01}-\varepsilon_{b02} \approx -2(\varepsilon_{a01}-\varepsilon_{a02}) \approx -2(\varepsilon_{c01}-\varepsilon_{c02}) \, Fault\ b \\ \varepsilon_{c01}-\varepsilon_{c02} \approx -2(\varepsilon_{a01}-\varepsilon_{a02}) \approx -2(\varepsilon_{b01}-\varepsilon_{b02}) \, Fault\ c \end{cases} \quad (57)$$

where ε_{a01}, ε_{a02}, ε_{b01}, ε_{b02}, ε_{c01}, ε_{c02} are the current slope difference of phase *a*, phase *b* and phase *c* during two consecutive zero voltage vectors, respectively. In the condition of high-frequency voltage signal injection, the current slope during other active voltage vectors can be estimated using two slopes in the zero voltage vectors. Consequently, the injection magnitude can be reduced by a factor of 7 to 10 compared to a standard single-sampling PWM [37]. Common approaches to the dead-time compensation rely on the polarity of the sampled current with the single sampling. Due to the measurement noise, this method may cause a false compensation in the case of small currents. Based on the multi-sampling and the current slope

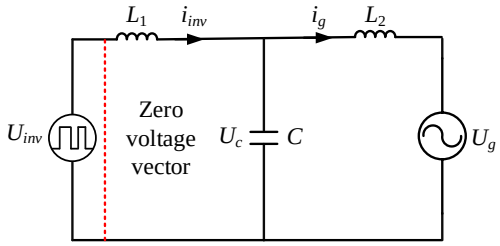


Fig. 23. Single-phase equivalent circuit of LCL-filtered inverter.

measurement, the phase current at the beginning of dead-time can be predicted in an FPGA and the computing process is fast due to the parallel data processing [36]. Using the voltage vector and the current slope, the motor inductance can be estimated in real time and the effect of inductor saturation is removed [33, 85]. Similarly, for an LCL-filtered inverter (see Fig. 23), the filter capacitor voltage can be estimated using the current slope within zero voltage vectors [34], and it is given as

$$U_c = -L_1 \frac{di_{inv}}{dt} \quad (58)$$

B. DC-Link Capacitor Monitoring

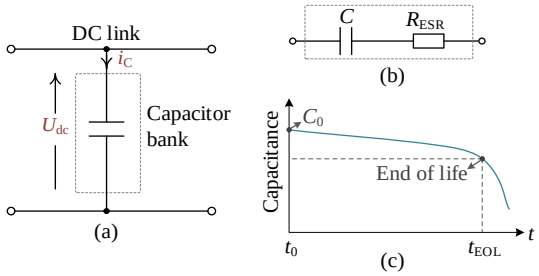


Fig. 24. Typical structure, equivalent circuit, and degradation characteristics of dc-link capacitors. (a) Typical structure, (b) Equivalent circuit, (c) Capacitance degradation characteristic.

In dc-link applications, multi-sampling is used to estimate the dc-link capacitor, which aims to identify the degradation status and improve the reliability of systems [38, 86-87]. Fig. 24(a) shows the typical structure of dc-link capacitors. Generally, three types of capacitors are used in dc-link capacitor banks, i.e., electrolytic capacitors (E-Caps), film capacitors (F-Caps), and multi-layer ceramic capacitors (MLC-Caps). The equivalent circuit of dc-link capacitors is shown in Fig. 24(b), where *C* denotes the capacitance of capacitors, R_{ESR} represents the equivalent series resistance (ESR). According to Fig. 24 (a) and (b), we have

$$\Delta U_{dc}(t) = \frac{1}{C}\int_0^t i_C(t)\,dt + R_{ESR}\cdot \Delta i_C(t) \quad (59)$$

where ΔU_{dc} and Δi_C represent the capacitor voltage ripple and capacitor current ripple, respectively. With the degradation of capacitors, a series of physical and chemical changes occur inside capacitors, which will cause the change of capacitor parameters (e.g. R_{ESR} and *C*). Taking capacitance change as an example, Fig. 24(c) gives the degradation curve of capacitors. Usually, dc-link capacitors are defined as fault states when the parameters reach the end-of-life criteria, as summarized in Table II [88]. Fig. 25(a) shows the implementation of the multi-

sampling in buck converters, which aims to estimate R_{ESR} and C of dc-link capacitors. The difference between the capacitor voltages sampled at points *a* and *b* is due to R_{ESR} and C. Based on (59), the estimation model is calculated as (60), where D represents the duty cycle. Here, to sample the voltage at points *a* and *b*, a PWM signal is needed [89-90]. Similarly, the two-point sampling based method can be used to estimate capacitor parameters in PV H5 inverter, as shown in Fig. 25(b), the capacitance is calculated during the zero vector state, i.e., the power switch S_5 is turned OFF, and C is calculated as (61) [91].

$$\begin{cases} R_{ESR} = \dfrac{2L_1 f_{sw}\left[\Delta U_{dc}(0) + 2\dfrac{2(D-1)}{(2-D)} \times \Delta U_{dc}\left(\dfrac{DT_{sw}}{2}\right)\right]}{U_{dc}(D-1)} \\ C = \dfrac{V_o(2-D)(D-1)}{24L_1 f_{sw}^2 \Delta U_{dc}\left(\dfrac{DT_{sw}}{2}\right)} \end{cases} \tag{60}$$

$$C = \frac{i_{pv\_1} \times \Delta t}{U_{dc\_2} - U_{dc\_2}} \tag{61}$$

Fig. 25(c) shows the circuit structure and key waveforms of a fly-back converter with continuous conduction mode. According to the relationship between R_{ESR}, C and capacitor voltage in (59), capacitor parameters can be calculated as (62) and (63), where f_{sw} and U_{dc} represent the switching frequency and capacitor voltage respectively. Here, the capacitor voltage at sampling points *c*, *d*, *e* is employed [92-93].

Similarly, the multi-sampling can be used in PV boost converter. Referring to Fig. 25(d), the difference between the capacitor voltages sampled at points *f* and *h* is due to R_{ESR}. The voltage difference at points *g* and *f* is only due to C. Using (59), R_{ESR} and C are calculated in (64) [93-94].

$$C = \frac{U_{dc}(1-D)^3}{24L_s^2 f_s^2 \left\{(1-D)\Delta U_{dc}\left(\dfrac{1+D}{2f_s}\right) + D\Delta U_{dc}\left(\dfrac{D}{2Df_s}\right)\right\}} \tag{62}$$

$$\begin{cases} R_{ESR} = \left[U_{dc}(0) - U_{dc}(DT_s)\right] L_2 \big/ \left(U_{dc} DT_s\right) \\ C = \dfrac{U_{dc} DT_s^2}{8L_2\left\{U_{dc}\left(DT_s/2\right) - U_{dc}\left[(1+D)T_s/2\right]\right\}} \end{cases} \tag{64}$$

TABLE II
TYPICAL END-OF-LIFE CRITERIA OF CAPACITORS

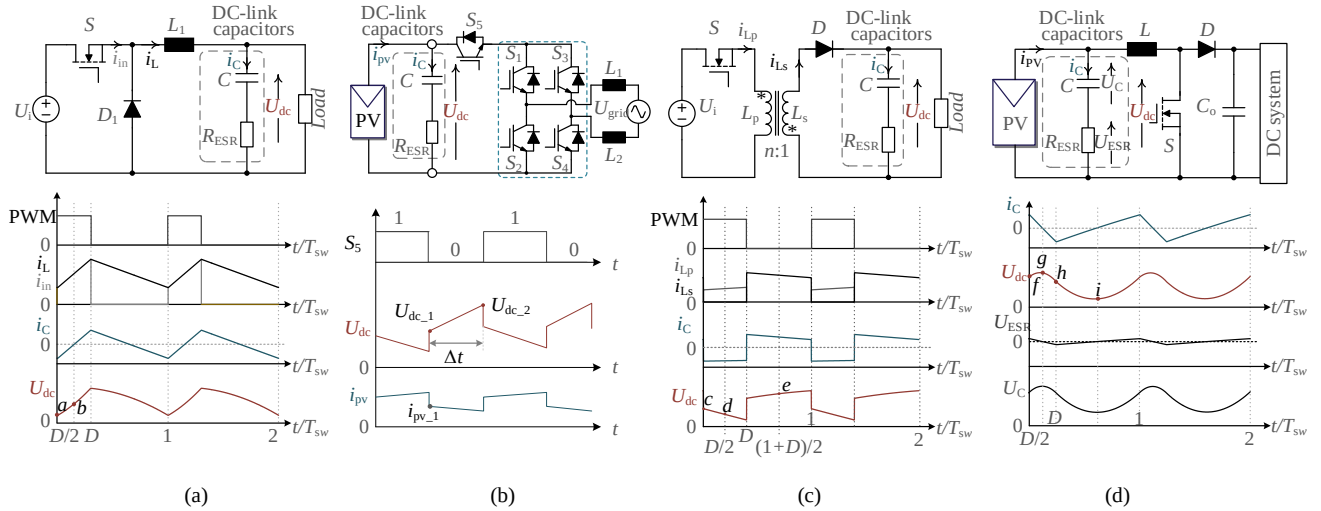
	Al-Caps	MPPF-Caps	MLC-Caps
End-of-life criteria	C/C_0 <80% R_{ESR}/R_{ESR0}>2	C/C_0 <95%	C/C_0 <90%

C: capacitance, R_{ESR}: equivalent series resistance, C_0: initial capacitance, R_{ESR0}: initial equivalent series resistance.

C. Grid Impedance Estimation

The stability of grid-connected inverters is mainly affected by the grid impedance. One method is to make the inverter output impedance dissipative by reducing control delay and adding extra state feedback [8]. The other one is to estimate the grid impedance, and the real grid voltage instead of the PCC voltage is feedforwarded [40]. By four-sampling the inverter-side currents, as shown in Fig. 26, the grid impedance can be estimated using two consecutive examples. Due to the sensitivity to sampling noise, the estimation method in [40] is not effective in identifying the grid impedance resistance. For a single-phase H-bridge inverter or an interleaved three-phase inverter, the apparent switching frequency is twice larger than the preset switching frequency. The grid impedance can also be

$$R_{ESR} = \frac{12L_s D f_s \left[2(1-D)\Delta U_{dc}\left(\dfrac{1+D}{2f_s}\right) + (1+2D)\Delta U_{dc}\left(\dfrac{D}{2f_s}\right)\right]\left[(1-D)\Delta U_{dc}\left(\dfrac{1+D}{2f_s}\right) + D\Delta U_{dc}\left(\dfrac{D}{2f_s}\right)\right]}{U_{dc}(1-D)^3\left[\Delta U_{dc}(0) - \Delta U_{dc}\left(\dfrac{D}{2f_s}\right)\right]} \tag{63}$$



(a) (b) (c) (d)

Fig. 25. Multi-sampling techniques used for capacitor parameters identification. (a) Buck converter, (b) Single-phase grid-connected PV H5 inverter, (c) Flyback converter, (d) PV boost converter.

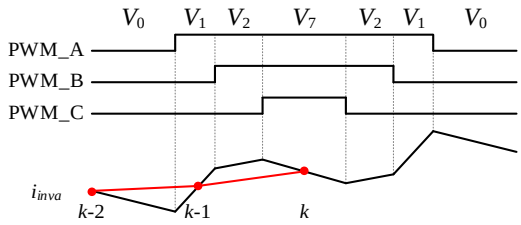


Fig. 26. Measurement instants within one switching period for a three-phase inverter.

estimated by sampling the PCC voltage four times within one switching period [39, 95]. As shown in Fig. 9, the inverter output voltage is equal to zero at the peak/valley of the carrier and equal to the dc-link voltage at the intersection point of the carrier, respectively. Then the grid impedance can be estimated through the bias between the PCC grid voltage at the peak/valley and the intersection points, as shown in (65). Both of the grid impedance estimation methods are based on multi-sampling, but the resistance cannot be acquired. Moreover, the more complex grid impedance including capacitance cannot be estimated because only the filter inductance is considered in [39, 40, 95].

$$\begin{aligned} L_g &= L_f \frac{U_{pcc\,inter} - U_{pccpeak/valley}}{U_{inv\,inter} - (U_{pcc\,inter} - U_{pccpeak/valley})} \\ &\underbrace{-L_f \frac{U_{g\,inter} - U_{gpeak/valley}}{U_{inv\,inter} - (U_{pcc\,inter} - U_{pccpeak/valley})}}_{\text{small}} \\ &\approx L_f \frac{U_{pcc\,inter} - U_{pccpeak/valley}}{U_{inv\,inter} - (U_{pcc\,inter} - U_{pccpeak/valley})} \end{aligned} \tag{65}$$

V. Challenges and Future Trends

A. Sampled Switching Ripple Suppression

For the multi-sampling control of power electronic converters, a digital filter should be inserted in the control loop in order to remove the sampled switching harmonics. The LPLRF is mainly used in the DC-DC converter, where the introduced phase lag below switching frequency is little and the advantage of multi-sampling phase boost is fully exploited. However, for a two-level three-phase inverter, the sampled switching harmonics are at side switching frequencies, and the IRF/MRF still introduces a large delay that is equal to 1/4 switching period. Consequently, the total loop control delay will be close to 1/4 switching period with the increase of sampling rate. In order to further reduce the control delay, a more effective digital filter with low-phase-lag should be proposed. Similarly, for the multi-level inverter, the maximum allowable sampling rate is related to the apparent switching frequency. For example, the sampling rate is only four for a single-phase HB inverter, where no switching harmonics are introduced. Hence, the same challenge exists and the feasibility of using a higher sampling rate is not available. Until now, the multi-sampling control is only applied in a few power electronic converters, and the potentiality of multi-sampling on other effective converters needs to be further researched in the future. Besides the digital filter, single-edge modulator with a pre-distorted carrier or the FOH sampler can also help to remove the switching ripple from a physical point of view. Actually, how to remove the multi-sampled switching ripple is still an open topic.

B. Stability Analysis

In the practical implementation, there are a set of nonlinearities including multi-switching, dead-band and jitter. Although some solutions are provided to linear the modulation behavior, the focus is the gain margin and the phase margin is not considered. In addition, the control system is discretized with the multi-sampling period when designing the switching ripple filter and analyzing the stability. As a result, the Nyquist frequency is equal to half of the sampling frequency instead of the switching frequency, and the stability above the switching frequency is still not considered. Hence, a more accurate small-signal multi-sampling model should be proposed considering discretization and the related nonlinearities. In terms of large-signal stability, only the effect of reference change is investigated. How multi-sampling affects transient stability should be further investigated.

C. Estimating More States and Parameters

The multi-sampled switching ripple is used to estimate the current slope, dc-link parameters, and grid impedance. It is worth to note that all these three applications mainly focus on a few power electronic converters, and their feasibility in more converters should be further researched. In addition, all these three applications are model-based methods, and it is hard to estimate more states and parameters. Artificial intelligence is already widely used in practice, and a large data-set is the prerequisite. Fortunately, the multi-sampling can provide enough data within one switching period. Therefore, it is possible to combine the artificial intelligence and the multi-sampling to improve the stability and reliability of power converters, such as fault diagnosis, sensorless control, complex grid impedance estimation, etc.

VI. Conclusion

With the gradually decreasing cost of high-performance digital processors, multi-sampling becomes a promising technology in power electronics. In this paper, the application of multi-sampling in power electronic converters is discussed and reviewed. Compared with the variants of regular single/double-sampling PWM, the multi-sampling PWM can not only reduce the control delay, but also will not introduce the aliasing and the duty cycle limitation. In addition, solutions to the issues in practical implementation are provided. With respect to the condition monitoring and parameter estimation, three kinds of applications are surveyed including current slope estimation, dc-link parameter estimation, and grid impedance estimation. In particular, more multi-sampled-data based applications in power electronics system will be seen in the future since they provide new important information and better performance.

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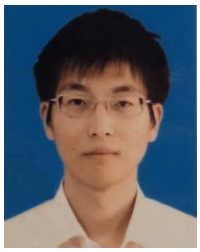

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