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Line Voltage Sensorless Control of Grid-Connected Inverters Using Multisampling

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***Abstract*—Multisampling control provides an attractive way to improve the dynamics and stability of high-power three-phase grid-connected inverters. Beyond the desired performance in current control, more information can be acquired through multisampling. However, such an assumption is rarely discussed in grid-connected inverters. In order to fill this gap, a line voltage sensorless control scheme is proposed for LCL-filtered inverters. In this paper, a multisampling is performed on the inverter-side current, and the linear regression of the multisampled current during zero vectors of inverter-modulation voltage is employed to estimate the filter capacitor voltage. Consequently, the cost of line voltage sensors is reduced and the failure of line voltage sensors is prevented when using multisampling current control. Further, to address start-up transients, the line voltage can still be estimated by temporarily locking the upper arms of the inverter, and dc-link voltage can be pre-charged to the target value at the same time. Experimental results validate the effectiveness of the method on a down-scale inverter.**

***Index Terms*—Multisampling, zero voltage vectors, linear regression, sensorless control, soft start-up.**

I. Introduction

LCL-filtered grid-connected inverters have been widely used in distributed generation systems based on photovoltaic panels, wind turbines, and battery storage [1]. For high-power inverters operating at a low switching frequency, the regular sampling methods (i.e., single-sampling or double-sampling within a switching period) impose constraints on the transient dynamics of the system due to the control delay [2]. With the gradually decreased cost of high-performance digital processors [3], multisampling control is a potential candidate to overcome the bandwidth limits. The control delay including computation delay and pulse width modulation (PWM) delay is inversely proportional to the multisampling rate [4]. For the multisampling current control of a two-level inverter, a repetitive filter is necessary to remove the sampled switching harmonics and suppress the low-order aliasing [5]. In particular, for a cascaded H-bridge inverter, the optimum sampling rate is four times larger than the number of cells without any filters [6]. Since the equivalent switching frequency is higher, the average value can be acquired and the aliasing effect is little. Besides the improved current control performance from multisampling, more information from the multisampled data can also be utilized to unleash more controllability. One application is to estimate the current-derivative term during active/zero voltage vectors, which has been used in motor drives to estimate the speed and stator inductance [7-8]. However, such an estimation technique is rarely discussed in grid-connected inverters. For the control of LCL filtered inverters, line voltage sensors are usually replaced by estimation in order to prevent the sensor failure in high-power inverters and to detect the voltage in remote grid connections [9]. The sensors for inverter-side current and dc-link voltage are indispensable for the over-current and over-voltage protection [10]. Hence, the motivation in this work is using multisampled current data to estimate the line voltage.

Many research efforts have been devoted to estimating the line voltage. A simple method is to use the sum of the inverter output voltage and the voltage drop on the inverter-side inductor (calculated by current derivative) to estimate the line voltage [11]. In order to suppress the noise from the derivative operation, a low-pass filter is inserted in the feedback loop, which, however, leads to a trade-off between the system dynamics and the noise suppression [12]. Moreover, the current derivative can also be replaced by a product of the current and fundamental angle frequency, and the grid-side current harmonics cannot be separated accurately [13]. By ignoring the feedback current derivative in steady-state, the modulation signal is used to acquire the grid phase angle through a phase-locked loop (PLL), but the real line voltage is still unknown [14].

Alternatively, the virtual flux concept can help to avoid the derivative operator, but the estimation accuracy is sensitive to grid harmonics [15-16]. In [17], a neural network is used to emulate the characteristics of a pure integrator, and the parameter tuning is still lack of analytical insight. Regarding the grid distortion and parameter variations as unknown disturbances, a series of adaptive observers are proposed to estimate the grid voltage [18-19]. However, it is difficult to analyze the robustness of the system due to the nonlinearity of the aforementioned observers. On the contrary, linear observers can facilitate the design and analysis of the control system. In [20-21], the grid voltage is estimated by the Luenberger observer and extended-state observer, respectively. It is worth noting that many observer-based methods only measure the grid-side currents to estimate the grid voltage [18-20]. As a result, the inverter-side current sensors are still required for the over-current protection and the goal of reducing sensors cannot be fulfilled. To summarize the prior art, the direct calculation method is simple but it is sensitive to noise. The virtual flux- and observer-based methods require expert knowledge for parameter tuning, and the observer dynamics and parameter mismatch are often coupled together [21].

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Another important issue with the line voltage sensorless control is the start-up transients. One method is to inject a short-time zero voltage vector, and the line current derivative is used to estimate the initial grid phase angle [22-23]. However, the duration time of the zero voltage vector is set to three switching periods, and the risk of over-current still exists if using a low switching frequency and/or a small filter inductor. By utilizing the ac current flowing in the diode rectifier operation mode, some initial grid phase angle estimators are proposed which are dependent on the current sensor accuracy [24-25]. In some observer-based methods, the grid voltage can be estimated in advance by measuring the grid-side currents [19, 26], which is, however, not feasible if only the inverter-side currents are measured.

In order to fully exploit the benefit of multisampling control in high-power LCL-filtered grid-connected inverters, a line voltage sensorless control method is proposed in this paper. By utilizing the sampled inverter-side currents during zero voltage vectors, the current derivative is estimated based on the linear regression. Consequently, the filter capacitor voltage can be calculated from the product of the inverter-side current derivative and the inverter-side inductor, which is used for the synchronization through a PLL. In addition, based on a single-loop multisampling current controller, a modified repetitive filter is introduced to remove the sampled switching harmonics. The first main contribution in this paper is using multisampling current control to estimate the line voltage, which is the fundamental difference with the work in [5-6]. On the other hand, regarding the inverter as a boost converter, the dc-link capacitor can be pre-charged to a target value and the grid information can be known in advance based on multisampling. As a result, the start-up transients can be suppressed, which is another main contribution of this paper. Further, the proposed start-up method can also be used for other sensorless methods which only measure inverter-side currents. The subsequent content is organized as follows: Section II gives the procedure to estimate filter capacitor voltage and investigates the effect of duty ratio on the estimator. Then the design of multisampling current controller with a modified repetitive filter is proposed in Section III. The proposed start-up method and the related parameter design are introduced in Section IV. Several steady/transient state experimental tests including the start-up process, current reference step change and grid faults are provided in Section V. Finally, Section VI concludes this paper.

II. Filter Capacitor Voltage Estimation Using Linear Regression of Multisampled Current

The multisampling single-loop control with inverter-side current feedback is used as a case study, and the multisampling timing diagram is shown in Fig. 1, where T_s is the switching period and T_c is the sampling period. The currents are sampled and modulation signals are updated multiple times within one switching period, and the proposed line voltage sensorless control diagram is shown in Fig. 2. In order to suppress low-frequency aliasing, a repetitive filter is necessary to remove multisampled switching harmonics [5]. Besides the multisampling current control, the pre-filtered inverter-side currents are used to estimate the filter capacitor voltage, which is fed to the PLL to acquire the grid phase angle. Further, the estimated filter capacitor voltage is used to suppress the grid-side current harmonics based on pseudo-derivative-feedback and resonant current controller. The details of current controller design are introduced in Section III, and this section gives the mechanism of filter capacitor voltage estimator.

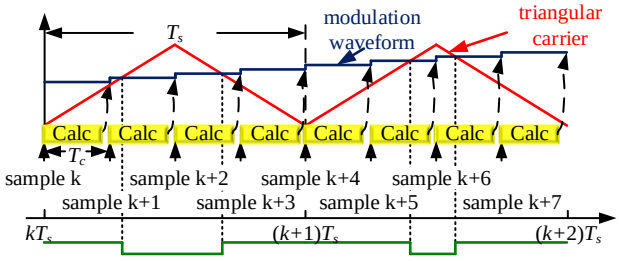


Fig. 1. Schematic diagram and switching pattern of multisampling PWM.

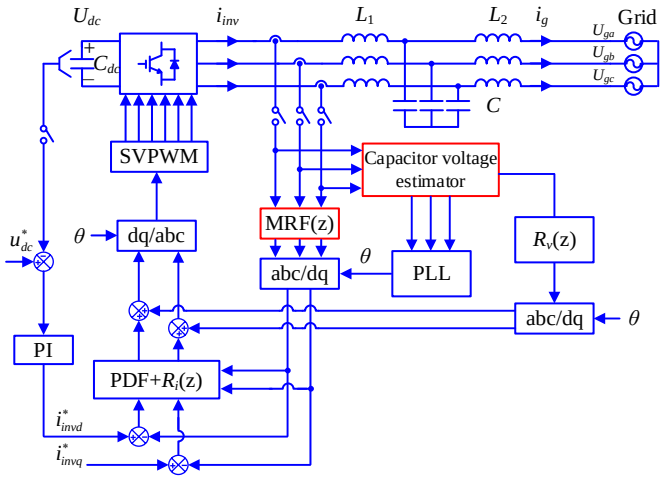


Fig. 2. Single-loop controlled inverter-side current feedback system (MRF: modified repetitive filter, PDF: pseudo-derivative-feedback).

The equivalent single-phase circuit of a grid-connected inverter is shown in Fig. 3(a), where U_{inv} is the inverter output voltage and U_g is the grid voltage. i_{inv} is the inverter-side current and i_g is the grid-side current. A three-phase PWM value can be transformed into two active vectors (U_{11} and U_{12}) and two zero vectors (U_{01} and U_{02}) within one switching period (see Fig. 3(b)). If the inverter-side current derivative is known, the filter capacitor voltage can be acquired during zero voltage vectors which is given as

$$U_c = -L_1 \frac{di_{inv}}{dt} \tag{1}$$

Based on numerous current-time pairs from multisampling, the least square based linear regression is used to calculate the current derivative. Assuming that the current evolves linearly during zero voltage vectors, a first-order function is introduced to fit the current data, i.e., linear regression, and it is given as

$$i(t) = a_1 t + a_0 \tag{2}$$

where $i(t)$, t, a_1, a_0 are the current, time, the current derivative and intercept, respectively. The error function is the sum of all squared deviations between measurements $i_{real}(t_k)$ and the regression curve $i(t_k)$.

$$E = \sum_{k=1}^{n} (i_{real}(t_k) - i(t_k))^2 \tag{3}$$

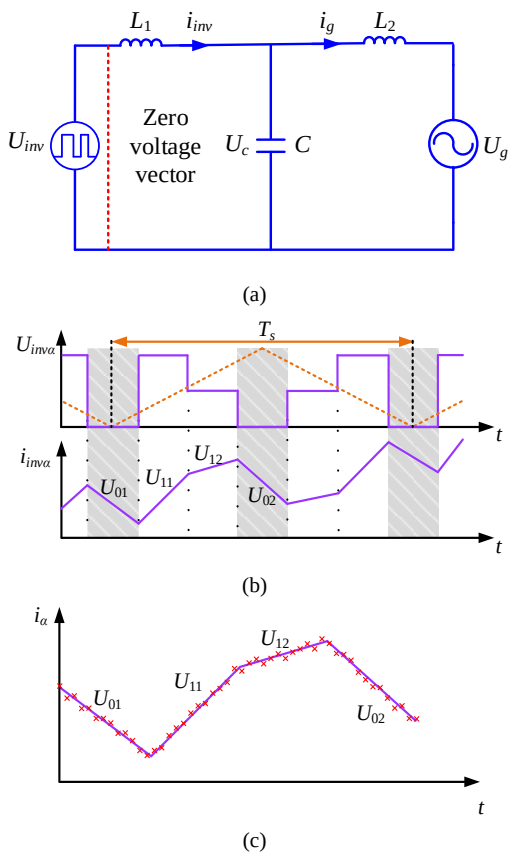


Fig. 3. Diagram of PWM voltage and current. (a) Single-phase equivalent circuit, (b) U_{inv} and i_{inv} within a switching period, (c) Fitting results using linear regression.

By deducing the roots of the partial derivatives of the error function in (4), the current derivative a_1 and intercept a_0 are given in (5) [8, 27].

$$\frac{\partial E}{\partial a_1}=0,\ \frac{\partial E}{\partial a_0}=0 \tag{4}$$

$$\begin{cases} a_1=\dfrac{\overline{it}-\bar{i}\bar{t}}{\overline{t^2}-\bar{t}^2}=\dfrac{\frac{1}{n}\sum_{k=1}^{n}i(t_k)t_k-\frac{1}{n^2}\sum_{k=1}^{n}i(t_k)\sum_{k=1}^{n}t_k}{\frac{1}{n}\sum_{k=1}^{n}t_k^2-\frac{1}{n^2}(\sum_{k=1}^{n}t_k)^2} \\ a_0=\bar{i}-a_1\bar{t}=\dfrac{1}{n}\sum_{k=1}^{n}i(t_k)-a_1\dfrac{1}{n}\sum_{k=1}^{n}t_k \end{cases} \tag{5}$$

where $\overline{it}$, $\bar{i}$, $\bar{t}$ and $\overline{t^2}$ are the average product of current and time, average current, average time and average time square during the zero voltage vectors. However, the computational effort scales with the number of data n, because these data would require allocated memory and processing time. In order to mitigate the computational effort in the practical implementation, the four average values $\overline{it}$, $\bar{i}$, $\bar{t}$ and $\overline{t^2}$ are calculated recursively as shown in (6). The computational effort remains the same for each sampling interval and is independent of the number of data n. The fitting results after linear regression is shown in Fig. 3(c).

$$\bar{x}[k]=\bar{x}[k-1]+\frac{x[k]-\bar{x}[k-1]}{k},\ k=1,2,...n \tag{6}$$

The flowchart to estimate the filter capacitor voltage is shown in Fig. 4. There are twelve state variables and the output is the estimated filter capacitor voltage. The state variable x_1 is used to count the number of the sampled data and to compute the average value. x_2-x_4 are the sampled three-phase inverter-side currents. x_5-x_7 are the product of the currents and time. x_8 and x_9 are the time and the square of the time. At the end of zero voltage vector, the counter x_1 is set to zero and the average values $\overline{it}$, $\bar{i}$, $\bar{t}$ and $\overline{t^2}$ are acquired. It is noted that the estimation accuracy highly depends on the sampling frequency. As shown in Fig. 5, based on the geometric principle, the duty ratio amplitude and multisampling rate determine the number of sampled current data. In order to estimate the current derivative, at least two current samples are required. In this paper, the multisampling rate is set to 50 (100 kHz) and the switching frequency is set to 2 kHz, and the boundary duty ratio is 0.04 and 0.96, respectively. Moreover, the current data during switching transients should be avoided due to the noise. Therefore, the practical duty ratio output should be limited in the boundary range. However, in some transient cases, the output duty ratio is out of the boundary range and no zero voltage vectors exist within one switching period. In these two cases, $\bar{t}$ and $\overline{t^2}$ are equal to 0, and the current derivative a_1 equals to infinite according to (5). According to Fig. 4, when x_8 equals to x_9, the solution is to output the last current derivative, and this will result in an estimation error.

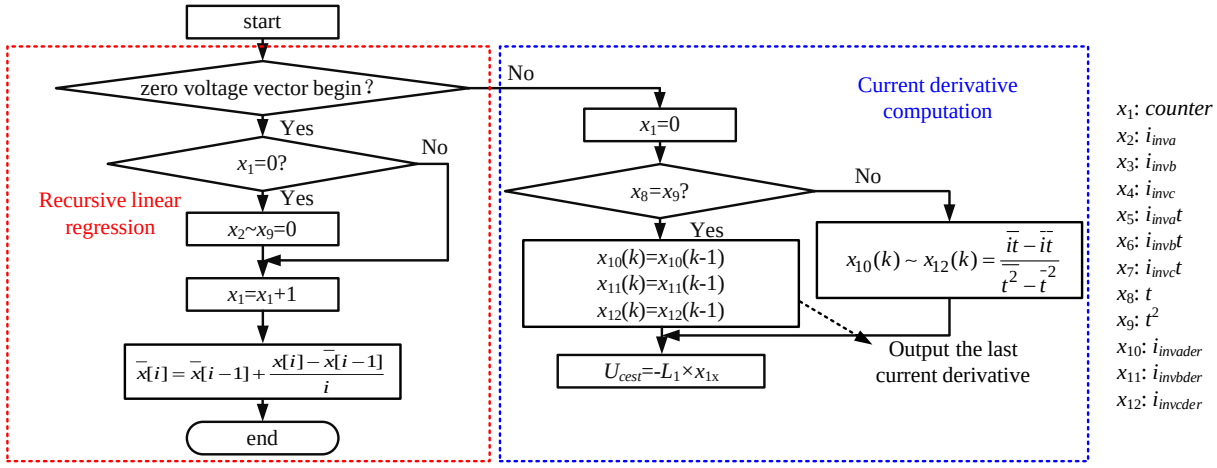


Fig. 4. Flowchart of filter capacitor voltage estimator.

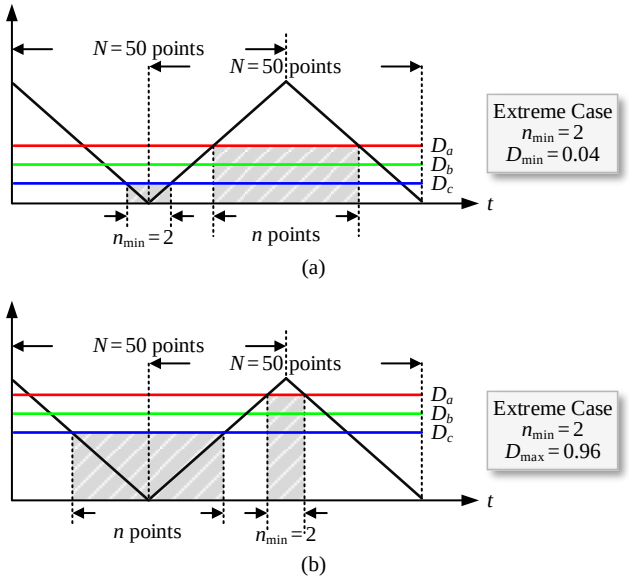


Fig. 5. Duty ratio limitation from a preset multisampling frequency. (a) Minimum duty ratio, (b) Maximum duty ratio.

Actually, the current derivative can also be estimated through the data during active voltage vectors, which can remove the duty ratio limitation and will be studied in the future. In addition, except a high-performance FPGA-based platform, the current derivative fitting method can also be achieved in a low-cost DSP-based platform. The ADC can be triggered by an internal timer block, and the direct memory access (DMA) engine is used to store the sampled currents in the software buffer after every ADC sampling is completed. The DMA engine is now common in most of the processors used in the automotive and aerospace industry [7-8].

If updating the estimated filter capacitor voltage immediately after the zero voltage vector ends, the update instant will change with the duration time of zero voltage vectors. For a fixed step digital processor, it is preferred to fix the updating instant. As shown in Fig. 6, the estimated filter capacitor voltage updates in the peak/valley of the carrier wave. Consequently, the estimated filter capacitor voltage equals to the real value using double sampling, and there is a phase lag, which is equal to half of the switching period.

Hence the estimated grid phase angle should be compensated and it is given as

$$\theta_{est} = \theta_{PLL} + 2\pi f_{PLL} \frac{T_s}{2} \tag{7}$$

where θ_{est} is the estimated grid phase angle, θ_{PLL} and f_{PLL} are the calculated grid phase angle and grid frequency from PLL, and T_s is the switching period. In practical applications, the measured current during zero voltage vectors cannot be ideally linear, and it is affected by ADC conversion noise and current sensor noise. In fact, increasing sampling frequency can effectively reduce the ADC conversion noise, but the ability in suppressing the current sensor noise is limited [28]. Therefore, using a higher sampling rate (e.g. 1000) is not necessary or economical. In [7], a Kalman filter is used to reconstruct the sampled current during zero voltage vectors, but the model matrix is not accurate. Since the current sensor noise suppression is still an open topic, and it is not considered in this work.

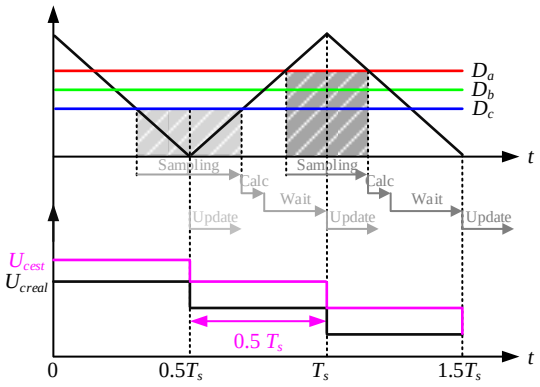


Fig. 6. Estimated filter capacitor voltage updating scheme.

III. Current Controller and Prefilter Design

A. Modified repetitive prefilter

As discussed in Section II, the multisampling rate is set to 50 (100 kHz) in order to have enough current data during zero voltage vectors. However, the improved repetitive filter (IRF) in [5] will amplify high-frequency components after 40 kHz when using a high multisampling rate, as shown in Fig. 7. The expression of IRF is given in (8). The compromised moving average filter (CMAF) in the IRF is used to remove the sampled switching harmonics, and the size of the window is half of the switching period. By comparing the amplitude-frequency characteristic between CMAF and IRF in Fig. 7, the linear delay compensator is the main reason for amplifying high-frequency noise.

$$IRF(z) = \underbrace{\frac{1}{25}\frac{1-z^{-50}}{1-z^{-2}}}_{\text{CMAF}} \underbrace{(11-10z^{-1})}_{\text{Linear delay compensator}} \tag{8}$$

In this paper, a more effective delay compensator in [29] is used to substitute the linear delay compensator, i.e., modified repetitive filter (MRF), as shown in (9).

$$MRF(z) = \underbrace{\frac{1}{25}\frac{1-z^{-50}}{1-z^{-2}}}_{\text{CMAF}} \underbrace{\frac{1-r^{50}}{1-r^{2}}\frac{1-r^{2}z^{-2}}{1-r^{50}z^{-50}}}_{\text{Delay compensator in [31]}} \tag{9}$$

where $r \in (0, 1)$ is called the attenuation factor. There is a trade-off between the delay compensation performance and high-frequency noise suppression ability in terms of the variation of r. When the switching frequency is set to 2 kHz, the switching harmonics around 2 kHz, 4 kHz and 6 kHz are the main high-frequency components [5]. When r is set to 0.99, the MRF has a lower phase lag compared with IRF and CMAF at half of the switching frequency (1 kHz). But the MRF(r=0.99) also has a weaker ability in suppressing high-frequency noise, e.g., its amplitude at 1900 Hz is only -5.6 dB. In order to suppress the sampled switching harmonics, r is set to 0.92 in this paper. Consequently, as shown in Fig. 7, the MRF(r=0.92) can not only achieve a similar low-frequency response with the IRF below 1 kHz, but its high-frequency amplitude response is always below −7dB after 20 kHz.

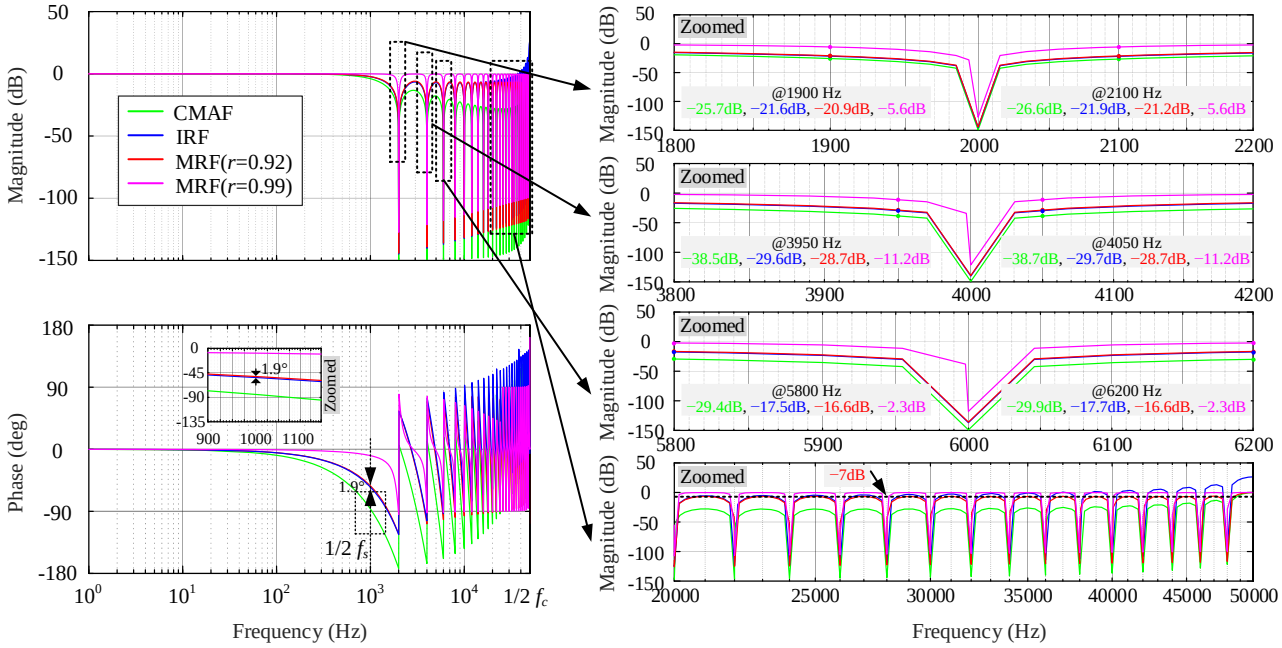


Fig. 7. Diagram of the single-loop controlled inverter-side current feedback system (MAF: moving average filter, IRF: improved repetitive filter, MRF: modified repetitive filter).

B. *Pseudo-derivative-feedback and resonant controller*

The single-loop current control diagram with inverter-side current feedback is presented in Fig. 8, where $i_{inv}^{*}(s)$ and $i_{inv}(s)$ are the inverter-side reference current and feedback current, K_p and K_i are PI controller parameters. The pseudo-derivative-feedback (PDF) controller is applied to substitute the PI controller in order to suppress the overshoot and improve the dynamic response at the same time [5], as shown in Fig. 8(a). Specifically, the PDF controller can be transformed into a PI controller, and a low-pass filter is inserted after the reference current. Moreover, the inserted low-pass filter will not change the system stability and the overshoot can be also suppressed. It can be seen from Fig. 8(b) that the delay from the low-pass filter is K_p/K_i, and increasing K_i can improve the response speed with the same open-loop bandwidth. $G_d(s)$ is the control delay, and $MRF(s)$ is the inserted modified repetitive filter to remove the sampled switching harmonics. $G_{i1v}(s)$ is the transfer function from the inverter output voltage to inverter-side current, $G_{vc}(s)$ is the transfer function from the inverter output voltage to estimated filter capacitor voltage, e^{-25sTc} is the phase lag between estimated and real filter capacitor voltage.

$$G_d(s) = e^{-1.5sT_c} \tag{10}$$

$$MRF(s) = \frac{1}{25}\frac{1-e^{-50sT_c}}{1-e^{-2sT_c}}\frac{1-r^{50}}{1-r^{2}}\frac{1-r^{2}e^{-2sT_c}}{1-r^{50}e^{-50sT_c}} \tag{11}$$

$$G_{i1v}(s) = \frac{L_2Cs^2+1}{L_1L_2Cs^3+(L_1+L_2)s} \tag{12}$$

$$G_{vc}(s) = \frac{L_2}{L_1L_2Cs^2+L_1+L_2}e^{-25sT_c} \tag{13}$$

In order to suppress the -5th and +7th grid-side current harmonics, a resonant controller $R_i(s)$ at 6th harmonic frequency is added [30].

$$R_i(s) = \frac{K_h(s\cos\theta_{hi} - 6\omega_1\sin\theta_{hi})}{s^2+(6\omega_1)^2} \tag{14}$$

where ω_1 is the fundamental angle frequency, and θ_{hi} is the compensation angle including the control delay and MRF delay. The MRF delay is similar with the simplified repetitive filter in low-frequency range, which is a quarter of switching period [5].

$$\theta_{hi} = 6\omega_1 T_c(\underset{\text{MRF delay}}{12.5} + \underset{\text{control delay}}{1.5}) \tag{15}$$

However, if using one resonant controller $R_i(s)$, the grid-side current harmonics can still freely flow into the filter capacitor and only inverter-side harmonic currents can be suppressed [31]. Therefore, the filter capacitor current should be estimated through a digital differentiator to indirectly suppress the grid-side current harmonics [30-31]. The digital differentiator [32] with a resonant controller $R_v(s)$ is inserted after the estimated filter capacitor voltage, and it is given as

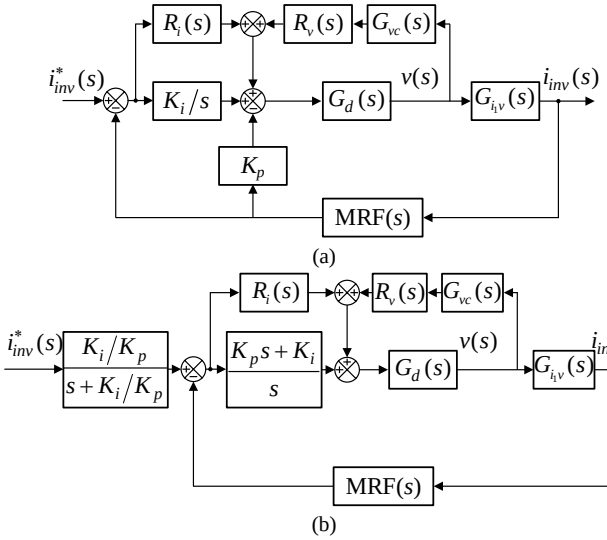


Fig. 8. Block diagram of the single-loop control. (a) PDF controller based control diagram, (b) Equivalent PI controller based control diagram.

$$R_v(s)=CR_i(s)\underbrace{\frac{1.8}{T_c}\frac{1-e^{-sT_c}}{1+0.8e^{-sT_c}}}_{\text{Digital differentiator}} \tag{16}$$

The principle to suppress the grid-side harmonics is

$$\begin{aligned}&(i_{ref}^{*}(s)-i_{ref}(s))R_i(s)+U_{cest}R_v(s)\\&\approx(i_{ref}^{*}(s)-i_{ref}(s)+sCU_{cest})R_i(s)\\&=(i_{ref}^{*}(s)-i_{ref}(s)+i_c(s))R_i(s)\\&=(i_{ref}^{*}(s)-i_g(s))R_i(s)\end{aligned} \tag{17}$$

Actually, the used grid harmonic currents suppression controller is a combination of an inverter-side current feedback control system and a grid-side current control system, where the inverter-side current is controlled by the PDF controller and the grid-side current is controlled by the resonant controller. Moreover, the controller inherits the stability characteristic of the single-loop inverter-side current control system and the harmonic attenuation capability of the single-loop grid-side current control system [31].

C. Parameter design

The open-loop transfer function of current control loop is

$$T_o(s)=(K_p+R_i(s))\frac{G_{i1v}(s)MRF(s)G_d(s)}{1-R_v(s)G_{vc}(s)G_d(s)} \tag{18}$$

Based on the LCL filter design in high-power inverters [33], the LCL parameters are set to 0.12 p.u. (L_1), 0.06 p.u. (L_2) and 0.13 p.u (C), respectively. The parameters of a down-scale three-phase grid-connected inverter are given in Table I.

TABLE I
MAIN PARAMETERS OF GRID-CONNECTED INVERTER

Symbol	Description	Value	Symbol	Description	Value
P_o	Output power	7 kW	U_{grms}	Grid voltage	220 V
L_1	Inverter-side inductor	8 mH	C	Filter capacitor	20 μF
L_2	Grid-side inductor	4 mH	C_{dc}	DC-link capacitor	297 μF
f_r	Resonance frequency	689 Hz	U_{dc}	DC-link voltage	600 V
f_s	Switching frequency	2 kHz	f_c	Sampling frequency	100 kHz
K_p	Proportional coefficient	20.5	K_i	Integral coefficient	8000
K_{pdc}	Proportional coefficient	0.03	K_{idc}	Integral coefficient	0.4
K_{ppre}	Proportional coefficient	0.1	K_{ipre}	Integral coefficient	4.5
$K_{pfastpll}$	Proportional coefficient	933	$K_{ifastpll}$	Integral coefficient	15550
$K_{pslowpll}$	Proportional coefficient	41.67	$K_{islowpll}$	Integral coefficient	723.38

According to the bandwidth oriented controller design, the open-loop bandwidth of the current control loop is set as 1/8 of switching frequency (250 Hz) and the proportional control coefficient K_p can be determined [34]. Then the integral control coefficient K_i gradually increases until the overshoot is within 5%. The bode diagram of the open-loop transfer function is shown in Fig. 9. As a result, the phase margin (PM) for IRF-based and MRF-based current controller is 47.2˚ and 48.5˚, respectively. The MRF-based controller can not only achieve similar PM with IRF-based controller, but also can suppress the high-frequency noise.

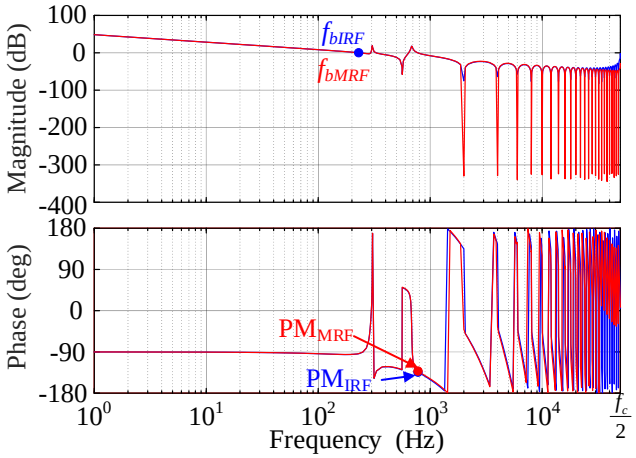


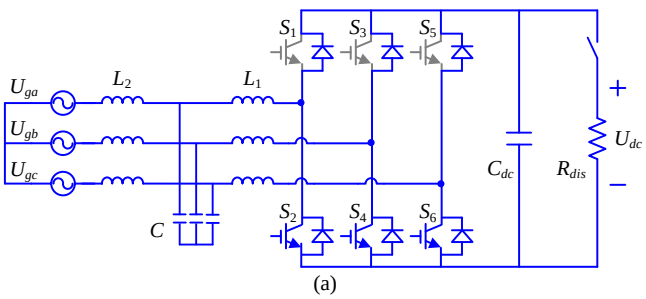
Fig. 9. Bode diagram of the current control loop with IRF and MRF (IRF: improved repetitive filter, MRF: modified repetitive filter).

IV. SOFT START-UP

It is well known that there is an inrush current during start-up process if the grid voltage information is unknown. Since the fundamental component plays a main role in the grid voltage, only the fundamental start-up current is considered and it is given as

$$L_1\frac{di_{inv}}{dt}=U_{inv}\sin(\omega t+\varphi_0)-U_c\sin(\omega t+\varphi_g) \tag{19}$$

where φ_0 and φ_g are the initial angle of inverter output voltage and filter capacitor voltage, respectively. It can be seen from (19) that the start-up current is related to the initial angle φ_0 and initial output voltage amplitude U_{inv}. Hence, it is necessary to estimate the filter capacitor voltage before start-up. Injecting zero voltage vectors is a common method, and the filter capacitor voltage can be estimated using (1). But the duration time of zero voltage vectors are not controlled, and it is usually set to three switching periods. As a result, the start-up current may be still large if the switching period is long or the inverter-side inductance is small. In order to overcome this bottleneck, a new zero voltage vector injection method is proposed. When injecting zero voltage vectors, as shown in Fig. 10(a), the upper three arms are locked and the lower three arms are in operation. When stoping injection, the inverter is in diode rectifier operation mode and the energy in the inductors is used to charge the dc-link capacitor. Hence, the inverter behavior with zero voltage vector injection is equivalent to a boost converter [35], as shown in Fig. 10(b). The input voltage U_{in} is equal to $\sqrt{3}U_c$ and the boost inductor is equal to twice larger than the inverter-side inductor L_1. R_{dis} is a discharging resistor, which is used to ensure personal safety after the inverter stops working.



(a)

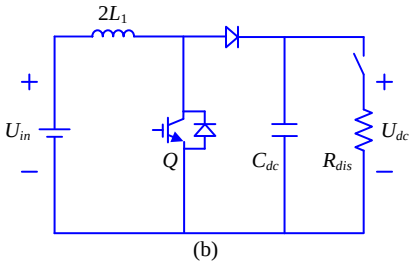


Fig. 10. Topology deviation when injection zero voltage vectors. (a) Three-phase inverter with locked three upper arms, (b) Equivalent boost converter.

In order to suppress the inrush current during zero voltage vector injection, a close-loop control with dc-link voltage feedback is proposed in Fig. 11. The boost converter will operate in the discontinuous conduction mode, because the discharging resistor R_{dis} is usually set to a high value. The critical load is smaller than the discharging resistor [36], as shown in (20).

$$R_{dis} > \underbrace{\frac{4L_1}{D_{on}(1-D_{on})^2 T_s}}_{\text{Critical load}} \tag{20}$$

where D_{on} is the steady-state duty ratio, and it is given in (21).

$$D_{on} = \sqrt{\frac{4L_1(U_{dc}^{*2} - U_{dc}^{*}U_{in})}{T_s R_{dis} U_{in}^2}} \tag{21}$$

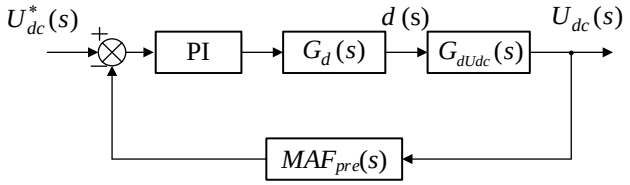


Fig. 11. Block diagram of pre-charging control.

In order to have enough sampled current data, the steady-state duty ratio should be larger than the boundary value in Section II, as shown in (22).

$$D_{on} > \frac{2}{N} \tag{22}$$

where N is the multisampling rate. Combining (21) and (22), a critical boundary for the discharging resistor is

$$R_{dis} < \frac{N^2 L_1(U_{dc}^{*2} - U_{dc}^{*}U_{in})}{T_s U_{in}^2} \tag{23}$$

Based on (23), the critical R_{dis} scales with the square of multisampling rate N. In this paper, the boundary value is 15.6 kΩ when the multisampling rate is set to 50. R_{dis} is set to 5 kΩ which is smaller than the boundary value. A moving average filter $MAF_{pre}(s)$ is added to remove the switching noise, and the size of the window is 100.

$$MAF_{pre}(s) = \frac{1}{100}\frac{1-e^{-100sT_c}}{1-e^{-sT_c}} \tag{24}$$

$G_{dU_{dc}}(s)$ is the transfer function between duty ratio and output dc-link voltage.

$$G_{dU_{dc}}(s) = \frac{2U_{dc}^{*}}{D_{on}(R_{dis}C_{dc}s+2)} \tag{25}$$

The open-loop transfer function is

$$T_{ov} = PIG_d(s)G_{dU_{dc}}(s)MAF_{pre}(s) \tag{26}$$

In terms of controller design, the bandwidth is set to 200 Hz which is 1/10 of switching frequency and the phase margin is 53˚. The bode diagram is shown in Fig. 12 and the controller parameters are presented in Table I.

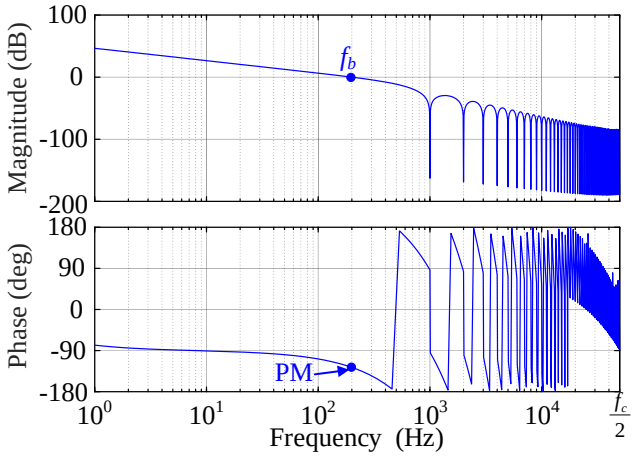


Fig. 12. Bode diagram of pre-charging control.

Moreover, the dc-link capacitor voltage reference should increase linearly, and the charging current through inductors will not have an overshoot. During the pre-charging process, the capacitor voltage can be estimated based on the method in Section II, and it is fed to a PLL to acquire the grid phase angle and fundamental grid voltage component. It is worth noting that the bandwidth of PLL affects the stability of grid-connected inverters under the weak grid, and a slow PLL is preferred [37]. In the pre-charging process, the bandwidth of PLL will not affect the stability because PLL is not used in the control of the boost converter. In order to accelerate the start-up process and acquire the grid phase angle quickly, a fast PLL is used at the beginning, and then a slow PLL substitutes the fast PLL. As shown in Fig. 13, the dc-link voltage increases linearly within 0.1s, and the transition between two PLL occurs at 0.04s.

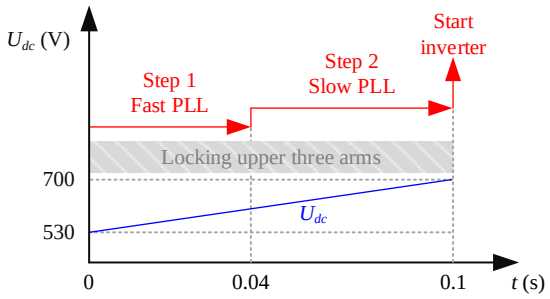


Fig. 13. Flowchart of start-up process.

The bandwidth of fast PLL is set to 150 Hz, as shown in Fig. 14, and the slow PLL uses an in-loop moving average filter where the window width is 0.02s and the bandwidth is 6.9 Hz [29]. The PI parameters for two PLLs are given in Table I. After the grid phase angle and grid voltage amplitude are known, special attention should be paid to the initial values of integrators of the current controller. According to (18), besides the initial angle, the initial amplitude of inverter output voltage U_{inv} should be the same with the filter capacitor voltage.

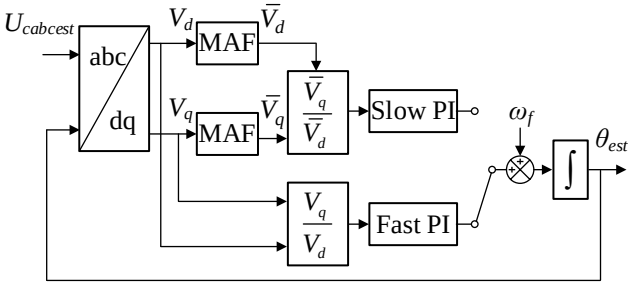


Fig. 14. Transition scheme between fast PLL and slow PLL.

Hence, the initial values are given as

$$\gamma_{dq} = U_{camp} + j0 \tag{27}$$

where U_{camp} is the amplitude of filter capacitor voltage and γ_{dq} is the initial value of integrators. In summary, the start-up procedures are given as follows:

(1) Upper three arms are locked and start pre-charging the dc-link capacitor;
(2) Sample the currents during zero voltage vectors and estimate the filter capacitor voltage;
(3) Switch fast PLL to slow PLL;
(4) When the dc-link voltage is pre-charged to the target value, set the initial values of integrators and start the inverter.

V. Experimental Results

To further verify the theoretical analysis, experiments are carried out in a down-scale three-phase grid-connected inverter with an LCL filter, as shown in Fig. 15. The grid is emulated with a Chroma Grid Simulator Model 61845. The applied half-bridge module and the control platform are a PEB-8024 module and a B-BOX RCP control platform from Imperix, respectively. The used current sensor is LEM CKSR 50-P with a bandwidth of 300 kHz. The related parameters of the grid-connected inverter are presented in Table I. Several tests are carried out including the start-up process, current reference step response and grid faults.

A. Start-up process

As shown in Fig. 16(a), when the start signal steps from 0 to 1, the dc-link voltage is pre-charged to 700 V within 100 ms and the inverter starts immediately. For the first 10 ms, the estimator cannot predict the filter capacitor voltage (see Fig. 16(b)). This is because the duty ratio is smaller than the boundary value 0.04, and the number of sampled current data during zero voltage vectors is not high enough. According to Fig. 16(c), the fast PLL helps to track the grid phase angle within 40 ms, and the transition between two PLL is smooth. Because the grid information is known in advance, the start-up inverter-side current is 3.6 A when the reference current in *q*-axis is set to zero, as shown in Fig. 16(d). Moreover, the steady-state inverter-side current is 2.8 A, which illustrates that the start-up transients are almost addressed.

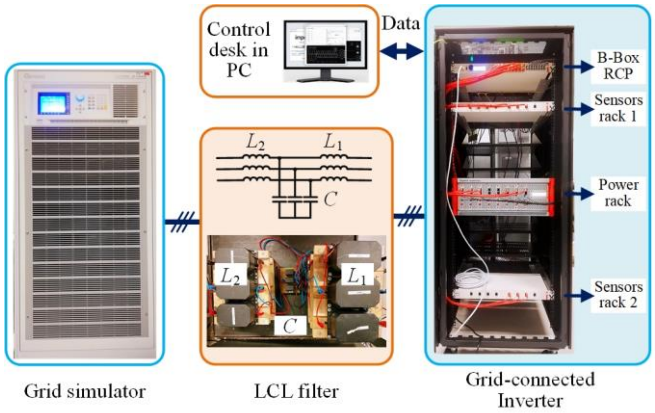


Fig. 15. A down-scaled three-phase grid-connected inverter.

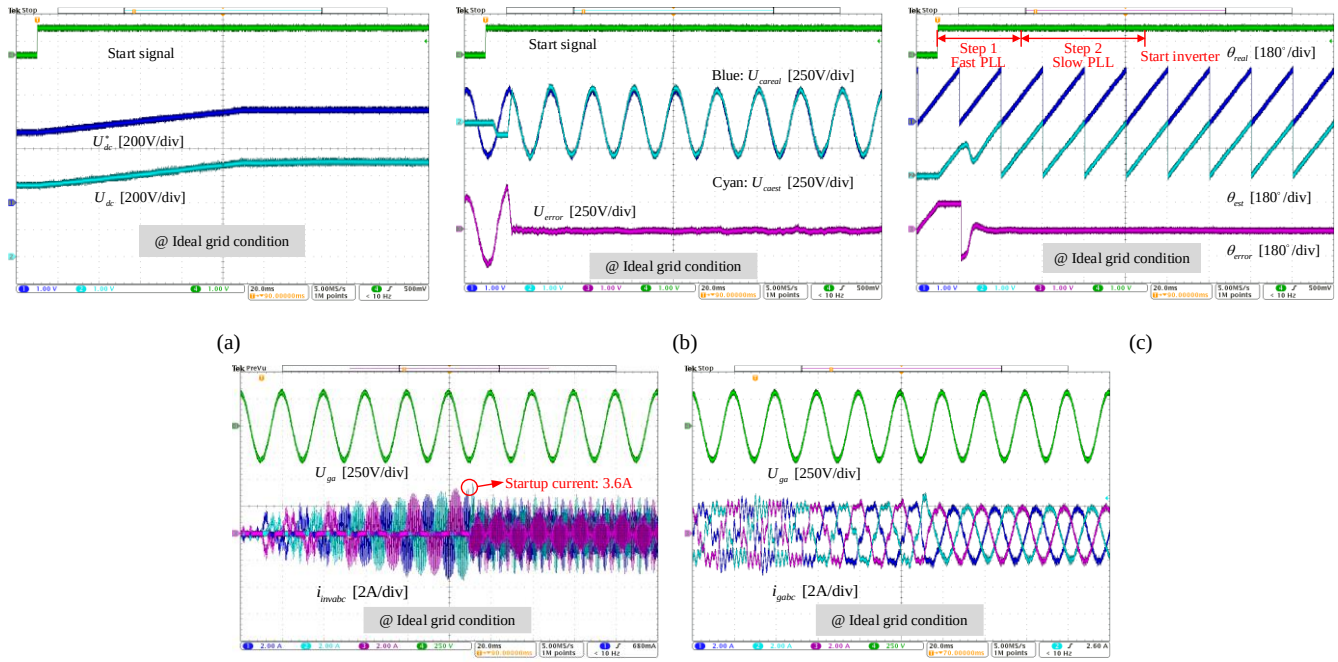


Fig. 16. Start-up process under an ideal grid condition. (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents.

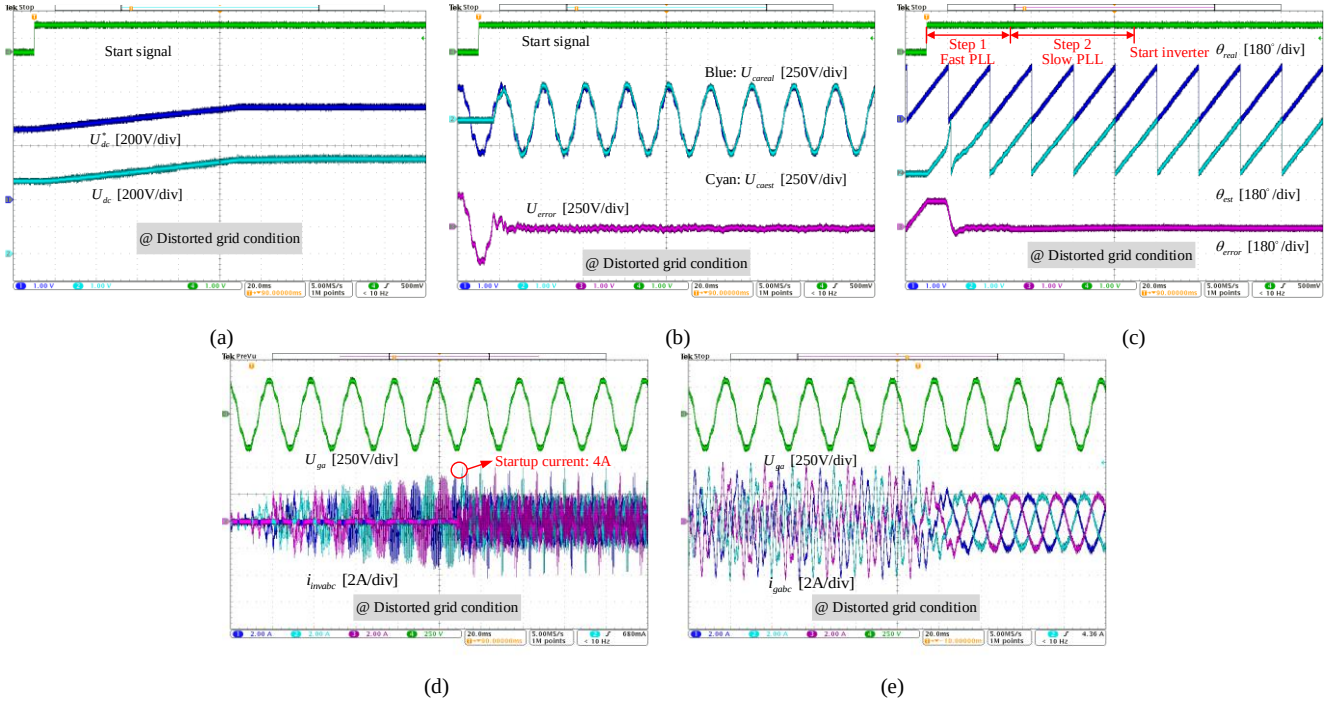


Fig. 17. Start-up process under an distorted grid condition. (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents.

The experimental results under the distorted grid condition are given in Fig. 17, and the magnitude of 5th and 7th grid harmonics are 10% of the fundamental component, respectively. Similarly, the dc-link voltage can track the reference value smoothly and accurately, as shown in Fig. 17(a). The estimated filter capacitor voltage and the estimated grid phase angle can also track the real value (see Fig. 17(b-c)). The start-up inverter-side current is 4 A and the steady-state current is also 4 A (see Fig. 17(d)). The reason is that the suppression of harmonic currents in Fig. 8 mainly improves the quality of grid-side currents, and the effect of grid harmonics on the inverter-side currents overlaps the start-up transients.

B. *Current reference step response*

When the reference current in *q*-axis steps from 7.5 A to 15 A, as shown in Fig. 18, the absolute filter capacitor voltage estimation error is always below 30 V. Moreover, due to the inverter-side inductor saturation, the filter capacitor voltage estimation error increased after the reference current changed to 15 A, as shown in Fig. 18(b). It can be observed from Fig. 18(c) that the absolute grid phase angle estimation error is always below 5˚.

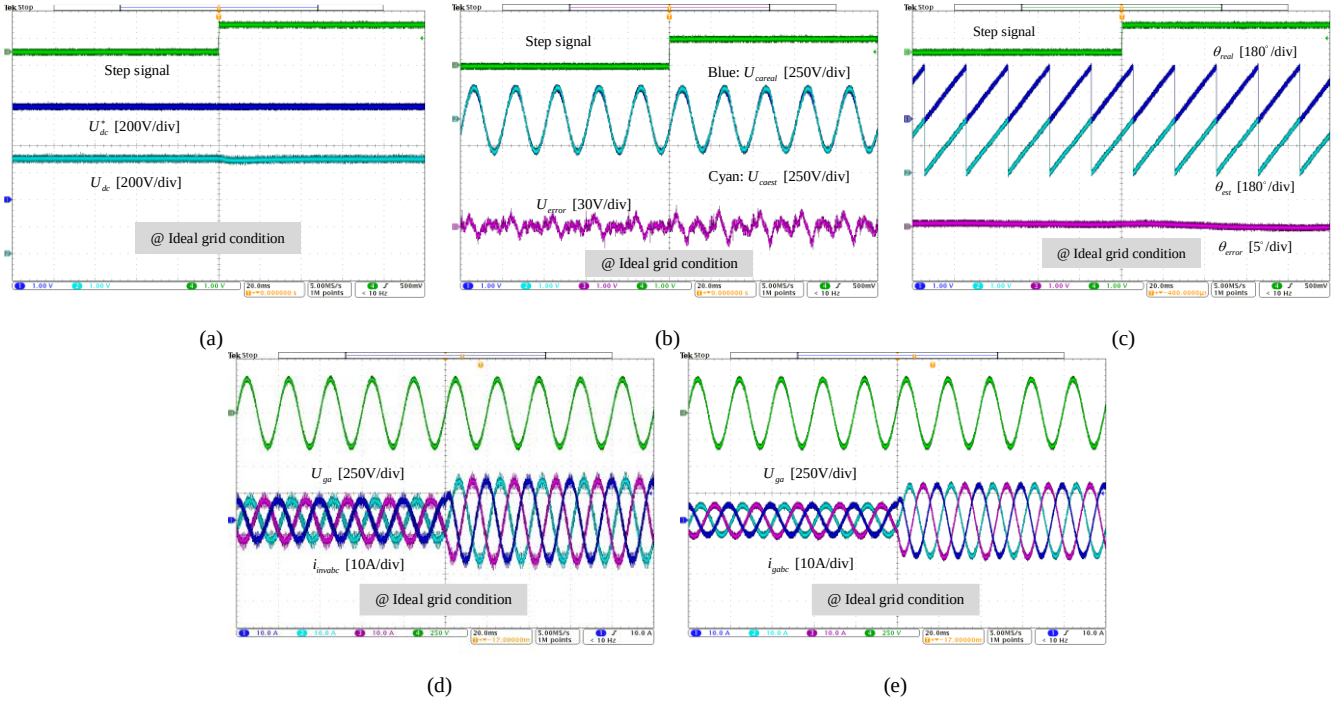


Fig. 18. Reference current step change performance under an ideal grid condition. (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents.

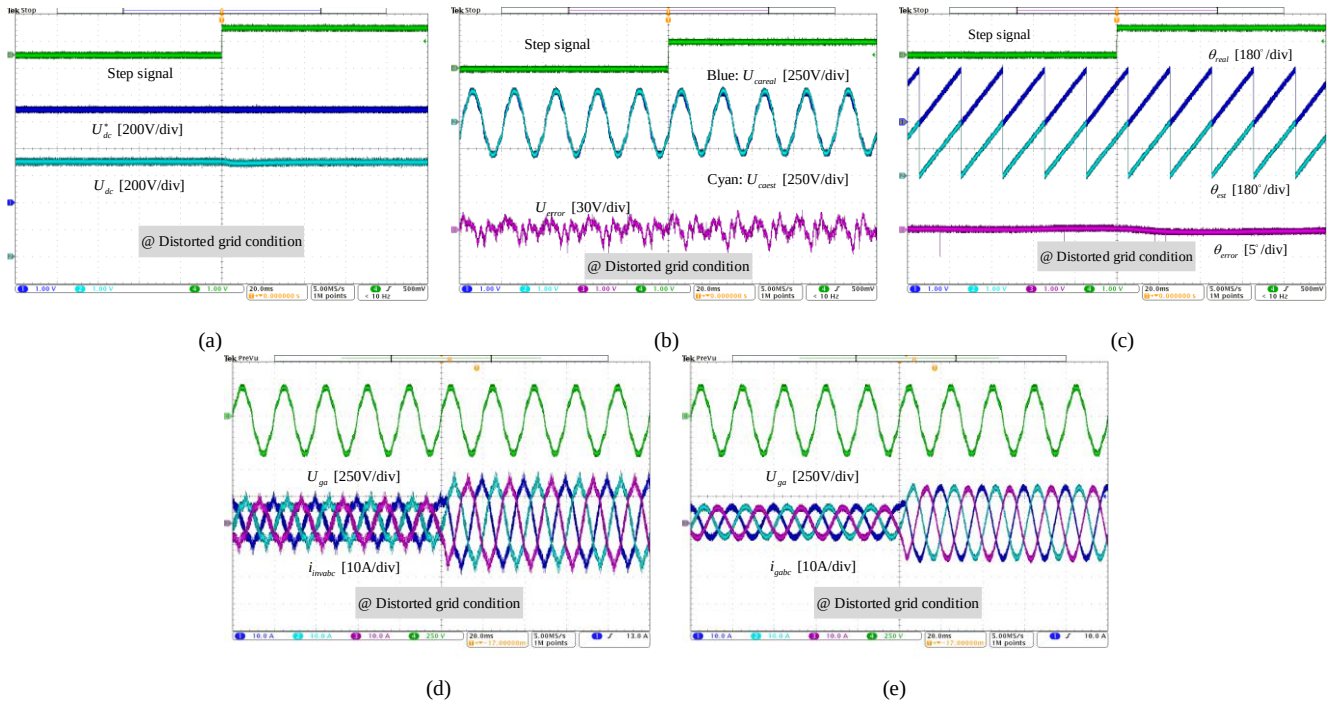


Fig. 19. Reference current step change performance under an distorted grid condition. (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents.

Under the distorted grid condition, the grid-side currents have a good quality and the inverter-side currents have more harmonics due to the harmonic currents suppression scheme, as shown in Fig. 19(d-e). The effect of inverter-side inductor saturation on the estimator accuracy also existed under a distorted grid condition (see Fig. 19(b)). It can be concluded that the estimator works well in both the steady and transient states, and the estimation errors related to filter capacitor voltage and grid phase angle are within a reasonable range.

C. 75% grid voltage sag

In terms of the transient performance of the proposed filter capacitor voltage estimator, 75% symmetrical grid voltage sag is considered and the reference current is set to 15 A. As shown in Fig. 20(b), the proposed filter capacitor voltage estimator can still track the real value. Special attention should be paid to the steady-state voltage estimation error with 75% grid voltage sag, which is smaller than the steady-state error under the normal condition. That is because the duty ratio amplitude is small and more data during zero voltage vectors are acquired. It can be seen from Fig. 20(c) that the maximum estimated grid phase angle error is 6.5°. Since the window size of MAF-based PLL is 20 ms, there is a delay between the estimated grid phase angle and sag signal. The inverter-side currents and grid-side currents are presented in Fig. 20(d-e).

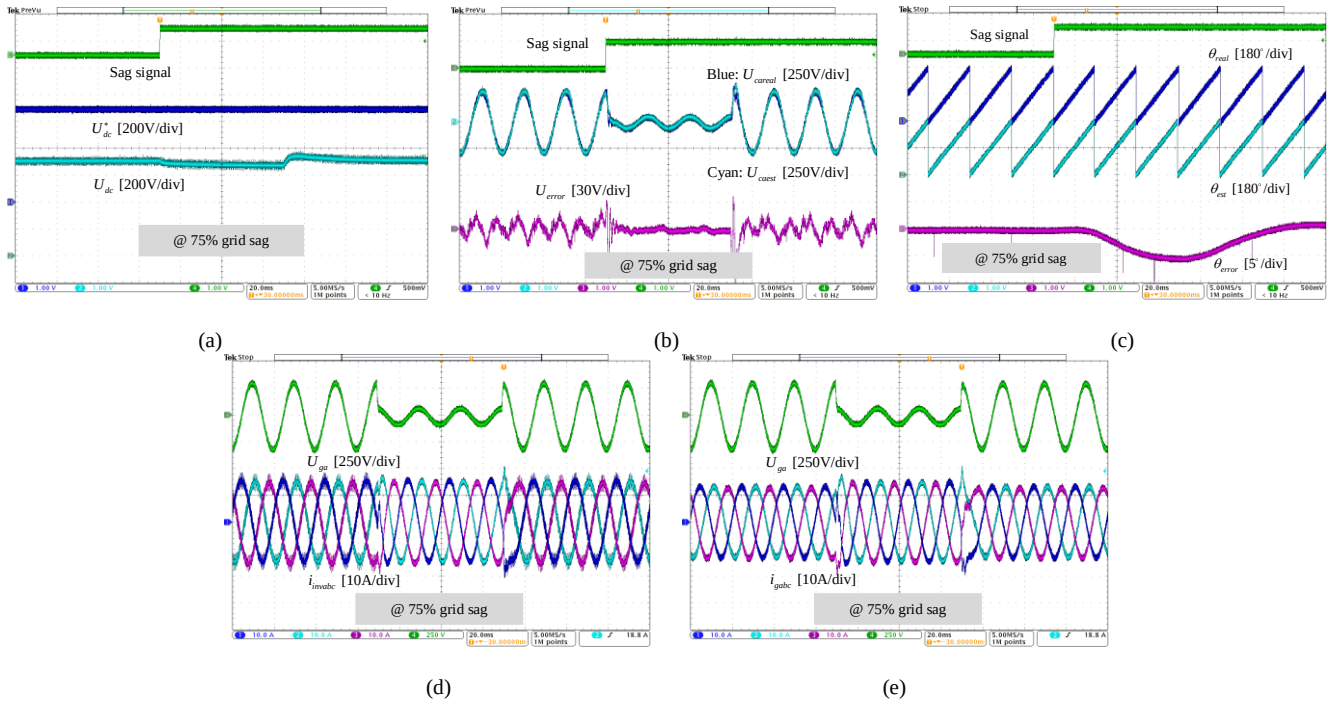


Fig. 20. Experimental results under a 75% grid voltage sag. (a) Dc-link voltage, (b) Estimated filter capacitor voltage, (c) Estimated grid phase angle, (d) Inverter-side currents, (e) Grid-side currents.

VI. Conclusion

In this paper, a line voltage sensorless control scheme is proposed for a high-power three-phase LCL-filtered grid-connected inverter. The inverter-side currents are multisampled to reduce the control delay and improve the bandwidth. At the same time, the multisampled currents during zero voltage vectors are reused to estimate the filter capacitor voltage. The main contribution is threefold:

1) Based on recursive linear regression, the filter capacitor voltage is estimated through the multisampled inverter-side current data during zero voltage vectors. The multisampling rate selection considering duty ratio limitation is discussed, and the practical implementation on chip is also given.

2) Since the improved repetitive filter from the multisampling current controller will amplify the high frequency noise when using a high multisampling rate (e.g. 50), a modified repetitive filter is proposed which can not only achieve a similar low-frequency response with the improved repetitive filter, but also provides low high-frequency amplitude response.

3) A boost converter based start-up concept is proposed to pre-charge the dc-link capacitor and estimate the filter capacitor voltage in advance. In addition, the PLL transition and initial values setting of the current controller is proposed to further optimize the start-up process.

Finally, the experimental results on a down-scale inverter validate the effectiveness of the proposed method.

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