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A Unified Capacitor Stress Emulation Method for High Power Converter Applications

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***Abstract*—This paper proposes a unified capacitors stress emulation method, which has two unique test capabilities: 1) concurrent electrical stress emulation to AC capacitors and DC capacitors; 2) different electrical stress levels (including different ripple current, ripple voltage, and DC voltage) can be individually controlled for the testing samples. It preserves the advantages of a recently reported method with a minimum required power supply and is robust to testing sample degradation. This method is suitable for application-oriented stress emulation testing with different types of DC / AC capacitors and multiple electrical stresses in high power converter systems. The circuit architecture and testing ability of this method are presented. Moreover, analytical models are derived to size the key components to realize various testing requirements. Proof-of-concept experimental results are presented to verify the feasibility of the proposed test method.**

***Index Terms*—Stress emulation, DC capacitors, AC capacitors, electrical stresses, high power converter, key components.**

I. Introduction

CAPACITOR is typically a high-failure component in power electronic converter systems and its reliability has become a major focus of attention in recent years [1]. The failure or deterioration of capacitors can lead to a decline in filtering capabilities, which can ultimately lead to the overstressing of components and even the catastrophic failure of the converter system [2]. The realistic stress emulation testing is a significant part of the performance characterization and reliability analysis of capacitors. Through these tests, reliable capacitor parametric models can be developed and design margins can be optimized to ensure the long-term reliability and safety of the system [3].

There are two emerging demands for capacitor testing in high power converter applications. On the one hand, it is desirable to perform application-oriented testing with realistic conditions. For the lifetime model and the accelerated aging model, it is necessary to determine its pending empirical coefficients by comparing multiple realistic stresses [4]. In the Safe Operating Area (SOA) testing, different stress ranges are required to analyze the boundary conditions [5] [6]. On the other hand, it would bring new values if AC and DC capacitors can be concurrently tested with the capability of individual stress control. This can significantly reduce overall test time compared to single stress testing by allowing for concurrent multi-stress control [7] [8]. The testing parameters of the capacitor stress emulation generally include ripple voltage, ripple current, and DC voltage (for DC capacitors) and the environmental conditions (e.g., temperature, humidity, etc.), as shown in Fig 1 [9]. Different ambient temperatures and humidity can be simulated by the climatic chambers [10]. Therefore, performing multiple electrical stresses under realistic conditions is critical for AC and DC capacitor testing in high power converter applications.

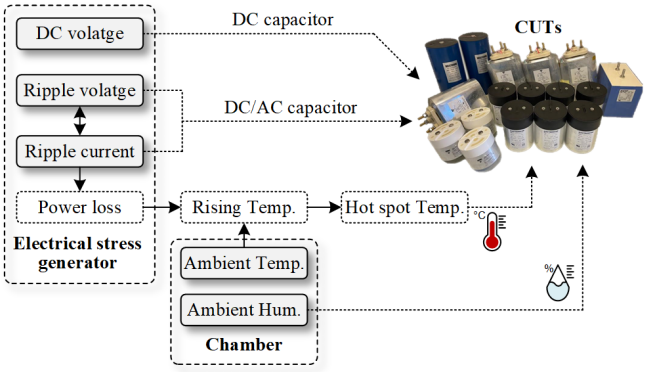

Fig. 1. Stress targets for capacitor stress emulation testing.

Recent studies have made significant efforts toward the capacitor stress emulation, as shown in Table I. In [11], [12], and [13], a voltage source and a current source converter are connected in parallel to apply the DC voltage and ripple current for CUTs (Capacitors Under Testing). However, the scope of testing electrical stresses in those methods is limited by the size of the power supplies. The commercial ripple current testers emulate up to 30∼100 V ripple voltage and 10∼30 A ripple current for CUTs, but the output ripple power range is restricted to 1k VA [14] [15]. The [16] and [17] use a circuit structure in which a converter is connected in series with CUTs, and the ripple current can be configured according to the converter specifications. Nevertheless, the converter needs to directly withstand the DC voltage component of the CUTs in those methods, which may not be feasible for high-power capacitor testing with thousands of volts of DC voltage. The power converters are used in the voltage sources with the fixed 120 °C three-phase symmetrical voltage in [18] [19]. The ripple voltage and ripple current can be controlled according to the control system, and the DC voltage of the CUTs can be expanded based on the additional DC bias supply.

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TABLE I
COMPARISONS OF THE EXISTING TEST METHODS.

Testing ability in existing capacitor stress emulation methods					Applicable field	Electrical stress emulation range	Reference
DC voltage		Ripple current and ripple voltage (pk to pk)					
10V	Single stress	1A	4V	Single stress	Low power Al capacitors	<1kW power	[11]
-	Single stress	10A	1V	Single stress	Low power Al capacitors		[12]
-	Single stress	< 0.1A	600V	Single stress	Low power ceramic capacitors		[13]
500V	Single stress	30A	30V	Single stress	Al capacitors / Ceramic capacitors	1kW~10kW	[14]
5000V	Single stress	30A 10A	30V 100V	Single stress	Medium power film capacitors		[15]
3000V	Single stress	600A	30V	Single stress	Medium power Film capacitors	10kW~100kW	[16]
	Single stress	18A	1000V	Single stress	Low power Film capacitors		[17]
400V	Single stress	80A	150V	Single stress	Al capacitors and medium power film capacitors		[18]
>3000V	Single stress	>1000A	>1000V	Single stress	High power film capacitors	MW power	[19]
>3000V	Different stress levels (Individually controlled)	>1000A	>1000V	Different stress levels (Individually controlled)	High power film capacitors	MW power	Lack

However, only single electrolytic stresses can be emulated at the same time in those testing methods. Existing methods for emulating realistic high-power capacitor electrical stress have limitations, either being unable to provide the megawatt-level testing requirements in high-power applications [11]-[18] or being able to provide such requirements but with the need for multiple test benches or longer testing time [19].

The authors have published a conference paper [20] that proposes a unified capacitor stress emulation method for concurrently testing DC and AC capacitors. This journal version has the following additional contributions: 1) Auxiliary inductors and bypass capacitors are proposed for the testing circuit, enabling individual control of the voltage and current stresses of multiple capacitor samples, which cannot be achieved by the method in [20]; 2) Analytical models and a design flow are provided which can be used for designing the testing system to fulfill certain specifications; and 3) Extended experimental testing and application scenarios are presented.

The structure of this paper is as follows: Section II presents the concept, circuit architecture, and test abilities of the proposed method; Section III gives the design models and typical testing scenarios; Section IV discusses the experimental verification, followed by the conclusions.

II. PROPOSED STRESS EMULATION METHOD

A. Circuit architecture of the proposed method

The circuit architecture of the proposed method is shown in Fig. 2. It is an extension of the circuit presented in the conference paper [20] by adding an auxiliary inductor module and a bypass capacitor module. Besides the capability to test both DC capacitors and AC capacitors concurrently, the AC voltage, ripple current, and DC bias voltage of the CUTs in different branches can be individually controlled.

1) Electrical stress generator and controller: The electrical stress generator 1 is used to apply ripple voltage and ripple current for CUTs. It generates sinusoidal current to the CUTs through the low voltage (LV) power supply U_L and the power stack. The electrical stress generator 2 provides the DC bias voltage if necessary, denoted as the high voltage (HV) power supply U_H, the filter capacitor C_{DCH}, and the stack resistors R_H are included.

In the controller, a three-phase SVPWM (Space Vector Pulse Width Modulation) scheme is used to modulate the three-phase current with the sinusoidal waveform. This controller can operate in either voltage mode or current mode to control the ripple voltage and ripple current, respectively.

2) Auxiliary inductor module: This module enables the individual ripple voltage and ripple current control of the CUTs in different testing branches. The auxiliary inductors provide reactive power that is opposite in phase to the ripple current and voltage for the CUTs, thereby boosting the output ripple voltage and ripple current of the main inductor. By selecting the different inductance of the auxiliary inductors, the individual ripple voltages and ripple currents for the CUTs are provided in different branches. The ripple voltage and ripple current can be maintained in the presence of capacitor degradation in any branch by the closed-loop control.

3) CUTs module: The CUTs can be Y- or Δ-connection for AC capacitors, and Y-connection for DC capacitors, with either a single or multiple parallel connections. The required ripple voltage and ripple current of the CUTs are provided by the electrical stress generator 1 and the auxiliary inductor module. For DC capacitor testing, the DC component voltage of the CUTs is provided by the electrical stress generator 2 and bypass capacitor module. The parallel resistors of CUTs R_{test} can serve dual purposes. On one hand, they can be used to discharge the CUTs at the end of the testing process, and on the other hand, they can divide the DC voltage component based on bypass capacitor modules.

4) Bypass capacitor module: This module is for provide individual DC-bias control of the DC capacitors in different testing branches. The capacitors and resistors in the circuit are responsible for dividing the output DC voltage of the HV power supply. By selecting specific capacitance C_{byp} for bypass capacitors, it is possible to provide controllable DC voltage components to the CUTs of different branches in the start up stage. The configured parallel resistors R_{byp} can serve dual purposes. On one hand, they can maintain a steady-state DC voltage component, and on the other hand, they can be used to discharge the CUTs at the end of the testing process. Thus, the DC voltage component can maintain a given value at steady-state, despite any changes to the capacitance of the CUTs due to aging [21]. The selection of bypass capacitors and parallel resistors enables the provision of individual DC voltage components to CUTs and ensures that the DC voltage remains constant throughout the testing process.

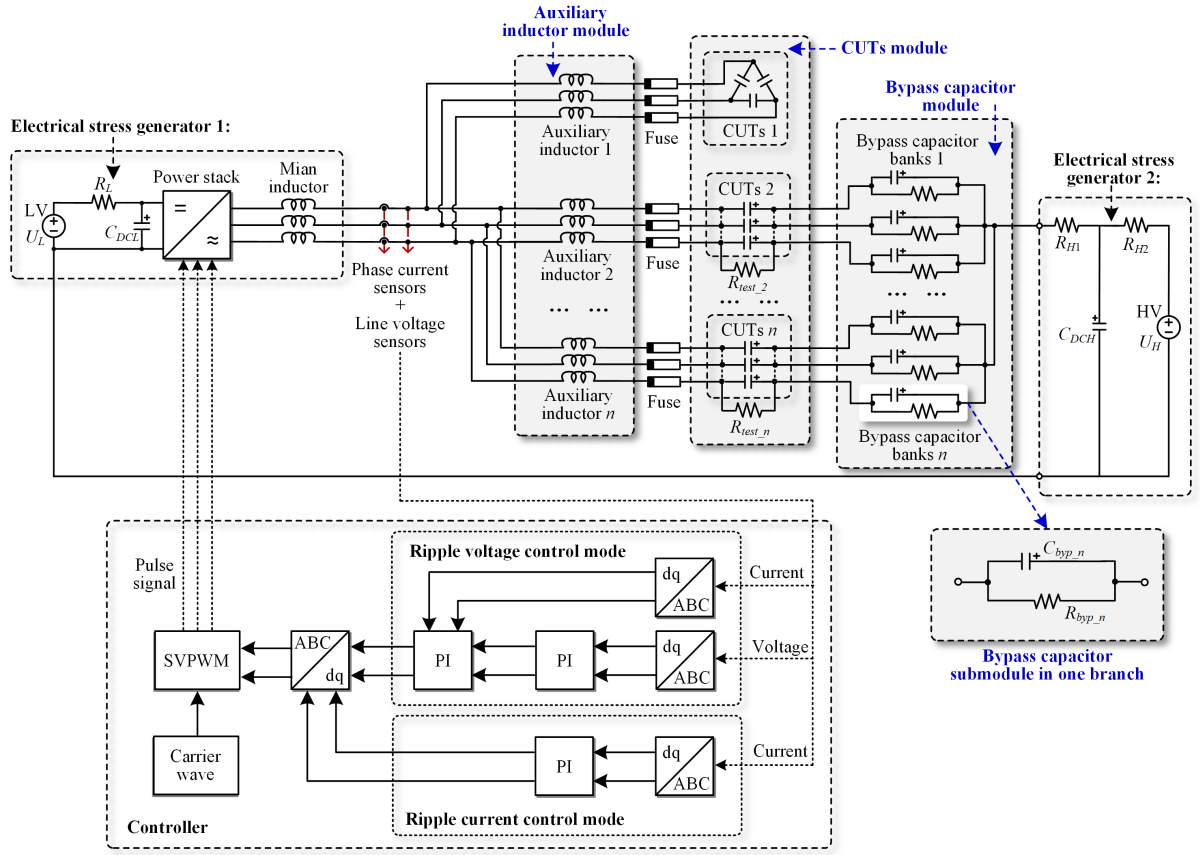


Fig. 2. Circuit architecture of the unified capacitors stress emulation method.

B. Testing scenarios and the corresponding circuit configurations

Table II shows ten achievable testing scenarios by configuring the circuit architecture shown in Fig. 2. Out of the them, Scenarios 3 to 10 are unique by the proposed method, with Scenario 7 being presented in [20]. Scenarios 3 and 4 support the function of "individual ripple voltage and ripple current", Scenario 5 supports the function of "individual DC voltage", and Scenario 7 supports the function of "concurrent AC and DC capacitor testing". Moreover, Scenario 6 supports both functions of "individual ripple voltage and ripple current" and "individual DC voltage". Scenario 8 supports both functions of "individual ripple voltage and ripple current" and "concurrent AC and DC capacitor testing". Scenario 9 supports both functions of "individual DC voltage" and "concurrent AC and DC capacitor testing". Scenario 10 supports all three functions.

When the single electrical stress is applied in the AC capacitors and DC capacitors testing, the RMS (root mean square) value of ripple voltage U_{ripple} and ripple current I_{ripple}, and the DC voltage component U_{DC} for the DC capacitors of CUTs can be shown as: (Scenario 1, 2, and 7 in Table II)

$$\begin{cases} U_{ripple} = U_{line} \quad (\Delta\text{-connection AC capacitors}) \\ U_{ripple} = \dfrac{1}{\sqrt{3}} U_{line} \quad (\text{Y-connection AC/DC capacitors}) \\ I_{ripple} = I_{AC} = U_{ripple} \times 2\pi f_R C_{test} \\ U_{DC} = U_{HV} - \dfrac{1}{2} U_{LV} \quad (\text{DC capacitors}) \end{cases} \tag{1}$$

where U_{line}, I_{AC}, C_{test}, and f_R represent the line RMS voltage between the inductors and CUTs, the AC-side RMS current, the capacitance of the CUTs, and the ripple frequency, respectively. In the DC capacitors testing, U_{HV} and U_{LV} represent the output voltage of the HV power supply and the LV power supply, respectively.

The auxiliary inductors can boost the output ripple voltage and ripple current based on the main inductor. On the AC side, the reactive power of the CUTs Q_C and the auxiliary inductors Q_L can be given as:

$$\begin{cases} Q_C = \dfrac{I_{ripple}^2}{2\pi f_R \times C_{test}} \\ Q_L = I_{ripple}^2 \times 2\pi f_R \times L_{aux} \end{cases} \tag{2}$$

where L_{aux} is the inductance of the auxiliary inductor in different branches.

When individual ripple current and ripple voltage in different branches are applied to CUTs, the RMS value of ripple current I_{ripple_i} and the RMS value of ripple voltage U_{ripple_i} of the CUTs at the i^{th} branch are given by: (Scenario 3, 4, 6, 8, and 10 in Table II)

$$\begin{cases} I_{ripple\_i} = \dfrac{|Q_c - Q_L|}{U_{ripple\_0}} = \dfrac{U_{ripple\_0}}{|\ \dfrac{1}{2\pi f_R C_{test\_i}} - 2\pi f_R L_{aux\_i}\ |} \\ U_{ripple\_i} = \dfrac{I_{ripple-i}}{2\pi f_R C_{test\_i}} = \dfrac{U_{ripple\_0}}{|\ 1 - 4\pi^2 f_R^2 L_{aux\_i} C_{test\_i}\ |} \end{cases} \tag{3}$$

TABLE II
TEN TESTING SCENARIOS WHICH CAN BE ACHIEVED BY THE PROPOSED CIRCUIT ARCHITECTURE SHOWN IN FIG. 2.

Testing scenarios	CUTs	Ripple voltage and ripple current	DC voltage	Electrical stress generator 1	Electrical stress generator 2	Auxiliary inductor module	Bypass capacitor module	Can be done by existing methods or new possibilities
1	AC capacitors	Single	-	√	-	-	-	Existing methods [1] – [19]
2	DC capacitors	Single	Single	√	√	-	-	
3	AC capacitors	Individual	-	√	-	√	-	Enabled by the extended ideas proposed in this journal paper
4	DC capacitors	Individual	Single	√	√	√	-	
5	DC capacitors	Single	Individual	√	√	-	√	
6	DC capacitors	Individual	Individual	√	√	√	√	
7	DC + AC capacitors	Single	Single	√	√	-	-	[20] (Conference version)
8	DC + AC capacitors	Individual	Single	√	√	√	-	Enabled by the extended ideas proposed in this journal paper
9	DC + AC capacitors	Single	Individual	√	√	-	√	
10	DC + AC capacitors	Individual	Individual	√	√	√	√	

where U_{ripple_0} represents the output ripple voltage of the main inductor and C_{test_i} represents the capacitance of the CUTs in the i^{th} branch.

In addition, considering that the individual DC voltage in different branches are applied to DC capacitors, the DC voltage components U_{DC_i} of CUTs at the ith branch are given (Scenario 5, 6, 9 and 10 in Table II).

At the start up of the testing (charge the CUTs and the bypass capacitors):

$$U_{DC\_i} = \frac{C_{byp\_i}}{C_{test\_i} + C_{byp\_i}} \left(U_{HV} - \frac{1}{2} U_{LV} \right) \tag{4}$$

At the steady state:

$$U_{DC\_i} = \frac{R_{test\_i}}{R_{test\_i} + R_{byp\_i}} \left(U_{HV} - \frac{1}{2} U_{LV} \right) \tag{5}$$

where R_{test_i}, R_{byp_i}, C_{byp_i} represents the parallel resistance of CUTs, the parallel resistance of the bypass capacitor, and the capacitance of the bypass capacitor in the ith branch, respectively. The resistance of parallel resistors set to 100 kΩ∼1 MΩ. In this state, the parallel resistance is much smaller than the insulation resistance of the film capacitors (typical value: 10^3 MΩ∼10^6 MΩ) [22], thus coping with the effects of insulation resistance temperature and aging changes.

III. DESIGN MODELS FOR COMPONENT PARAMETERS

The properly designed components can effectively minimize excessive margins in parameters. The identification of suitable design components for the testing method, based on application-specific testing requirements, is of concern to users. This section quantitatively analyzes the design parameters of the key components in the testing method. The analytical equations derived are universal and can be applied to the electrical stress requirements of different specifications and quantities of the CUTs testing. The presented numerical results in figures are based on a specific design case with the specifications described.

A. Power stack selection

The selection of the power stacks is determined primarily by the output current. When the required output current of the power stack is larger, the cost and volume of the power stack increase accordingly [23]. When the single ripple current and ripple voltage are applied to CUTs, the RMS value of the required output current for the power stack I_{PS-out} can be expressed as:

$$I_{PS-out} = mU_{rate} \times (2\pi f_R \times C_{test}) \tag{6}$$

where m and U_{rate} represent the ripple voltage acceleration factor and the rate ripple voltage for CUTs.

When the individual ripple current and ripple voltage are applied in different branches, the I_{PS-out} can be given as:

$$I_{PS-out} = \sum_{i=1}^{n} m_i U_{rate} \times \left(2\pi f_R \times C_{test\_i} \right) \tag{7}$$

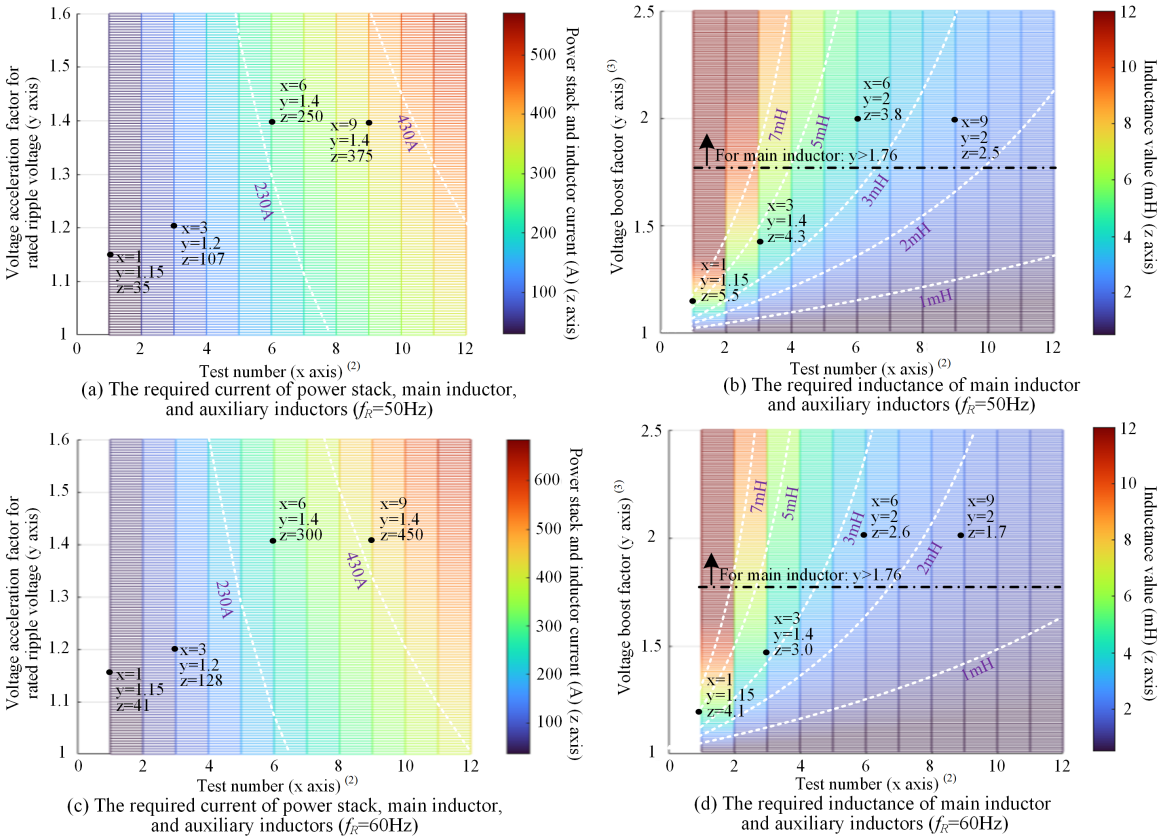
where m_i represent the ripple voltage acceleration factor for CUTs in the i^{th} branch.

As shown in Fig. 3 (a) and (c), the required output current of the power stack with different testing requirements is obtained. The results indicate that when the voltage acceleration factor is 1.4 and the number of CUTs is 9, the current required by the power stack is 375 A at the ripple frequency of 50 Hz. When the ripple frequency is 60 Hz, the required output current of the power stack rises to 450 A in this case.

B. Main inductor and auxiliary inductors design

The selection of the three-phase inductors is determined primarily by the inductance and rated current. When the inductance and the rated current of inductors are larger, the cost and volume of the inductors increase accordingly [24]. The primary function of the inductors is to boost the ripple voltage and ripple current. The main inductor can boost the output voltage of the power stack, and the auxiliary inductors can further boost the output voltage of the main inductor. When the single ripple current and ripple voltage are applied, the required inductance L_{main} and required current I_{L-main} of the main inductor can be given as:

$$\begin{cases} I_{L-main} = mU_{rate} \times (2\pi f_R \times C_{test}) \\ L_{main} = \left(1 - \dfrac{U_m}{U_{ripple}} \right) \times \dfrac{1}{4\pi^2 f_R^2 C_{test}} \end{cases} \tag{8}$$



(a) The required current of power stack, main inductor, and auxiliary inductors (f_R=50Hz)

(b) The required inductance of main inductor and auxiliary inductors (f_R=50Hz)

(c) The required current of power stack, main inductor, and auxiliary inductors (f_R=60Hz)

(d) The required inductance of main inductor and auxiliary inductors (f_R=60Hz)

Fig. 3. Selection of power stacks and parameters design of inductors. (1. CUTs parameters: Δ – connection AC capacitors; capacitance of single CUT C_{test_i} : $75\mu F$; rate ripple voltage $U_{rate} = 730V$.) (2. For the power stack and main inductor, the test number means the total number of CUTs in each of the three-phase branches; for the auxiliary inductors, the test number means the number of CUTs in this three-phase branch.) (3. For the main inductor, the voltage boost rate refers to the ratio of the main inductor output voltage to the power stack output voltage (530V); for auxiliary inductors, the voltage boost rate refers to the ratio of the auxiliary inductors output voltage to the main inductor output voltage.) (4. In (a) and (c), the ranges of 230 A and 430 A represent the rated output current of two power stacks [23].)

where U_m is the output RMS voltage in the power stack.

When the individual ripple currents and ripple voltages are applied in different branches, the required inductance L_{main} and required current I_{L-main} of the main inductor can be given as:

$$\begin{cases} I_{L-main} = \sum_{i=1}^{n} m_i U_{rate} \times \left(2\pi f_R \times C_{test\_i}\right) \\ L_{main} = \left(1 - \dfrac{U_m}{U_{ripple\_0}}\right) \times \dfrac{1}{4\pi^2 f_R^2 C_{test}} \end{cases} \tag{9}$$

Its required inductance L_{Aux_i} and required current I_{L-Aux_i} of the auxiliary inductors in the i^{th} branch can be given as:

$$\begin{cases} I_{L-Aux\_i} = m_i U_{rate} \times \left(2\pi f_R \times C_{test\_i}\right) \\ L_{Aux_i} = \left(1 - \dfrac{U_{ripple-0}}{U_{ripple\_i}}\right) \times \dfrac{1}{4\pi^2 f_R^2 C_{test\_i}} \end{cases} \tag{10}$$

The second function of the AC side inductor in this circuit architecture is filtering, which can convert the output square wave voltage of the power stack into the required sinusoidal ripple voltage. In the circuit architecture of this test method, the inductors and CUTs form an LC filter loop. The relationship between the cut-off frequency f_{cut} and the ripple frequency f_R can be used to characterize its filtering range. Its filter capability can be expressed by the relationship between the cut-off frequency f_{cut} and the ripple frequency f_R [25]. The ripple frequency should satisfy:

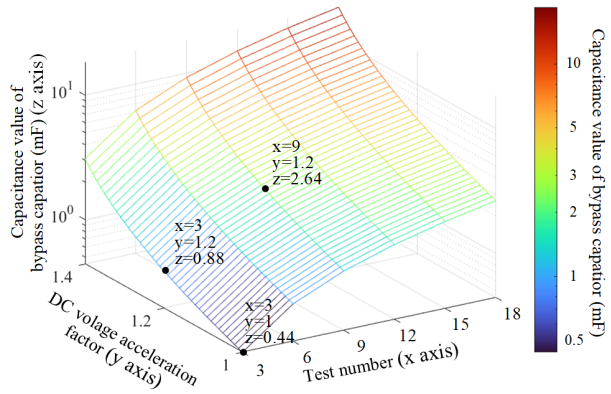
$$f_R > \frac{1}{2} f_{cut} = \frac{1}{2} \times \frac{1}{2\pi \times \sqrt{L_{\text{main}} C_{test}}} \tag{11}$$

Therefore, the inductance of the main inductor should satisfy:

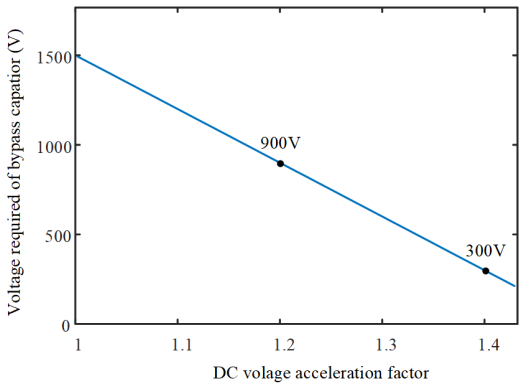
$$L_{main} > \frac{1}{16\pi^2 f_R^2 C_{test}} \tag{12}$$

The performance of the main inductor and the auxiliary inductors with respect to the current requirements is depicted in Fig. 3 (a) and (c). The results indicate that the output current of the main inductor is consistent with the output current of the power stack. For example, when the voltage acceleration factor for a single CUT is 1.15, the current required by the auxiliary inductor in this branch is 35 A. When the voltage acceleration factor with three CUTs is 1.2, the current required by the branch auxiliary inductor is 107 A in this branch.

The required inductance of the main inductor and the auxiliary inductors with different numbers of CUTs are shown in Fig. 3 (b) and (d). The results demonstrate that, when



(a) The required capacitance of bypass capacitor



(b) The required voltage of bypass capacitor

Fig. 4. Design parameters of bypass capacitor. (CUTs parameters: Y-connection DC capacitors; the capacitance of single CUT C_{test_i} : $220\mu F$; rate DC voltage U_{rate} : $3000V$; HV voltage U_{HV} : $5000V$; LV voltage U_{LV} : $1000V$; test number is the total number of CUTs in each of the three-phase branches.)

the boost voltage rate is 2 and the CUTs number is 9, the required inductance of the main inductor is 2.5 mH and 1.7 mH, respectively, for generating 50 Hz and 60 Hz ripple frequency. Additionally, when the boost voltage rate is 1.4 and the CUTs number is 3, the required inductance of the auxiliary inductor in this branch is 4.3 mH and 3.0 mH, corresponding to the ripple frequency at 50 Hz and 60 Hz, respectively. Moreover, according to (11) and (12), the inductance of the main inductor is constrained by the cut-off frequency. In this case, the inductance of the main inductor should not be lower than the range of 1.76 times the voltage boosting rate.

C. Bypass capacitor and its parallel resistor design

The selection of the bypass capacitor is primarily determined by the capacitance and rated voltage. The cost and volume of the capacitor are positively related to the capacitance and rated voltage [26].

Similarly, the selection of the parallel resistor depends on its resistance and power.

Different bypass capacitors and parallel resistors can provide individual DC voltage for the CUTs in different branches. The required bypass capacitance C_{byp_i} and parallel resistance R_{byp_i} in the ith branch can be expressed as:

$$\begin{cases} C_{byp\_i} = \dfrac{C_{test\_i} \times m_{DC\_i} U_{rate\_DC}}{\left(U_{HV} - \dfrac{1}{2}U_{LV}\right) - m_{DC\_i} U_{rate\_DC}} \\ R_{byp\_i} = \dfrac{R_{test\_i} \times \left(\left(U_{HV} - \dfrac{1}{2}U_{LV}\right) - m_{DC\_i} U_{rate\_DC}\right)}{m_{DC\_i} U_{rate\_DC}} \end{cases} \tag{13}$$

where m_{DC_i} represents the DC voltage acceleration factors in the i^{th} branch and U_{rate_DC} represents the rated DC voltage for DC capacitors.

The bypass capacitors and parallel resistors need to withstand partial DC voltage division provided by the HV power supply, which should satisfy:

$$U_{byp} = U_{HV} - \frac{1}{2}U_{LV} - m_{DC\_i} U_{rate\_DC} \tag{14}$$

The selection of the bypass capacitors with different CUTs numbers and different DC voltage acceleration factors are depicted in Fig. 4. The results indicate that as the number of CUTs and the DC voltage acceleration factors increase, the required capacitance of the bypass capacitors in this branch increases and the rated voltage of the bypass capacitors decreases accordingly. For example, when the voltage acceleration factors are 1.0 and 1.2, the capacitance of the bypass capacitors in this branch are 0.44 mF and 0.88 mF, respectively. In this case, the rated voltage of the bypass capacitors in this branch is 1500 V and 900 V, respectively.

D. Power supply sizing

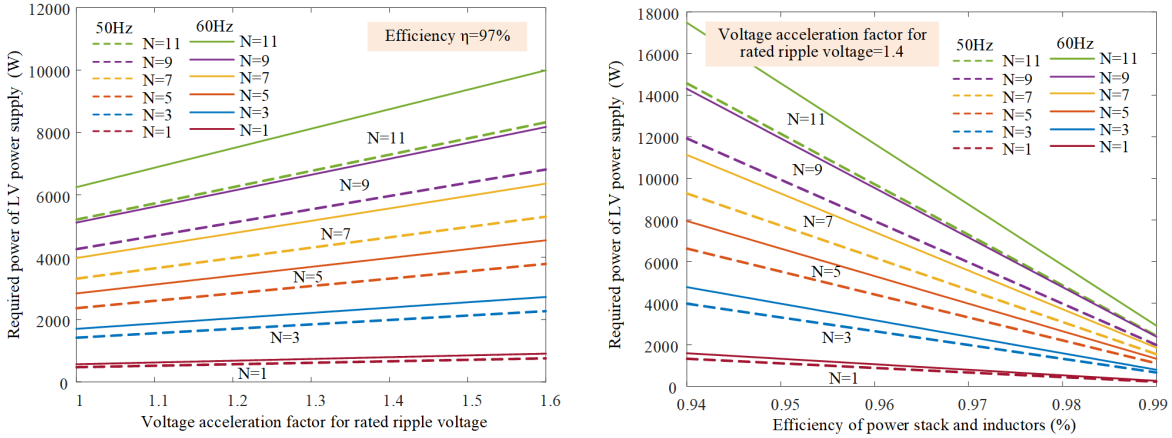
The selection of the power supply is determined primarily by the output power. The cost and volume of the power supply increase accordingly with the required output power of the power supply [27]. In the proposed testing method, the power losses of the power stack, inductors, and CUTs are provided by the LV power supply. And the output voltage of the LV power supply is limited by the output voltage of the power stack U_m. The power requirement P_{LV} and the output voltage U_{LV} of the LV power supply can be given as:

$$\begin{cases} P_{LV} \approx I_{ripple}^2 R_{total} + (1-\eta) I_{ripple} U_m \\ U_{LV} \geq M_r \times \dfrac{U_m}{0.707} \quad (M_r \leq 1) \end{cases} \tag{15}$$

where the η is the efficiency of the power stack and inductors at the specific operating condition of interest, and the R_{total} represents the Equivalent Series Resistance (ESR) of the CUTs. M_r represents the utilization rate of DC-link voltage in the SVPWM modulation [28].

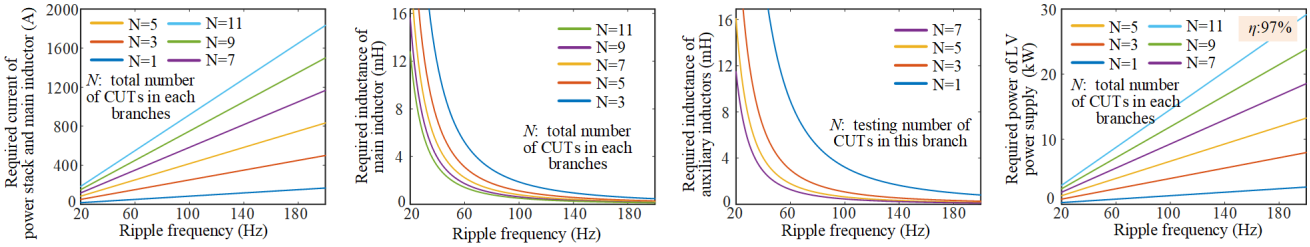
The selection of LV power supply based on a specific design case is shown in Fig. 5. As the ripple voltage acceleration factor and the number of CUTs increase, and the efficiency decreases, it can be observed that the output power required by the LV power supply increases. Meanwhile, the output voltage of the LV power supply should not be less than 750 V according to the limitation of the SVPWM modulation ratio and power stack output voltage in this case.

In DC capacitors testing, the DC voltage is determined by the output voltage of the HV power supply. The output current



(a) Required power of LV power supply with different voltage acceleration factor (b) Required power of LV power supply with different efficiency

Fig. 5. Selection of LV power supply size. (CUTs parameters: Δ – connection AC capacitors; the capacitance of single CUT C_{test_i} : $75\mu F$; rate ripple voltage U_{rate} : $730V$; N is the total number of CUTs in each of the three-phase branches.)



(a) Required current of power stack and main inductor (b) Required inductance of main inductor (c) Required inductance of auxiliary inductor in this branch (d) Required power of LV power supply

Fig. 6. Design parameters of the power stack, the inductors, and the LV power supply with different ripple frequencies. (1. CUTs parameters: Δ – connection AC capacitors; the capacitance of single CUT C_{test_i} : $75\mu F$; rate ripple voltage U_{rate} : $730V$.) (2. The voltage acceleration factor is 1.4 for the power stack and the LV power design; the voltage boost factor for the main inductor is 2.0 and for auxiliary inductors is 1.4.)

of the HV power supply can be limited by configuring the resistance of the stack resistor. The required voltage U_{HV} and the required current I_{HV} of the HV power supply can be given by:

$$\begin{cases} U_{HV} = U_{DC} + \dfrac{1}{2}U_{LV} \\ I_{HV} < \dfrac{U_{LV}}{R_{H1} + R_{H2}} \end{cases} \tag{16}$$

where the R_{H1} and R_{H2} are two stack resistors in the DC capacitor testing circuit.

E. Components design for different ripple frequencies

According to the preceding models, the design parameters of components such as the power stack, the inductors, and the power supply are affected by the ripple frequency of CUTs. Fig. 6 shows the design parameters of the power stack, inductors, and LV power supply with different ripple frequencies. As the ripple frequency increases, so does the required current of the power stack and inductors, and the required power of the LV power supply. Inversely, as the ripple frequency increases, the required inductance of the inductors decreases.

F. Design process and application-oriented cases

Based on the design models of component parameters, the design process of the proposed method is given in Fig. 7. According to the specific testing requirements, the output current of the power stack, the inductance and current of the inductors, and the bypass capacitance and parallel resistance can be restricted. Considering the power level of the power stack and inductors, and the ripple current for CUTs, the required size of the LV power supply can be given. Based on the selection of stack resistors and the DC voltage component for CUTs, the required size of the HV power supply can be obtained. If the design parameters obtained from these components can be implemented, the design process results in the desired output. Otherwise, the testing conditions need to be adjusted.

The examples of typical testing specifications for different power electronics applications are given in Table A1 (Appendix), including wind power converters [8], railway traction converters [29] and electric vehicle (EV) traction inverters [30].

IV. Experimental Verification and Implementation

A. Experimental platform and parameters

The capacitor testing system is shown in Fig. 8. As given in Table III, the capacitance of the CUTs is 75 μF (AC capacitors) and 220 μF (DC capacitors). The rated ripple voltage of the AC capacitor and the DC capacitor is 730 V and 422 V, respectively. The rated voltage of the DC capacitors is 3000 V, and the testing ripple frequencies are 50 and 60 Hz.

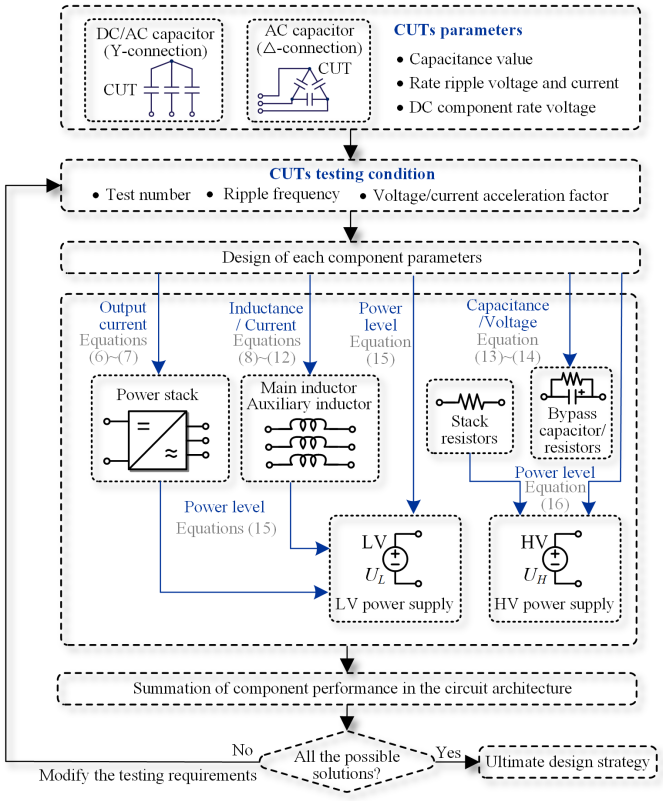


Fig. 7. Design process of the unified stress emulation method.

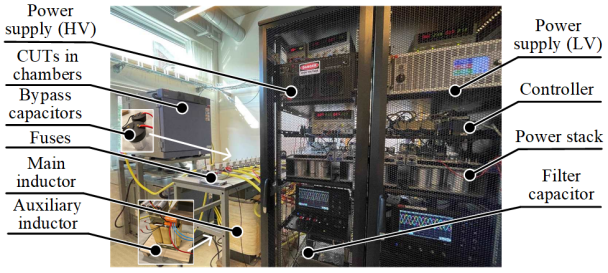


Fig. 8. Photo of the capacitor testing system.

TABLE III
EXPERIMENTAL PLATFORM PARAMETERS.

Experiment platform parameters		
Main inductor	2.5 mH	
Auxiliary inductor	5.6 mH	
Bypass capacitor and its parallel resistance	1.29 mF 200 kΩ	
Stack resistors	10*2 kΩ	
LV output voltage	750 V	
HV output voltage	3375 V (3000V DC voltage for DC capacitors + ½ LV voltage)	
Switch frequency	5000Hz	
CUTs parameters		
Test capacitor	AC capacitor (Δ-conection)	DC capacitor (Y-conection)
Capacitance of single CUT	75 μF	220 μF
Ripple testing voltage (RMS)	730 V/840 V//1022 V	422 V
DC testing voltage (RMS)	-	2000 V / 3000 V
Ripple frequency	50/60 Hz	

The specific platform parameters design process is as follows: Firstly, for the power stack and main inductor design, the 1.0 - 1.4 acceleration factors of ripple voltage and ripple current are applied to CUTs (9 pcs for AC capacitors and 6 pcs for DC capacitors). According to (6)∼(9), the rated current of power stack and main inductor should be greater than 375 A (50 Hz) and 450 A (60 Hz). Meanwhile, according to (8)∼(9) and (11)∼(12), the inductance of the main inductor should be greater than 2.5 mH (50 Hz), 1.7 mH (60 Hz) and 1.76 mH (cut-off frequency limitation).

For the auxiliary inductor design, one CUT (AC capacitor) is boosted 1.16 times the ripple voltage and current. According to (10), the inductance of the auxiliary inductor in this branch is calculated to be 5.5 mH, and the rated current should be greater than 35 A.

For the bypass capacitor and parallel resistor design, the individual DC voltage for one CUT (DC capacitor) is set to 2000 V. Therefore, according to (13) and (14), the bypass capacitance in this branch is calculated to be 1.29 mF and , and the rated DC voltage should be greater than 1000 V. The parallel resistance for bypass capacitor is set to 200 kΩ, while parallel resistance for CUTs in this branch is set to 400 kΩ.

For the power supply size, according to (15), the rated voltage and current of the low-voltage power supply should be greater than 750V, 6.8A (50 Hz) and 10.3A (60 Hz), respectively. According to (16), the voltage of the high-voltage power supply should be greater than 3375 V, and the rated current should be less than 100 mA (when the stack resistance value is 20 kΩ).

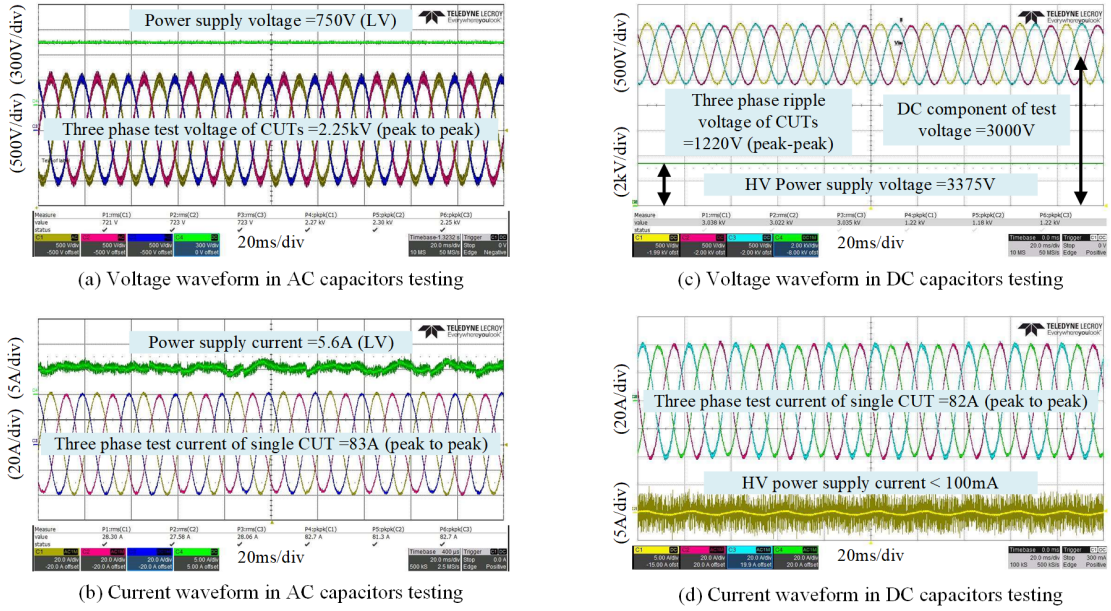
Therefore, the main component parameters are given in Table III. The auxiliary inductors and bypass capacitors are utilized to configure individual electrical stresses in different branches. The following testing results illustrate the functions of “concurrent AC and DC capacitor testing”, “individual AC ripple voltage and current”, “individual DC voltage”, and “different ripple frequency” in the proposed testing method, respectively.

B. Concurrent testing of DC and AC capacitors

The experimental waveforms for concurrently testing DC and AC capacitors are shown in Fig. 9. It shows the three-phase ripple voltage and the three-phase ripple current of the DC capacitors and the AC capacitors, and the DC voltage component of the DC capacitors. In this test case, the CUTs are 7 Δ-connection AC capacitors and 6 Y-connection DC capacitors in parallel, and the same ripple current is applied to the AC capacitors and the DC capacitors. The results show that the ripple voltage and ripple current of the CUTs are stable when AC capacitors and DC capacitors are concurrently tested.

C. Individual ripple voltage and ripple current stresses testing

The experimental waveforms for individual voltage ripple and current ripple stress testing in different branches are shown in Fig.10. In this test, the CUTs are 9 Δ-connection AC capacitors in parallel, and one of the CUTs is connected in series with a 5.5 mH three-phase auxiliary inductor in this branch. The results show that the ripple voltage of a single CUT in the branch without the auxiliary inductor is 2.25 kV (peak to peak), and the ripple current is 83 A (peak to peak).



(a) Voltage waveform in AC capacitors testing

(b) Current waveform in AC capacitors testing

(c) Voltage waveform in DC capacitors testing

(d) Current waveform in DC capacitors testing

Fig. 9. Experiment results for DC capacitors and AC capacitors concurrently testing. (Scenario 7 in Table II, 7 pcs AC capacitors and 6 pcs DC capacitors in parallel, ripple frequency: 50 Hz)

The ripple voltage of a single CUT in the branch with the auxiliary inductor is 2.63 kV (peak to peak), and the ripple current is 97A (peak to peak). It indicates that this auxiliary inductor boosts the ripple voltage and ripple current by 16% from the output of the main inductor.

D. Individual DC voltage component stresses testing

The experimental waveforms for concurrently testing individual DC voltage stresses in different branches are shown in Fig.11. In this case, the CUTs are 6 Y-connection DC capacitors in parallel, and one of the branches of 3 CUTs is connected in series with a 1.29 mF bypass capacitor and a 200 kΩ parallel resistor. The results indicate that the DC voltage component of 3 CUTs without the bypass capacitor branch is 3.0 kV. The DC component voltage of 3 CUTs with the bypass capacitor branch is 1.98 kV, which shows that this bypass capacitor divides 34% of the DC voltage component.

E. Different ripple frequencies testing

The experimental waveforms for different ripple frequencies are shown in Fig. 12. The 1.4 voltage acceleration factor for rated ripple voltage (730 V) is applied to the CUTs with 50 Hz to 360 Hz ripple frequency. When the multiple ripple frequencies are applied, the ripple voltage of the CUTs is stable and under control. If the switching frequency is applied to CUTs, it can be achieved by reducing the inductance of the main inductor according to the calculation of (10) and (11).

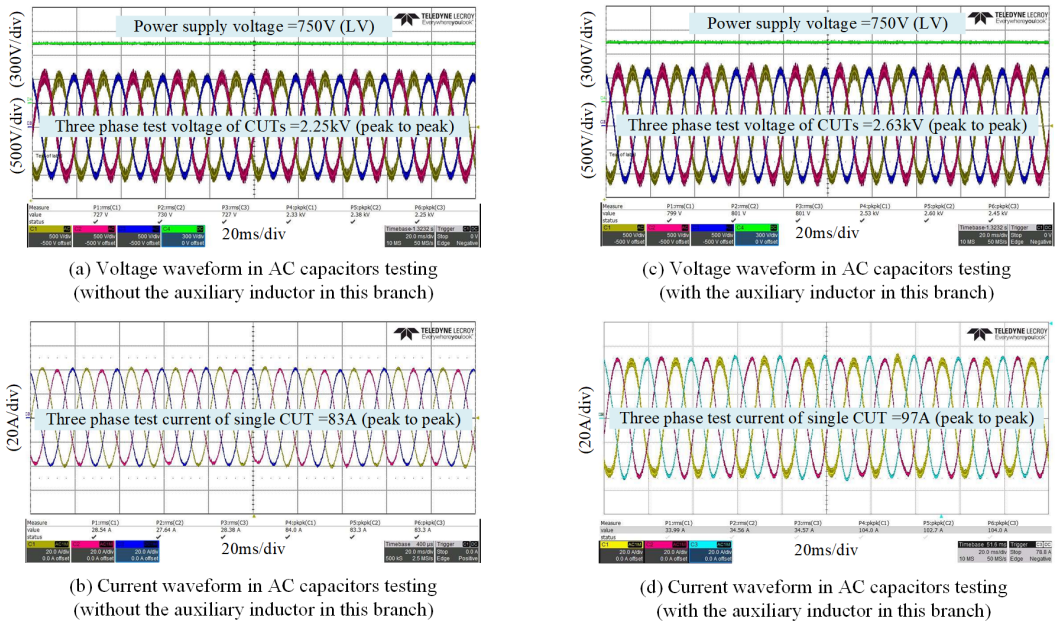
F. AC and DC capacitor gradient testing

The experimental waveforms for AC and DC capacitor gradient testing are shown in Fig. 13. In the AC capacitor testing, three testing modes are configured to simulate the gradient rise of the ripple current. In mode 1, the given ripple current is 270 A (rate current: 30A and 9 CUTs in parallel). In mode 2, the given ripple current is 324 A (acceleration factor: 1.2). In mode 3, the given ripple current is 378 A (acceleration factor: 1.4). It is possible to emulate the gradient ripple current of the AC capacitor. Due to the closed-loop control system, the actual ripple current gradually increases with the given current until it reaches the given one.

In the DC capacitor testing, three testing modes are configured to simulate the gradient rise of the DC voltage. In mode 1, the given DC voltage is 2400 V (acceleration factor: 0.8). In mode 2, the given DC voltage is 3000 V (rated voltage: 3000 V). In mode 3, the given DC voltage is 3600 V (acceleration factor: 1.2). Meanwhile, in three modes, the ripple voltage is maintained at 1200V. The stress emulation of the gradient DC voltage of the DC capacitor can be realized. The stack resistors R_{H1}, R_{H2}, and CUTs form the charging loop. When the given DC voltage increases, the test voltage increases accordingly based on the RC charging. When the CUTs are fully charged, they maintain the given DC voltage.

G. Three-phase capacitance mismatch testing

The experimental waveforms for DC capacitor testing with three-phase mismatch are shown in Fig. 14. In this case, the CUTs of one phase are disconnected to simulate the aging and failure of the CUTs in the DC capacitor testing. The capacitance of one phase CUTs is reduced from 480 μF to 440 μF. The capacitance of other two phases CUTs keeps 480 μF. When the capacitance of the CUTs mismatches, the ripple voltage and ripple current of the CUTs and the output current of the power supplies remain stable. Three phase ripple voltage of CUTs keeps 500V. Two phase ripple current of CUTs is 75.2 A and other one phase ripple current of CUTs is 69.1 A. Therefore, the test bench can generate stable ripple current and ripple voltage for the CUTs, and maintain the same required power supply, even if the CUTs degrade and have open circuit during the testing.



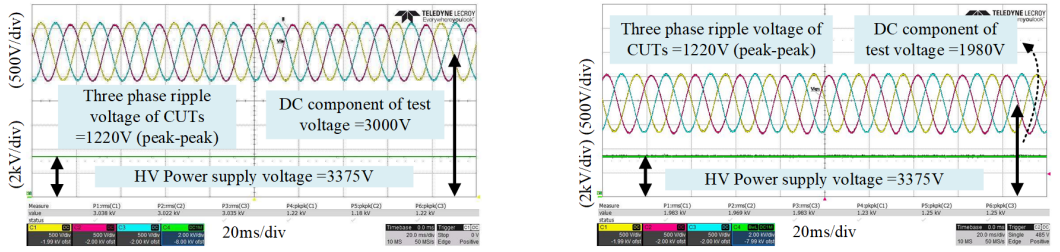
(a) Voltage waveform in AC capacitors testing (without the auxiliary inductor in this branch)

(c) Voltage waveform in AC capacitors testing (with the auxiliary inductor in this branch)

(b) Current waveform in AC capacitors testing (without the auxiliary inductor in this branch)

(d) Current waveform in AC capacitors testing (with the auxiliary inductor in this branch)

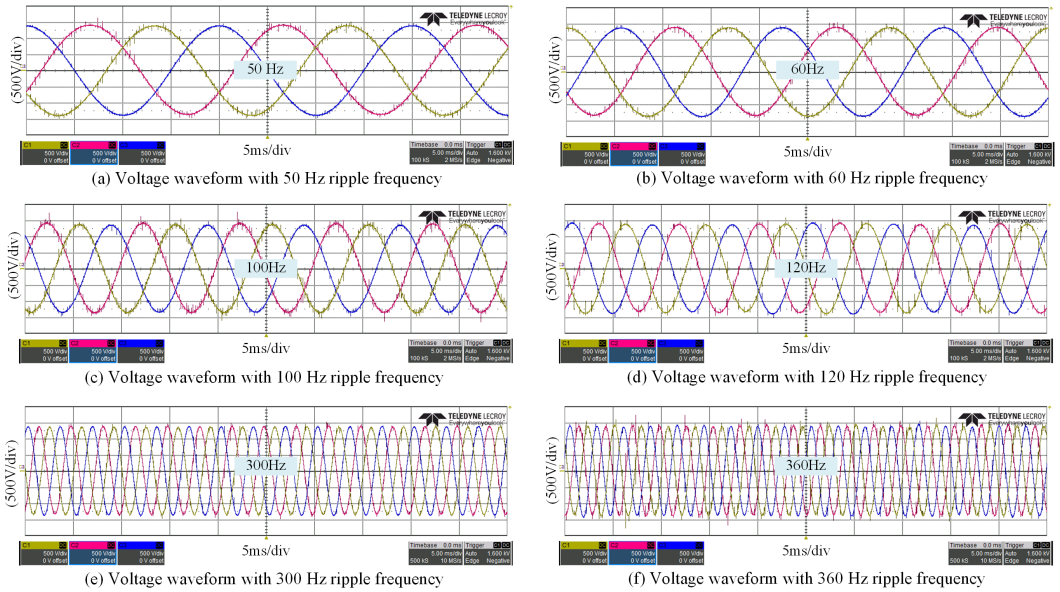
Fig. 10. Experiment results for individual ripple voltage and current testing. (Scenario 3 in Table II, 8 pcs AC capacitors without auxiliary inductors and 1 pcs DC capacitor with auxiliary inductors in parallel, ripple frequency: 50 Hz)



(a) Voltage waveform in DC capacitors testing (without the bypass capacitor in this branch)

(b) Voltage waveform in DC capacitors testing (with the bypass capacitor in this branch)

Fig. 11. Experiment results for individual DC voltage component testing. (Scenario 5 in Table II, 6 pcs DC capacitors without bypass capacitors and 6 pcs DC capacitors with bypass capacitors in parallel, ripple frequency: 50 Hz)



(a) Voltage waveform with 50 Hz ripple frequency

(b) Voltage waveform with 60 Hz ripple frequency

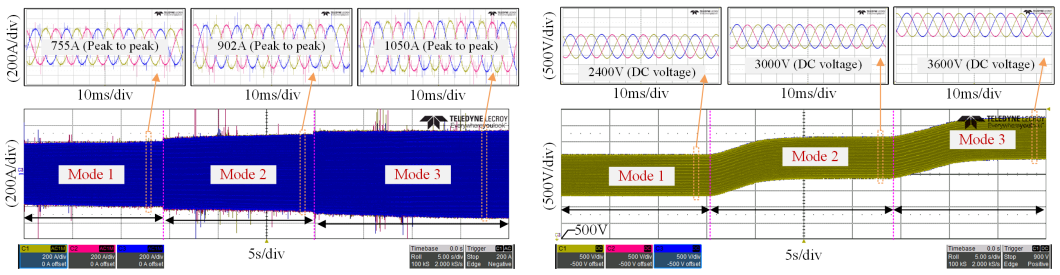
(c) Voltage waveform with 100 Hz ripple frequency

(d) Voltage waveform with 120 Hz ripple frequency

(e) Voltage waveform with 300 Hz ripple frequency

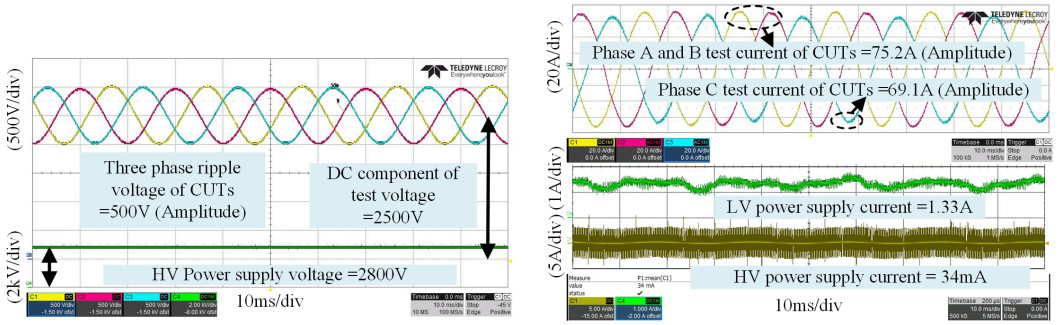
(f) Voltage waveform with 360 Hz ripple frequency

Fig. 12. Experiment results for different ripple frequency testing. (Ripple frequency: 50 Hz, 60 Hz, 100 Hz, 120 Hz, 300 Hz, and 360 Hz)



(a) Current waveform in AC capacitor gradient testing (b) Voltage waveform in DC capacitor gradient testing

Fig. 13. Experiment results for AC and DC capacitor gradient testing. (In (a): Mode 1- 270 A ripple current; Mode 2- 324 A ripple current; Mode 3- 378 A ripple current; In (b): Mode 1- 2400 V DC voltage; Mode 2- 3000 V DC voltage; Mode 3- 3600 V DC voltage; Ripple frequency: 50 Hz)



(a) Voltage waveform in DC capacitor testing (Three-phase mismatch of CUTs)

(b) Current waveform in DC capacitor testing (Three-phase mismatch of CUTs)

Fig. 14. Experiment results for DC capacitor testing with the three-phase mismatch of CUTs (one phase capacitance is reduced from 480 μF to 440 μF)

TABLE IV
ERROR ANALYSIS OF THE TESTING SYSTEM.

Testing	Parameter (RMS)	Calculation	Testing	Accuracy
Exp.1 (Fig.9)	Ripple voltage for AC capacitor	730V	724V	99.2%
	Ripple current for AC capacitor	29.7A	29.3A	98.7%
	Ripple voltage for DC capacitor	422V	420V	99.5%
	Ripple current for DC capacitor	29.0A	29.1A	99.6%
	DC voltage for DC capacitor	3000V	3022V	99.3%
	LV required current	5.8A	6.0A	96.7%
Exp.2 (Fig.10)	Ripple voltage with auxiliary inductor	840V	848V	99.1%
	Ripple current with auxiliary inductor	34.2A	34.5A	99.2%
Exp.3 (Fig.11)	DC voltage with bypass capacitor	2000V	1980V	99.0%
Exp.4 (Fig.12)	Ripple voltage (f_R=50 Hz)	1022V	1013V	99.2%
	Ripple voltage (f_R=60 Hz)	1022V	1011V	98.9%
	Ripple voltage (f_R=100 Hz)	1022V	1027V	99.5%
	Ripple voltage (f_R=120 Hz)	1022V	1035V	98.7%
	Ripple voltage (f_R=300 Hz)	1022V	1016V	99.4%
	Ripple voltage (f_R=360 Hz)	1022V	1013V	99.1%

H. Error analysis of design and testing

Comparing the design calculation with the test results in Table IV, the calculated accuracy of ripple current, ripple voltage, and DC voltage of the CUTs between the design value and the test results is more than 98.5%. The calculated accuracy of source output current between the design value and the test results exceeds 96%. Considering that there are sampling errors of voltage and current sensors, potential noise interference, and power loss by other components, the results indicate that the theoretical analysis of the proposed method is reasonable.

V. CONCLUSION

This paper proposes a unified capacitor stress emulation method for high power converter applications. The proposed method has the unique capability to emulate different electrical stress levels, such as ripple voltage, ripple current, and DC voltage, in individual branches, allowing for concurrent testing of both AC and DC capacitors. The testing capabilities and scenarios are given in Table II, which is suitable for application-oriented testing with different stress conditions. The architecture of the circuit and the analytical models for component sizing are described in detail. Examples of typical engineering testing scenarios for different power electronics applications are given in Table A1, such as wind power converters, electric vehicle inverters, and railway traction systems. Experimental results with 3.0 kV DC voltage, 3.0 kV ripple voltage, and 1.2 kA ripple current verify the feasibility of the proposed testing method for high power converter applications. The accuracy of simulated electrical stresses is more than 98.5%, indicating that the derived analytical models of the proposed method are reasonable.

APPENDIX A
EXAMPLES OF TYPICAL TESTING SCENARIOS

Examples of typical engineering testing scenarios for different power electronics applications are given in Table A1.

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TABLE A1
EXAMPLES OF TYPICAL ENGINEERING TESTING SCENARIOS FOR DIFFERENT POWER ELECTRONICS APPLICATIONS.

Testing reqirement (RMS value)						Required design parameters (RMS value)						
CUTs	Application	CUTs parameter (C_{test}/f_R / I_{ripple} or U_{ripple} / U_{rate_DC})	Test Number	Acceleration factor for rated ripple voltage/current	Acceleration factor for rated DC voltage	Power stack output current	AC inductor inductance	AC inductor current	Bypass capacitor capacitance	Bypass capacitor voltage	Required power (LV)	Required voltage (HV)
AC	Wind power	75μF/50Hz /730V/-	9	m=1.4	-	375A	2.5mF	375A	-	-	6830W	-
	Wind power	75μF/60Hz /730V/-	9	m=1.4	-	450A	1.7mF	450A	-	-	10350W	-
	Wind power	75uF/50Hz /730V/-	9	m_1=1.0 (N_1=3) m_2=1.2 (N_2=3) m_3=1.4 (N_3=3)	-	321A	Main=1.35mF Aux 1=2.5mF Aux 2=4.3mF	Main=321A Sub1=107A Sub2=125A	-	-	5860W	-
	Railway	416μF/50Hz /600V/-	8	m=1.4 (840V)	-	1523A	0.37mF	1523A	-	-	27720W	-
	Railway	416μF/50Hz /600V/-	8	m_1=1.0 (N_1=2) m_2=1.2 (N_2=2) m_3=1.4 (N_3=2) m_4=1.6 (N_4=2)	-	1410A	Main=0.12mF Aux 1=0.68mF Aux 2=1.16mF Aux 3=1.53mF	Main=1410A Sub1=325A Sub2=380A Sub3=434A	-	-	25680W	-
DC	Wind power	645μF/50Hz /40A/1250V	24	m=1.4	m_{DC}=1.0	448A	0.49mF	448A	-	-	8100W	1625V
	Wind power	645μF/50Hz /40A/1250V	24	m_1=1.2 (N_1=12) m_2=1.4 (N_2=12)	m_{DC1}=1.0 (N_1=18) m_{DC1}=1.4 (N_2=6)	416A	Main=0.49mF Aux 1=0.57mF	Main=416A Sub1=192A	9.675mF	500V	7500W	2125V
	Railway	750μF/50Hz /200A/3000V	12	m_1=1.2 (N_1=6) m_2=1.4 (N_2=6)	m_{DC1}=1.0 (N_1=9) m_{DC1}=1.4 (N_2=3)	976A	Main=1.62mF Aux 1=1.93mF	Main=976A Sub1=560A	5.625mF	1200V	17550W	4575V
	Electric vehicle	440μF/50Hz /90A/600V	24	m=1.4	m_{DC1}=1.0 (N_1=18) m_{DC1}=1.4 (N_2=6)	1008A	0.72mF	1008A	6.6mF	240V	18150W	1215V
AC+DC	Wind power	75μF/50Hz /730V/- 645μF/50Hz /40A/1250V	9 (AC) 24 (DC)	m=1.4	m_{DC}=1.0	823A	Main=0.35mF Aux 1=3.64mF	Main=823A Sub1=375A	-	-	14850W	1625V
	Railway	416μF/50Hz /600V/- 750μF/50Hz /200A/3000V	4 (AC) 6 (DC)	m=1.4	m_{DC1}=1.0 (N_1=3) m_{DC1}=1.4 (N_2=3)	1321A	Main=0.57mF Aux 1=1.97mF	Main=1321A Sub1=560A	5.625mF	1200V	23760W	4575V

1.Using Semikron's SKS SL150 power stack (Rated output current=1600A), Elektro-automatik's EA-PSI 10000 LV power supply (Rated output power=30 kW) and Technix's SR20-40 HV power supply (Rated output voltage= 10 kV) can be applied to all the above cases, as shown in Fig. 8.
2. In the cases: efficiency η, 96.6%; power stack rated output voltage, 530V; LV output voltage, 750V.
3. The configuration of inductors and capacitors can be selected according to needs.

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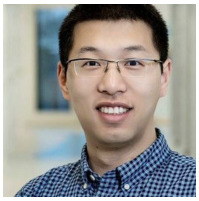

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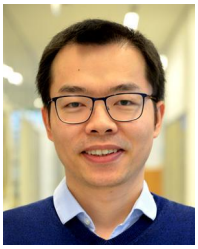

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