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Optimal Modulation Strategy for Ripple Current Reduction of DC-link Capacitor in Multi-drive Systems

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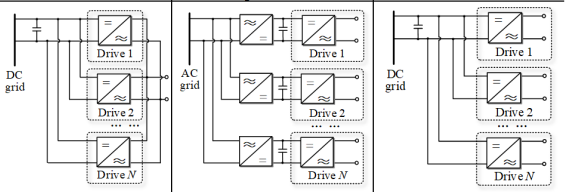
***Abstract*—This paper proposes a modulation method that significantly reduces the ripple current of the DC-link capacitor in multi-drive systems. It is based on the derived analytical model for the capacitor ripple current with an arbitrary number of drives connected in parallel at the DC-link side. The effects of different parameters (including load, power factor, modulation ratio, and switching frequency) on the modulation method in multiple drives are analyzed. Both the low-frequency and high-frequency current components are minimized by the optimal phase shifts of the modulation signal and the carrier signal. The cases with three drives for the optimal phase shifts corresponding to different parameter configurations are given. Benchmark studies of multi-drives systems with 2 to 20 drives reveal that the total capacitor Root Mean Square (RMS) current is reduced to 34.3%∼15.9%. Proof-of-concept experimental results verify the theoretical analysis and the effectiveness of the proposed method.**

***Index Terms*—multi-drive systems, DC-link capacitor, analytical model, modulation method, ripple current**

TABLE I
THREE CONFIGURATIONS OF THE MULTI-DRIVE SYSTEMS.

	Configuration 1	Configuration 2	Configuration 3
Definition	DC-side parallel with one AC load	Grid-side parallel with multiple AC loads	DC-link parallel with individual AC loads
Structure			
Application	On-board ships, electric vehicle (EV)	Paper, metal, mining, marine, and production lines applications	
Advantage	High power inverters for AC load	Configurable individual AC loads	Lightweight of the system
Limitations	Single AC load application	Multiple rectifiers for the DC link of each inverter	High ripple currents in DC link

I. INTRODUCTION

RECENTLY, multi-drive system concepts have been used in industrial and residential applications [1], [2]. There are three typical configurations of multi-drive systems: DC-side parallel with single AC load [3], [4]; grid-side parallel with multiple AC loads [5], [6]; and DC-link parallel with multiple AC loads [7]–[9], as shown in Table I. In Configuration 1, multiple drives are connected in parallel to provide a high-power system, which can be used in on-board ships, electric vehicles (EVs) and hybrid EVs (HEVs) [3], [4]. However, this structure is just suitable for a single load system, and cannot connect multiple loads. In Configuration 2 and Configuration 3, multiple loads are provided by the AC grid or the DC grid, which can be used in pulp and paper, metal and mining, marine, and production lines applications [5]–[7]. Compared with Configuration 2, Configuration 3 with a common DC-link system has been advocated as a possibility for future integration of drives to reduce the number of conversion stages, improve the reliability, and optimize the cost and volume, which is of interest in this paper [7]. Furthermore, Configuration 3 can be more flexible and scalable as the system capacity can be increased by adding more drives without removing existing drives and additional rectifier modules [8], [9].

Despite these benefits, one of the concerns in Configuration 3 is the ripple current generated by harmonic interaction between these parallel connected drives and from pulse width modulation (PWM) switching [10]. The ripple current in this multi-drive system linearly increases with the number of drives connected with the DC link. On the one hand, a common practical solution in the market to suppress the DC-link harmonics is to use a large DC-link capacitor, yet the overall system compromises in terms of volume, weight, and cost [11], [12]. On the other hand, the considerable ripple current increases the hot spot temperature and reduces the lifetime of the DC-link capacitor [13], [14]. Therefore, it is important to reduce the DC-link capacitor current in multi-drive systems with DC-side parallel and multiple AC loads (i.e., Configuration 3 in Table I).

Existing methods for reducing the DC-link capacitor current in multi-drive systems have the following issues: In Configuration 1, a method is proposed to reduce the ripple current of the DC link capacitors by extracting the switching signals of drives [15], which needs the shared single AC load for multiple drives, only limited to such a configuration. The modulation methods using phase shifts of the carrier signal are given in [16] and [17], and its derived models consider the effect of different modulation ratios and power factors, respectively, which can be extended to Configuration 3 to reduce the high-order harmonics of the capacitor current. Nevertheless, this method can not deal with the effects of low-order harmonics caused by multiple loads. In Configuration 2, the method in [18] considers the phase shifts of the modulation signal

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to reduce the low-order harmonics of the capacitor current. Ref. [19] further considers the influence of different loads. However, the derived models in [18], [19] have mandatory conditions to configure the multiple rectifiers for the DC-link of each drive, thus the derived models are applicable for Configuration 2 only. In Configuration 3, a method is presented to suppress DC link current harmonics by phase shifts of the carrier and the modulation signal [20]. However, this method only derives the analytical equation for DC-link capacitor ripple current with identical parameters of two drives. In addition, it cannot be used to analyze the optimal phase shifts in systems with different parameters (e.g., different loads, switching frequency, etc.) of more than two drives.

This paper proposes a modulation scheme to minimize the DC-link capacitor current ripple for the multi-drive systems in Configuration 3. The contribution lies in three aspects: 1) the DC-link capacitor ripple current is analytically derived and applicable for systems with a different number of drives connected in parallel; 2) this method can be applied to different parameters (including load, power factor, modulation ratio, and switching frequency) in multiple drives; 3) the modulation scheme features optimal phase shifts of both the low-frequency modulation signal and the switching-frequency carrier signal among the drives.

The structure of this paper is as follows: Section II presents the proposed optimal modulation modeling; Section III gives the case study; Section IV discusses the experimental verification, followed by the conclusions.

II. Proposed Optimal Modulation Modeling

The multi-drive system with a common DC bus and DC-link capacitors is shown in Fig. 1. It consists of N parallel drives, connected to a common DC bus and DC-link capacitors, powered by the DC grid. In applications such as paper, metal, mining, marine, and production lines, the parallel drives can be considered synchronized and have the same initial phase [7]–[9]. This section analyzes the ripple current of DC-link capacitors and the optimal modulation scheme considering the operating condition of identical parameters and different parameters (including different loads, power factors, modulation ratios, and switching frequencies) in multiple drives.

A. Ripple current for the single drive

The double Fourier analysis method can be used to develop spectral models for regular-sampled PWM [21]. The switching model S_{pwm} under SPWM modulation based on the triangular carrier can be expressed as [22]:

$$\begin{aligned} S_{pwm} &= M\sin\left(\omega_0 t+\theta_0\right) \\ &+\frac{4}{\pi}\sum_{m=2,4,\ldots}^{\infty}\sum_{n=\pm1,\pm3,\ldots}^{\infty}\left[\begin{array}{l}\frac{(-1)^{\frac{m}{2}}}{m}J_n\left(\frac{\pi mM}{2}\right)\times \\ \sin\left(n\left(\omega_0 t+\theta_0\right)+m\left(\omega_c t+\theta_c\right)\right)\end{array}\right] \end{aligned} \tag{1}$$

where ω_o, ω_c, θ_o, and θ_c represent the angular velocity of the modulation signal and the carrier signal, the phase angle of the modulation signal and the carrier signal, respectively. M represents the modulation ratio of the drive and $J_n\left(\frac{m\pi M}{2}\right)$ is the Bessel function.

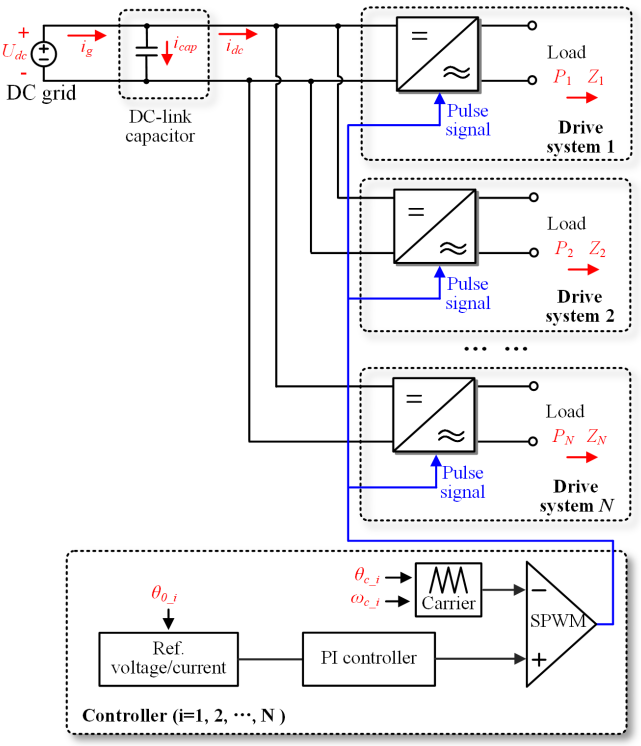


Fig. 1. Multi-drive system with DC-side parallel and multiple AC loads.

The DC-link input current i_{dc} for the drive can be given as:

$$i_{dc}=S_{pwm}\times\frac{U_p}{ZP}\sin\left(\omega_0 t+\theta_0\right) \tag{2}$$

where U_p, Z, and P represent the amplitude of the AC voltage, the load, and the power factor of the drive, respectively.

According to (1) and (2), the DC-link input current i_{dc} can be expressed as:

$$\left\{\begin{array}{l} i_{dc}=i_{dc\_1}+i_{dc\_2} \\ i_{dc\_1}=M\sin\left(\omega_0 t+\theta_0\right)\times\frac{U_p}{ZP}\sin\left(\omega_0 t+\theta_0\right) \\ i_{dc\_2}=\frac{4}{\pi}\times\frac{U_p}{ZP}\sin\left(\omega_0 t+\theta_0\right)\times \\ \sum_{m=2,4,\ldots}^{\infty}\sum_{n=\pm1,3,\ldots}^{\infty}\left[\begin{array}{l}\frac{(-1)^{\frac{m}{2}}}{m}J_n\left(\frac{\pi mM}{2}\right) \\ \times\sin\left(n\left(\omega_0 t+\theta_0\right)+m\left(\omega_c t+\theta_c\right)\right)\end{array}\right] \end{array}\right. \tag{3}$$

where i_{dc_1} and i_{dc_2} represent the two calculated components of the DC-link input current i_{dc}.

The first calculated component i_{dc_1} can be simplified to:

$$i_{dc\_1}=\frac{U_pM}{2ZP}-\frac{U_pM}{2ZP}\cos\left(2\left(\omega_0 t+\theta_0\right)\right) \tag{4}$$

When $n=\pm1,\pm3,\ldots$, the function of $\cos\left(n\left(\omega_0 t+\theta_0\right)\right)$ times is point symmetry, and its sum is 0. Meanwhile, from the properties of the Bessel function, it applies:

$$\begin{aligned} J_{-n}\left(\frac{\pi mM}{2}\right)&=(-1)^n J_n\left(\frac{\pi mM}{2}\right) \\ &=J_n\left(\frac{\pi mM}{2}\right)\quad(n=\pm1,\pm3,\ldots) \end{aligned} \tag{5}$$

Therefore, i_{dc_2} can be further simplified as:

$$i_{dc\_2} = \frac{8U_p}{\pi ZP} \times \sum_{m=2,4,\dots}^{\infty} \sum_{n=1,3,\dots}^{\infty} \left[\begin{array}{l} \frac{(-1)^{\frac{m}{2}}}{m} J_n\left(\frac{\pi m M}{2}\right) \times \sin\left(\omega_0 t + \theta_0\right) \\ \times \sin\left(n\left(\omega_0 t + \theta_0\right)\right) \cos\left(m\left(\omega_c t + \theta_c\right)\right) \end{array} \right] \tag{6}$$

According to (4) and (6), it reveals that the DC-link current of one drive consists of the DC component, low-frequency harmonics, and high-frequency harmonics. The DC component i_{dc_DC}, the low-frequency harmonic component (double-fundamental frequency) i_{dcl}, and the high-frequency harmonic component (m^{th}-order harmonic of the carrier frequency) i_{dch} can be expressed as:

$$\begin{cases} i_{dc} = i_{dc\_DC} + i_{dcl} + i_{dch} \\ i_{dc\_DC} = \frac{U_p M}{2ZP} \\ i_{dcl} = -\frac{U_p M}{2ZP} \cos\left(2\left(\omega_0 t + \theta_0\right)\right) \\ i_{dch} = \sum_{m=2,4,\dots}^{\infty} \left[\begin{array}{l} (-1)^{\frac{m}{2}} \frac{8U_p M}{\pi m ZP} \times \\ \sin\left(\omega_0 t + \theta_0\right) \cos\left(m\left(\omega_c t + \theta_c\right)\right) \times \\ \sum_{n=1,3,\dots}^{\infty} \left[J_n\left(\frac{\pi m M}{2}\right) \sin\left(n\left(\omega_0 t + \theta_0\right)\right)\right] \end{array} \right] \end{cases} \tag{7}$$

B. Ripple current for the Multiple drives

In Fig.1, the low-frequency harmonic component i_{dcl} for multiple drives can be given as:

$$i_{dcl} = -\frac{U_p}{2} \sum_{i=1}^{N} \left[\frac{M_i}{Z_i P_i} \cos\left(2\left(\omega_0 t + \theta_{0\_i}\right)\right)\right] \tag{8}$$

where θ_{o_i}, M_i, Z_i, and P_i represent the shifted phase angles of the modulation signal, the amplitude of the AC voltage, the modulation ratio, the impedance, and the power factor in the i^{th} drive, respectively, and N is the number of drives.

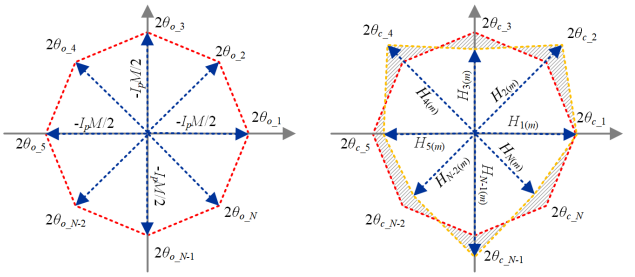
The high-frequency harmonic current of the m^{th}-order carrier frequency $i_{dch(m)}$ can be expressed as:

$$\begin{cases} i_{dch(m)} = \sum_{i=1}^{N} H_{i(m)} \frac{8U_p M_i}{\pi Z_i P_i} \cos\left(m\left(\omega_{c\_i} t + \theta_{c\_i}\right)\right) \\ H_{i(m)} = \frac{(-1)^{\frac{m}{2}}}{m} \sin\left(\omega_0 t + \theta_{0\_i}\right) \times \\ \sum_{n=1,3,\dots}^{\infty} \left[J_n\left(\frac{\pi m M}{2}\right) \sin\left(n\left(\omega_0 t + \theta_{0\_i}\right)\right)\right] \end{cases} \tag{9}$$

where ω_{c_i} and θ_{c_i} are the angular velocity of the modulation signal and the phase shift angles of the carrier signal of the i^{th} drive, respectively. $H_{i(m)}$ is the coefficient in the high-frequency current harmonics.

Therefore, the DC-link capacitor current i_{cap} can be expressed as:

$$i_{cap} = i_{dcl} + i_{dch(m)} \tag{10}$$



(a) Optimal phase shifts for modulation signal (b) Optimal phase shifts for carrier signal

Fig. 2. Optimal phase shifts of the modulation signal and the carrier signal with identical parameters in different drives.

C. Optimal Phase Shift Scheme for Multiple Drives with Identical Parameters

When the load, the power factor, and the modulation ratio of multiple drives are identical:

$$E = \frac{M_1}{Z_1 P_1} = \frac{M_2}{Z_2 P_2} = \cdots = \frac{M_N}{Z_N P_N} \tag{11}$$

In this case, the magnitude of the low-frequency harmonic current I_{dcl_mag} can be simplified as:

$$I_{dcl\_mag} = \frac{U_p E}{2} \sqrt{\left[\sum_{i=1}^{N} \sin\left(2\theta_{0\_i}\right)\right]^2 + \left[\sum_{i=1}^{N} \cos\left(2\theta_{0\_i}\right)\right]^2} \tag{12}$$

When switching frequencies are identical in the multiple drives, the magnitude of the m^{th}-order harmonic of the carrier frequency $I_{dch(m)\_mag}$ can be simplified as:

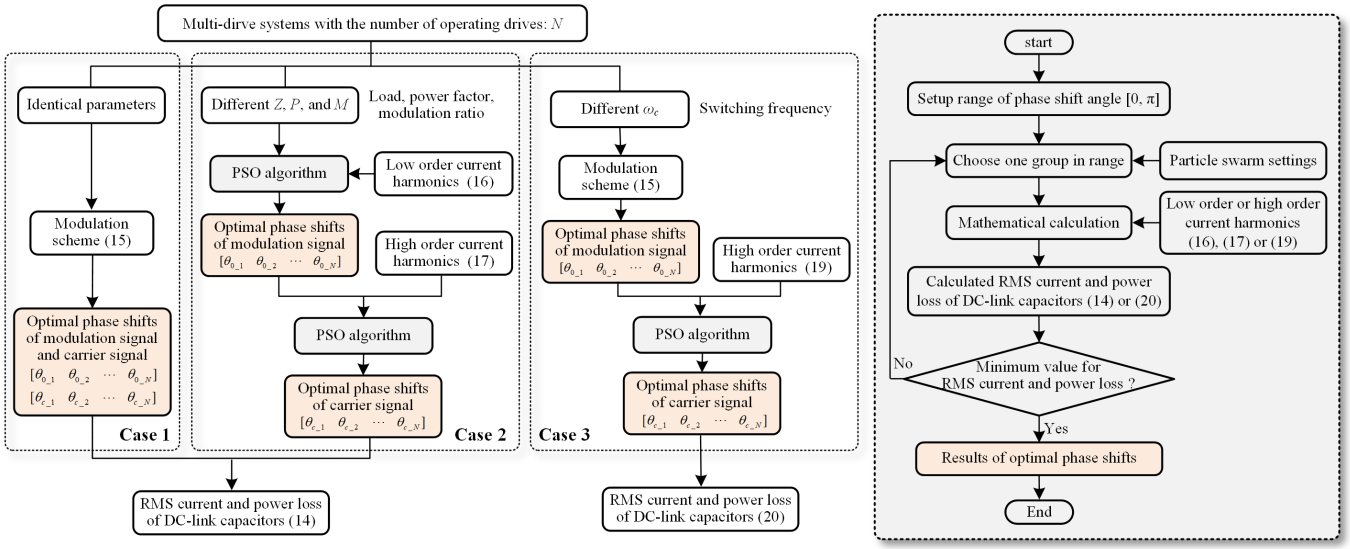
$$I_{dch(m)\_mag} = \frac{8U_p E}{\pi} \sqrt{\left[\sum_{i=1}^{N} H_{i(m)} \sin\left(m\theta_{c\_i}\right)\right]^2 + \left[\sum_{i=1}^{N} H_{i(m)} \cos\left(m\theta_{c\_i}\right)\right]^2} \tag{13}$$

The RMS current $i_{cap(RMS)}$ and power loss P_{cap} of the DC-link capacitor can be expressed as:

$$\begin{cases} i_{cap(RMS)} = \sqrt{I_{dcl\_mag}^2 + \sum_{m=2,4,\dots}^{\infty} I_{dch(m)\_mag}^2} \\ P_{cap} = I_{dcl\_mag}^2 R_{(f_{dcl})} + \sum_{m=2,4,\dots}^{\infty} I_{dch(m)\_mag}^2 R_{(f_{\text{dch }(m)})} \end{cases} \tag{14}$$

where $R_{(f_{dcl})}$ and $R_{(f_{\text{dch }(m)})}$ are the equivalent series resistance (ESR) of the DC-link capacitor at low and high frequencies, respectively.

According to (12), when the $2\theta_{o\_i}$ in multi-drive systems is equally divided into 360°, that is, the phase shifts of the modulation signal in the i^{th} drive are $\frac{180}{N} \times (i-1)$, thus low-frequency current harmonics can be completely canceled, as shown in Fig. 2(a). According to (13), the $2\theta_{c\_i}$ can also be equally divided into 360°. The phase shifts of the carrier signal



(a) Proposed optimal modulation scheme for three cases for multiple drives

(b) Calculation process of the PSO algorithm

Fig. 3. Proposed optimal modulation scheme. (In (a), Case 1, Case 2, and Case 3 represent the scheme for multi-drive systems with identical parameters, different load / power factor / modulation ratio, and different switching frequency among multiple drives, respectively.)

in the i^{th} drive are $\frac{180}{N} \times (i-1)$. It can significantly reduce the high-frequency current harmonic components. It should be noted that the above phase shifts method cannot eliminate all the high-frequency harmonics since $H_{i(m)}$ magnitudes are unequal in different drives. The shaded area in Fig. 2(b) represents the remaining high-frequency current components.

The selection of the phase shifts of the carrier signal or the modulation signal depends on the number of running drives. When the number of drives is N, the θ_{o_i} and θ_{c_i} of the i^{th} drive are:

$$i \in \{1, 2, \cdots, N\} \quad \theta_{o\_i} = \theta_{c\_i} = \left\{ \frac{180}{N} \times (i-1) \right\} \tag{15}$$

Therefore, the implementation of the proposed optimal modulation scheme for multiple drives with identical parameters is described in Case 1 of Fig. 3(a).

D. Optimal Phase Shift Scheme for Multiple Drives with Different Parameters

1) Different loads, power factors, and modulation ratios: When the load, the power factor, and the modulation ratio are different in multiple drives, the magnitude of the low-frequency harmonic current I_{dcl_mag} can be simplified as:

$$I_{dcl\_\mathrm{mag}} = \frac{U_p}{2} \sqrt{\left[\sum_{i=1}^{N} \frac{M_i}{Z_i P_i} \sin\left(2\theta_{0\_i}\right)\right]^2 + \left[\sum_{i=1}^{N} \frac{M_i}{Z_i P_i} \cos\left(2\theta_{0\_i}\right)\right]^2} \tag{16}$$

The magnitude of the m^{th}-order harmonic of the carrier frequency $I_{dch(m)\_mag}$ can be simplified as:

$$I_{dch(m)\_\mathrm{mag}} = \frac{8U_p}{\pi} \times \sqrt{\left[\sum_{i=1}^{N} \frac{M_i H_{i(m)}}{Z_i P_i} \sin\left(m\theta_{c\_i}\right)\right]^2 + \left[\sum_{i=1}^{N} \frac{M_i H_{i(m)}}{Z_i P_i} \cos\left(m\theta_{c\_i}\right)\right]^2} \tag{17}$$

In this case, the RMS current $i_{cap(RMS)}$ and power loss P_{cap} of the DC-link capacitor can be expressed by (14).

The implementation of the proposed optimal modulation scheme for multiple drives with different loads, power factors, and modulation ratios is described in Case 2 of Fig. 3(a). In the scheme, the optimal phase shifts of the modulated signal and the carrier signal are obtained, respectively, through the Particle Swarm Optimization (PSO) algorithm. PSO is a global optimization algorithm, which can be used to find the optimal solution for the undetermined parameters and is suitable for analyzing the optimal phase shifts in this method [23] [24]. When different drives are set with different parameters, the PSO algorithm can be used to obtain the optimal phase shifts, as shown in Fig 3. (b). To implement PSO, the first step is to set the range of the phase shifts in different drives, whose values can be assumed as $[0, 2\pi]$. The next step is to set particle swarm settings in the algorithm, whose values can be assumed empirically and updated in follow-up calculations [25]. According to the analytical model derived in this paper, the low-order or high-order current harmonics corresponding to different groups of phase shifts within the set range are calculated, and the RMS current and power loss corresponding to different phase shifts are further obtained. When the calculation result of RMS current and power loss of DC-link capacitors is the minimum, the corresponding optimal phase shifts in different drives are output, which is the optimal solution.

2) Different switching frequencies: When the switching frequencies are different in multiple drives, the magnitude of

TABLE II
LOOK-UP TABLE FOR OPTIMAL PHASE SHIFTS IN DIFFERENT CONDITIONS OF MULTIPLE DRIVES (TAKE THREE DRIVES AS AN EXAMPLE).

Table I.(a)
Individual conductance/modulation ratio/power factor in the drives

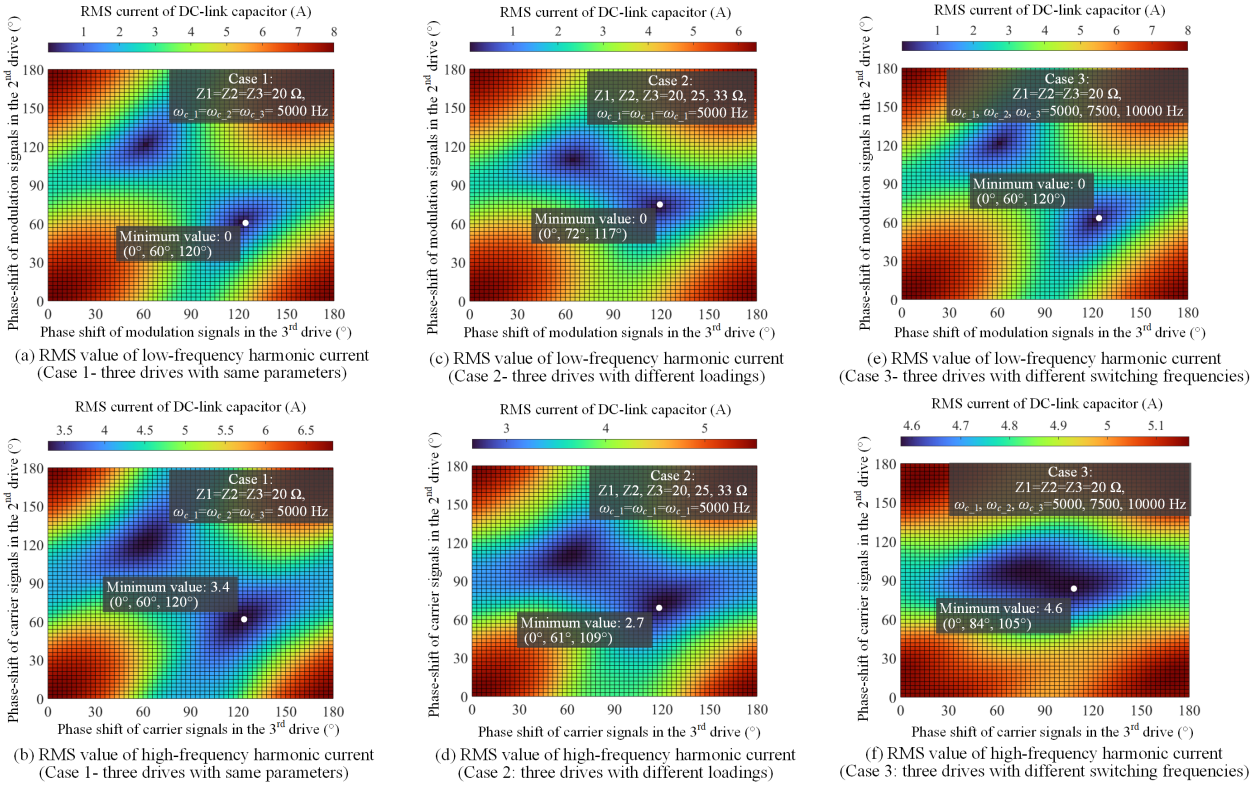
		Rate of conductance/modulation ratio/power factor in the 2nd drive				
		100%	80%	60%	40%	20%
Rate of conductance /modulation ratio/power factor in the 3rd drive	100%	M: (60°, 120°) C: (60°, 120°)	M: (66°,123°) C: (67°, 123°)	M: (72°, 126°) C: (73°, 126°)	M: (78°, 129°) C: (81°, 131°)	M: (84°, 132°) C: (87°, 134°)
	80%	M: (66°,123°) C: (67°, 123°)	M: (64°, 116°) C: (64°, 116°)	M: (72°, 117°) C: (61°, 109°)	M: (79°, 115°) C: (58°, 99°)	M: (90°, 90°) C: (50°, 93°)
	60%	M: (72°, 126°) C: (73°, 126°)	M: (72°, 117°) C: (61°, 109°)	M: (73°, 107°) C: (70°, 110°)	M: (90°, 90°) C: (73°, 99°)	M: (90°, 90°) C: (86°, 110°)
	40%	M: (78°, 129°) C: (81°, 131°)	M: (79°, 115°) C: (58°, 99°)	M: (90°, 90°) C: (73°, 99°)	M: (90°, 90°) C: (80°, 100°)	M: (90°, 90°) C: (79°, 95°)
	20%	M: (84°, 132°) C: (87°, 134°)	M: (90°, 90°) C: (50°, 93°)	M: (90°, 90°) C: (86°, 110°)	M: (90°, 90°) C: (79°, 95°)	M: (90°, 90°) C: (90°, 90°)

1. Keep the conductance/modulation ratio/power factor in the 1st drive at 100%;
(Conductance is the inverse of the loading.)
2. Keep the phase shift of the carrier signal and modulation signal in the 1st drive both at 0°;
3. M indicates phase shift of the modulation signals of the second and third drives;
4. C indicates phase shift of the carrier signals of the second and third drives.

Table I.(b)
Individual switching frequency in the drives

		Multiples of switching frequency in the 2nd drive				
		1.0	1.5	2.0	3.0	5.0
Multiples of switching frequency in the 3rd drive	1.0	M: (60°, 120°) C: (60°, 120°)	M: (60°, 120°) C: (84°, 108°)	M: (60°, 120°) C: (90°, 90°)	M: (60°, 120°) C: (76°, 114°)	M: (60°, 120°) C: (101°, 162°)
	1.5	M: (60°, 120°) C: (84°, 108°)	M: (60°, 120°) C: (90°, 90°)	M: (60°, 120°) C: (92°, 163°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (90°, 180°)
	2.0	M: (60°, 120°) C: (90°, 90°)	M: (60°, 120°) C: (92°, 163°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (84°, 105°)	M: (60°, 120°) C: (18°, 85°)
	3.0	M: (60°, 120°) C: (76°, 114°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (84°, 105°)	M: (60°, 120°) C: (45°, 126°)	M: (60°, 120°) C: (90°, 180°)
	5.0	M: (60°, 120°) C: (101°, 162°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (18°, 85°)	M: (60°, 120°) C: (90°, 180°)	M: (60°, 120°) C: (37°, 132°)

1. Keep the multiple of switching frequecny in the 1st drive at 1.0;
2. Keep the phase shift of the carrier signal and modulation signal in the 1st drive both at 0°;
3. M indicates phase shift of the modulation signals of the second and third drives;
4. C indicates phase shift of the carrier signals of the second and third drives.



(a) RMS value of low-frequency harmonic current (Case 1- three drives with same parameters)
(c) RMS value of low-frequency harmonic current (Case 2- three drives with different loadings)
(e) RMS value of low-frequency harmonic current (Case 3- three drives with different switching frequencies)
(b) RMS value of high-frequency harmonic current (Case 1- three drives with same parameters)
(d) RMS value of high-frequency harmonic current (Case 2: three drives with different loadings)
(f) RMS value of high-frequency harmonic current (Case 3: three drives with different switching frequencies)

Fig. 4. RMS current of DC-link capacitor by the analytical equations in the three drives system. ((a) and (b) indicate Case 1 - identical parameters in multiple drives; (c) and (d) indicate Case 2 - different loads in multiple drives; (e) and (f) indicate Case 3 - different switching frequency in multiple drives. The phase shift of the carrier signal in the 1^{st} drive is 0° in each case. The numerical results are specific to the system with the specifications shown in Table III discussed later in Section IV)

the low-frequency harmonic current I_{dcl_mag} can be expressed by (12).

The $\mathrm{Hash}(s)$ indicates the number of elements in the combination of m orders the different switching frequencies for multiple drives:

$$\mathrm{Hash}(s) = \begin{bmatrix} 2\omega_{c\_1} & 4\omega_{c\_1} & \cdots & m\omega_{c\_1} \\ 2\omega_{c\_2} & 4\omega_{c\_2} & \cdots & m\omega_{c\_2} \\ \cdots & \cdots & \cdots & \cdots \\ 2\omega_{c\_N} & 4\omega_{c\_N} & \cdots & m\omega_{c\_N} \end{bmatrix} \tag{18}$$

The magnitude of the s^{th}-order harmonic of the carrier frequency $I_{dch(s)\_mag}$ can be simplified as:

$$I_{dch(s)\_\,\mathrm{mag}} = \frac{8U_p}{\pi} \times \sqrt{\left[\sum_{i=1}^{x_{pq}} \frac{M_i H_{i(s)}}{Z_i P_i} \sin\left(p\theta_{c\_q}\right)\right]^2 + \left[\sum_{i=1}^{x_{pq}} \frac{M_i H_{i(s)}}{Z_i P_i} \cos\left(p\theta_{c\_q}\right)\right]^2} \tag{19}$$

where $p\theta_{c\_q}$ and x_{pq} denote the same element in $\mathrm{Hash}(s)$ and the number of that group, respectively.

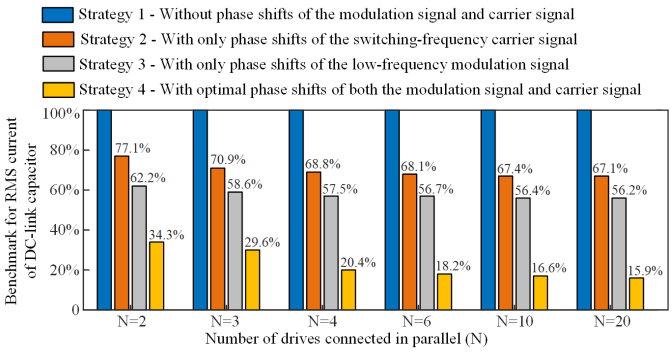


Fig. 5. Benchmark for the RMS value of DC-link capacitor ripple current with identical parameters in the multiple drives

In this case, the RMS current $i_{cap(RMS)}$ and power loss P_{cap} of the DC-link capacitor can be expressed as:

$$\begin{cases} i_{cap(RMS)} = \sqrt{I_{dcl\_mag}^2 + \sum_{i=1}^{s} I_{dch(i)\_mag}^2} \\ P_{cap} = I_{dcl\_mag}^2 R_{(f_{dcl})} + \sum_{i=1}^{s} I_{dch(s)\_mag}^2 R_{(f_{dch(s)})} \end{cases} \tag{20}$$

The implementation of the proposed optimal modulation scheme for multiple drives with different switching frequencies is described in Case 3 of Fig. 3(a). In addition, the optimal phase shifts of the carrier signal are obtained by the PSO algorithm in Fig. 3(b).

III. Case Study

According to the derived analytical model and the modulation strategy proposed in Fig. 3, the optimal phase shifts of the drives under different parameters can be obtained, as shown in Table II. Taking three drives as an example, Table II (a) gives the calculation results of the optimum phase shifts for each drive at different power factors. Similarly, the table can also represent the results for different conductance (reciprocal of load) and modulation factors for multiple drives. With the identical power factors in the multiple drives, it can be seen that both the optimal phase shifts of the carrier signal and modulation signal are 0°, 60°, and 120° in the multiple drives, which agrees well with (15). With the different power factors in the multiple drives, the optimal phase shifts of the carrier signal and the modulation signal are dynamic, which is obtained by the PSO algorithm. Meanwhile, if N drives have the same switching frequency, and one of those has a significantly lower load, the optimal phase shifts of the modulation signal would converge towards that of $N-1$ drives. Table II (b) gives the calculation results of the optimum phase shifts for each drive at the different switching frequencies. The optimal phase shifts of the modulation signal are all 0°, 60°, and 120°, which are consistent with (15). Furthermore, with the different switching frequency in the multiple drives, the optimal phase shifts of the carrier signal are dynamic, which is obtained by the PSO algorithm. The method adopted is to obtain the look-up table according to the offline pre-computation of the optimized modulation scheme proposed in Fig. 3. The table is then embedded into the control program.

Fig. 4 shows the RMS current of the DC-link capacitors of low-frequency harmonic and high-frequency harmonic with different carrier and modulation phase shifts when three drives are connected in parallel. In Fig. 4, three cases are considered, respectively, with identical parameters, different loads, and different switching frequency in the multiple drives. When the identical parameters in the three drives are set in Fig. 4 (a) and (b), it can be seen that both the optimal phase shifts of the carrier signal and the modulation signal are 0°, 60°, and 120° in the multiple drives, which agrees well with Table I. When the different loads with 100%, 80%, and 60% values in the three drives are set in Fig. 4 (c) and (d), it can be seen that the optimal phase shifts of the carrier signal and the modulation signal are [0°, 72°, 117°] and [0°, 61°, 109°], respectively, which consistent with the results in Table I. When the different switching frequency with 1.0, 1.5, and 2.0 times in the three drives are set in Fig. 4 (e) and (f), it can be seen that the optimal phase shifts of the carrier signal and the modulation signal are [0°, 60°, 120°] and [0°, 84°, 105°], respectively, which is also consistent with the results in Table I.

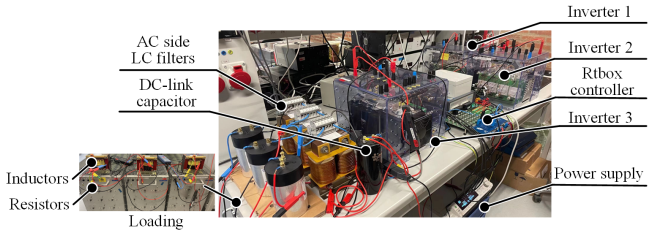
The benchmark of the DC-link capacitor RMS current with identical parameters and different N is further analyzed in Fig. 5. The RMS current ratios of DC-link capacitors, including four phase shift strategies of the carrier signal and the modulation signal, are compared. It can be seen that the RMS current of the DC-link capacitor with the proposed modulation method is only 34.3% to 15.9% of that without a phase shift scheme if N varies from 2 to 20, respectively. Based on the frequency-dependent ESR values and DC-link capacitor ripple current spectrum, the power loss of the specific DC-link capacitors can be obtained.

IV. Experimental Verification

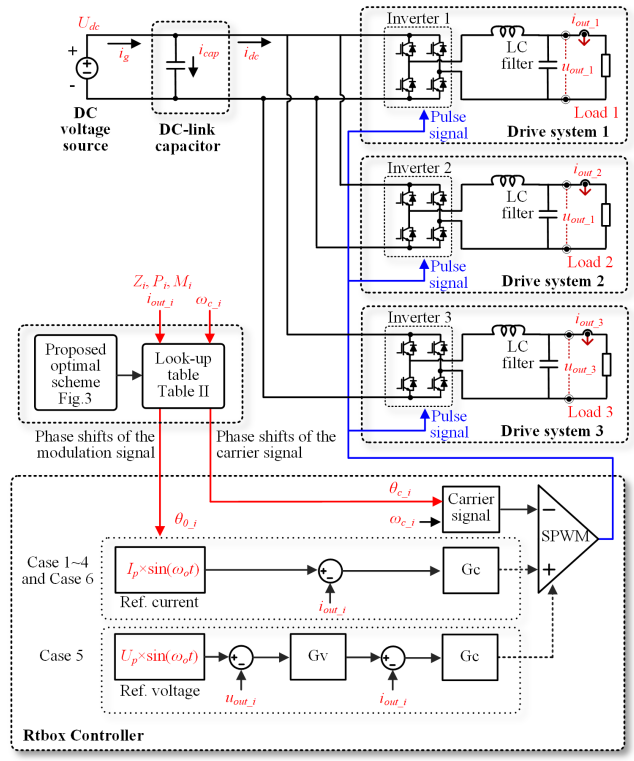
A. Experimental setup

The experimental platform and the control schematic are shown in Fig. 6, where three drives are connected in parallel. Each inverter consists of four IGBTs (with antiparallel diodes). In addition, each inverter is configured with an LC-type filter and a load. The RT-box controller is used, which integrates the FPGA chip to control multiple drives simultaneously, thus the clock frequency of each drive is synchronized. It should be noted that when each drive has a separate control platform, the clock synchronization settings for the DSPs or FPGAs of different drives can be achieved by the clock synchronization methods [26], [27].

The control schematic is presented in Fig. 6(b), where the double-loop control method and single-loop control method are both adopted. Firstly, the reference voltage $U_P \times \sin(\omega_o t)$ or reference current $I_P \times \sin(\omega_o t)$ are given, and the frequency ω_0 can be changed along with different motor speed. In the double-loop control method, compared to the reference voltage and the measurement voltage u_{out-i}, the voltage error goes through a PI voltage controller (Gv) to generate the reference current. In the single-loop control method, the current error, generated by comparing the reference current and the feedback current i_{out-i}, passes through a PI current controller Gc to generate modulation ratios of full-bridge drives. Finally, the triangular carrier (switching frequency is ω_{c-i}) and the



(a) Experimental prototype of the multiple drives



(b) Schematic diagram of the multiple drives

Fig. 6. Experimental prototype and the schematic diagram.

modulation ratios can generate the PWM signals through modulation methods, where the pulse signal PWMs 1-3 are set for drive system 1-3, respectively. A dead time of 200 ns is set in the SPWM.

Meanwhile, how to integrate the proposed optimal scheme into the controller is given in Fig. 6(b). According to the modulation scheme shown in Fig. 3 for the three cases, the obtained Table II is embedded in the controller. The proposed optimal scheme aims to generate θ_{0-i} and θ_{c-i}, which can be obtained by setting different parameters of the drives (e.g., load, power factor, modulation ratio, switching frequency, etc.).

The specifications are shown in Table III, including six experimental cases. In Case 1, three drives have the same parameters, i.e., loads are 20 ohm and switching frequencies are 5 kHz. Case 2 has different loads in those three drives, i.e., the loads of drive 1-3 are 20 ohm, 25 ohm, and 33 ohm, respectively, and the switching frequencies are 5 kHz. Case 3 sets different switching frequencies, where loads are 20 ohm, and switching frequencies are 5 kHz, 7.5 kHz, and 10 kHz in drives 1-3, respectively. Case 4 sets both different loads and

TABLE III
SYSTEM PARAMETERS.

Circuit parameters	
DC source output voltage	150 V
AC side output voltage	110 V
Capacitance and ESR of DC-link capacitor	2.75 mF (100 Hz)
	122 mΩ (100 Hz)
LC filters in AC side	2 mH / 40 μF
PWM dead time	2×10^{-7} s
Inductance of LC nonlinear load	5.6 mH
Output frequency of inverters	Case 1-4, Case 6: 50 Hz
	Case 5: 30 ~ 90 Hz
AC side loads of three inverters	Case 1, Case 3, and Case 5: 20 Ω / 20 Ω / 20 Ω
	Case 2 and Case 4: 20 Ω / 25 Ω / 33 Ω
	Case 6: [20 20 20]→[20 20 25]→[20 25 33]→[20 33 50] Ω
Switching frequency of three inverters	Case 1-2, Case 5-6: 5 kHz / 5 kHz / 5 kHz
	Case 3 and Case 4: 5 kHz / 7.5 kHz / 10 kHz

different switching frequencies in drives 1-3, respectively. In Case 5, the experiment of dynamic output current frequency is given, where the single-loop current control method is used. Step changes in load and number of drives are shown in Case 6. Four different modulation schemes are compared, where Strategy 1 is the modulation method without the phase shift scheme, Strategy 2 represents the modulation scheme with only phase shifts of the switching-frequency carrier signal, Strategy 3 is the modulation method with phase shifts of only the low-frequency modulation signal, and Strategy 4 is the proposed modulation strategy with optimal phase shifts of both the low-frequency modulation signal and the switching-frequency carrier signal.

B. Case 1: Multiple drives with identical load and switching frequency

Fig. 7 shows the waveforms of the DC-side supply current i_g, the DC bus current i_{dc}, and the capacitor ripple current i_{cap} with identical parameters in multiple drives for all four strategies. i_{dc} and i_{cap} vary according to different phase shift schemes. The phase shifts are obtained from Case 1 in Fig. 3. The FFT analysis verifies the results that when the phase shifts of the modulation signal are 0°, 60°, and 120° (with Strategy 3 and Strategy 4), the low-frequency harmonics can be eliminated. When the phase shifts of the carrier signal are 0°, 60°, and 120° (with Strategy 2 and Strategy 4), the high-frequency harmonic current can be reduced. With Strategy 2 and Strategy 4, there are still high-order harmonics, which correspond to the shaded areas in Fig. 2. It shows that the RMS current of the DC-link capacitor with Strategy 2, Strategy 3, and Strategy 4 are 66.7%, 58.5%, and 31.3% of that with Strategy 1. The error of the experimental results with the benchmark in Fig. 5 is within 6%, indicating that the proposed analytical model is accurate. Meanwhile, the power loss of the DC-link capacitor with Strategy 4 is only 6.5% of that with Strategy 1.

To characterize the effect of nonlinear loads on the motor, the R-L nonlinear load (the inductor in series with the resistor) is set in the experimental prototype to emulate the AC motor non-linearity, as shown in Fig. 8. Due to the non-linear loads, its DC-link current harmonics increase, the ripple current of

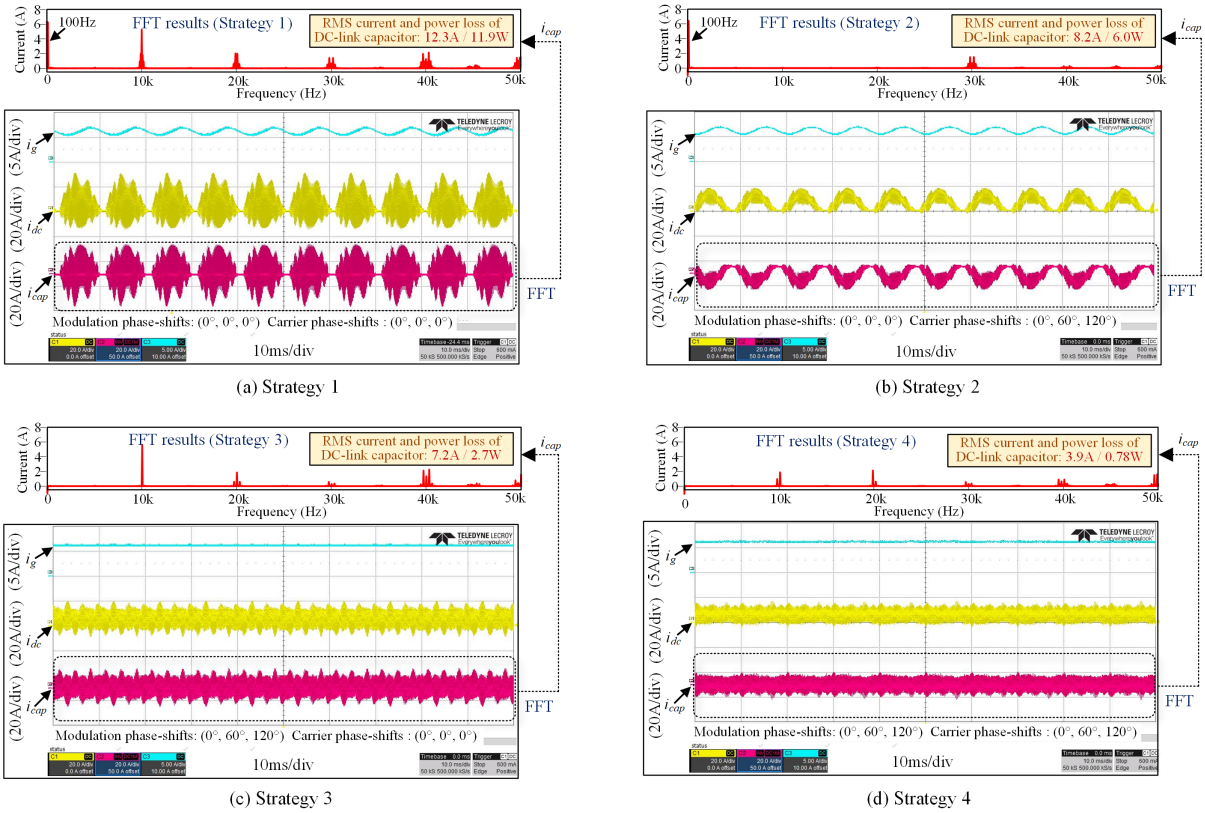


Fig. 7. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with identical parameters in multiple drives. (Three drives are in parallel with an identical load of 20 ohm and identical switching frequency of 5 kHz; i_g - DC-side supply current, i_{dc} - DC bus current; i_{cap} - capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

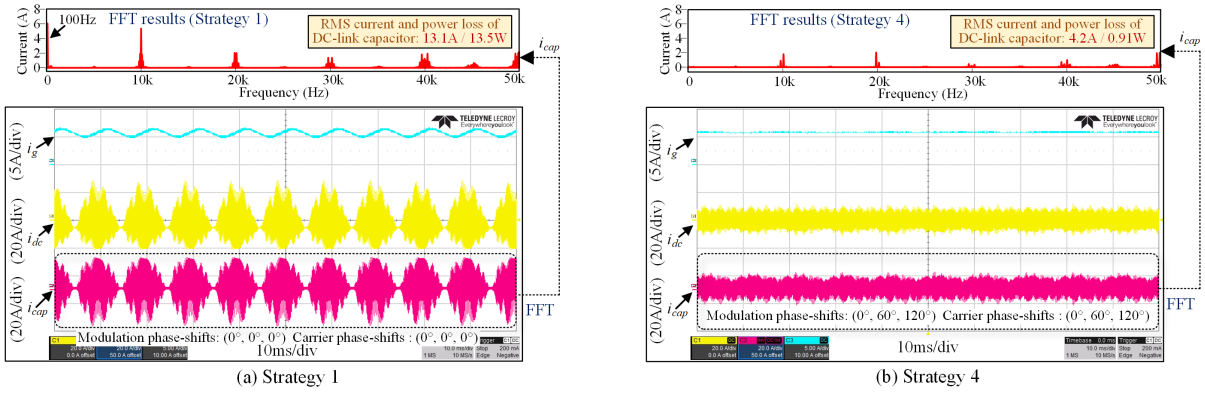


Fig. 8. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with R-L nonlinear load in multiple drives. (Three drives are in parallel with an identical load of 20 ohm resistor and 5.6 mH inductor, and identical switching frequency of 5 kHz; i_g - DC-side supply current, i_{dc} - DC bus current; i_{cap} - capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

the DC-link capacitor increases from 12.3A (experimental results for linear load in Fig. 7 of this paper) to 13.1 A in Strategy 1. In Fig. 8(a) and Fig. 8(b), comparing the results of the modulation strategy without phase shift and the modulation strategy with the proposed optimized phase shift, it can be found that considering the R-L nonlinear loads in operation, the modulation with the proposed optimized phase shift can also effectively reduce the ripple current of DC-link capacitor. In this case, the RMS current and power loss of the DC-link capacitor with the proposed optimized phase shift are 32% and 6.7% of that without phase shift, respectively. The results imply that the ripple current of the DC-link capacitor can be also optimized in multiple drives with R-L load.

C. Case 2: Multiple drives with identical switching frequency and different loads

Fig. 9 shows the waveforms of the DC-side supply current i_g, the DC bus current i_{dc}, and the capacitor ripple current i_{cap} with different loads in multiple drives for all four strategies. The i_{dc} and i_{cap} vary according to different phase shift strategies. With Strategy 2, the phase shifts of the carrier signal are 0°, 60°, and 120°. With Strategy 3, the phase shifts of the

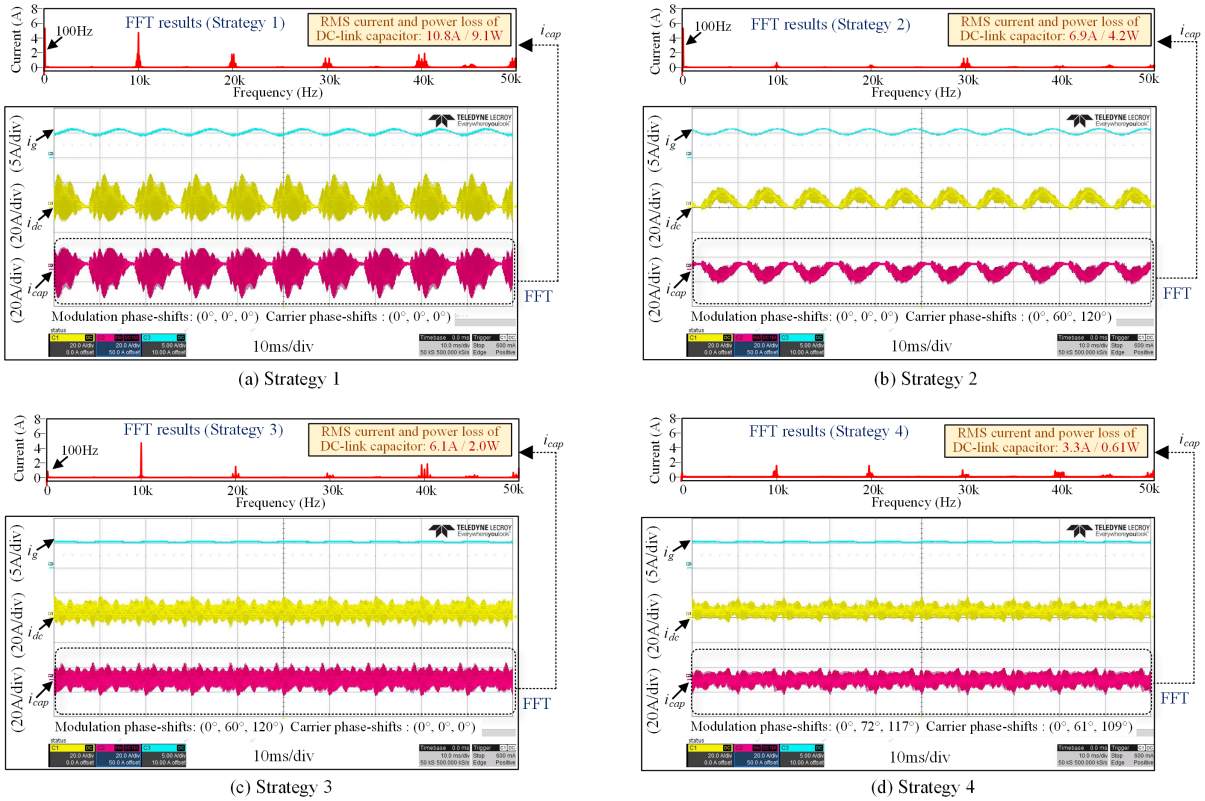


Fig. 9. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with different loads in multiple drives. (Three drives are in parallel with different loads of 20 ohm, 25 ohm, and 33 ohm, and an identical switching frequency of 5 kHz; i_g - DC-side supply current, i_{dc} - DC bus current; i_{cap} - capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

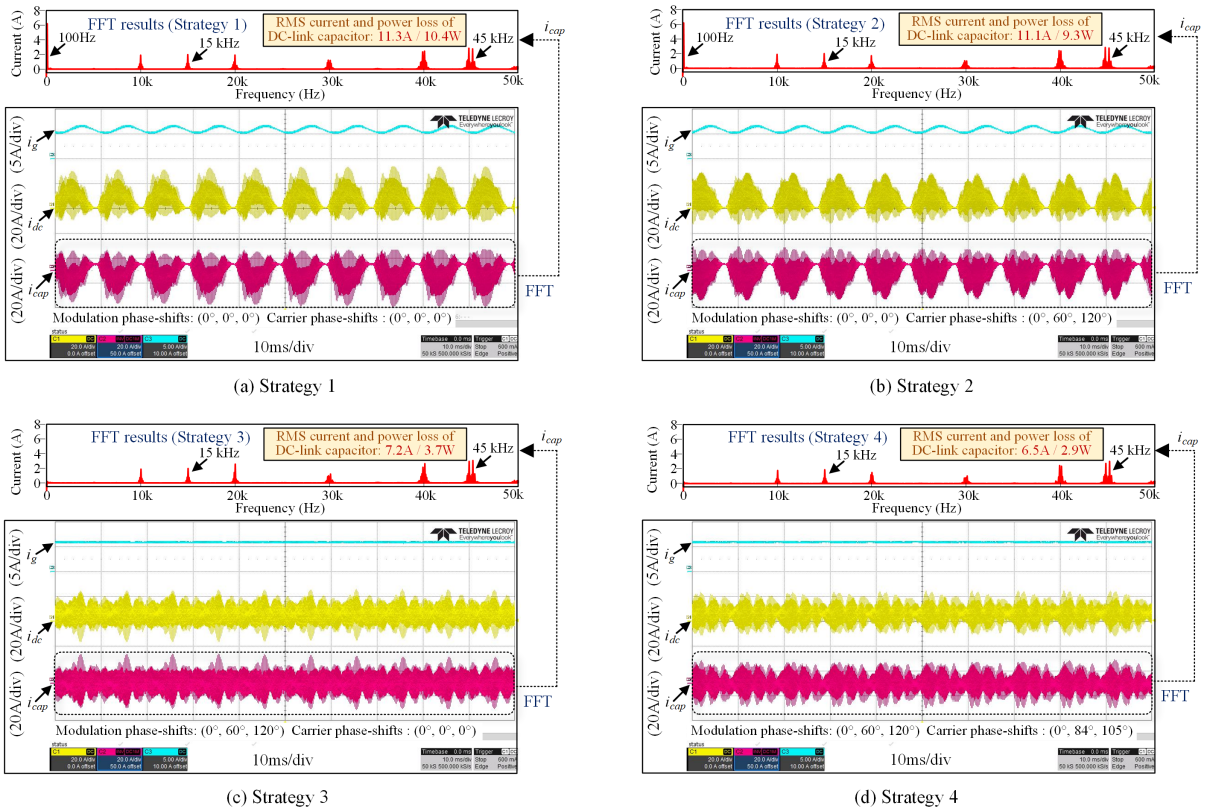
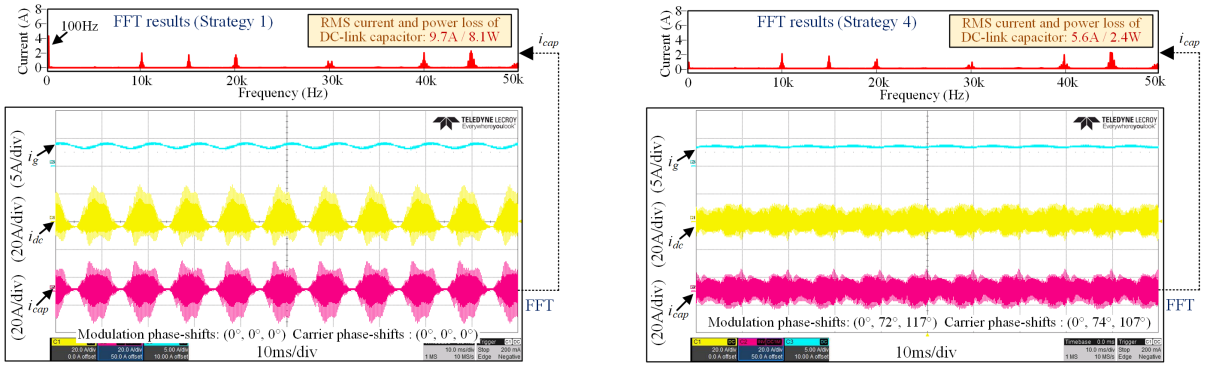
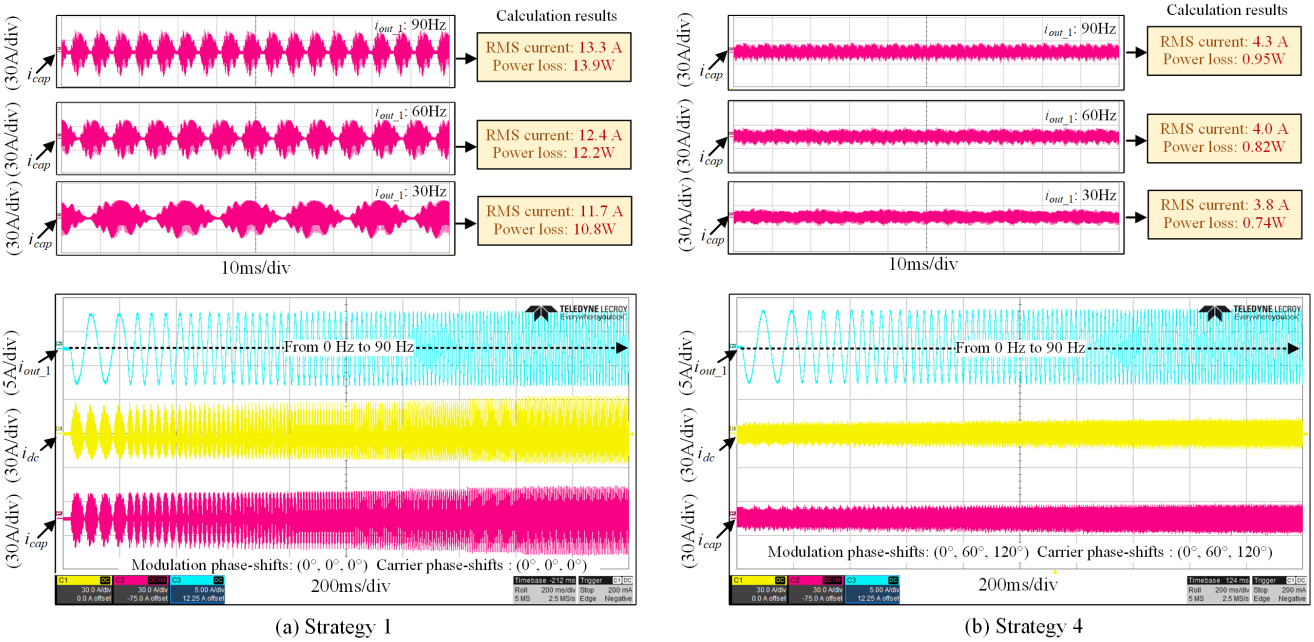


Fig. 10. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with different switching frequencies in multiple drives. (Three drives are in parallel with an identical load of 20 ohm, and different switching frequencies of 5 kHz, 7.5 kHz, and 10 kHz; i_g - DC-side supply current, i_{dc} - DC bus current; i_{cap} - capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)



(a) Strategy 1 (b) Strategy 4

Fig. 11. Steady-state experimental current waveforms and DC-link capacitor ripple current spectrum with both different loads and switching frequencies in multiple drives. (Three drives are in parallel with an identical load of 20 ohm, 25 ohm, and 33 ohm, and different switching frequencies of 5 kHz, 7.5 kHz, and 10 kHz; i_g - DC-side supply current, i_{dc} - DC bus current; i_{cap} - capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)



(a) Strategy 1 (b) Strategy 4

Fig. 12. Experimental current waveforms and DC-link capacitor ripple current spectrum with dynamic output current frequency. (Output current frequency change from 0 Hz to 90 Hz in operation; i_g - DC-side supply current, i_{dc} - DC bus current; i_{cap} - capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

modulation signal are 0°, 60°, and 120°. With Strategy 4, the optimal phase shifts (0°, 72°, 117° in the modulation signal and 0°, 61°, and 109° in the carrier signal) are obtained from the proposed modulation scheme in Fig. 3 and results in Table. II. The FFT analysis verifies the results that when the phase shifts of the modulation signal are 0°, 72°, and 117° with different loads of 20 Ω, 25 Ω, and 33 Ω in three drives (in strategy. 4), the low-frequency harmonics can be eliminated. When the phase shifts of the carrier signal are 0°, 61°, and 109° (in Strategy 4), the high-frequency harmonic current can be reduced. Through the calculation, the RMS current of the DC-link capacitor with Strategy 2, Strategy 3, and Strategy 4 are 63.9%, 56.5%, and 30.6% of that with Strategy 1. Meanwhile, the power loss of the DC-link capacitor with Strategy 4 is only 6.7% of that with Strategy 1. It indicates that the proposed optimal modulation method is reasonable in multiple drives with different loads.

D. Case 3: Multiple drives with identical load and different switching frequency

Fig. 10 shows the waveforms of the DC-side supply current i_g, the DC bus current i_{dc}, and the capacitor ripple current i_{cap} with different switching frequencies in multiple drives for all four strategies. i_{dc} and i_{cap} vary according to different phase shift strategies. With Strategy 2, the phase shifts of the carrier signal are 0°, 60°, and 120°. With Strategy 3, the phase shifts of the modulation signal are 0°, 60°, and 120°. With Strategy 4, the optimal phase shifts (0°, 60°, and 120° in the modulation signal and 0°, 84°, and 105° in the carrier signal) are obtained from the proposed modulation scheme in Fig. 3 and the results in Table. II. The FFT analysis verifies the

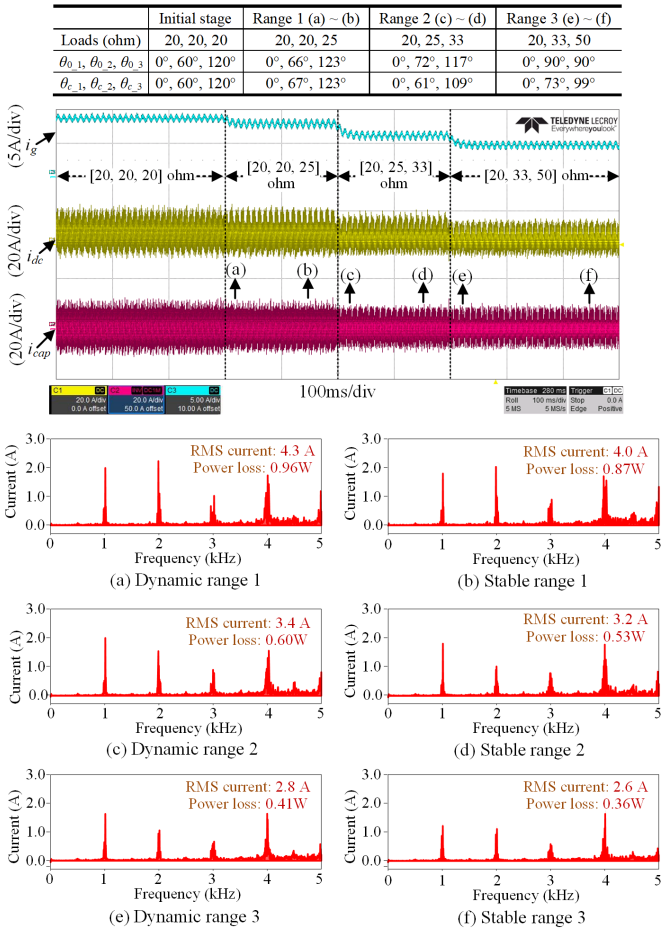


Fig. 13. Experimental capacitor ripple current waveforms and FFT analysis results with load steps and continuous changes. (i_g - DC-side supply current, i_{dc} - DC bus current; i_{cap} - capacitor ripple current; In Strategy 4 - modulation with proposed optimal phase shifts.)

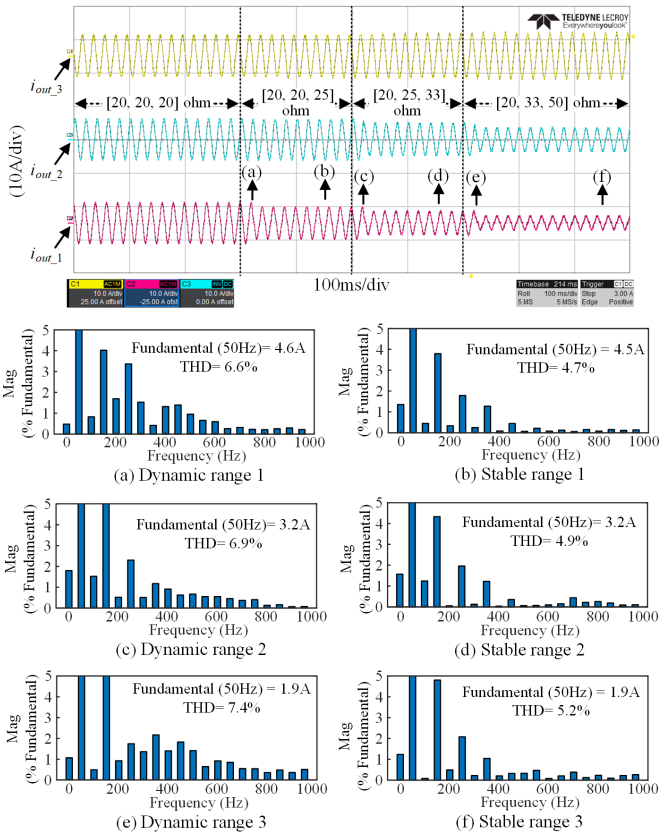


Fig. 14. Experimental output current waveforms and FFT analysis results with load steps and continuous changes. (i_{out-1}, i_{out-2}, and i_{out-3} respectively represent the output current of those three drives.)

results that when the phase shifts of the modulation signal are 0°, 60°, and 120° with different switching frequencies in three drives (with Strategy 3 and Strategy 4), the low-frequency harmonics can be eliminated, which is consistent with Case 1. When the phase shifts of the carrier signal are 0°, 84°, and 105° (with Strategy 4), the high-frequency harmonic current can be reduced. Through the calculation, the RMS current of the DC-link capacitor with Strategy 2, Strategy 3, and Strategy 4 are 98.2%, 63.7%, and 57.5% of that with Strategy 1. Meanwhile, the power loss of the DC-link capacitor with Strategy 4 is 27.9% of that with Strategy 1. It indicates that the proposed optimal modulation method is still effective in multiple drives with different switching frequencies.

E. Case 4: Multiple drives with different loads and switching frequency

Fig. 11 shows the current waveforms and DC-link capacitor ripple current spectrum with both different loads and switching frequencies in multiple drives. In this case, three drives are in parallel with different loads of 20 ohm, 25 ohm, and 33 ohm, and different switching frequencies of 5 kHz, 7.5 kHz, and 10 kHz. In Fig. 11(a), the phase shifts of the modulation signal and carrier signal are all 0°. In Fig. 11(b), according to the modulation strategy of Case 2 in Fig. 3, since the different switching frequencies do not affect the low-frequency harmonics, the optimal modulation phase shift can be obtained as (0°, 72°, 117°) based on the different loads in three drives. Meanwhile, additionally according to the modulation strategy of Case 3 in Fig. 3, considering the different switching frequency, the optimal carrier phase shift can be obtained as (0°, 74°, 107°). Through the calculation, the RMS current and power loss of the DC-link capacitor with the optimal phase shift are 57.7% and 29.6% of that without phase shift, respectively. It indicates that the proposed optimal modulation method is reasonable in multiple drives with both different loads and different switching frequency.

F. Case 5: Dynamic output frequency of drives

The R-L load is used to emulate the nonlinearity of the AC motor in this case. In this arrangement, the motor speed dynamic represents with output frequency of the drives. The experimental waveforms with dynamic output frequency are given to simulate the change in motor speed. Fig. 12 shows the results with the output frequency change from 0 Hz to 90 Hz in operation. The results show that the modulation strategy proposed in this paper can still reduce the ripple current of the DC-link capacitor when the output frequency of the drives varies dynamically. According to Fig. 12(a) and

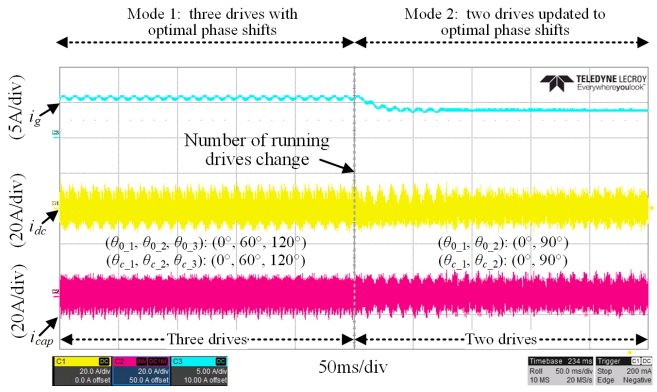


Fig. 15. Experimental current waveforms with switching from three drives to two drives. (i_g - DC-side supply current, i_{dc} - DC bus current; i_{cap} - capacitor ripple current; In Strategy 4 - modulation with proposed optimal phase shifts.)

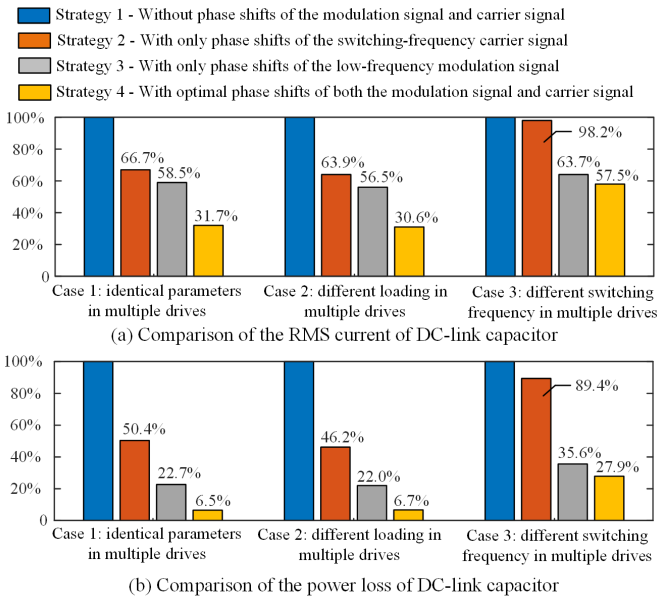


Fig. 16. Comparison of experimental results of the DC-link capacitor RMS current and power loss with different cases and different modulation strategies in the three drives.

Fig. 12(b), comparing the modulation strategy without phase shift and the modulation strategy with the proposed optimized phase shift, it can be found that at different output frequencies, the modulation with the proposed optimized phase shift can effectively reduce the ripple current of the DC-link capacitor. For example, when the output frequency is 30 Hz, the RMS current and power loss of the DC-link capacitor with the proposed optimized phase shift are 32.4% and 6.8% of that without phase shift, respectively. When the output frequency is 90 Hz, the RMS current and power loss of the DC-link capacitor with the proposed optimized phase shift are 32.5% and 7.0% of that without phase shift, respectively. The results imply that the optimized performance can be also maintained with dynamic output frequency in operation.

G. Case 6: Dynamic change of the load and number of drives

Fig. 13 shows the results of the source output current, the drive input current, and the DC-link capacitor ripple current with the load step and continuous changing of drives in operation. Four sets of load changes are given in three drives. The optimized modulation and carrier phase shifts are given in the table of Fig. 13 based on the load changes. The (a) represents the dynamic stage of Range 1, (b) represents the stable stage of Range 1, (c) represents the dynamic stage of Range 2, (d) represents the stable stage of Range 2, (e) represents the dynamic stage of Range 3, and (f) represents the stable stage of Range 3. Comparing the stable and dynamic stages of each range shows that continuous modifications to the modulation and carrier phase shift produce spectral effects. During dynamic changes, high-frequency components of the harmonics are higher than in the steady state. However, the dynamic stage only lasts for 1 to 2 fundamental periods before operating in the low-harmonic stable state.

In addition, the dynamic variation of the drive output current based on various operating conditions and phase shift changes is presented in Fig. 14. The four sets of load variations and optimized modulation and carrier phase shifts are consistent with Fig. 13. Similarly, the AC output current of the drives (using output current of drive 1 as an example) collected is subjected to FFT analysis, and the frequency spectrum analysis results and THD values are given. The (a)-(f) represent the dynamic and stable state of range 1, the dynamic and stable state of range 2, and the dynamic and stable state of range 3, respectively. Comparing the stable and dynamic stages of each range, it can be observed that the continuous modification of the modulation wave and carrier wave forms can also have spectral effects on the output current. During dynamic changes, the THD value is higher than the steady-state stage.

Fig. 15 shows the results under a dynamic change in the number of drives in operation. Before the change, Mode 1 is three drives with optimal phase shifts. Mode 2 is when the 3^{rd} drive is turned off, and the phase shifts of the 1^{st} and the 2^{nd} drives are updated to the optimal ones. In Mode 2, the DC-side supply current i_g reduces from 6.6 A to 4.4 A since the load of each drive in operation remains the same. In Mode 2, the controller only needs 2 to 3 fundamental cycles (within 100 ms) to update to the optimal phase shift. The results imply that the performance can be maintained by updating the optimal phase shifts according to the number of drives in operation.

H. Comparison of experimental results with different cases and different modulation strategies

Fig. 16 compares the capacitor ripple current and power loss under the four different modulation strategies and three cases for three drives system. When identical parameters or different loads are applied in multi-drive systems, the proposed modulation scheme can greatly reduce the RMS current and power loss of the DC-link capacitor. The results are consistent with the benchmark in Fig. 5. When different switching frequencies are applied in multi-drive systems, using the proposed modulation scheme also reduces the RMS current and power loss of the DC-link capacitors. Relatively, low-frequency ripple current components have a higher impact on the capacitor loss compared to high-frequency ones due

to frequency-dependent ESR values. In Strategy 4, the low-frequency ripple currents are reduced almost to zero. Therefore, from the capacitor power loss perspective, the percentage of reduction is even more significant compared to that of ripple current RMS value. In addition, different switching frequencies generate higher current harmonic distributions on the DC side than the identical switching frequency, such as the harmonic currents at 15 kHz and 45 kHz shown in Fig. 11. Therefore, the larger RMS currents and power losses of DC-link capacitors are introduced with different switching frequencies in multiple drives system.

V. Conclusions

This paper proposes an optimal modulation method for minimizing the ripple current of DC-link capacitors in multi-drive systems. Based on the derived analytical model and the calculated scheme, the method can concurrently reduce the low- and high-frequency harmonics of DC-link capacitors and is applicable for systems with different loads, power factors, modulation ratios, and switching frequency in multi-drive systems. In the case studies given in Fig. 5, the RMS current of the DC-link capacitors is reduced to 34.3% to 15.9% for systems with 2 to 20 drives, respectively, compared to that without the phase shift scheme. The RMS current and power loss of the DC-link capacitor are reduced to 31.7% and 6.5% with the identical parameters, 30.6% and 6.7% with the different loads, 57.5% and 27.9% with the different switching frequencies, respectively, for an experimental system with three multi-drive based on the proposed method. The performance is also verified under a dynamic change of the load, switching frequency, output frequency, and number of multi-drive in operation by updating the phase shifts.

References

[1] D. Kumar, F. Zare, and A. Ghosh, "DC microgrid technology: System architectures, AC grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects," *IEEE Access*, vol. 5, pp. 12 230–12 256, Jun. 2017.

[2] A. K. Kaviani, B. Hadley, and B. Mirafzal, "A time-coordination approach for regenerative energy saving in multiaxis motor-drive systems," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 931–941, Feb. 2012.

[3] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "Impact of interleaving on ac passive components of paralleled three-phase voltage-source converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, May-Jun. 2010.

[4] "Slimline IGBT Stacks." Semikron, https://www.semikron.com/products/product-lines/air-cooled-igbt-stacks/semikube-slimline-igbt-stacks.html, 2022.

[5] H. M. Delpino and D. Kumar, "Line harmonics on systems using reduced DC-link capacitors," in *Proc. 39th Annu. Conf. IEEE Ind. Electron.*, Nov. 2013, pp. 961–966.

[6] H. Wang, S. Huang, D. Kumar, Q. Wang, X. Deng, G. Zhu, and H. Wang, "Lifetime prediction of DC-link capacitors in multiple drives system based on simplified analytical modeling," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 844–860, Jan. 2021.

[7] D. Kumar, P. W. Wheeler, J. C. Clare, and T.-W. Kim, "Weight/volume effective multi-drive system based on two-stage matrix converter," in *Proc. 34th Annu. Conf. IEEE Ind. Electron.*, Nov 2008, pp. 2782–2787.

[8] "The benefits of DC-sharing—focus on drives." Danfoss, https://www.focusondrives.com/the-benefits-of-dc-sharing/, 2015.

[9] "Vacon nxp common DC bus utilize and redistribute energy efficiently." VACON, https://files.danfoss.com/download/DrivesDKDDPB911A122_NXP_Common_DC_Bus_LR.pdf, 2016.

[10] Z. Ni, Q. Qian, S. Xie, J. Xu, and B. Zeng, "Harmonic suppression and stability enhancement for grid-connected inverters based on UPQC," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sept. 2018, pp. 4922–4926.

[11] H. Wang, C. Li, G. Zhu, Y. Liu, and H. Wang, "Model-based design and optimization of hybrid dc-link capacitor banks," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8910–8925, Sep. 2020.

[12] B. Yao, X. Ge, D. Xie, S. Li, Y. Zhang, H. Wang, and H. Wang, "Electrothermal stress analysis and lifetime evaluation of dc-link capacitor banks in the railway traction drive system," *IEEE J. of Emerg. Se. Topics in Power Electron.*, vol. 9, no. 4, pp. 4269–4284, 2021.

[13] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—an overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.

[14] B. Yao, X. Ge, H. Wang, H. Wang, D. Zhou, and B. Gou, "Multi-timescale reliability evaluation of DC-link capacitor banks in metro traction drive system," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 1, pp. 213–227, Mar. 2020.

[15] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, Mar. 2008.

[16] X. Lyu, Y. Li, and D. Cao, "DC-link RMS current reduction by increasing paralleled three-phase inverter module number for segmented traction drive," *IEEE J. Emerg. Sel. Topics in Power Electron.*, vol. 5, no. 1, pp. 171–181, Mar. 2017.

[17] J. S. Siva Prasad and G. Narayanan, "Minimization of grid current distortion in parallel-connected converters through carrier interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan. 2014.

[18] Y. Yang, P. Davari, F. Zare, and F. Blaabjerg, "A DC-link modulation scheme with phase-shifted current control for harmonic cancellations in multidrive applications," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1837–1840, Mar. 2016.

[19] Y. Yang, P. Davari, Z. Firuz, and F. Blaabjerg, "Enhanced phase-shifted current control for harmonic cancellation in three-phase multiple adjustable speed drive systems," *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 996–1004, Apr. 2017.

[20] S. Baburajan, H. Wang, F. Mandrile, B. Yao, Q. Wang, D. Kumar, and F. Blaabjerg, "Design of common DC-link capacitor in multiple-drive system based on reduced DC-link current harmonics modulation," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9703–9717, Aug. 2022.

[21] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice*. John Wiley & Sons, 2003, vol. 18.

[22] F. Vasca and L. Iannelli, *Dynamics and control of switched electronic systems*. London, U.K.: Springer, 2012.

[23] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proc. Int. Conf. Neural Netw.*, vol. 4, 1995, pp. 1942–1948 vol.4.

[24] M. Steczek, P. Chudzik, M. Lewandowski, and A. Szelag, "PSO-based optimization of DC-link current harmonics in traction VSI for an electric vehicle," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8197–8208, Oct. 2020.

[25] Y. Peng, S. Zhao, and H. Wang, "A digital twin based estimation method for health indicators of DC–DC converters," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2105–2118, Oct. 2021.

[26] T. Xu, F. Gao, X. Wang, and F. Blaabjerg, "A carrier synchronization method for global synchronous pulsewidth modulation application using phase-locked loop," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10 720–10 732, Nov. 2019.

[27] J.-S. Kim, D.-H. Kim, J.-H. Lee, and J.-S. Lee, "Smooth pulse number transition strategy considering time delay in synchronized svpwm," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2252–2261, Feb. 2023.

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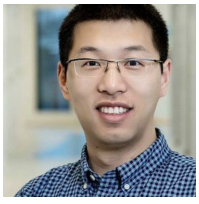

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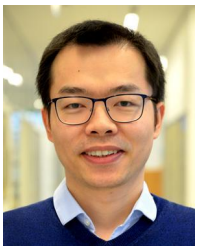

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