AALBORG UNIVERSITY

Selective compensation of voltage harmonics in grid-connected microgrids

Savaghebi, Mehdi; Vasquez, Juan Carlos; Jalilian, Alireza; Guerrero, Josep M.; Lee, Tzung-lin

Selective compensation of voltage harmonics in grid-connected microgrids

Mehdi Savaghebi [a], Juan C. Vasquez [b], Alireza Jalilian [a], Josep M. Guerrero [b], Tzung-Lin Lee [c]

Emails: savaghebi@iust.ac.ir, juq@et.aau.dk, jalilian@iust.ac.ir, joz@et.aau.dk, tzunglin.lee@gmail.com

[a] Center of excellence for power system automation and operation, Electrical engineering department, Iran University of science and technology, Tehran 16846-13114, Iran

[b] Institute of energy technology, Aalborg University, Aalborg east DK-9220, Denmark

[c] Department of electrical engineering, National Sun Yat-sen University, Kaohsiung 80424, Taiwan

Corresponding author:

Mehdi Savaghebi

Email: savaghebi@iust.ac.ir , mhsavagh@gmail.com

Tel: (+98) 937 458 1790

Fax: (+98) 21 73225777

Address: Electrical engineering department, Iran University of science and technology, Tehran 16846-13114, Iran

Abstract

In this paper, a novel approach is proposed for selective compensation of main voltage harmonics in a grid-connected microgrid. The aim of compensation is to provide a high voltage quality at the point of common coupling (PCC). PCC voltage quality is of great importance due to sensitive loads that may be connected. It is assumed that the voltage harmonics are originated from distortion in grid voltage as well as the harmonic current of the nonlinear loads. Harmonic compensation is achieved through proper control of distributed generators (DGs) interface converters. The compensation effort of each harmonic is shared considering the respective current harmonic supplied by the DGs. The control system of each DG comprises harmonic compensator, fundamental power controllers, voltage and current proportional-resonant controller and virtual impedance loop. Virtual impedance is considered at fundamental frequency to enhance power control and also at harmonic frequencies to improve the nonlinear load sharing among DGs. The control system design is discussed in detail. The presented simulation results demonstrate the effectiveness of the proposed method in compensation of the voltage harmonics to an acceptable level.

Keywords

1. Introduction

The proliferation of different nonlinear loads in electrical systems has resulted in the voltage harmonic distortion. This distortion can cause variety of problems such as protective relays malfunction, overheating of motors and transformers and failure of power factor correction capacitors [10,27]. Thus, in different standards some limits are recommended for voltage harmonics, e.g. IEEE Standard 519-1992 [18].

On the other hand, it is well-known that the Distributed Generators (DGs) often consist of a prime mover connected through a power-electronic interface converter to the utility grid or microgrid. Microgrid is a local grid consisting of DGs, energy storage systems and dispersed loads which may operate in both grid-connected and islanded modes [20].

The main role of an interface converter is to control active power injection. However, compensation of power quality problems, such as voltage harmonics can be achieved through proper control strategies. A single-phase DG capable of improving voltage waveform is presented in [9]. DG is controlled to operate as a shunt active power filter. In other words, DG injects harmonic current to improve voltage waveform.

The voltage harmonic compensation methods of [17,30,31,34] are based on making the DG emulate a resistance at harmonic frequencies. The idea of resistance emulation is originally proposed in [2] for active power filters.

A method for compensation of voltage harmonics in an islanded microgrid has been presented in [24]. This method is also based on the resistance emulation. Furthermore, a droop characteristic based on the DG harmonic reactive power has been considered to achieve sharing of the harmonic compensation effort. That was the first approach toward cooperative control of DGs to compensate voltage harmonics. A similar approach applicable to both grid-connected and islanded operating modes of microgrid is proposed in [33].

It is well known for the active power filters that the selective compensation of harmonics can provide some advantages in terms of filter rating and control robustness [23,25,28]. Similarly, it can be concluded that selective compensation methods are more appropriate in the case of harmonic compensation by DG units while the approaches of [24, 33] are based on compensating the voltage harmonics of a microgrid in a non-selective manner. Furthermore, the aforementioned harmonic compensation methods are designed for compensation of voltage harmonics at the DG terminal while usually the power quality at the point of common coupling (PCC) is

the main concern due to the sensitive loads that may be connected. In addition, if the DGs try to compensate the local voltage harmonics, the harmonic distortion may be amplified in some of the buses of electrical system. This phenomenon is called "whack-a-mole" [38]. Thus, by direct compensation of PCC voltage harmonics, good power quality can be guaranteed for the sensitive loads connected to PCC.

In this paper, a method is proposed for compensation of the PCC main voltage harmonics in a grid-connected microgrid. It is assumed that the harmonic distortion is caused by the nonlinear loads as well as grid voltage distortion. Compensation is performed selectively for the main voltage harmonic orders. Compensation effort of each harmonic is shared considering the respective current harmonic supplied by the DGs.

The rest of the paper is organized as follows. DG control system structure is explained in section 2. The details of power calculation and control, voltage and current controllers, virtual impedance loop and harmonic compensation method are presented in this section. Section 3 is dedicated to the control system design in order to select proper control parameters. Simulation results are presented in section 4.

2. Microgrid DGs control system

Fig. 1 shows the single-line diagram of a grid-connected microgrid consisting of electronically-interfaced DGs and dispersed linear and nonlinear loads which are connected to PCC through some tie lines. Microgrid is connected to the utility grid through a tie line (Z_g) and a transformer with the equal impedance of Z_t.

As shown in Fig. 1, PCC voltage harmonics data are extracted by the measurement block and sent to all DGs. These data are applied by the DG control system to generate proper control signals. Compensation is performed for the main harmonics of PCC voltage; thus, it is only necessary to extract and send these harmonics data. In this paper, 5th and 7th harmonics are considered as the main voltage harmonic orders.

Considering this fact that PCC can be far from DGs, low bandwidth communication (LBC) is applied for sending PCC voltage harmonic data. Low communication bandwidth is selected in order to avoid dependence on the high bandwidth availability which may endanger the system reliability. In order to ensure that LBC is sufficient, the transmitted data should consist of approximately dc signals. Hence, the PCC voltage harmonic components are extracted in *dq* (synchronous) reference frame and then transmitted to each DG controller. Afterwards, as shown in Fig. 2, harmonic voltages are transformed to *αβ* (stationary) reference frame and fed to "Selective Harmonic Compensator" block. The rotation angles of transformations are set to -5ϕ* and 7ϕ* for the 5th and 7th harmonics, respectively. ϕ* is the reference of DG voltage phase angle which is generated by the active power controller.

The details of PCC 5th and 7th harmonic extraction are depicted in the "Measurement Block" of Fig. 2. At first, the measured PCC voltage (v_{abc}) is transformed to *dq* frames rotating at -5ω, and 7ω, respectively. ω is the system angular frequency estimated by a phase-locked loop (*PLL*) [22]. Afterwards, two second-order low pass filters (*LPF*) with 2Hz cut-off frequency are used to extract 5th and 7th harmonics (v_{dq}^{5} and v_{dq}^{7}, respectively).

Second-order filters are applied since the first-order ones were not able to provide acceptable performance. For instance, the performance of first- and second-order filters (both with 2Hz cut-off frequency) in extracting *d*-component of PCC voltage fifth harmonic (v_{d}^{5}) is compared in Fig. 3. As it can be seen, first-order one is not able to filter the oscillations, properly and thus cannot meet the requirement of low bandwidth communication. It should be emphasized that the harmonic compensation control signals are generated and applied locally by each DG controller without using any data communication.

The detailed structure of each DG power stage and control system is shown in Fig. 2. The power stage consists of a dc link, an interface inverter and an LC filter. It is assumed that an approximately constant dc voltage (V_{dc}) is maintained at the dc link. The details about the control of dc link voltage for different distributed resources can be found in [4]. However, a feedforward loop can be included as shown in Fig. 2 in order to consider small V_{dc} variations in generation of the inverter gate signals by pulse width modulator (*PWM*).
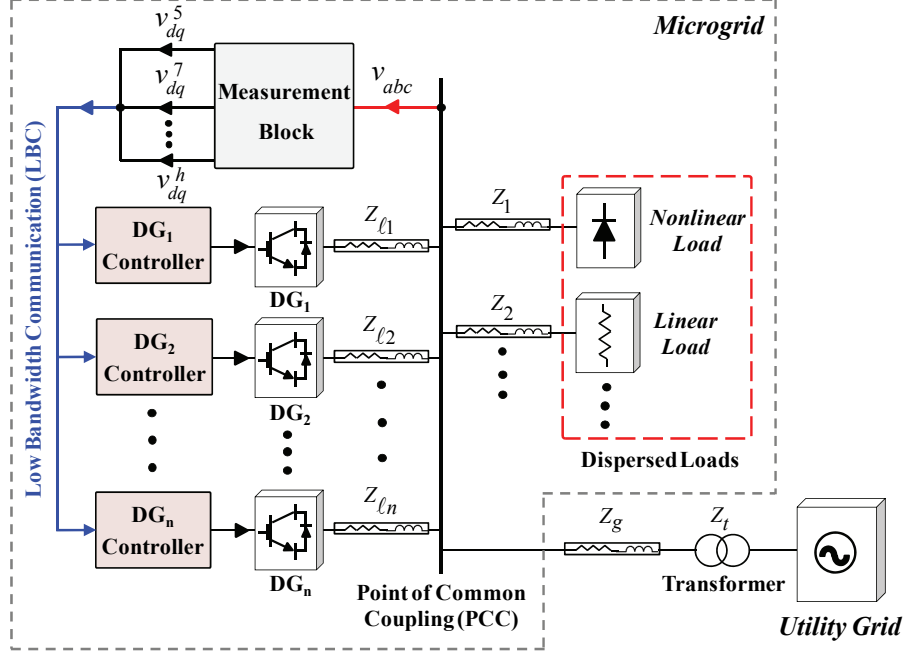
3

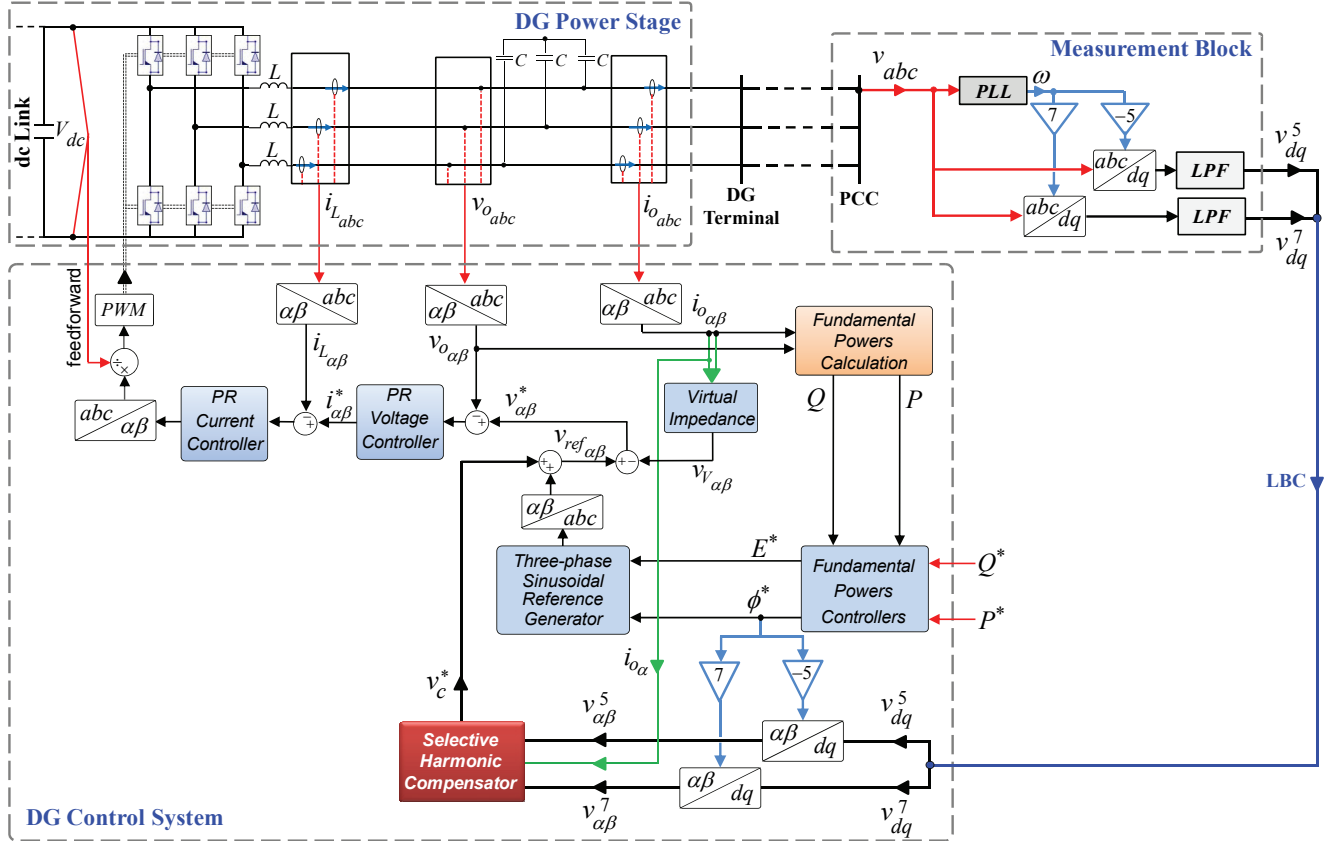Fig. 1. Structure and control system of a grid- connected microgrid.

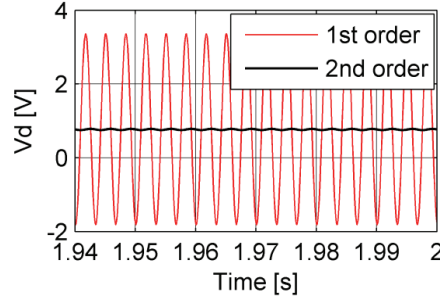Fig. 2. DG power stage and control system.

Fig. 3. *d*-component of PCC voltage fifth harmonic.

The DG control system is designed in *αβ* reference frame; thus, Clarke transformations are used to transform the variables between *abc* and *αβ* coordinates. As shown in Fig. 2, the reference of the DG output voltage in *αβ* frame ($v_{\alpha\beta}^*$) is provided by power controllers, virtual impedance loop and harmonic compensator. On the other hand, instantaneous output voltage ($v_{o_{abc}}$) is measured and transformed to *αβ* frame ($v_{o_{\alpha\beta}}$). Then, according to $v_{\alpha\beta}^*$ and $v_{o_{\alpha\beta}}$, the reference current ($i_{\alpha\beta}^*$) is generated. As seen in Fig. 2, LC filter inductor current is transformed to *αβ* frame ($i_{L_{\alpha\beta}}$) and controlled by the current controller. The output of the current controller is transformed back to *abc* frame to provide three-phase voltage reference for *PWM* block. Finally, *PWM* controls the switching of the inverter based on this reference.

2.1. Fundamental powers calculation

As seen in Fig. 2, instantaneous output voltage and current in *αβ* frame ($v_{o_{\alpha\beta}}$ and $i_{o_{\alpha\beta}}$, respectively) are used for calculation of the fundamental powers.

Based on the instantaneous reactive power theory [1], the instantaneous values of active and reactive powers should be calculated using equations (1) and (2), respectively:

$$p = v_{o_\alpha} i_{o_\alpha} + v_{o_\beta} i_{o_\beta} \qquad (1)$$

$$q = v_{o_\beta} i_{o_\alpha} - v_{o_\alpha} i_{o_\beta} \qquad (2)$$

Each of the instantaneous powers consists of dc and ac (oscillatory) components. The dc components (average values of *p* and *q*) are fundamental active and reactive powers (*P* and *Q*, respectively) [29]. The oscillatory parts are generated by the harmonic and/or unbalance contents of the voltage and current. The dc components are extracted using two first-order low pass filters. The cut-off frequency of these filters is set to 2Hz.

2.2. Fundamental powers controllers

Assuming a mainly inductive electrical system, fundamental frequency three-phase active and reactive powers can be expressed by the following equations, respectively [12]:

$$P \approx 3 \cdot \frac{E \cdot V}{X} \sin\phi \qquad (3)$$

$$Q \approx 3 \cdot \frac{E \cdot V \cos\phi - V^2}{X} \qquad (4)$$

where *X* is the reactance between DG and electrical grid, *E* and *V* are the phase rms values of the DG inverter

5

output voltage and the grid voltage and ϕ represents the angle between E and V. Assuming that the phase angle of the grid voltage to be zero, ϕ will be equal to phase angle of the inverter voltage.

In practical applications, ϕ is normally small; thus, P and Q can be assumed decoupled $(\cos\phi \approx 1$ and $\sin\phi \approx \phi)$ and be controlled by DG output voltage phase angle and amplitude, respectively [3,12,15]. According to this, the following characteristics are considered for DG output power control in a grid-connected microgrid [15,26,37]:

$$\phi^* = \phi_0 + m_P(P^* - P) + m_I \int (P^* - P)\,dt \qquad (5)$$

$$E^* = E_0 + n_P(Q^* - Q) + n_I \int (Q^* - Q)\,dt \qquad (6)$$

where

- P^*: active power reference
- Q^*: reactive power reference
- E^*: phase voltage amplitude reference
- ϕ^*: phase angle reference
- E_0: rated phase voltage amplitude
- ϕ_0: rated phase angle ($\int \omega_0 dt = \omega_0 \cdot t$)
- ω_0: rated frequency
- m_P: active power proportional coefficient
- m_I: active power integral coefficient
- n_P: reactive power proportional coefficient
- n_I: reactive power integral coefficient

P^* can be determined to coincide with the maximum power which is provided by the DG prime mover. For instance, in the case of photovoltaic (PV) generation, a maximum power point tracker (MPPT) is applied to set P^* [36]. Alternatively, P^* and Q^* can be set by a centralized controller aiming the economic optimization of the microgrid [35].

2.3. Voltage and current controllers

Due to the difficulties of using proportional-integral (PI) controllers to track non-dc variables, proportional-resonant (PR) controllers are usually preferred in the stationary reference frame [5]. In this paper, PR voltage and current controllers are respectively as follow:

$$G_V(s) = k_{pV} + \sum_{k=1,5,7} \frac{2k_{rV_k} \cdot \omega_{cV_k} \cdot s}{s^2 + 2 \cdot \omega_{cV_k} \cdot s + (k \cdot \omega_0)^2} \qquad (7)$$

$$G_I(s) = k_{pI} + \sum_{k=1,5,7} \frac{2k_{rI_k} \cdot \omega_{cI_k} \cdot s}{s^2 + 2 \cdot \omega_{cI_k} \cdot s + (k \cdot \omega_0)^2} \qquad (8)$$

where k_{pV} (k_{pI}) and k_{rV_k} (k_{rI_k}) are the proportional and k^{th} harmonic (including fundamental component as the first harmonic) resonant coefficients of the voltage (current) controller, respectively. ω_{cV_k} and ω_{cI_k} represent the voltage and current controllers cut-off frequencies at k^{th} harmonic, respectively.

2.4. Virtual impedance loop

It has been assumed for the control of fundamental powers that the system impedances are mainly inductive. Thus, the accuracy of the power control is affected by the output impedance of the DG units as well as the line impedances. By including virtual impedance at fundamental frequency, the phase and magnitude of the output impedance can be fixed at the desired values and the effect of the line impedances can be mitigated [12-15].

Virtual resistance makes the oscillations of the system more damped [14]. The damping can also be provided by a physical resistance at the expense of efficiency decrease due to ohmic losses. In contrast with a physical resistance, the virtual resistance has no power losses, since is provided by a control loop; thus, it is possible to implement it without decreasing the efficiency [15]. Also, virtual inductance is considered to make the DG output impedance more inductive in order to improve the decoupling of P and Q. Thus, the virtual impedance enhances the droop controllers performance and stability [12,16].

Furthermore, the virtual impedance can provide additional features such as sharing of nonlinear (harmonic) load. Some methods for harmonic current sharing among parallel converters are presented in [6-8] and [11-14]. It is suggested in [6] to use each order of the harmonic current to produce a proportional voltage drop which is leading the current by 90°. In fact, a virtual output inductance is inserted at the harmonic frequencies. As an alternative approach, it is proposed in [7,8] and [11-14] to make the converters generate a virtual output resistance at the harmonic frequencies. This idea is applied for nonlinear load sharing in the present paper.

A three-phase system can be modeled as two independent single-phase systems in $\alpha\beta$ reference frame. Thus, the concept of virtual impedance can be demonstrated as Fig. 4 which shows the single-phase equivalent Thévenin circuit of an inverter with a virtual impedance loop [14]. Based on Fig. 4, the following equations can be extracted:

$$v_o(s) = G(s) \cdot v_{ref}(s) - Z_o(s) \cdot i_o(s) \tag{9}$$

$$Z_o(s) = Z'_o(s) + Z_v(s) \tag{10}$$

where $v_{ref}(s)$, $G(s)$ and $Z_o(s)$ are the reference voltage, control system closed-loop transfer function and output impedance, respectively. $Z'_o(s)$ represents the inverter output impedance without virtual impedance $Z_v(s)$.

The basic structure of the virtual impedance for $\alpha\beta$ frame is proposed in [16]. Here, this structure is extended as shown in Fig. 5 by including the harmonic virtual resistance. In this Fig., R_v and L_v are the fundamental frequency virtual resistance and inductance, respectively, and $R_{v,h}$ is the virtual resistance at 5th and 7th harmonics as the main harmonic orders.

As seen in Figs. 2 and 5, $\alpha\beta$ components of instantaneous output current ($i_{o_{\alpha\beta}}$) are fed to virtual impedance loop. Then, fundamental component ($i^1_{o_{\alpha\beta}}$) and 5th and 7th harmonic orders ($i^5_{o_{\alpha\beta}}$ and $i^7_{o_{\alpha\beta}}$) are extracted as explained in [32] and applied to implement selective virtual impedance. Applying the approach of [32], fundamental and harmonic frequencies can be directly extracted in $\alpha\beta$ frame. Finally, the output of virtual impedance loop ($v_{V_{\alpha\beta}}$) is subtracted from voltage reference ($v_{ref_{\alpha\beta}}$) in order to generate $v^*_{\alpha\beta}$.
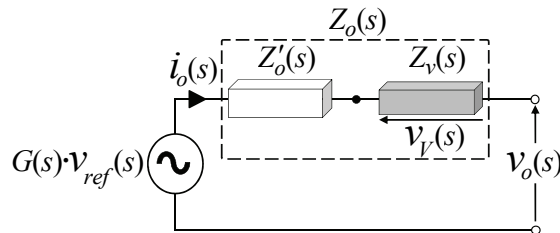

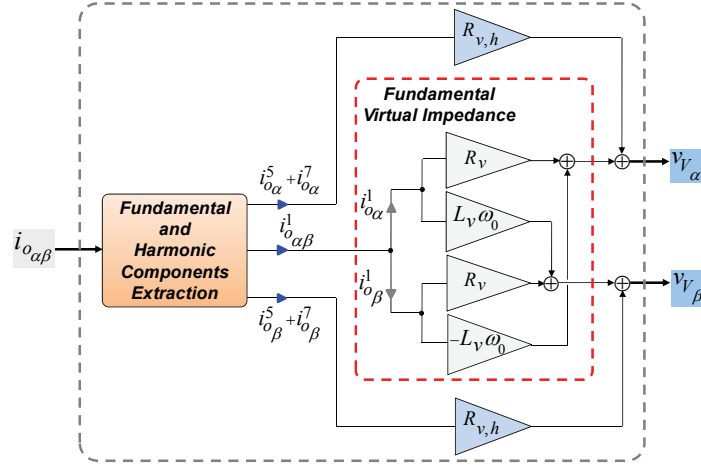**Fig. 4. Equivalent circuit of an inverter**

Fig. 5. Block diagram of selective virtual impedance.

2.5. Selective harmonic compensator

The details of "*Selective Harmonic Compensator*" block of Fig. 2 are presented in Fig. 6 for DG number i (DGi). As mentioned before, harmonic compensation is performed selectively for the main PCC voltage harmonics. Compensation reference of each harmonic ($v_{c,h}^*$ for h^{th} voltage harmonic) is generated separately and then, all of the compensation references are added together. Afterwards, the resultant value is multiplied by the ratio of DGi rated power ($S_{0,i}$) and the total power of the microgrid DGs ($\sum\limits_{j=1}^{n} S_{0,j}$) to generate total compensation reference (v_c^*) which is inserted as a voltage reference in the control system of Fig. 2. This way, the compensation workload is distributed among microgrid DGs according to their rated powers.

According to Fig. 6, $v_{c,h}^*$ is generated as follows:

$$v_{c,h}^* = v_{\alpha\beta}^h \cdot CG_h \cdot \left(HD_{I,h}^{\max} - HD_{I,h} \right) \qquad (11)$$

In equation (11), $v_{\alpha\beta}^h$ is PCC voltage h^{th} harmonic component in $\alpha\beta$ frame and CG_h is the compensation gain for h^{th} voltage harmonic. CG_h is a negative constant which is the same for all DGs. CG_h should be negative in order to generate a harmonic voltage with the polarity opposite of $v_{\alpha\beta}^h$ and consequently cancel the PCC voltage harmonic distortion. $HD_{I,h}$ represents the current h^{th} harmonic distortion index and $HD_{I,h}^{\max}$ is the maximum value of $HD_{I,h}$.
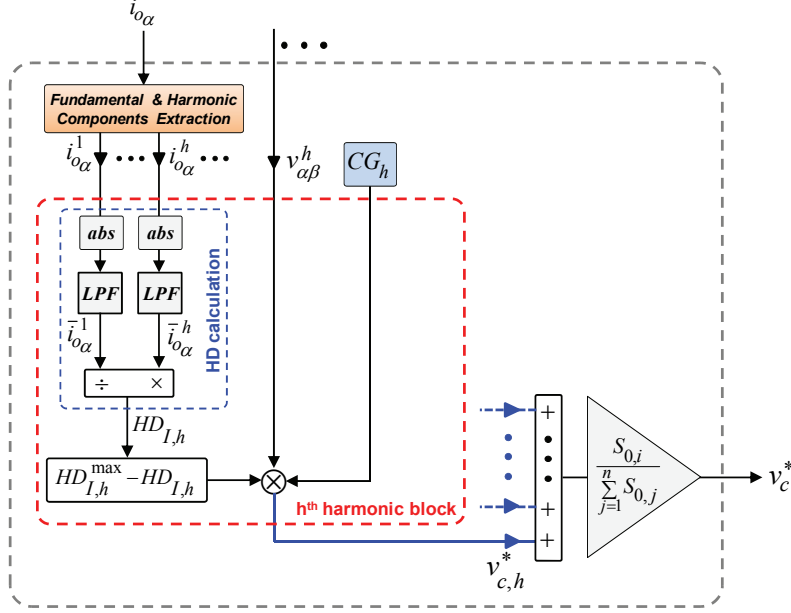
Fig. 6. Selective harmonic compensator block of DGi.

$HD_{I,h}$ is defined as the ratio of current h[th] harmonic and fundamental component magnitudes. Here, it is calculated as the ratio of rectified waveforms average values. The details of $HD_{I,h}$ calculation are provided in Fig. 6. Firstly, fundamental component and h[th] harmonic of α-axis output current ($i_{o_\alpha}^1$ and $i_{o_\alpha}^h$, respectively) are extracted [32] and then, $i_{o_\alpha}^1$ and $i_{o_\alpha}^h$ are rectified using absolute (*abs*) functions. Afterwards, *LPF*s (second-order with 2Hz cut-off frequency) are applied to calculate average values ($\bar{i}_{o_\alpha}^1$ and $\bar{i}_{o_\alpha}^h$, respectively). Finally, $HD_{I,h}$ is calculated through division $\bar{i}_{o_\alpha}^h$ by $\bar{i}_{o_\alpha}^1$.

It should be noted that the electrical system is assumed to be balanced. Thus, using β-component for calculation of $HD_{I,h}$ leads to the same result. However, in unbalanced condition it is necessary to extract positive and negative sequence of each harmonic to calculate harmonic distortion indices. Harmonic compensation in unbalanced condition is out of this paper scope.

Assuming that the magnitude of harmonic current remains less than the fundamental component, $HD_{I,h}^{\max}$ is set to 1. However, larger constants can be used as $HD_{I,h}^{\max}$ value.

$HD_{I,h}$ is considered as the index of hth voltage harmonic compensation effort. In fact, compensation of each PCC voltage harmonic is achieved through injecting respective current harmonic by the DGs. Thus, including $\left(HD_{I,h}^{\max} - HD_{I,h}\right)$ term in equation (11) contributes towards harmonic compensation effort sharing among DGs. Increase of compensation effort leads to $HD_{I,h}$ increase; thus, $\left(HD_{I,h}^{\max} - HD_{I,h}\right)$ and consequently the effort is decreased. So, an inherent negative feedback exists in the compensation method. This sharing method is similar to droop-control approach which is extensively used for fundamental power sharing in islanded microgrids [15].

9

A similar sharing idea has been presented in [24] using a droop characteristic based on the DG harmonic reactive power (*H*). But, calculation of *H* requires extracting the rms values of oscillatory parts of instantaneous powers calculated by equations (1) and (2). This kind of rms calculation needs a high computational effort and convergence time due to broad harmonic spectrum.

3. Control system design

3.1. Power controllers

A small signal analysis similar to what has been performed in [14] is applied as follows in order to select the parameters of power controllers. Equations (3) and (4) can be linearized as follows:

$$\hat{P} = 3 \cdot \frac{V}{L_v \cdot s} \left(E \cdot \cos\phi \cdot \hat{\phi} + \hat{E} \cdot \sin\phi \right) \qquad (12)$$

$$\hat{Q} = 3 \cdot \frac{V}{L_v \cdot s} \left(\hat{E} \cdot \cos\phi - E \cdot \sin\phi \cdot \hat{\phi} \right) \qquad (13)$$

where the symbol ^ represents the small signal value.

Then, by replacing (12) and (13) in the small signal forms of (5) and (6) and including the first-order low pass filter used for power calculation, the following equations are achieved:

$$\hat{\phi} = -\left(\frac{\omega_c}{s + \omega_c} \right) \cdot \left(m_P + \frac{m_I}{s} \right) \cdot 3 \cdot \frac{V}{L_v \cdot s} \left(E \cdot \cos\phi \cdot \hat{\phi} + \hat{E} \cdot \sin\phi \right) \qquad (14)$$

$$\hat{E} = -\left(\frac{\omega_c}{s + \omega_c} \right) \cdot \left(n_P + \frac{n_I}{s} \right) \cdot 3 \cdot \frac{V}{L_v \cdot s} \left(\hat{E} \cdot \cos\phi - E \cdot \sin\phi \cdot \hat{\phi} \right) \qquad (15)$$

where ω_c represent the low pass filter cut-off frequency.

Afterwards, by substituting (15) in (14) and assuming $\phi \approx 0$, small-signal dynamics of the closed-loop system can be expressed as follows:

$$s^6 + As^5 + Bs^4 + Cs^3 + Ds^2 + Es + F = 0 \qquad (16)$$

where

$$A = 2 \cdot \omega_c$$

$$B = \omega_c \left[\omega_c + \frac{3 \cdot V}{L_v} (E \cdot m_P + n_P) \right]$$

$$C = \frac{3 \cdot \omega_c \cdot V}{L_v} \left[E(m_I + \omega_c \cdot m_P) + \omega_c \cdot n_P + n_I \right]$$

$$D = \frac{3 \cdot \omega_c^2 \cdot V}{L_v} \left[E \left(m_I + \frac{3 \cdot V \cdot n_P \cdot m_P}{L_v} \right) + n_I \right]$$

$$E = \frac{9 \cdot \omega_c^2 \cdot V^2 \cdot E}{L_v^2} (n_P m_I + n_I \cdot m_P)$$

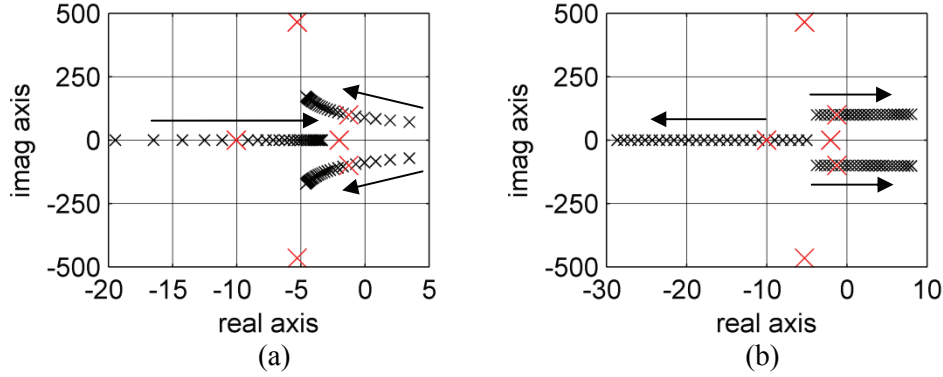$$F = \frac{9 \cdot \omega_c^2 \cdot V^2 \cdot E \cdot n_I \cdot m_I}{L_v^2}$$

Fig. 7. Root locus diagram: (a) $0.5 \times 10^{-5} \leq m_{P1} \leq 3 \times 10^{-5}$, **(b)** $0.5 \times 10^{-4} \leq m_{I1} \leq 3 \times 10^{-4}$

Based on (16) the stability of the closed-loop system can be evaluated. For instance, by using the parameters listed in Table 2 for DG1 and changing m_{P1} and m_{I1}, the values of the eigenvalues are as depicted in Figs. 7(a) and 7(b), respectively. As it can be observed in Fig. 7(a), three of the roots don't move with the change of m_{P1}, one moved to right and two others move to the left. It can be noticed that for low values of m_{P1} the control system is unstable. Here, the value of m_{P1} is fixed at 10^{-5} to provide proper stability. The respective roots are shown by larger markers. According to Fig. 7(b), three of the roots don't move with the change of m_{I1}, one moved to left and two others move to the right and can cause instability for high values of m_{I1}. Here, 10^{-4} is selected for m_{I1}. Similar analyses can be performed for the reactive power controller of DG1 and also for selecting respective parameters of DG2.

3.2. Voltage and current controllers

According to Fig. 2, the control block diagram of Fig. 8 can be considered for the design purpose. In this Fig., $d(s)$ and r_L are the duty cycle and filter inductor resistance, respectively. r_L is set to 0.05Ω. $G_{PWM}(s)$ represents *PWM* transfer function which is usually modeled as a delay element. In this paper, the delay of *PWM* is neglected (i.e. $G_{PWM}(s)=1$). $G(s)$ and $Z'_o(s)$ are as follows:

$$G(s) = \frac{G_V(s) \cdot G_I(s)}{LCs^2 + (r_L + G_I(s)) \cdot Cs + G_V(s) \cdot G_I(s) + 1} \qquad (17)$$

$$Z'_o(s) = \frac{r_L + Ls + G_I(s)}{LCs^2 + (r_L + G_I(s)) \cdot Cs + G_V(s) \cdot G_I(s) + 1} \qquad (18)$$

The Bode diagram of $G(s)$ considering the power stage and control system parameters (listed in Tables 1 and 2) is depicted in Fig. 9. As it can be seen, the gain and the phase angle of the closed-loop transfer function are respectively unity and zero at fundamental and 5th (250Hz), and 7th (350 Hz) harmonic frequencies. Thus, proper tracking of voltage reference is ensured.

Fig. 10 shows the magnitude plot of $Z'_o(s)$. It can be observed that the magnitude of $Z'_o(s)$ is approximately zero at fundamental and 5th and 7th harmonic frequencies. This fact again shows the control system effectiveness in tracking the voltage reference. Thus, the DG unit output impedance is fixed by the virtual impedance.
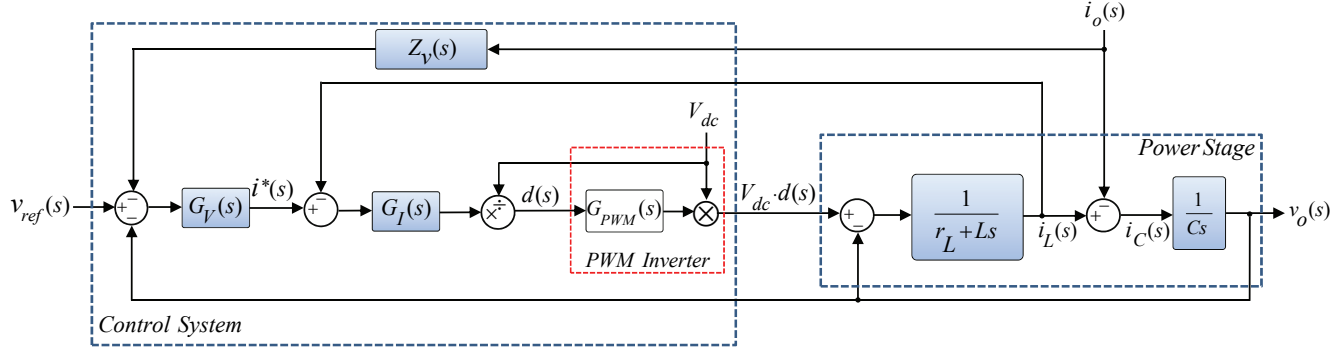
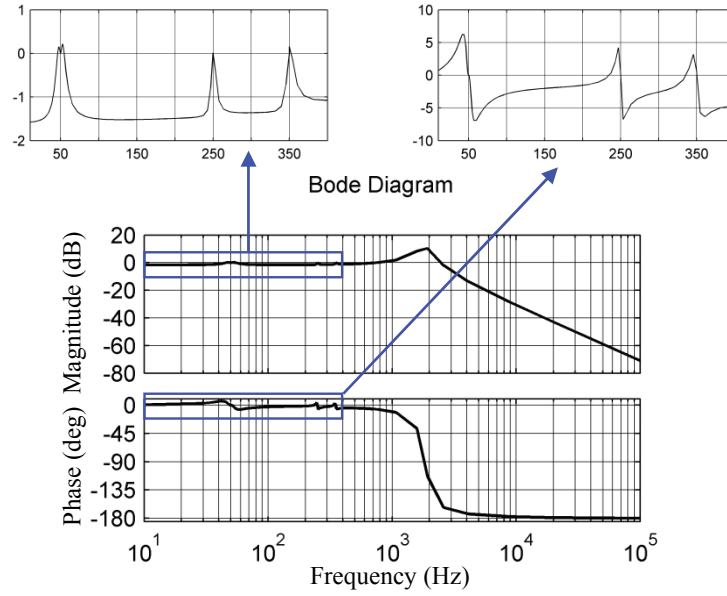**Fig. 8. Model of DG power stage and control system.**

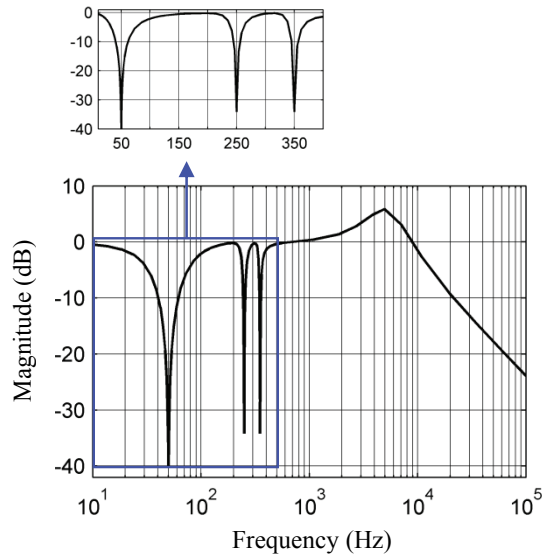**Fig. 9. Bode diagram of closed loop transfer function.**

Fig. 10. Magnitude plot of $Z'_O(s)$

3.3. Virtual impedance

As mentioned before, the fundamental virtual impedance parameters should be selected in a way that the electrical system is kept mainly inductive. Also, small virtual resistance is added to make the system oscillations more damped. In this paper, a two-DG microgrid is considered as the test system. The values listed in Table 2 are selected as the DGs fundamental virtual impedance. According to these values, the phase angles of DGs output impedance are set to about 81°. Furthermore, by adding DGs tie line impedances (listed in Table 1) to the output impedances, the total impedance between each DG and PCC can be calculated. According to this, the phase angles of the total impedances are about 76° and 79° for DG1 and DG2, respectively. Thus, the mainly inductive behavior is provided.

As demonstrated in Fig. 10, the magnitude of $Z'_O(s)$ is very low at harmonic frequencies. Hence, the values of distribution line impedances between DG units and load bus significantly affect the harmonic load sharing among DGs. Thus, the virtual resistance values at harmonic frequencies should be high enough to mitigate the effect of distribution lines effectively and a proper sharing of harmonic current can be provided. It should be noted that some amount of sharing error can be acceptable especially in the cases that the inverters are not operating at their power limit. In addition, note that the sharing improvement is achieved at the expense of distorting DG output voltage as a result of harmonic voltage drop on $R_{v,h}$. Thus, for selection of $R_{v,h}$ a trade-off should be considered between the amount of output voltage distortion and nonlinear load sharing accuracy. It is also noteworthy that the rating of DGs interface converters should be taken into account. Here, the values shown in Table 2 are selected as DGs $R_{v,h}$.

3.4. Harmonic compensator

CG_h should be selected according to the required amount of compensation. In fact, by increase of CG_h, the hth harmonic of PCC voltage is more compensated. In practical application, the value of CG_h can be controlled by an up-down counter according the required harmonic distortion at PCC as explained in [21]. However, as it will be shown later, PCC voltage compensation is achieved by the change of DGs output distortion and it is possible that the output voltage distortions of some DGs are increased. In some cases (e.g. connection of sensitive loads at DG terminal) the maximum distortion of DG output voltage should be kept below a pre-determined value and it can restrict the maximum value of CG_h. Also, it should be noted that using very high values for CG_h can make the control system unstable.

4. Simulation results

The electrical system of Fig. 11 which comprises a two-DG grid-connected microgrid and the utility grid is considered as the test system. DG1 is rated at double power comparing to DG2 ($S_{01}=2S_{02}$). The microgrid and utility grid are rated at 230V (phase rms voltage) and 50Hz. It is assumed that the grid voltage is distorted by 3% (of fundamental voltage) 5th and 7th voltage harmonics. Switching frequency of the DGs inverters is 10 kHz. A diode rectifier is considered as the nonlinear load; also, a star-connected linear load (Z_L) is connected to PCC.

As it can be seen in Table 1, $Z_{\ell 1}$ is considered double of $Z_{\ell 2}$ in order to simulate asymmetrical DG tie lines. In order to simulate a general case, resistive-inductive impedances are considered for the tie lines. The parameters of power controllers and virtual impedances are selected considering the different ratings of the DGs ($S_{01}=2S_{02}$) while the parameters of voltage and current controllers are the same for both DGs. DG1 and DG2 reference values of fundamental active powers are $P_1^* = 2000W$ and $P_2^* = 1000W$, respectively while the reference reactive powers are set to $Q_1^* = 500VAr$ and $Q_2^* = 250VAr$.
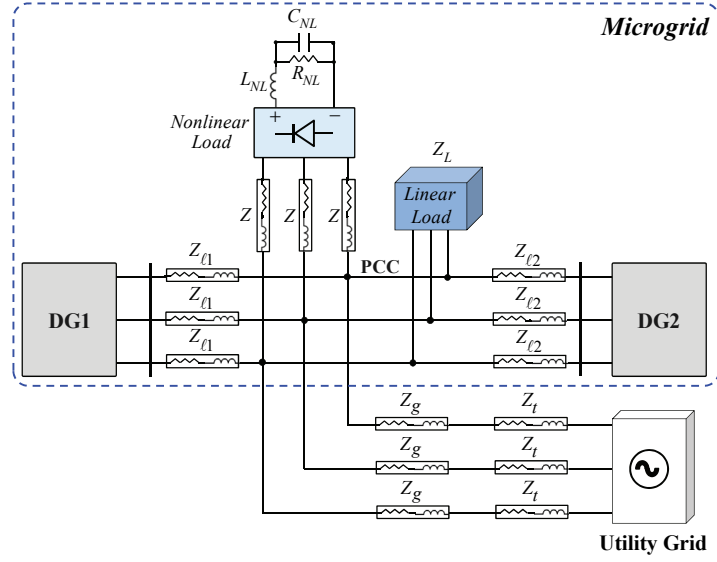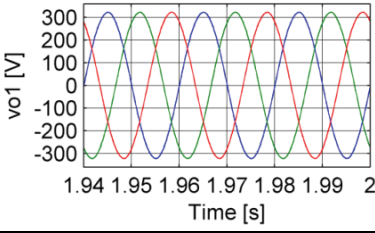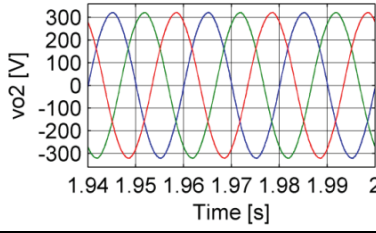
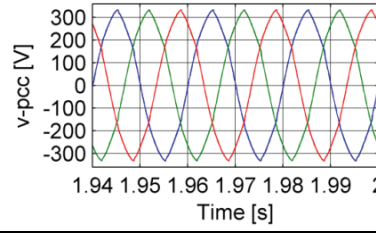**Fig. 11. Test system for simulation studies.**
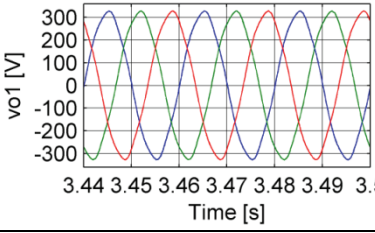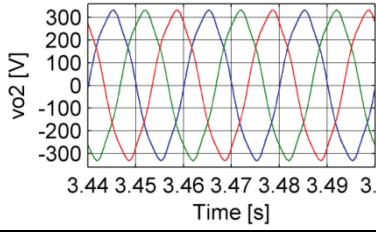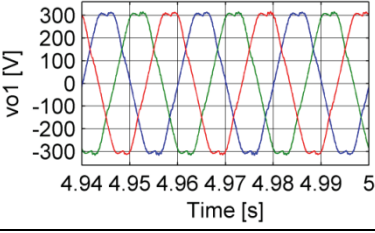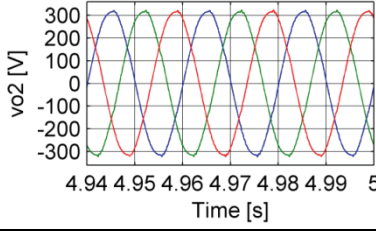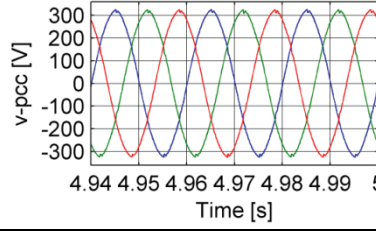
Table 1. Power stage parameters

dc link voltage	LC filter inductance	LC filter capacitance	nonlinear load tie line
V_{dc} (V)	L (mH)	C (μF)	Z (Ω)
650	1.8	25	0.15+j0.4712
DG$_1$/DG$_2$ tie line	nonlinear load	utility tie line	linear load
$Z_{\ell1}(\Omega)$ / $Z_{\ell2}(\Omega)$	$C_{NL}(\mu F)$ / $R_{NL}(\Omega)$ / $L_{NL}(mH)$	$Z_g + Z_t(\Omega)$	$Z_L(\Omega)$
0.3+j0.9424/0.15+j0.4712	235/100/0.084	1+j1.8848	50+j6.28

Table 2. Control system parameters

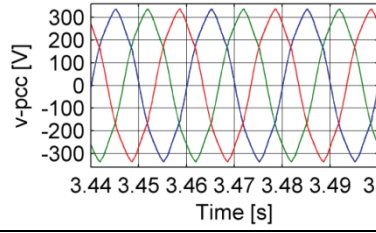| power controllers							
m_{P1} (rad/W)	m_{I1} (rad/W.s)	n_{P1} (V/VAr)	n_{I1} (V/VAr.s)	m_{P2} (rad/W)	m_{I2} (rad/W.s)	n_{P2} (V/VAr)	n_{I2} (V/VAr.s)
10^{-5}	10^{-4}	0.05	0.1	2×10^{-5}	2×10^{-4}	0.1	0.2
virtual impedance							
R_{v1} (Ω)	L_{v1} (mH)	R_{v2} (Ω)	L_{v2} (mH)	$R_{v,h1}$ (Ω)		$R_{v,h2}$ (Ω)	
0.1	2	0.2	4	4		8	
voltage controller							
k_{pV}	k_{rV_1}	k_{rV_5}	k_{rV_7}	ω_{cV1} (rad/s)	ω_{cV5} (rad/s)	ω_{cV7} (rad/s)	
1	100	100	175	1	1	1	
current controller							
k_{pI}	k_{rI_1}	k_{rI_5}	k_{rI_7}	ω_{cI1} (rad/s)	ω_{cI5} (rad/s)	ω_{cI7} (rad/s)	
5	1000	100	100	1	1	1	
selective harmonic compensator							
CG_5				CG_7			
-70				-25			

Table 3. Voltage waveforms at different simulation steps

	DG$_1$	DG$_2$	PCC
step1			
step2			
step3			

Simulations are performed in *MATLAB/Simulink* using *SimPowerSystems* toolbox. Three simulation steps are considered:

Step1 ($0 \leq t < 2s$): DGs operate with only fundamental virtual impedance and harmonic compensation is not acting.
Step2 ($2 \leq t < 3.5s$): Harmonic virtual resistances are added.
Step3 ($3.5 \leq t < 5s$): Harmonic compensation is activated.

4.1. Simulation step 1

As seen in Table 3, before activating the harmonic virtual resistance, DGs output voltages are approximately free of harmonic distortion. This fact can be seen in Fig. 12(a)-(c) as very low of total and 5th and 7th harmonic distortions (*THD*, *HD$_5$* and *HD$_7$*, respectively) of output voltages. It demonstrates the effectiveness of DGs controller in tracking the voltage reference. But, as shown in Table 3 and Fig. 12(a)-(c), PCC voltage is distorted noticeably due to harmonic voltage drop on the DG tie lines. The details of *THD* calculation can be found in [21]. *HD$_5$* and *HD$_7$* can be calculated similar to $HD_{I,h}$ calculation in Fig. 6.

As shown in Figs. 13(a) and (b), the reference of active and reactive powers are tracked, properly. But, it can be noticed from Fig. 13(c) that before addition of harmonic virtual resistance at *t*=2s, non-fundamental (harmonic) power (*S$_n$*) is shared in inverse proportion to the tie lines impedances and DG$_2$ supplied *S$_n$* is approximately double while it has half rated power.

S$_n$ is calculated according to the following equation [19]:

$$S_n = S_f \cdot \sqrt{(THD_I)^2 + (THD_V)^2} \qquad (19)$$

15

where S_f, THD_I and THD_V are the fundamental apparent power ($S_f = \sqrt{P^2 + Q^2}$) and total harmonic distortions of current and voltage, respectively.

DGs output current harmonic spectrums in Step 1 are depicted in Fig. 14(a). These spectrums are achieved by applying DG1 fundamental current as the common base for both DGs. It can be observed that fundamental components (first harmonic) of DGs current are shared in proportion to the DGs rating. This result is in compliance with those of Figs. 13(a) and (b). But, other current harmonics are not properly shared. Especially, it can be seen that DG2 5th and 7th current harmonics (main harmonic orders) are approximately double of the 5th and 7th harmonics of DG1. This fact has also been observed in Fig. 13(c) in terms of non-fundamental powers.
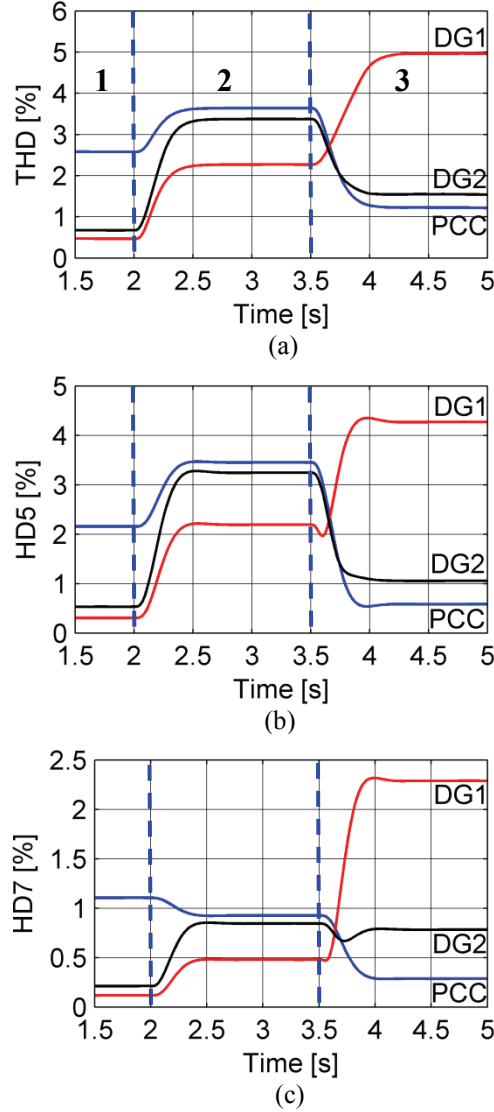

Fig. 12. Voltage harmonic distortions (fundamental component=100%)
(a) total harmonic distortion, (b) 5th harmonic distortion, (c) 7th harmonic distortion

16

4.2. Simulation step 2

Harmonic virtual resistances are added at t=2s. As mentioned before, virtual impedance is selectively inserted at 5th and 7th harmonics. As seen in Fig. 13(c), sharing of S_n is improved noticeably by the harmonic virtual resistances, however, still is not in proportion to the DGs rated powers. The improvement of main current harmonics (5th and 7th) sharing can also be noticed by comparing Figs. 14(a) and (b).

The sharing improvement is achieved at the expense of voltage distortion increase at DGs terminals as it can be observed in Table 3 and Figs. 12(a)-(c). Consequently, PCC voltage distortion increases as observed in Table 3 and Fig. 12.

According to Figs. 13(a) and (b) fundamental active and reactive powers are kept at the reference values. It shows the effectiveness of the power controllers.
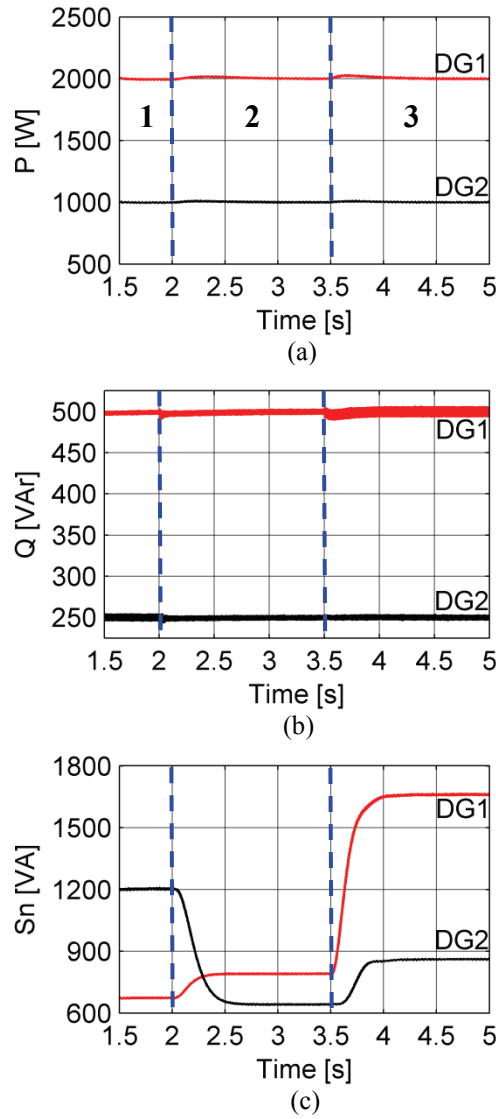

Fig. 13. (a) fundamental active power, (b) fundamental reactive power, (c) non-fundamental power

17

4.3. Simulation step 3

In the next simulation step, selective compensation of PCC voltage main harmonics is activated at t=3.5s. As seen in Figs. 12(b) and (c), HD_5 and HD_7 of PCC voltage are mitigated, effectively. It leads to significant reduction of PCC voltage THD according to Fig. 12(a). Improvement of PCC voltage quality can also be observed in Table 3.

Also, it can be observed in Table 3 and Figs. 12(a)-(c) that the harmonic compensation is achieved by the increase of DG_1 output voltage distortion. Note that DG_1 tie line impedance is relatively high; also, the nonlinear load supplied by this DG is higher than the amount supplied by DG_2. Thus, before compensation, the harmonic voltage drops over DG_1 tie line and its harmonic virtual resistance distort PCC voltage, noticeably. Hence, after compensation activation, the output voltage of this DG has become distorted in order to compensate these harmonic voltage drops and provide approximately sinusoidal voltage at PCC. On the other hand, due to low value of the tie line impedance and non-fundamental power of DG_2, harmonic distortion of PCC and DG_2 change with approximately similar behavior, as seen in Fig. 12 and Table 3.
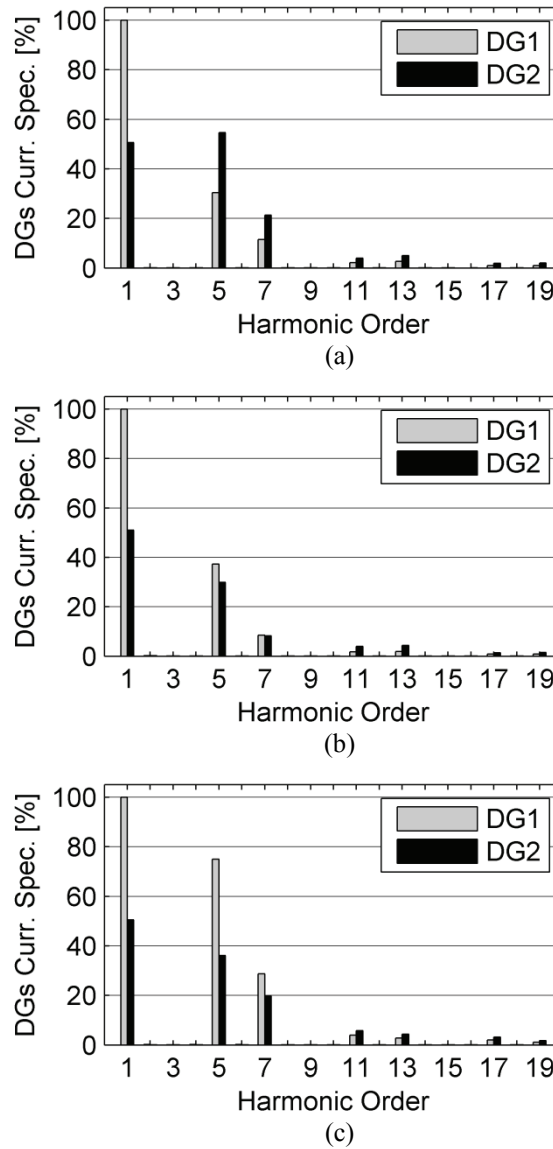

(a)

(b)

(c)

Fig. 14. DGs current spectrum (fundamental component of DG1, $I_{1,rms}$=100%)
(a) step 1 ($I_{1,rms}$=3.02A), (b) step 2 ($I_{1,rms}$=3.04A), (c) step 3 ($I_{1,rms}$=3.03A)

18

Moreover, as depicted in Fig 13(c), DGs non-fundamental powers increase as a result of harmonic compensation. It is mainly originated from the increase of main harmonic currents supplied by the DGs as shown in Fig. 14(c). As seen, DGs 5th and 7th current harmonics are increased significantly at simulation step 3 to provide compensation of respective voltage harmonics. Thus, as mentioned in subsection 2.5, compensation effort can be considered as the amount of current harmonic distortion ($HD_{I,h}$ in Fig. 6) increase. Due to double rated power of DG1, the compensation should be more supported by this DG. This fact can be observed in Figs. 13(c) and 14(c) as noticeably more increase of DG1 non-fundamental power and current distortion, respectively. It demonstrates the effectiveness of the proposed approach for sharing of compensation effort.

Furthermore, as shown in Fig. 13(c) sharing of non-fundamental powers is improved, significantly, after harmonic compensation and S_n is shared approximately in proportion of the DGs rating. The proper sharing is provided by harmonic virtual resistances as well as compensation effort sharing. In addition, fundamental powers references are tracked in this simulation step according to Figs. 13(a) and (b).

5. Conclusions

A new method has been proposed for selective compensation of PCC voltage main harmonics in a grid-connected microgrid. Harmonic compensation is achieved through proper control of DGs interface converters. The compensation effort of each harmonic is shared based on a novel approach which considers the respective harmonic distortion. Furthermore, a selective virtual resistance loop is included in the control system of each DG in order to improve non-fundamental power sharing. The control system design is discussed and simulation results are provided. The presented simulation results show that by application of the proposed method, PCC voltage quality is improved significantly. Also, DGs supplied fundamental and non-fundamental powers are in proportion to their rated powers.

References

[1] H. Akagi, Y. Kanagawa, A. Nabase, Instantaneous reactive power compensator comprising switching devices without energy storage components, IEEE Trans. Ind. Appl. IA-20 (3) (1984) 625-630.

[2] H. Akagi, Control strategy and site selection of a shunt active filter for damping of harmonic propagation in power distribution systems, IEEE Trans. Power Deliv. 12 (1) (1997) 354-363.

[3] E. Barklund, N. Pogaku, M. Prodanovic, C.H. Aramburo, T.C. Green, Energy management in autonomous microgrid using stability-constrained droop control of inverters, IEEE Trans. Power Electron. 23 (5) (2008) 2346-2352.

[4] F. Blaabjerg, Z. Chen, S.B. Kjaer, Power electronics as efficient interface in dispersed power generation systems, IEEE Trans. Power Electron. 19 (5) (2004) 1184-1194.

[5] F. Blaabjerg, R. Teodorescu, M. Liserre, A.V. Timbus, Overview of control and grid synchronization for distributed power generation systems, IEEE Trans. Ind. Electron. 53 (5) (2006) 1398-1409.

[6] U. Borup, F. Blaabjerg, P.N. Enjeti, Sharing of nonlinear load in parallel-connected three-phase converters, IEEE Trans. Ind. Appl. 37 (6) (2001) 1817–1823.

[7] S.J. Chiang, C.Y. Yen, K.T. Chang, A multimodule parallelable series-connected PWM voltage regulator, IEEE Trans. Ind. Electron. 48 (3) (2001) 506-516.

[8] S.J. Chiang, J.M. Chang, "Parallel control of the UPS inverters with frequency-dependent droop scheme, Power Electron. Specialist Conf. PESC (2001), 957–961.

[9] M. Cirrincione, M. Pucci, G. Vitale, A single-phase DG generation unit with shunt active power filter capability by adaptive neural filtering, IEEE Trans. Ind. Electron. 55 (5) (2008) 2093-2110.

[10] R.C. Dugan, M.F. McGranaghan, S. Santoso, H.W. Beaty, Electrical Power Systems Quality, second ed., McGraw-Hill, New York, 2003.

[11] D. De, V. Ramanarayanan, Decentralized parallel operation of inverters sharing unbalanced and nonlinear loads, IEEE Trans. Power Electron. 25 (12) (2010) 3015-3025.

[12] J.M. Guerrero, L.G. Vicuna, J. Matas, M. Castilla, J. Miret, Output impedance design of parallel connected UPS inverters with wireless load sharing control, IEEE Trans. Ind. Electron. 52 (4) (2005) 1126-1135.

[13] J.M. Guerrero, J. Matas, L.G. de Vicuña, M. Castilla, J. Miret, Wireless-control strategy for parallel operation of distributed-generation inverters, IEEE Trans. Ind. Electron. 53 (5) (2006) 1461-1470.

[14] J.M. Guerrero, J. Matas, L.G. de Vicuña, M. Castilla, J. Miret, Decentralized control for parallel operation of distributed generation inverters using resistive output impedance, IEEE Trans. Ind. Electron. 54 (2) (2007) 994-1004.

[15] J.M. Guerrero, J.C. Vasquez, J. Matas, L.G. de Vicuña, M. Castilla, Hierarchical control of droop-controlled AC and DC microgrids—a general approach toward standardization, IEEE Trans. Ind. Electron. 58 (1) (2011) 158-172.

[16] J. He, Y.W. Li, Analysis and design of interfacing inverter output virtual impedance in a low voltage microgrid, Energy Conv. Cong. and Exp. ECCE (2010), 2857–2864.

[17] J. He, Y.W. Li, M.S. Munir, A flexible harmonic control approach through voltage controlled DG-grid interfacing converters, IEEE Trans. Ind. Electron., Early Access (2011).

[18] IEEE Standard 519-1992, IEEE recommended practices and requirements for harmonic control in electrical power systems (1992).

[19] IEEE Standard 1459-2010, IEEE standard definitions for the measurement of electric power quantities under sinusoidal, nonsinusoidal, balanced, or unbalanced conditions (2010).

[20] IEEE Standard 1547.4-2011, IEEE guide for design, operation, and integration of distributed resource island systems with electric power systems (2011).

[21] P. Jintakosonwit, H. Akagi, H. Fujita, S. Ogasawara, Implementation and performance of automatic gain adjustment in a shunt active filter for harmonic damping throughout a power distribution system, IEEE Trans. Power Electron. 17 (3) (2002) 438-447.

[22] M. Karimi-Ghartemani, O. Boon-Teck, A. Bakhshai, Application of enhanced phase-locked loop system to the computation of synchrophasors, IEEE Trans. Power Deliv. 26 (1) (2011) 22-32.

[23] C. Lascu, L. Asiminoaei, I. Boldea, F. Blaabjerg, High performance current controller for selective harmonic compensation in active power filters, IEEE Trans. Power Electron. 22 (5) (2007) 1826-1835.

[24] T.L. Lee, P.T. Cheng, Design of a new cooperative harmonic filtering strategy for distributed generation interface converters in an islanding network, IEEE Trans. Power Electron. 22 (5) (2007) 1919-1927.

[25] T.L. Lee, J.C. Li, P.T. Cheng, Discrete frequency tuning active filter for power system harmonics, IEEE Trans. Power Electron. 24 (5) (2009) 1209-1217.

[26] Y. Li, D.M. Vilathgamuwa, P.C. Loh, Design, analysis, and real-time testing of a controller for multibus microgrid system, IEEE Trans. Power Electron. 19 (5) (2004) 1195-1204.

[27] M.I. Marei, E.F. El-Saadany, M.M.A. Salama, A novel control algorithm for the DG interface to mitigate power quality problem, IEEE Trans. Power Deliv. 19 (3) (2004) 1384-1392.

[28] P. Mattavelli, F.P. Marafão, Repetitive-based control for selective harmonic compensation in active power filters, IEEE Trans. Ind. Electron. 51 (5) (2004) 1018-1024.

[29] F.Z. Peng, G.W. Ott, D.J. Adams, Harmonic and reactive power compensation based on the generalized instantaneous reactive power theory for three-phase four-wire systems, IEEE Trans. Power Electron. 13 (6) (1998) 1174-1181.

[30] N. Pogaku, T.C. Green, Harmonic mitigation throughout a distribution system: a distributed-generator-based solution, IEE Proc.-Gener. Transm. Distrib. 153 (3) (2006) 350-358.

[31] M. Prodanovic, K.D. Brabandere, J.V. Keybus, T.C. Green, J. Driesen, Harmonic and reactive power compensation as ancillary services in inverter-based distributed generation, IET Gener. Transm. Distrib. 1 (3) (2007) 432-438.

[32] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, F. Blaabjerg, Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions, IEEE Trans. Ind. Electron. 58 (1) (2011) 127-138.

[33] M. Savaghebi, A. Jalilian, J.C. Vasquez, J.M. Guerrero, T.L. Lee, Voltage harmonic compensation of a microgrid operating in islanded and grid-connected modes, 19th Iranian Conf. of Elec. Eng. ICEE (2011), 1-6.

[34] T. Takeshita, N. Matsui, Current waveform control of PWM converter system for harmonic suppression on distribution system, IEEE Trans. Ind. Electron. 50 (6) (2003) 1134-1139.

[35] A.G. Tsikalakis, N.D. Hatziargyriou, Centralized control for optimizing microgrids operation, IEEE Trans. Energy Conv. 23 (1) (2008) 241-248.

[36] J.C. Vasquez, R.A. Mastromauro, J.M. Guerrero, M. Liserre, Voltage support provided by a droop-controlled multifunctional inverter, IEEE Trans. Ind. Electron. 56 (11) (2009) 4510-4519.

[37] J.C. Vasquez, J.M. Guerrero, M. Savaghebi, R. Teodorescu, Modeling, analysis, and design of stationary reference frame droop controlled parallel three-phase voltage source inverters, 8th Int. Conf. on Power Electron. ICPE (2011) 272-279.

[38] K. Wada, H. Fujita, H. Akagi, "Considerations of a shunt active filter based on voltage detection for installation on a long distribution feeder," IEEE Trans. Ind. Appl. 38 (4) (2002) 1123-1130.