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STABILITY AND CONTROL OF GRIDFORMING CONVERTERS WITH REGULATED DC-LINK DYNAMICS

BY
LIANG ZHAO

DISSERTATION SUBMITTED 2023

AALBORG UNIVERSITY
DENMARK

STABILITY AND CONTROL OF GRID-FORMING CONVERTERS WITH REGULATED DC-LINK DYNAMICS

by

Liang Zhao

AALBORG UNIVERSITY
DENMARK

Dissertation submitted November 2023

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CV

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His research interests include the modeling, stability analysis, and control of power electronics systems.

ENGLISH SUMMARY

Grid-forming (GFM) control has become an attractive solution for voltage-source converters (VSCs) used in power electronic-based power systems. The dc-link voltage regulation needs to be implemented with GFM-VSCs in scenarios that lack a stiff dc voltage source and necessitate the operation of both inverter and rectifier modes. However, their control dynamics and interactions may result in instability issues. To systematically address those challenges, this Ph.D. thesis focuses on the analytical modeling, dynamics analysis, and enhanced control strategies for GFM-VSCs with dc-link voltage regulation under various operating conditions.

The dynamics of dc-link voltage can be utilized to synchronize GFM-VSCs with ac networks, thereby leading to the dc-link voltage-synchronization control (DVSC). The small-signal synchronization stability of GFM-VSCs using various DVSC approaches is comparatively analyzed. When employing the single-loop DVSC approach, GFM-VSCs connected to dc-link constant-power sources and loads encounter low-frequency oscillations. To address this issue, the active power and the *q*-axis voltage are fed forward to the frequency deviation, which are configured in parallel with the DVSC to achieve synchronization with ac networks. The proposed control approach enhances the stability of GFM-VSCs under a wide range of grid strengths and at both inverter and rectifier modes.

The inner control loops are another critical concern of GFM-VSCs. An analytical approach is proposed to reveal the impact of inner control loops on the system damping. First, an impedance model is employed to characterize the behaviors of different inner-loop schemes. On this basis, the complex torque coefficient method is used to characterize the influence of inner-loop dynamics on the outer-loop dynamics and the associated instability issues within synchronous and sub-synchronous frequencies. Finally, the proposed approach is exemplified with virtual admittance and vector-current control as inner control loops.

In addition to the outer-loop and inner-loop control strategies, the external interactions of GFM-VSCs with ac grids and dc-link sources and loads are investigated using impedance-based analytical methods. The dc-link impedance reveals the interactions between GFM-VSCs and various loads connected through the dc link, including constant-power, constant-resistance, and constant-current loads. Furthermore, ac impedance-based analyses evaluate the impact of dc-link sources and loads on ac-side impedance characteristics and the resulting interactions with ac grids. It is revealed that the constant-power load poses the highest risk of instability in the rectifier mode, while the constant-current source presents the highest risk of instability in the inverter mode.

DANSK RESUME

Grid-forming (GFM) kontrol er blevet en attraktiv løsning for spændingskildeomformere (VSC'er), der anvendes i strømelektronikbaserede energisystemer. Reguleringen af dc-link spændingen skal implementeres med GFM-VSC'er i scenarier, der mangler en dc-spændingskilde med en fast spænding og nødvendiggør drift i både inverter- og rectifier-tilstande. Dog kan deres kontrolmekanik og interaktioner resultere i ustabilitetsproblemer. For at systematisk tackle disse udfordringer fokuserer denne Ph.D.-afhandling på analytisk modellering, dynamikanalyse og forbedrede kontrolstrategier for GFM-VSC'er med regulerede dc-link-dynamikker under forskellige driftsbetingelser.

DC-link spændingsdynamikken kan anvendes til at synkronisere GFM-VSC'er med ac-nettet, hvilket fører til dc-link spændingssynkroniseringskontrol (DVSC). Småsignal-synkroniseringsstabiliteten af GFM-VSC'er ved brug af forskellige DVSC-tilgange sammenlignes. Når enkeltløkke DVSC-tilgangen benyttes observeres der lavfrekvente svingninger ved GFM-VSC'er, der er tilsluttet dc-link konstanteffektkilder og belastninger. For at adressere denne udfordring foreslås en fleksibel synkroniseringskontrol, der omfatter parallelle konfigurationer af DVSC, aktiv effekt-frekvens feedforward og q-akse spændingsfrekvens feedforward-styringer. Den foreslåede kontroltilgang forbedrer stabilitetsrobustheden af GFM-VSC'er under et bredt spektrum af netstyrker og i både inverter- og rectifier-tilstande.

De indre kontrolsløjfer er en anden kritisk bekymring for GFM-VSC'er. Der foreslås en analytisk tilgang til at afsløre indvirkningen af indre kontrolsløjfer på dæmpningen. Først anvendes en impedansmodel til at karakterisere adfærden af forskellige indre kontrolsløjfer. Baseret på dette anvendes den komplekse momentkoefficientmetode til at karakterisere indflydelsen af indre kontrolsløjfers dynamik på de ydre kontrolsløjfers dynamik og de tilknyttede ustabilitetsproblemer inden for sub-synkrone og synkrone frekvenser. Endelig eksemplificeres den foreslåede tilgang med virtuel admitans og vektorstrømskontrol som indre kontrolsløjfer.

Udover de ydre kontrolsløjfer og indre kontrolsløjfer strategier, undersøges de eksterne interaktioner mellem GFM-VSC'er og ac-net samt dc-link kilder og belastninger ved brug af impedansbaserede analytiske metoder. DC-link impedansen afslører interaktionerne mellem GFM-VSC'er og forskellige dc-link belastninger, herunder konstant-modstand, -effekt og -strøm belastninger. Derudover benyttes ac-impedansbaserede analyser til at vurdere hvordan dc-link kilder og belastninger påvirker ac-sidens impedanskarakteristika og dertil de resulterede interaktioner. Det observeres, at konstant-effektbelastningen udgør den højeste risiko for ustabilitet i rectifier-tilstanden, mens konstant-strømkilden udgør den højeste risiko for ustabilitet i inverter-tilstanden.

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Liang Zhao

Aalborg University, September 2023

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AVC	ac-bus voltage magnitude control
BESS	battery energy storage system
CIL	constant-current load
CIS	constant-current source
CPL	constant-power load
CPS	constant-power source
CRL	constant-resistance load
DVSC	dc-link voltage-synchronization control
EMF	electromotive force
GFL	grid-following
GFM	grid-forming
HPF	high-pass filter
HVDC	high-voltage direct current
LFO	low-frequency oscillation
LHP	left-half plane
LPF	low-pass filter
PCC	point of common coupling
PFF	active power-frequency feedforward
RHP	right-half plane
PLL	phase-locked loop
PSC	power-synchronization control
RPC	reactive power control
SCR	short-circuit ratio
SG	synchronous generator
SISO	single-input single-output
SO	synchronous oscillation
SSO	sub-synchronous oscillation
STATCOM	static synchronous compensator
V_qFF	*q*-axis voltage-frequency feedforward
VSC	voltage-source converter

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CHAPTER 1. INTRODUCTION

1.1. BACKGROUND AND MOTIVATION

Recent years have witnessed a significant transformation in power grids, largely attributed to renewable energy resources such as photovoltaic and wind power plants [1]. In Denmark, the Energy Islands in the Baltic and North Seas are being built to facilitate the large-scale integration of multi-gigawatt offshore wind capacity into future energy systems [2], where high-voltage direct current (HVDC) transmission lines and static synchronous compensators (STATCOMs) play critical roles in enhancing the flexibility, efficiency, and stability of energy islands. Unlike traditional power grids that predominantly rely on synchronous generators (SGs), future power grids will be built on power electronic converters, thereby leading to power electronic-based power systems [1], [3], [4].

Voltage-source converters (VSCs) exhibit advantages in terms of full controllability and rapid response when compared to traditional SGs [3]. However, their wide-timescale dynamics introduce the instability issues. Interactions between VSCs and power grids may result in oscillations and resonances over a wide frequency range [4], which have become more common in modern power systems [5], [6]. Consequently, it is critical to investigate the interactions and enhanced control strategies of VSCs in power-electronic-based power systems [4].

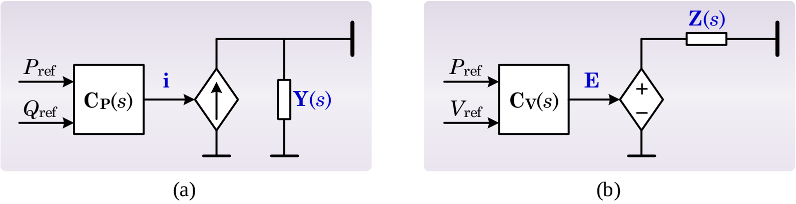


Figure 1.1. Representation of dynamics behaviors. (a) GFL-VSCs. (b) GFM-VSCs. Source: [8].

Grid-following (GFL) control techniques have been used with grid-connected VSCs for decades [3]. GFL-VSCs exhibit frequency-dependent current-source behavior in the sub-transient timeframe [7], which can be characterized via a current source with a paralleled output admittance [8], as depicted in Figure 1.1(a). Grid synchronization of GFL-VSCs is achieved by measuring the frequency and the phase angle of the voltage at the point of connection, typically employing a phase-locked loop (PLL) [4]. The current is injected into ac grids by following the measured frequency [9]-[11]. The stability of GFL-VSCs is crucially dependent on the voltage stiffness at the point of connection [9], which is, however, not always guaranteed in modern power grids. Instability issues thus arise from dynamic interactions between GFL-VSCs and weak grids [10], [11]. Furthermore, GFL-VSCs are usually incapable of performing certain functions such as islanding operation and black start [7].

In contrast, grid-forming (GFM) control has emerged as a promising solution for large-scale integration of converter-based resources into power systems [12]. The GFM-VSC behaves as an internal voltage source with an output impedance [8], as illustrated in Figure 1.1(b). Due to this voltage source behavior, GFM-VSCs can provide a series of stability services and functions to enhance the security and resiliency of power grids [13]. These functions include the active power responses to frequency and phase angle disturbances, the system strength support, and the ability to maintain stable operations even in the loss of the last SG [7], [14]. Thanks to the advantages, a growing consensus on the need for GFM-VSCs in the future renewable power grids is reached among power system operators worldwide [13], [14]. Numerous research and development efforts are recently reported, with a particular focus on functional specifications, grid-code requirements, hardware, and control solutions for GFM-VSCs [7], [13]-[16].

GFM-VSCs typically employ the power control for the purpose of synchronization [17]-[27]. A basic control strategy involves the active power-frequency droop control, a method originally employed for autonomous load sharing among paralleled inverters [17]. A similar approach, namely the power-synchronization control (PSC), is later proposed for interconnecting HVDC transmission lines into ultraweak ac grids, where the short-circuit ratio (SCR) is nearly one [18]-[20]. Both the PSC and the active power-frequency droop control manifest the first-order power control dynamics, providing the droop and damping characteristics while lacking the inertial response [9]. To incorporate the inertial response with GFM-VSCs, the second-order power control dynamics is employed [21]-[27]. The concept of inertial power control is initially developed for the battery energy storage system (BESS) [21]. Later, similar control techniques, known as the virtual synchronous machine [22], the virtual synchronous generator [23], and the synchronverter [24], are reported. The mathematical equivalence between the active power-frequency droop control embedded with a low-pass filter (LPF) and the virtual synchronous machine control is further proved in [25]. In addition to the LPF, the active power-frequency control can adopt the proportional-integral controller, the proportional-derivative controller, and the lead-lag controller [26], [27]. Notably, the lead-lag controller facilitates the flexible configuration of the droop characteristic, damping, and inertial response [27]. Nevertheless, a constant dc-link voltage is often employed for those power-based synchronization strategies, and it is assumed to be supported by the front-end devices [17]-[27].

However, a constant dc-link voltage source may not be readily accessible in certain operational scenarios, such as railway traction converters [28], hybrid ac/dc grids [29], and STATCOMs [30]. Besides, the GFM-VSCs are, in some cases, required to operate under both inverter and rectifier modes, thereby necessitating the dc-link voltage regulation. Therefore, this Ph.D. thesis is centered on the stability and control of the GFM-VSCs with dc-link voltage regulation, and a wide range of operating conditions on both ac- and dc-sides of GFM-VSCs are evaluated.

1.2. STATE OF THE ART AND CHALLENGES

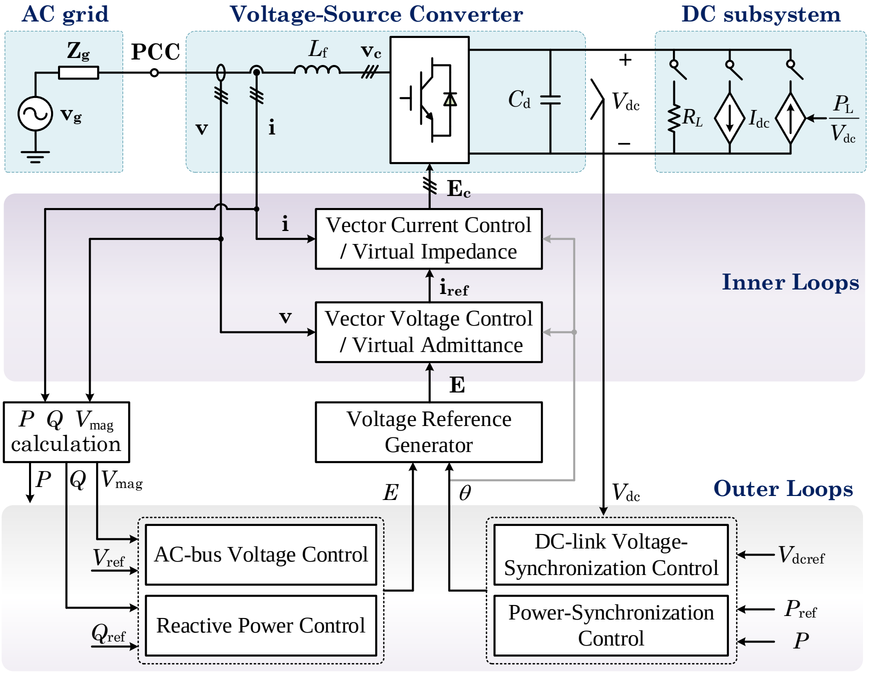

AC grid
Voltage-Source Converter
DC subsystem
$\mathbf{Z_g}$
PCC
L_f
$\mathbf{v_c}$
$\mathbf{v_g}$
v
i
C_d
+
V_{dc}
−
R_L
I_{dc}
P_L/V_{dc}
$\mathbf{E_c}$
i
Vector Current Control / Virtual Impedance
$\mathbf{i_{ref}}$
Inner Loops
v
Vector Voltage Control / Virtual Admittance
E
Voltage Reference Generator
P Q V_{mag} calculation
P
Q
V_{mag}
E
θ
V_{dc}
Outer Loops
V_{ref}
AC-bus Voltage Control
Q_{ref}
Reactive Power Control
DC-link Voltage-Synchronization Control
Power-Synchronization Control
V_{dcref}
P_{ref}
P

Figure 1.2. General block diagram of GFM-VSCs. Source: [8], [9], [J1].

Figure 1.2 presents a general block diagram of GFM-VSCs [8], [9], [J1]. The VSC interfaces with the ac grid at the point of common coupling (PCC) and connects to sources and loads through the dc bus [J1]. The control architecture comprises outer and inner control loops [8]. The outer control loops are responsible for generating the internal voltage reference and maintaining the desired GFM capability [13]. The inner control loops employ vector voltage and/or vector current control for shaping output impedance and preventing GFM-VSCs from overcurrent tripping [8].

This Ph.D. thesis investigates the stability and control of GFM-VSCs from three perspectives: (1) The dc-link voltage-synchronization control (DVSC), (2) The inner-loop dynamics and their damping effects, and (3) External interactions of GFM-VSCs with both ac grids and dc-link sources and loads.

1.2.1. DC-LINK VOLTAGE-SYNCHRONIZATION CONTROL

The dynamics of the dc-link voltage essentially reflect the active power balance of the dc-link capacitor [31]. Thus, the power-based synchronization mechanism can be extended with the dc-link voltage regulation, thereby leading to the DVSC [31]. Methods of DVSC have recently been documented in the literature [18], [20], [30]-[40]. They employ different control variables and structures. In terms of the control variables utilized in the DVSC, two variables are generally considered: the dc-link voltage in [30], [32]-[38], and the square of dc-link voltage in [18], [20], [31], [39], [40], the latter of which essentially denotes the energy of the dc-link capacitor [20].

In terms of control structures, the dynamic of dc-link voltage can be employed to generate the frequency of GFM-VSCs, thereby avoiding the use of PSC [32]. This single-loop DVSC method is reported as the voltage angle control in grid-connected wind turbines [32]. After that, similar control strategies are presented in [30], [31], [33]-[35], [39]. Despite having a simple control architecture, this method exhibits underdamped dc-link voltage control, which may lead to collapses of dc-link voltage when subject to large disturbances [39]. An alternative control structure comprises a cascaded configuration of DVSC and PSC [18], [20], [36], [40]. In this setup, the output of the DVSC represents the active power, serving as the reference for the PSC, while the PSC regulates the internal frequency [18]. However, the response speed of the DVSC is constrained by the PSC, and the interaction between the DVSC and PSC may result in unstable oscillations [36]. Further, to enhance the control flexibility, the PSC and the DVSC are configured in parallel for synchronization [37], recently named the dual-port GFM control [38]. Despite the variety of documented DVSC approaches, there is a lack of comparative evaluations on their synchronization stability performance under small disturbances.

The small-signal synchronization stability of GFM-VSCs using the cascaded and paralleled DVSC+PSC methods is reported in [36] and [37]. It is found that the DVSC may interact with the PSC, thereby giving rise to unstable oscillations under weak grids [36], [37]. The inertia and damping coefficients of PSC significantly impact the adverse interaction with the DVSC when employing the cascaded DVSC+PSC method [36], while such effects are alleviated with the paralleled DVSC+PSC method [37]. However, the dc link of GFM-VSCs in [36] and [37] is interconnected with resistance and constant current loads rather than a constant power load (CPL), which implies that more challenging operating scenarios are not considered. It is recognized that the CPL exhibits negative-resistance behavior and thus poses a significant risk to system stability [41], [42]. Therefore, the small-signal stability of GFM-VSCs and the enhanced DVSC strategies, considering various operation scenarios, need further exploration.

Therefore, the research gaps for the DVSC approaches can be summarized as follows:

- Different types of DVSC methods are documented, while the comparative analysis of small-signal synchronization stability among those methods has not been thoroughly investigated.
- Considering various operation conditions, exploring the DVSC strategies that can enhance the stability robustness remains an open issue.

1.2.2. INNER CONTROL LOOPS AND DYNAMICS EFFECTS

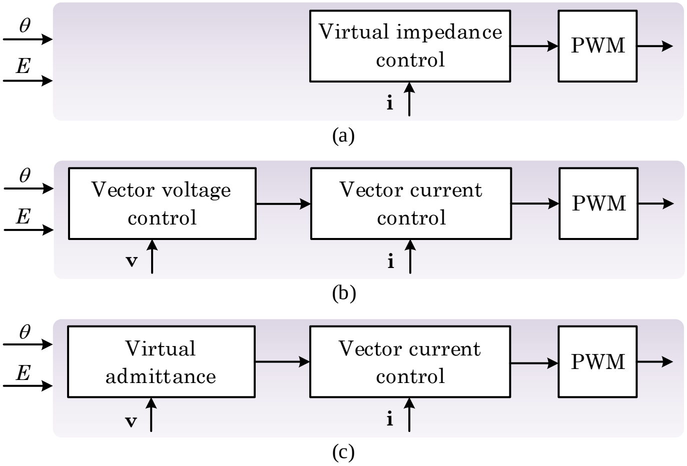


Figure 1.3. Typical inner-loop control schemes of GFM-VSCs. (a) Virtual impedance control. (b) Vector voltage and vector current control. (c) Virtual admittance and vector current control. Source: [J3].

The inner control loops are of critical concern for GFM-VSCs. Some GFM control schemes omit the inner control loops, directly using the reference of the internal voltage vector generated by outer control loops as the modulation voltage vector [18], [43], [44]. Despite its simple control architecture, the open-loop vector-voltage control is vulnerable to large disturbances [45], [46], and may even encounter instability challenges when interconnected with stiff ac grids [18]. As a result, it is critical to explore the impact of inner control loops on the system damping.

Figure 1.3 shows three typical inner-loop control schemes for GFM-VSCs, consisting of the voltage and/or the current control with various controller forms [8]. Figure 1.3(a) illustrates the virtual impedance control, a simple approach to shaping the output impedance of GFM-VSCs [18], [47]-[49]. The quasi-static virtual reactance and the virtual inductance can be implemented, while the emulation of virtual inductance requires derivative computations [48]. The dual-loop vector voltage and vector current control is an alternative strategy [8], [50], as shown in Figure 1.3(b). This approach is capable of reference tracking, harmonics rejection, and current limiting, but it may result in underdamping or even instability under stiff ac grids [50]. In contrast, using a grid-side current disturbance feedforward loop in this dual-loop control can improve the damping effect, yet at the cost of additional sensors [51]. Recently, an asymmetrical vector voltage controller is proposed to enhance the system damping for high stability robustness [52], [53]. In [52], a generalized vector voltage control is implemented through the use of an integral control loop connecting the *d*-axis voltage to the *q*-axis current reference. Nevertheless, the implementation of this method requires a sophisticated parameter design, and its effectiveness in enhancing damping remains limited under the weak grids [53]. Furthermore, the virtual admittance and vector current control represent an alternative form of inner control loops, as illustrated in Figure 1.3(c) [54]. This approach can shape the output inductance of GFM-VSCs without the need for derivative computations. However, the voltage decrement across the virtual admittance results in a reduction of the PCC voltage magnitude [55]. Consequently, the ac-bus voltage magnitude control (AVC) becomes necessary to keep the PCC voltage magnitude around one per unit (p.u.) [55]. Besides the above inner-loop configurations, a unified voltage control is proposed recently [56], where a universal control architecture is developed to synthesize different types of voltage control approaches and reveal their structural resemblance.

The inner control loops interact with outer loops, thereby affecting the dynamics of GFM-VSCs. While small-signal instability issues of GFM-VSCs arise in a wide frequency range, the outer-inner loop control interactions mainly affect two oscillation modes: sub-synchronous oscillation (SSO) and synchronous oscillation (SO) [9], [57]. The SO issue arises from the active power control plant of GFM-VSCs [18]. The closed-loop control system exhibits poles located at the fundamental frequency, arising from the inductive component of the power transfer impedance [9]. Mitigating the SO issue fundamentally involves enhancing the real or equivalent resistance component of the power transfer impedance [9]. This objective can be achieved through inner control loops, which, in turn, regulate the output impedance and thus affect the dynamics of SO mode. Specific inner-loop configurations for enhancing the resistive component encompass the virtual impedance control [18], the vector current control [57], and the virtual admittance control [57].

The SSO issue in GFM-VSCs is typically characterized by power oscillations occurring below the fundamental frequency [49], [50], [52], [57]-[59]. When employing the virtual impedance control, the inclusion of a high-pass filter (HPF) with the virtual resistance adversely affects the SSO-mode damping [49], while such instability issues can be mitigated by increasing the quasi-static virtual reactance. When inner loops are configured with vector voltage and vector current control, the SSO issue, arising from interactions between the PSC and vector voltage control, may occur under stiff grids [50]. Mitigating such adverse control interactions involves enhancing the bandwidth of vector voltage control and utilizing an asymmetrical vector voltage control [53], [58]. Furthermore, as for the virtual admittance and the vector current control, the influence of inner-loop parameters on the damping ratio of the SSO mode is examined in [57] and [59] using sensitivity analysis. Nevertheless, those analyses rely on numerical methods, thereby lacking analytical insights into the outer-inner loop control interactions and their stability implications. Studies in [58] analyze the stability effect of vector voltage and vector current control using the damping torque. However, a quantitative evaluation of their impacts on damping remains absent.

Therefore, the research gap for the inner control loops of GFM-VSCs is identified:

- There is a lack of analytical approaches to characterizing the impact of inner-loop control dynamics on outer-loop control dynamics and the associated oscillation modes.

1.2.3. EXTERNAL DYNAMICS INTERACTIONS

GFM-VSCs generally interact with external dc networks on the dc link and with external ac grids on the ac side. Those external interactions are critical to ensure the robust operation of GFM-VSCs under different system conditions.

A variety of sources can feed GFM-VSCs through the dc link, including the constant-power source (CPS) [60], [61], and the constant-current source (CIS) [62]. Further, different loads can also be connected to GFM-VSCs, including the CPL [41], [42], the constant-current load (CIL) [63], and the constant-resistance load (CRL) [64]. Table 1.1 shows those different sources and loads, along with their application scenarios [J4]. Despite various DVSC approaches being documented, those studies solely take a specific type of source or load into consideration.

Table 1.1. Different DC-Link Sources and Loads. Source: [J4]

Sources and loads	**Application scenario**
Constant-power source (CPS)	Wind turbines [60]; Photovoltaic arrays [61]
Constant-current source (CIS)	BESS [62]
Constant-power load (CPL)	Motor drives [41], [42]
Constant-current load (CIL)	BESS [63]
Constant-resistance load (CRL)	DC chopper [64]; Electric heater

The impedance-based analytical method serves as a promising approach to investigate the control interactions in converter-based systems [65]-[68]. The dc-link impedance can characterize the interactions of interconnected systems through the dc bus [65]. The dc-link CPL may lead to instability issues due to its negative-resistance behavior [41]. Conversely, the dc-link CRL exhibits a positive resistance. Nevertheless, the comparative analysis of interactions with those different dc-link connections remains unclear.

In addition to the interactions on the dc side, GFM-VSCs interact with ac grids through the PCC [66], [67]. The ac impedance matrix serves to characterize the behaviors of GFM-VSCs as well as the interactions on the ac side [68]. Prior research indicates that when VSCs integrate the dc-link voltage regulation during the rectifier operation, the *d-d* channel of ac input impedance demonstrates a low-frequency negative real part, resulting in the CPL behavior of VSCs on the ac side [10]. Such phenomena have been documented in both GFL-VSCs [10], [69], [70], and GFM-VSCs [36], [37]. Nonetheless, studies in [36] and [37] primarily center on the influence of dc-link voltage control approaches while overlooking the diversity of sources and loads. Consequently, the impedance characteristics of GFM-VSCs on the ac side, when connected to different dc-link sources and loads, along with their implications for stability, remain to be thoroughly investigated.

Therefore, two research gaps for the external interactions of GFM-VSCs are identified:

- On the dc side of GFM-VSCs, the influence of different dc-link sources and loads on system dynamics and the related stability risks are not fully revealed.
- On the ac side of GFM-VSCs, the influence of different dc-link sources and loads on ac-side impedance characteristics and the resulting grid-converter interactions have not yet been examined.

1.3. RESEARCH OBJECTIVES

In light of the identified research gaps, this Ph.D. thesis focuses on the analytical modeling, dynamic analysis, and enhanced control strategies for GFM-VSCs with regulated dc-link dynamics. The research objectives are defined as follows:

- **Analysis and enhancement of small-signal synchronization stability with DVSC approaches.** (Obj. 1)

  The small-signal stability of GFM-VSCs, using different DVSC approaches, will be comparatively analyzed. The potential risks of instability arising from the dc-link dynamics will be formulated. Moreover, enhanced synchronization control strategies are expected to improve stability robustness against various operation conditions.

- **Analytical approaches for exploring the damping effects of inner control loops.** (Obj. 2)

  Analytical approaches will be developed to evaluate the inner-loop dynamics and their effects on outer-loop dynamics. The approach is expected to be applicable to various controller configurations. Further, the interactions of outer and inner control loops will be analyzed under different ac grid conditions.

- **Dynamics analysis of external interactions with ac grids and dc-link sources and loads.** (Obj. 3)

  The interactions between GFM-VSCs and different types of dc-link connections will be evaluated. Moreover, the effects of dc-link sources and loads on the ac-side impedance characteristics and the resulting grid-converter interactions will be analyzed. The worst-case operational scenarios under rectifier and inverter modes will be identified.

1.4. RESEARCH METHODOLOGY

Table 1.2 lists the research methodology for the identified research objectives, including the scientific methods and tools.

Table 1.2. Research Methodology.

	Scientific methods	**Tools**
Obj. 1	• Transfer function modeling. • Closed-loop poles analysis.	• Simulations with MATLAB and PLECS. • Experimental tests.
Obj. 2	• Impedance model for inner control loops. • Complex torque coefficient method.	• Simulations with MATLAB and PLECS. • Frequency-scan technique for impedance measurement. • Experimental tests.
Obj. 3	• DC and ac impedance modeling. • Open-loop gains analysis. • Closed-loop poles analysis.	• Simulations with MATLAB and PLECS. • Frequency-scan technique for impedance measurement. • Experimental tests.

1.5. THESIS STRUCTURE

Figure 1.4 depicts the structure of this Ph.D. thesis. The main chapters are correlated with publications [J1]-[J4], and [C1]-[C3].

Chapter 1 is the introduction of the background, state-of-the-art, identification of research gaps, and research objectives.

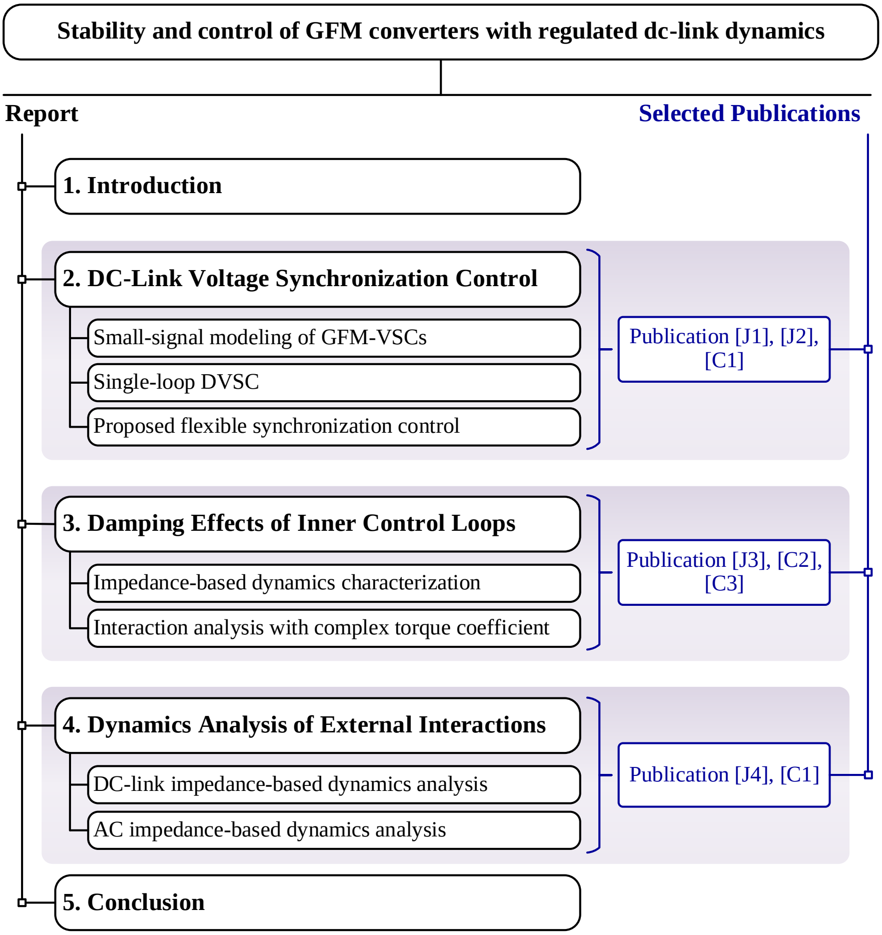

Stability and control of GFM converters with regulated dc-link dynamics
Report
Selected Publications
1. Introduction
2. DC-Link Voltage Synchronization Control
Small-signal modeling of GFM-VSCs
Single-loop DVSC
Proposed flexible synchronization control
Publication [J1], [J2], [C1]
3. Damping Effects of Inner Control Loops
Impedance-based dynamics characterization
Interaction analysis with complex torque coefficient
Publication [J3], [C2], [C3]
4. Dynamics Analysis of External Interactions
DC-link impedance-based dynamics analysis
AC impedance-based dynamics analysis
Publication [J4], [C1]
5. Conclusion

Figure 1.4. Thesis structure.

Chapter 2 analyzes the small-signal synchronization stability of GFM-VSCs with various DVSC approaches, based on [J1], [J2], and [C1]. A single-input single-output (SISO) model of the GFM-VSC is established first. Based on the model, it is analytically illustrated that the GFM-VSC using the single-loop DVSC method encounters the low-frequency oscillation (LFO) issue when connecting to a CPS or CPL through the dc link. A flexible synchronization control is subsequently proposed to mitigate the LFO issue. In this method, active power and q-axis voltage are utilized to synthesize the frequency of the ac output, which is configured with the DVSC in parallel. The GFM-VSC employing the proposed synchronization control demonstrates stability robustness across a range of grid strengths and at both inverter and rectifier modes.

Chapter 3 analyzes the effects of inner control loops on the dynamics of GFM-VSCs, based on [J3], [C2], and [C3]. Firstly, an impedance model is utilized to depict the inner-loop control dynamics. Subsequently, the complex torque coefficient method is used to characterize how inner-loop dynamics affect outer-loop dynamics and the related instability issues across synchronous and sub-synchronous frequencies. The method is applied to case studies involving virtual admittance and vector current control, followed by parameter tuning and experimental validations.

Chapter 4 analyzes the external interactions of GFM-VSCs with ac grids and dc-link sources and loads, based on [J4] and [C1]. The dc-link impedance reveals the interactions between GFM-VSCs and various loads. Furthermore, the ac impedance matrix illustrates the influence of dc-link connections and DVSC strategies on the ac impedance characteristics, as well as their interactions with ac grids. The dc-link sources and loads that lead to the highest risk of instability under inverter and rectifier modes are identified, respectively.

Chapter 5 finally presents the conclusions of this Ph.D. thesis, along with the future perspectives.

1.6. LIST OF PUBLICATIONS

This Ph.D. thesis is an extended summary of published journal and conference papers. They are listed as follows.

Journal Papers

[J1] **Liang Zhao**, Zheming Jin, and Xiongfei Wang, “Analysis and damping of low-frequency oscillation for dc-link voltage-synchronized VSCs,” *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8177-8189, July 2023.

[J2] **Liang Zhao**, Zheming Jin, and Xiongfei Wang, “Small-signal synchronization stability of grid-forming converters with regulated dc-link dynamics,” *IEEE Trans. Ind. Electron.*, vol. 70, no. 12, pp. 12399-12409, Dec. 2023.

[J3] **Liang Zhao**, Xiongfei Wang, and Zheming Jin, “Exploring damping effect of inner control loops for grid-forming VSCs,” *IEEE Trans. Power Electron.*, under review.

[J4] **Liang Zhao**, Xiongfei Wang, and Zheming Jin, “Impedance-based dynamics analysis for dc-link voltage-synchronized voltage-source converters,” *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 10829-10844, Sept. 2023.

Conference Papers

[C1] **Liang Zhao**, Xiongfei Wang, and Zheming Jin, “Flexible synchronization control for grid-forming converters with regulated dc-link dynamics,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1-8.

[C2] **Liang Zhao**, Xiongfei Wang, Hong Gong, and Zheming Jin, “Stability impact of hybrid synchronization strategy on virtual-admittance-based grid-forming inverters,” in *Proc. IEEE Appl. Power Electron. Conf. Expo*., Mar. 2023, pp. 2735-2740.

[C3] **Liang Zhao**, Xiongfei Wang, and Zheming Jin, “Impedance-based damping effect analysis for the inner loop of grid-forming VSCs,” in *Proc. 22nd Wind Sol. Integr. Workshop*, Sep. 2023, pp. 1–6.

CHAPTER 2. DC-LINK VOLTAGE-SYNCHRONIZATION CONTROL FOR GFM-VSCS

The content of this chapter is based on publications [J1], [J2], and [C1].

2.1. INTRODUCTION

GFM-VSCs typically employ the active power control to maintain synchronism with external ac systems [9]. This synchronization mechanism can be extended with dc-link voltage dynamics when GFM-VSCs incorporate the dc-link voltage regulation, thereby leading to the DVSC [J1].

Several DVSC approaches have been reported, encompassing the single-loop DVSC method [30]-[35], [39], the cascaded DVSC+PSC method [18], [20], [36], [40], and the paralleled DVSC+PSC method [37], [38]. Nevertheless, there is no comparative assessment of the small-signal synchronization stability among those different methods. Furthermore, the small-signal synchronization stability with cascaded and paralleled DVSC+PSC methods has been investigated in [36] and [37]. Yet, the GFM-VSCs in those studies are connected to current and resistance loads rather than the CPL or CPS on the dc bus. It is reported that the CPL exhibits negative-resistance behavior and thereby negatively affects the system stability [41], which thus denotes a more challenging operating scenario for GFM-VSCs. Consequently, it is crucial to investigate the stability robustness of those DVSC approaches under various operation scenarios.

To address the limitations, this Chapter comparatively analyses the small-signal stability of GFM-VSCs considering different DVSC methods and operation conditions [J1], [J2]. Using a SISO model from the dc-link voltage control reference to the output, it is revealed that GFM-VSCs employing the single-loop DVSC method encounter the LFO issue. A flexible synchronization control approach is subsequently proposed in [J1] and [J2] to tackle the LFO issue. This method configures the active power-frequency feedforward (PFF) and the *q*-axis voltage-frequency feedforward ($\mathrm{V_qFF}$) controls in parallel with the DVSC to synchronize the GFM-VSC with ac systems. The synchronization stability enhancement and dynamics analysis of GFM-VSCs using the proposed methods are corroborated through experimental results.

2.2. DESCRIPTION OF MAIN CIRCUIT AND CONTROL SYSTEM

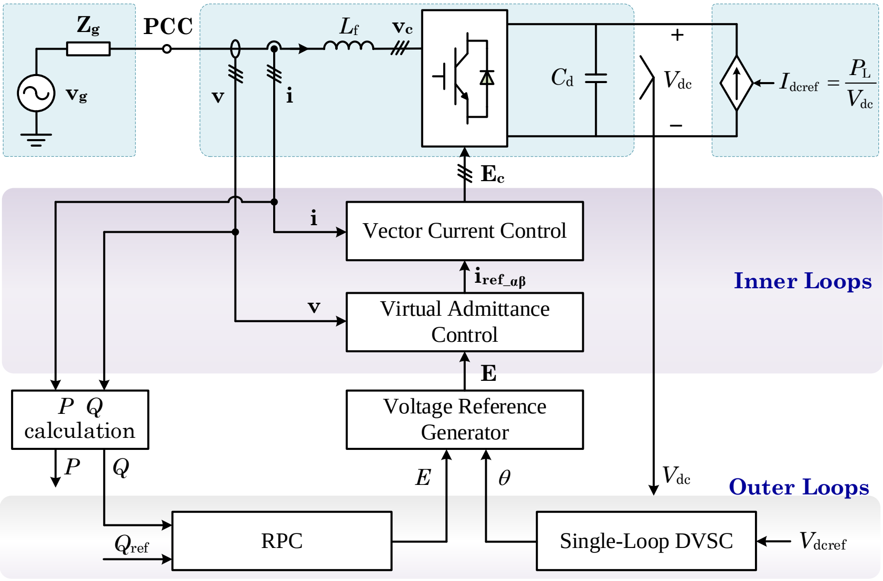

Zg
PCC
vg
v
i
Lf
vc
Cd
+
Vdc
−
Idcref = PL/Vdc
Ec
i
Vector Current Control
iref_αβ
Inner Loops
v
Virtual Admittance Control
E
P Q calculation
Voltage Reference Generator
P
Q
E
θ
Vdc
Outer Loops
Qref
RPC
Single-Loop DVSC
Vdcref

Figure 2.1. Main circuit and control diagrams of the studied GFM-VSC. Source: [J1], [J2].

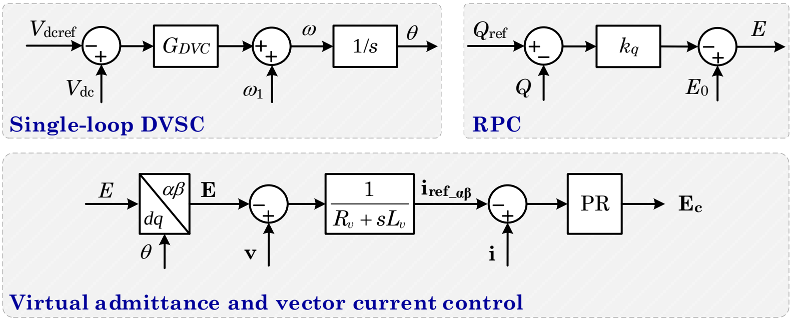

Vdcref
−
+
Vdc
GDVC
+
+
ω1
ω
1/s
θ
Single-loop DVSC
Qref
+
−
Q
kq
−
+
E0
E
RPC
E
αβ
dq
θ
E
−
+
v
1/(Rv + sLv)
iref_αβ
−
+
i
PR
Ec
Virtual admittance and vector current control

Figure 2.2. Detailed GFM control diagrams. Source: [J1].

In this Ph.D. thesis, complex space vectors are indicated by bold letters, while real space vectors and scalar variables are represented by italic letters. For example, the complex space and real space representations of current and voltage are denoted as $\mathbf{i} = i_\alpha + j i_\beta \quad \leftrightarrow \quad i = [i_\alpha, \quad i_\beta]^T$ and $\mathbf{v} = v_\alpha + j v_\beta \quad \leftrightarrow \quad v = [v_\alpha, \quad v_\beta]^T$.

Figure 2.1 shows the diagrams of the studied GFM-VSC [J1], [J2]. The ac grid is emulated by Thevenin's equivalent circuit [71], comprising a voltage source $\mathbf{v_g} = v_g \cdot e^{j\theta_g}$ behind a grid impedance $\mathbf{Z_g}$. v_g refers to the magnitude of grid voltage, while θ_g represents the phase angle. The GFM-VSC adopts an inductor filter at the ac output, denoted as L_f. The variable $\mathbf{i}$ denotes the grid current, and $\mathbf{v}$ stands for the PCC voltage. P refers to the active power at the PCC, whereas Q represents the reactive power. On the dc side, the GFM-VSC is connected to a CPS during its inverter mode operation and to a CPL when it operates in the rectifier mode [41], [42]. Their dynamics are represented by

$$I_\mathrm{dcref}(t) = \frac{P_\mathrm{L}}{V_\mathrm{dc}(t)} \tag{2.1}$$

where I_dcref represents the reference of the controlled current source, P_L represents the CPS or CPL, and V_dc represents the dc-link voltage.

Figure 2.2 shows the detailed diagrams of the studied GFM control [J1], [J2], including the outer and inner control loops. The outer control loops synthesize the internal electromotive force (EMF), denoted as $\mathbf{E} = E \cdot e^{j\theta}$. The phase angle θ is produced using the single-loop DVSC method, with G_{DVC} representing the dc-link voltage controller. The magnitude of the internal EMF, denoted as E, is regulated by the reactive power control (RPC) loop, employing a Q-E droop control. Moreover, the inner control loops employ the virtual admittance and vector current control implemented in the $\alpha\beta$-frame [54]. The parameters of the studied GFM-VSC and their values are detailed in Table 2.1.

Table 2.1. Circuit and Control Parameters of the Studied GFM-VSC. Source: [J1], [J2].

Symbol	Description	Value (p.u.)
P_0	Rated active power	2kW (1 p.u.)
v_g	RMS value of grid voltage	110V/50Hz (1 p.u.)
ω_1	Nominal angular frequency	100π rad/s (1 p.u.)
V_dcref	Reference of dc-link voltage	400V (3.64 p.u.)
L_f	Filter inductor	3 mH (0.052 p.u.)
C_d	DC-link capacitor	1.45mF
E_0	Rated magnitude of EMF	1 p.u.
Q_ref	Reference of reactive power	0
k_q	Droop coefficient of RPC	0.1 p.u.
R_v	Virtual resistance	0.1 p.u.
L_v	Virtual inductance	0.15 p.u.
k_{pi}	Proportional gain of vector current control	1 p.u.
k_{ri}	Resonant gain of vector current control	0.5 p.u.
T_d	Control time delay	150 μs

2.3. SMALL-SIGNAL MODELING OF GFM-VSCS

2.3.1. MODELING OF CIRCUIT

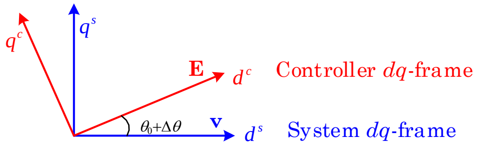


Figure 2.3. Controller and system *dq*-frames. Source: [J1].

Figure 2.3 depicts the controller and system *dq*-frames, which arise from the synchronization control dynamics [11]. The system *dq*-frame is established based on the PCC voltage, with the *d*-axis aligning with the PCC voltage vector, while the controller *dq*-frame is determined by the internal EMF vector. Variables in controller and system *dq*-frames are denoted by appended superscripts "*c*" and "*s*", respectively. Furthermore, steady-state operating points and small perturbations of variables are denoted by appended subscript "$_0$" and symbol "^", respectively. For example, $V_{\mathrm{dc}0}$ and $\hat{V}_{\mathrm{dc}}$ indicate the operating point and the small perturbation of the dc-link voltage, respectively.

The *dq*-frame real-space representations of grid voltage $\mathbf{v_g}$, PCC voltage $\mathbf{v}$, grid current $\mathbf{i}$, and VSC's terminal voltage $\mathbf{v_c}$ are expressed as

$$\begin{aligned} v_{gdq}^s &= \left[v_{gd}^s,\quad v_{gq}^s\right]^T, \quad v_{dq}^s = \left[v_d^s,\quad v_q^s\right]^T, \\ i_{dq}^s &= \left[i_d^s,\quad i_q^s\right]^T, \quad v_{cdq}^s = \left[v_{cd}^s,\quad v_{cq}^s\right]^T. \end{aligned} \tag{2.2}$$

The grid impedance is given by

$$Z_g = \begin{bmatrix} sL_g & -\omega_1 L_g \\ \omega_1 L_g & sL_g \end{bmatrix}. \tag{2.3}$$

The ac circuit dynamics, under small perturbations, are given by

$$\begin{aligned} v_{gdq}^s - \left(v_{dq0}^s + \hat{v}_{dq}^s\right) &= Z_g \cdot \left(i_{dq0}^s + \hat{i}_{dq}^s\right) \\ \hat{v}_{dq}^s &= -Z_g \cdot \hat{i}_{dq}^s \end{aligned} . \tag{2.4}$$

The impedance model of the inductor filter is given by

$$Z_p = Y_p^{-1} = \begin{bmatrix} sL_{\mathrm{f}} & -\omega_1 L_{\mathrm{f}} \\ \omega_1 L_{\mathrm{f}} & sL_{\mathrm{f}} \end{bmatrix} . \tag{2.5}$$

The calculation of active power at the PCC follows the instantaneous power theory [72], given by

$$P = v_d^s \cdot i_d^s + v_q^s \cdot i_q^s , \tag{2.6}$$

$$\hat{P} = \underbrace{\begin{bmatrix} i_{d0}^s & i_{q0}^s \end{bmatrix}}_{G_P^u} \cdot \hat{v}_{dq}^s + \underbrace{\begin{bmatrix} v_{d0}^s & v_{q0}^s \end{bmatrix}}_{G_P^i} \cdot \hat{i}_{dq}^s \quad \Rightarrow \quad \hat{P} = \left(-G_P^u \cdot Z_g + G_P^i\right) \cdot \hat{i}_{dq}^s . \tag{2.7}$$

Similarly, the reactive power at the PCC is derived as

$$Q = v_q^s \cdot i_d^s - v_d^s \cdot i_q^s , \tag{2.8}$$

$$\hat{Q} = \underbrace{\begin{bmatrix} -i_{q0}^s & i_{d0}^s \end{bmatrix}}_{G_Q^u} \cdot \hat{v}_{dq}^s + \underbrace{\begin{bmatrix} v_{q0}^s & -v_{d0}^s \end{bmatrix}}_{G_Q^i} \cdot \hat{i}_{dq}^s \quad \Rightarrow \quad \hat{Q} = \underbrace{\left(-G_Q^u \cdot Z_g + G_Q^i\right)}_{G_Q} \cdot \hat{i}_{dq}^s . \tag{2.9}$$

The VSC’s terminal voltage behind the inductance filter is expressed as

$$v_{cdq}^s = v_{dq}^s - Z_p \cdot i_{dq}^s . \tag{2.10}$$

Under the assumption that power losses in power semiconductors and filter inductors are neglected, the active power exchanged between ac and dc sides is expressed as

$$P_{\mathrm{dc}} = v_{cd}^s \cdot i_d^s + v_{cq}^s \cdot i_q^s , \tag{2.11}$$

$$\begin{aligned} \hat{P}_{dc} &= \underbrace{\begin{bmatrix} i_{d0}^s & i_{q0}^s \end{bmatrix}}_{G_{Pdc}^u} \cdot \hat{v}_{dq}^s + \underbrace{\begin{bmatrix} v_{d0}^s - sL_{\mathrm{f}} i_{d0}^s & v_{q0}^s - sL_{\mathrm{f}} i_{q0}^s \end{bmatrix}}_{G_{Pdc}^i} \cdot \hat{i}_{dq}^s \\ &= \left(G_{P_{dc}}^i - G_{P_{dc}}^u \cdot Z_g\right) \cdot \hat{i}_{dq}^s \end{aligned} \tag{2.12}$$

The active power balance of the dc-link capacitor, under small disturbances, is represented as

$$\left(P_{\mathrm{dc}} + \hat{P}_{\mathrm{dc}}\right) - P_{\mathrm{L}} = C_{\mathrm{d}} \left(V_{\mathrm{dc}0} + \hat{V}_{\mathrm{dc}}\right) \cdot \frac{d\left(V_{\mathrm{dc}0} + \hat{V}_{\mathrm{dc}}\right)}{dt} . \tag{2.13}$$

Note that P_{L} exhibits no small perturbations, owing to its constant-power behavior. The relationship between $\hat{P}_{\mathrm{dc}}$ and $\hat{V}_{\mathrm{dc}}$ is thus expressed as

$$\hat{V}_{\mathrm{dc}} = \frac{1}{sC_{\mathrm{d}} V_{\mathrm{dc}0}} \cdot \hat{P}_{\mathrm{dc}} . \tag{2.14}$$

2.3.2. MODELING OF CONTROL SYSTEM

The control law and the small-signal dynamic of the single-loop DVSC, as shown in Figure 2.2, are expressed as

$$\omega = G_{DVC} \cdot \left(V_{\mathrm{dc}} - V_{\mathrm{dcref}}\right) + \omega_1, \quad \theta = \frac{\omega}{s}, \tag{2.15}$$

$$\hat{\theta} = \frac{1}{s} \cdot G_{DVC} \cdot \left(\hat{V}_{\mathrm{dc}} - \hat{V}_{\mathrm{dcref}}\right). \tag{2.16}$$

The control law and the small-signal dynamic of the RPC, as shown in Figure 2.2, are expressed as

$$E = -k_q \cdot \left(Q_{\mathrm{ref}} - Q\right) + E_0, \tag{2.17}$$

$$\hat{E}^c_{dq} = I_{21} \cdot k_q \cdot \hat{Q}, \quad I_{21} = \begin{bmatrix} 1 & 0 \end{bmatrix}^T. \tag{2.18}$$

The dynamic of the voltage reference generator is denoted by the transformation from controller to system *dq*-frames. It is derived based on Figure 2.3 and is given by

$$\hat{E}^s_{dq} = \underbrace{\begin{bmatrix} \cos\theta_0 & -\sin\theta_0 \\ \sin\theta_0 & \cos\theta_0 \end{bmatrix}}_{T^{-1}} \cdot \hat{E}^c_{dq} + \underbrace{\begin{bmatrix} \cos\theta_0 & -\sin\theta_0 \\ \sin\theta_0 & \cos\theta_0 \end{bmatrix} \cdot \begin{bmatrix} -E^c_{q0} \\ E^c_{d0} \end{bmatrix}}_{G_E^{\theta}} \hat{\theta}, \tag{2.19}$$

$$T^{-1} = \begin{bmatrix} \cos\theta_0 & -\sin\theta_0 \\ \sin\theta_0 & \cos\theta_0 \end{bmatrix} \tag{2.20}$$

For the virtual admittance and vector current control depicted in Figure 2.2, their control laws are expressed as

$$\mathbf{i}_{\mathbf{ref\_\alpha\beta}} = Y_{v\_\alpha\beta}\left(s\right) \cdot \left(\mathbf{v} - \mathbf{E}\right), \quad Y_{v\_\alpha\beta}\left(s\right) = \frac{1}{sL_v + R_v}. \tag{2.21}$$

$$\mathbf{E_c} = G_{PR}\left(s\right) \cdot \left(\mathbf{i} - \mathbf{i}_{\mathbf{ref\_\alpha\beta}}\right), \quad G_{PR}\left(s\right) = k_{pi} + \frac{k_{ri}\, s}{s^2 + \omega_1^2}. \tag{2.22}$$

$Y_{v\_\alpha\beta}$ denotes the virtual admittance. G_{PR} denotes the vector current controller. Using *dq*-frame voltage and current, the control laws are expressed as

$$\begin{cases} e^{j\theta^s} \mathbf{i}^{\mathbf{s}}_{\mathbf{dqref}} = Y_{v\_\alpha\beta}\left(s\right) \cdot \left(e^{j\theta^s} \mathbf{v}^{\mathbf{s}}_{\mathbf{dq}} - e^{j\theta^s} \mathbf{E}^{\mathbf{s}}_{\mathbf{dq}}\right) \\ e^{j\theta^s} \mathbf{E}^{\mathbf{s}}_{\mathbf{cdq}} = G_{PR}\left(s\right) \cdot \left(e^{j\theta^s} \mathbf{i}^{\mathbf{s}}_{\mathbf{dq}} - e^{j\theta^s} \mathbf{i}^{\mathbf{s}}_{\mathbf{dqref}}\right) \end{cases}, \tag{2.23}$$

where the operator $e^{j\theta^s}$ is utilized for the *αβ*-*dq* frame transformation. The *dq*-frame models can be obtained using the frequency translation [73], given by

$$\begin{cases} \mathbf{i}^{\mathbf{s}}_{\mathbf{dqref}} = \underbrace{e^{-j\theta^s} Y_{v\_\alpha\beta}(s) e^{j\theta^s}}_{\mathbf{Y_{v\_dq}}(s)} \cdot \left(\mathbf{v}^{\mathbf{s}}_{\mathbf{dq}} - \mathbf{E}^{\mathbf{s}}_{\mathbf{dq}}\right) \\ \mathbf{E}^{\mathbf{s}}_{\mathbf{cdq}} = \underbrace{e^{-j\theta^s} G_{PR}(s) e^{j\theta^s}}_{\mathbf{G_i}(s)} \cdot \left(\mathbf{i}^{\mathbf{s}}_{\mathbf{dq}} - \mathbf{i}^{\mathbf{s}}_{\mathbf{dqref}}\right) \end{cases} \tag{2.24}$$

$$\begin{cases} \mathbf{Y_{v\_dq}}(s) = Y_{v\_\alpha\beta}(s + j\omega_1) \\ \mathbf{G_i}(s) = G_{PR}(s + j\omega_1) \end{cases}. \tag{2.25}$$

The matrix of virtual admittance and vector current controller are expressed as

$$\begin{cases} Y_{v\_dq}(s) = \dfrac{1}{(sL_v + R_v)^2 + (\omega_1 L_v)^2} \cdot \begin{bmatrix} sL_v + R_v & \omega_1 L_v \\ -\omega_1 L_v & sL_v + R_v \end{bmatrix} \\ G_i(s) = \left(K_p + \dfrac{K_r}{2s}\right) \cdot \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + \dfrac{K_r}{2\left(s^2 + 4\omega_1^2\right)} \cdot \begin{bmatrix} s & 2\omega_1 \\ -2\omega_1 & s \end{bmatrix} \end{cases}. \tag{2.26}$$

The control time delay is expressed as

$$G_d = \begin{bmatrix} e^{-sT_d} & 0 \\ 0 & e^{-sT_d} \end{bmatrix}. \tag{2.27}$$

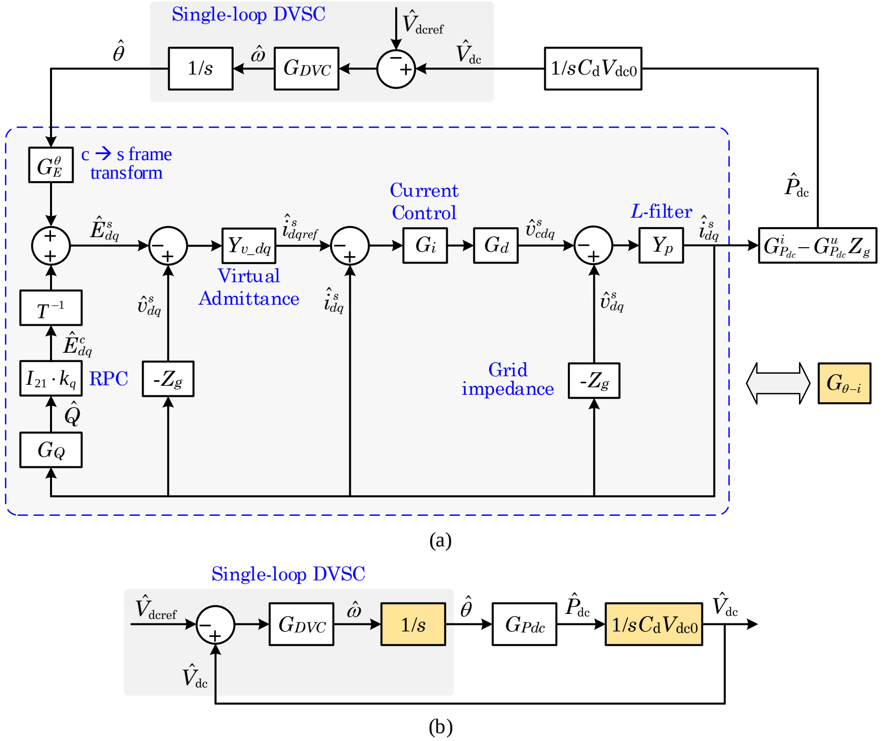
2.3.3. SISO TRANSFER FUNCTION MODEL

Figure 2.4(a) depicts the small-signal model of the studied GFM-VSC. Block diagrams indicated with blue dotted lines are described by a transfer function model from phase angle $\hat{\theta}$ to current $\hat{i}^s_{dq}$, as described in

$$G_{\theta-i} = \frac{\hat{i}^s_{dq}}{\hat{\theta}} = -\begin{bmatrix} Z_g + Z_p + G_d G_i + G_d G_i Y_{v\_dq} Z_g \\ +G_d G_i Y_{v\_dq} T^{-1} I_{21} k_q \left(G^i_Q - G^u_Q Z_g\right) \end{bmatrix}^{-1} G_d G_i Y_{v\_dq} G^{\theta}_E . \tag{2.28}$$

Figure 2.4(b) shows the SISO small-signal model from the dc-link voltage control reference to the output. The transfer function model from phase angle $\hat{\theta}$ to dc-link active power $\hat{P}_{dc}$, recalling (2.12) and (2.28), is expressed as

$$G_{Pdc} = \frac{\hat{P}_{dc}}{\hat{\theta}} = \left(G^i_{P_{dc}} - G^u_{P_{dc}} Z_g\right) \cdot G_{\theta-i} . \tag{2.29}$$


Single-loop DVSC
$\hat{V}_{\mathrm{dcref}}$
$\hat{\theta}$
1/s
$\hat{\omega}$
G_{DVC}
$\hat{V}_{\mathrm{dc}}$
$1/sC_{\mathrm{d}}V_{\mathrm{dc0}}$
G_E^θ
c → s frame transform
$\hat{P}_{\mathrm{dc}}$
Current Control
L-filter
$\hat{E}_{dq}^s$
Y_{v_dq}
$\hat{i}_{dqref}^s$
G_i
G_d
$\hat{v}_{cdq}^s$
Y_p
$\hat{i}_{dq}^s$
$G_{P_{dc}}^i - G_{P_{dc}}^u Z_g$
T^{-1}
$\hat{v}_{dq}^s$
Virtual Admittance
$\hat{i}_{dq}^s$
$\hat{v}_{dq}^s$
$\hat{E}_{dq}^c$
$I_{21} \cdot k_q$
RPC
-Z_g
Grid impedance
-Z_g
$G_{\theta-i}$
$\hat{Q}$
G_Q
Single-loop DVSC
$\hat{V}_{\mathrm{dcref}}$
G_{DVC}
$\hat{\omega}$
1/s
$\hat{\theta}$
G_{Pdc}
$\hat{P}_{\mathrm{dc}}$
$1/sC_{\mathrm{d}}V_{\mathrm{dc0}}$
$\hat{V}_{\mathrm{dc}}$
$\hat{V}_{\mathrm{dc}}$

(a)

(b)

Figure 2.4. Small-signal model of the studied GFM-VSC. (a) Original block diagram. (2) SISO block diagram. Source: [J1].

The open-loop and closed-loop transfer function models, from $\hat{V}_{\mathrm{dcref}}$ to $\hat{V}_{\mathrm{dc}}$, are expressed as

$$T_{DVSC} = -\frac{1}{s\,C_{\mathrm{d}}\,V_{\mathrm{dc}\,0}} \cdot G_{P_{dc}} \cdot \frac{G_{DVC}}{s}, \qquad T_{closed} = \frac{\hat{V}_{\mathrm{dc}}}{\hat{V}_{\mathrm{dcref}}} = \frac{T_{DVSC}}{1+T_{DVSC}}. \tag{2.30}$$

2.4. SINGLE-LOOP DVSC METHOD

The single-loop DVSC method, as depicted in Figure 2.2, employs the dynamic of dc-link voltage to synthesize the ac output frequency directly. Different controller forms can be employed in G_{DVC}. The small-signal stability of the GFM-VSC, using the single-loop DVSC method, is assessed through closed-loop poles obtained from (2.30) [74], which is illustrated in Figure 2.5. The GFM-VSC in this study is interconnected with a dc-link CPL, with the SCR of the ac grid set to 1.2. In Figure 2.5(a), the DVSC employs a proportional controller [35], as indicated by

$$G_{DVC} = K_p, \tag{2.31}$$

where K_p denotes its proportional gain. Figure 2.5(b) adopts a proportional controller in series with an LPF in the DVSC loop [34]. The controller configuration is expressed as

$$G_{DVC} = K_p \cdot \frac{\omega_p}{s + \omega_p}, \tag{2.32}$$

where ω_p denotes the cut-off frequency of the LPF. Figure 2.5(c) shows a proportional-integral controller for the DVSC loop [37], given by

$$G_{DVC} = K_p + \frac{K_i}{s}, \tag{2.33}$$

where K_i denotes the integral gain. In those closed-loop pole trajectories, it is evident that poles $\lambda_{1\text{–}2}$ are always positioned within low frequencies of the right-half plane (RHP), indicating the presence of the LFO issue in GFM-VSCs.

The LFO issue arises from the CPS and CPL interconnected with the GFM-VSC through the dc link [J1]. The SISO model depicted in Figure 2.4(b) shows that the closed-loop control system includes two integrators, which is also indicated in its transfer function model (2.30). The first integrator is employed in the DVSC loop, as described in Figure 2.2 and (2.16). The second integral relationship is demonstrated in the plant of dc-link CPS and CPL, as described by the transfer function model (2.14). The double-integrator configuration results in a 180-degree phase lag in the SISO control system, thereby giving rise to the LFO issue.

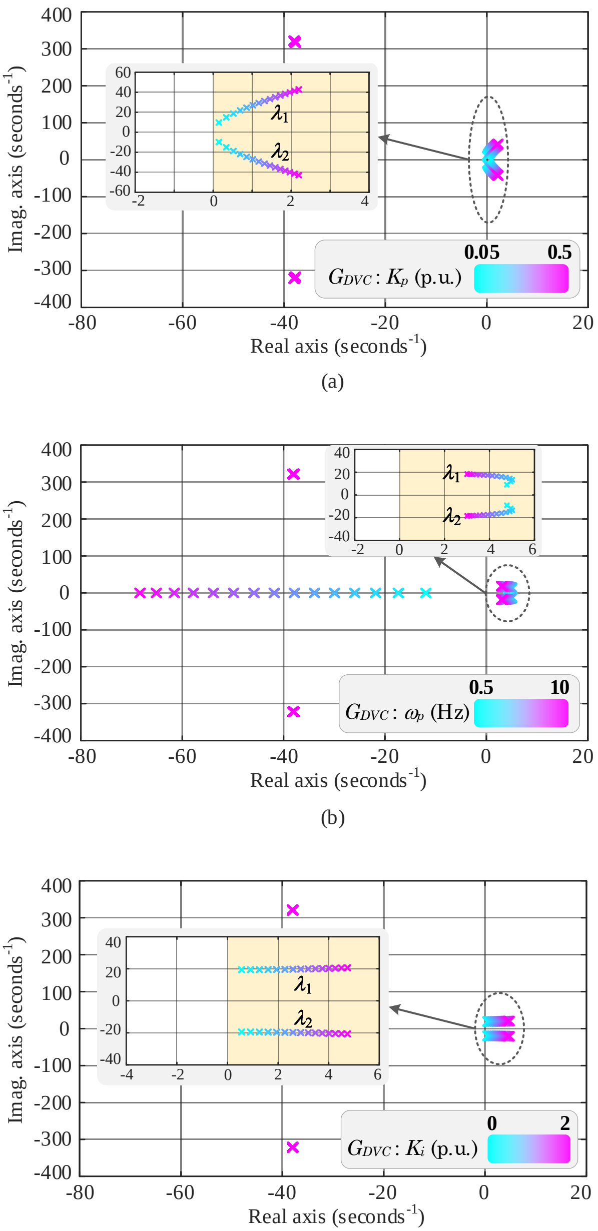
In addition, the control variable of the DVSC method can adopt the square of the dc-link voltage, denoted as V_{dc}^2 [31], [39]. The control law with V_{dc}^2 is expressed as

$$\omega = \omega_1 + G_{DVC} \cdot \left(V_{\mathrm{dc}}^2 - V_{\mathrm{dcref}}^2\right), \quad \theta = \frac{\omega}{s} \tag{2.34}$$

Recalling (2.13), the active power balance of the dc-link capacitor and the plant of constant-power dynamics are expressed as

$$\left(P_{\mathrm{dc}} + \hat{P}_{\mathrm{dc}}\right) - P_{\mathrm{L}} = \frac{1}{2} C_{\mathrm{d}} \cdot \frac{d\left[V_{\mathrm{dc0}}^2 + \hat{V}_{\mathrm{dc}}^2\right]}{dt} \quad \Rightarrow \quad \hat{V}_{\mathrm{dc}}^2 = \frac{2}{sC_{\mathrm{d}}} \cdot \hat{P}_{\mathrm{dc}} \tag{2.35}$$

It is apparent that the plant of constant-power dynamics exhibits an integral characteristic with both V_{dc} and V_{dc}^2 serving as control variables. Consequently, the LFO issue arises with both control variables utilized in the DVSC.



(a)

(b)

(c)

Figure 2.5. Closed-loop poles with single-loop DVSC method and different controller forms. (a) Proportional controller. (b) Proportional controller in series with an LPF. (c) Proportional-integral controller. Source: [J1].

2.5. PROPOSED FLEXIBLE SYNCHRONIZATION CONTROL

To furnish the active damping control with GFM-VSC, it is necessary to improve the synchronization control strategy. For the SISO system exhibiting a double-integrator characteristic, the basic principle behind the active damping control involves the adjustment or the compensation for the integral relationship. Inspired by this principle, the DVSC+PFF and DVSC+V_qFF methods are proposed in [J1] and [J2], thereby resulting in a flexible synchronization architecture [C1]. The PFF and V_qFF controls introduce negative feedback loops from phase angle dynamics to frequency deviations, thereby providing active damping to mitigate the LFO issue [J1], [J2].

2.5.1. DVSC+PFF CONTROL METHOD

Figure 2.6 illustrates the DVSC+PFF method that is proposed in [J1]. The active power at the PCC is fed forward to synthesize the frequency deviation through the controller K_{PFF}. This control loop and the DVSC loop are connected in parallel to synchronize GFM-VSCs with ac grids. The DVSC utilizes a proportional-integral controller expressed in (2.33). Notably, it is essential to keep the integral controller in G_{DVC} to accurately track V_{dcref}, given that the PFF control output, $\Delta\omega_2$, remains non-zero in the steady state.

Besides the paralleled DVSC+PFF method, a cascaded DVSC+PSC method is depicted in Figure 2.7, which is reported in [18], [20], [36], [40]. The cascaded control method can be mathematically equivalent to the paralleled control method. Their relationship is obtained using the block diagram algebra [74], which is expressed as

$$\begin{cases} G_{DVC\_parallel} = G_{DVC\_cascaded} \cdot K_{PSC} \\ K_{PFF} = K_{PSC} \end{cases} \tag{2.36}$$

where the controllers of cascaded and paralleled configurations are denoted by subscripts *cascaded* and *parallel*, respectively. However, the paralleled configuration allows independent tuning of the DVSC and the active damping parameters. Moreover, the paralleled configuration facilitates faster control dynamics of V_{dc} compared to the cascaded configuration, especially when the PFF/PSC loop incorporates the inertial emulation functionality.

Figure 2.8 illustrates the SISO model of the studied GFM-VSC using the DVSC+PFF method. This model is derived by incorporating the PFF control dynamics into the SISO model depicted in Figure 2.4(b). It is shown that the PFF control employs phase angle dynamics $\hat{\theta}$ as feedback into the frequency control. The plant of active power control, denoted by G_P, exhibits a negative gain since the specified active power direction is from ac grid to VSC. Consequently, the PFF control establishes a negative feedback loop, effectively compensating for the double-integrator characteristics inherent in the SISO model. This, in turn, leads to the mitigation of the LFO issue.

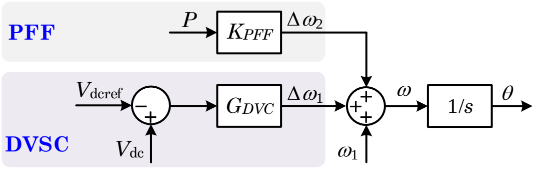

PFF
P
K_{PFF}
$\Delta\omega_2$
V_{dcref}
−
+
G_{DVC}
$\Delta\omega_1$
+
+
+
ω
1/s
θ
DVSC
V_{dc}
ω_1

Figure 2.6. Proposed DVSC+PFF method. Source: [J1].

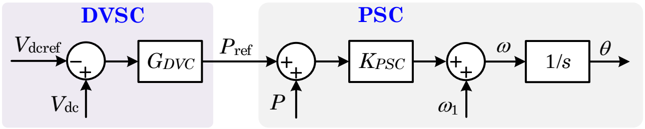

DVSC
PSC
V_{dcref}
−
+
G_{DVC}
P_{ref}
+
+
K_{PSC}
+
+
ω
1/s
θ
V_{dc}
P
ω_1

Figure 2.7. Block diagram of cascaded DVSC+PSC method. Source: [J1].

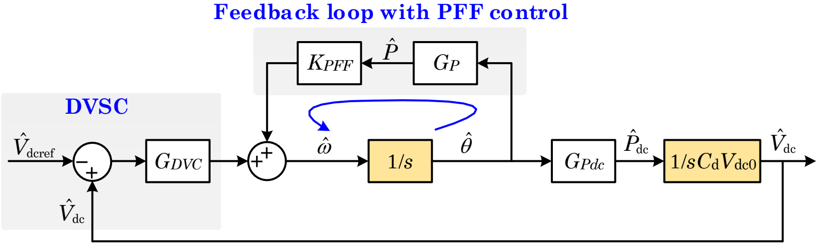

Feedback loop with PFF control
K_{PFF}
$\hat{P}$
G_P
DVSC
$\hat{V}_{dcref}$
−
+
G_{DVC}
+
+
$\hat{\omega}$
1/s
$\hat{\theta}$
G_{Pdc}
$\hat{P}_{dc}$
$1/sC_d V_{dc0}$
$\hat{V}_{dc}$
$\hat{V}_{dc}$

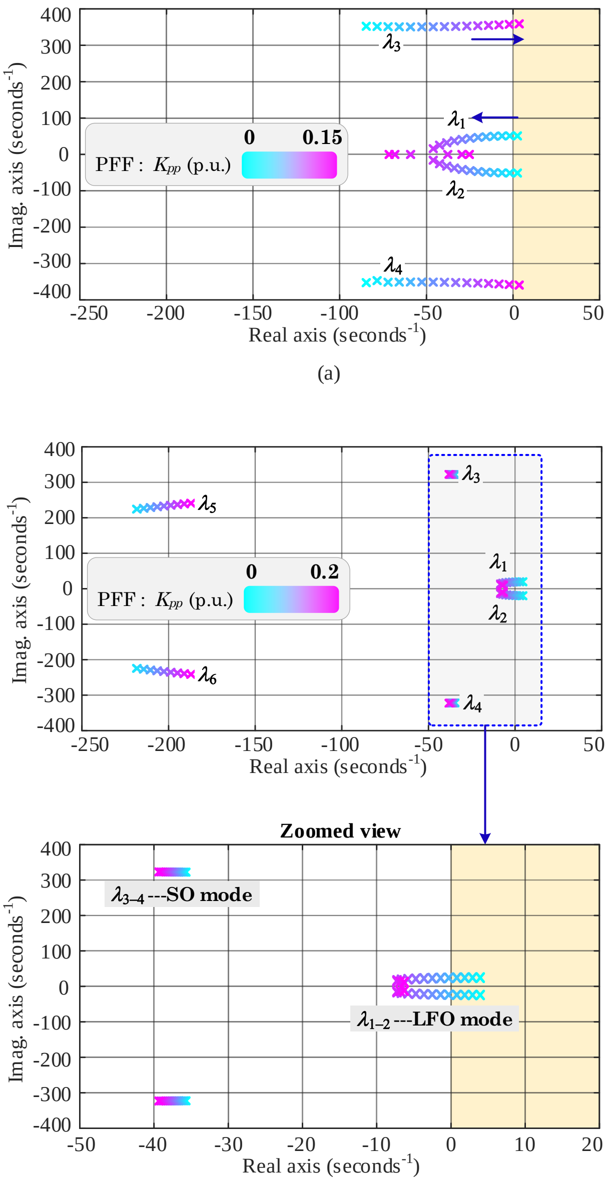
Figure 2.8. SISO model with DVSC+PFF method. Source: [J1].

Dynamics of the PFF control can be derived by recalling (2.7) and (2.28), given by

$$\hat{P} = G_P \cdot \hat{\theta}, \quad G_P = \left(G_P^i - G_P^u Z_g\right) \cdot G_{\theta-i} \;. \tag{2.37}$$

The open-loop and closed-loop transfer function models, from $\hat{V}_{\mathrm{dcref}}$ to $\hat{V}_{\mathrm{dc}}$, are expressed as

$$T_{PFF} = -\frac{G_{P_{dc}} \cdot K_{DVC}}{sC_{\mathrm{d}} V_{\mathrm{dc}0} \cdot \left(s - K_{PFF} G_P\right)}, \quad T_{closed} = \frac{\hat{V}_{\mathrm{dc}}}{\hat{V}_{\mathrm{dcref}}} = \frac{T_{PFF}}{1 + T_{PFF}} \;. \tag{2.38}$$



(a)

(b)

Figure 2.9. Closed-loop poles with DVSC+PFF method. (a) With proportional controller in the PFF loop. (b) With cascaded proportional controller and notch filter in the PFF loop. Source: [J1].

Figure 2.9 illustrates the closed-loop poles with the DVSC+PFF method, where different controllers are employed with the PFF control. The GFM-VSC in this study is interconnected with a dc-link CPL, whereas the SCR of the ac grid is set to 5. In Figure 2.9(a), the PFF control adopts a proportional controller, as indicated by

$$K_{PFF} = K_{pp}. \tag{2.39}$$

The pole trajectories demonstrate that the system stability is dominated by two sets of poles: $\lambda_{1\text{–}2}$ and $\lambda_{3\text{–}4}$. Poles $\lambda_{1\text{–}2}$ located within low frequencies correspond to the LFO mode, whereas poles $\lambda_{3\text{–}4}$ are positioned around the fundamental frequency, indicating the SO mode. It is apparent that as K_{pp} of the PFF control increases, poles $\lambda_{1\text{–}2}$ shift to the left-half plane (LHP), whereas poles $\lambda_{3\text{–}4}$ transition towards the RHP. This phenomenon indicates that the PFF control using a proportional controller effectively mitigates the LFO issue yet aggravates the SO issue.

The SO issue is inherently associated with the dynamic of the active power control plant [18]. The transfer function model G_P exhibits conjugate poles positioned at the fundamental frequency. Therefore, in the SISO model shown in Figure 2.8, the feedback loop introduced by the PFF control demonstrates a resonant peak at the fundamental frequency. A large PFF proportional gain increases the amplitude of this resonance peak, thus leading to the SO issue [75].

To address the trade-off between the SO and the LFO issues, the PFF loop gain at the fundamental frequency is reshaped to mitigate the resonant peak. Based on this principle, the PFF control is embedded with a notch filter, which is thus modified as

$$K_{PFF} = K_{pp} \cdot \frac{s^2 + \omega_1^2}{s^2 + 2\zeta \omega_1 s + \omega_1^2}, \tag{2.40}$$

where K_{pp} represents the proportional gain. ω_1 refers to the nominal angular frequency. ζ represents the damping ratio and is set to 0.7 [76]. The tuning of the notch filter is detailed in [J1].

Figure 2.9(b) presents trajectories of closed-loop poles with the DVSC+PFF method, where the PFF control employs a proportional controller in series with a notch filter. The results show that poles $\lambda_{1\text{–}2}$ transition towards the LHP as K_{pp} of the PFF control increases, which means the LFO issue is effectively mitigated. Meanwhile, poles $\lambda_{3\text{–}4}$ of the SO mode consistently reside in the LHP, indicating that the SO issue is also avoided. Moreover, poles $\lambda_{5\text{–}6}$ are observed in Figure 2.9(b), induced by the notch filter. However, those poles stay away from the RHP, implying that their stability influence is not dominant. Finally, the pole trajectories validate that the PFF control employed the notch filter effectively addresses the LFO issue without aggravating the SO issue.

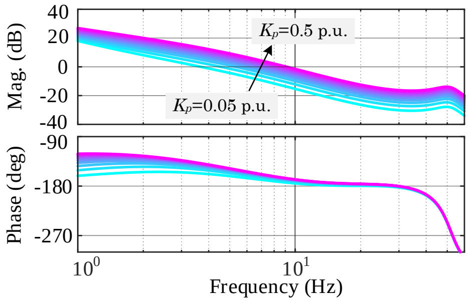


Figure 2.10. Bode plots of open-loop transfer function model with the DVSC+PFF method. Source: [J1].

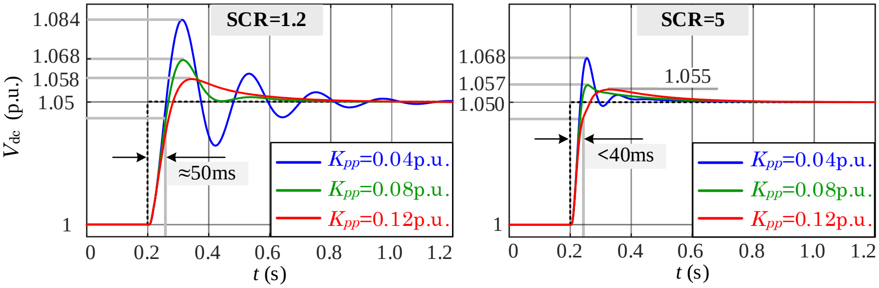


Figure 2.11. Simulation step responses of V_{dc} with DVSC+PFF method. Source: [J1].

In light of the above analysis, the parameters of the DVSC+PFF method are tuned with the following guidelines:

1) K_p of the DVSC loop is tuned considering the dynamic response of V_{dc}. Figure 2.10 illustrates Bode diagrams of the open-loop transfer function model from $\hat{V}_{\mathrm{dcref}}$ to $\hat{V}_{\mathrm{dc}}$. The control bandwidth of the DVSC is set below 10Hz [20], which complies with most operation scenarios. Given the cut-off frequency ω_{dc} as 40 rad/s in this study, K_p is set to 0.25p.u.

2) K_i of the DVSC loop is tuned to eliminate the steady-state error while minimizing the phase lag impact. The frequency response of the DVSC, at the cut-off frequency ω_{dc}, is expressed as $G_{DVC} = K_p + K_i / j\omega_{\mathrm{dc}}$. The phase lag impact of K_i can be minimized when the real component is ten times the imaginary component, i.e., $K_p = 10 \cdot K_i / \omega_{\mathrm{dc}}$. Therefore, K_i is set to 1p.u.

3) K_{pp} of the PFF control is tuned to enhance the active damping, ensuring that (1) all the poles are located in the LHP, and (2) the LFO-mode damping ratio guarantees the effective mitigation of V_{dc} overshoot. Specifically, K_{pp} is set to

0.12p.u. based on Figure 2.9(b). Simulation step responses of V_{dc} are presented in Figure 2.11, confirming the active damping with the PFF control.

2.5.2. DVSC+V$_{\mathrm{Q}}$FF CONTROL METHOD

Figure 2.12 shows the proposed DVSC+V$_{\mathrm{q}}$FF control method in [J2]. The *q*-axis voltage is fed forward to synthesize the frequency deviation through a proportional controller K_{pv}. This control loop and the DVSC loop are configured in parallel to achieve synchronization with ac grids. The DVSC utilizes a proportional-integral controller expressed in (2.33). Notably, the V$_{\mathrm{q}}$FF control differs from the PLL because the *αβ-dq* transformation utilizes the phase angle generated by the DVSC+V$_{\mathrm{q}}$FF control loops rather than solely the V$_{\mathrm{q}}$FF loop [52].

Figure 2.13 shows the SISO model of the studied GFM-VSC using the DVSC+V$_{\mathrm{q}}$FF method. This model is derived by incorporating the dynamics of V$_{\mathrm{q}}$FF control into the SISO model in Figure 2.4(b). In this model, the *q*-axis voltage is derived as

$$\mathbf{v}_{\mathbf{dq0}}^{\mathbf{c}} + \hat{\mathbf{v}}_{\mathbf{dq}}^{\mathbf{c}} = e^{-j\left(\theta_0+\hat{\theta}\right)} \cdot \left(\mathbf{v}_{\mathbf{dq0}}^{\mathbf{s}} + \hat{\mathbf{v}}_{\mathbf{dq}}^{\mathbf{s}}\right) \tag{2.41}$$

$$\hat{v}_q^c = \underbrace{\left[-\sin\theta_0 \quad \cos\theta_0\right]}_{G_{Vq}^{u}} \cdot \hat{v}_{dq}^{s} \underbrace{-\left(\cos\theta_0 \cdot v_{d0}^{s} + \sin\theta_0 \cdot v_{q0}^{s}\right)}_{G_{Vq}^{\theta}} \cdot \hat{\theta} \tag{2.42}$$

Dynamics of the V$_{\mathrm{q}}$FF control is expressed by recalling (2.4) and (2.28), given by

$$\begin{cases} \hat{v}_q^c = \underbrace{G_{Vq}^{\theta} - G_{Vq}^{u} \cdot Z_g \cdot G_{\theta-i}}_{G_{Vq}} \cdot \hat{\theta} \\ \Delta\hat{\omega}_2 = K_{pv} \cdot G_{Vq} \cdot \hat{\theta} \end{cases} \tag{2.43}$$

The open-loop and closed-loop transfer function models, from $\hat{V}_{\mathrm{dcref}}$ to $\hat{V}_{\mathrm{dc}}$, are expressed as

$$T_{VqFF} = \frac{-G_{P_{dc}} \cdot G_{DVC}}{s C_{\mathrm{d}} V_{\mathrm{dc0}} \left(s - K_{pv} G_{Vq}\right)}, \quad T_{closed} = \frac{\hat{V}_{\mathrm{dc}}}{\hat{V}_{\mathrm{dcref}}} = \frac{T_{VqFF}}{1 + T_{VqFF}} \tag{2.44}$$

The SISO model demonstrates that the V$_{\mathrm{q}}$FF control results in a negative feedback relationship from phase angle $\hat{\theta}$ to frequency $\hat{\omega}$, due to the inherent relationship between the *q*-axis voltage $\hat{v}_q^c$ and the phase angle $\hat{\theta}$, as denoted by (2.43). Consequently, the SISO model no longer demonstrates the double-integrator characteristics, which means that the LFO issue is mitigated. Furthermore, the plant of V$_{\mathrm{q}}$FF control, denoted by G_{Vq}, does not include poles at the fundamental frequency, indicating that the V$_{\mathrm{q}}$FF control doesn’t lead to adverse effects on the SO issue.

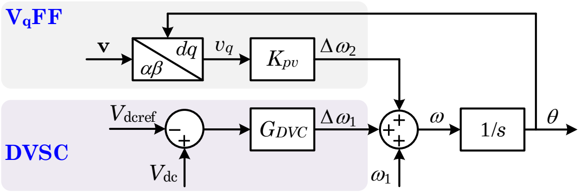

VqFF
v
dq
αβ
vq
Kpv
Δω2
Vdcref
DVSC
GDVC
Δω1
Vdc
ω
1/s
θ
ω1

Figure 2.12. Proposed DVSC+V_qFF method. Source: [J2].

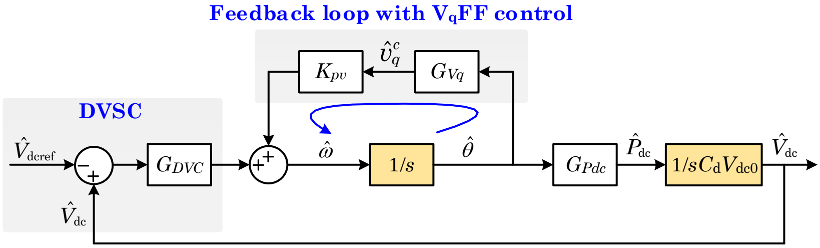

Feedback loop with VqFF control
Kpv
v̂qc
GVq
DVSC
V̂dcref
GDVC
ω̂
1/s
θ̂
GPdc
P̂dc
1/sCdVdc0
V̂dc
V̂dc

Figure 2.13. SISO model with DVSC+V_qFF method. Source: [J2].

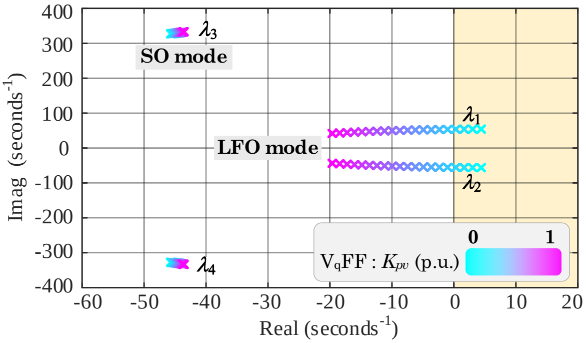


Figure 2.14. Closed-loop poles with DVSC+V_qFF method. Source: [J2].

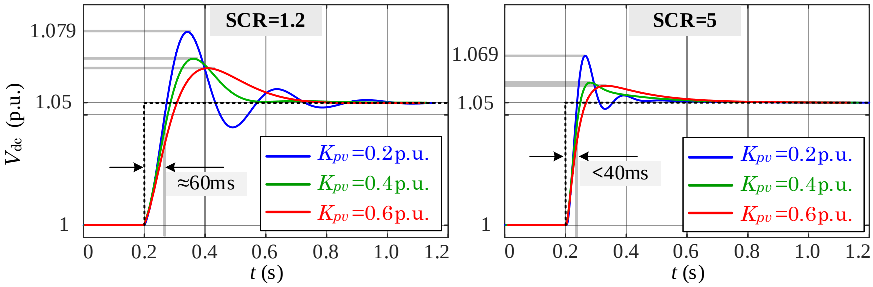


Figure 2.15. Simulation step responses of V_{dc} with DVSC+V_qFF method. Source: [J2].

Figure 2.14 illustrates the trajectories of closed-loop poles using the DVSC+$\mathrm{V_q}$FF method. The GFM-VSC is interconnected with a dc-link CPS, with the SCR of the ac grid set to 5. It is evident that poles λ_{1-2} transition towards the LHP as K_{pv} of the $\mathrm{V_q}$FF control increases, which means the LFO issue is effectively mitigated. Meanwhile, poles λ_{3-4} are consistently located in the LHP with minor variations, indicating that the $\mathrm{V_q}$FF control does not aggravate the SO issue.

The parameter tuning of the DVSC+$\mathrm{V_q}$FF method follows the same way as that of the DVSC+PFF method. The detailed tuning processes are presented in [J2], with K_p set to 0.25p.u., K_i set to 1p.u., and K_{pv} set to 0.6p.u. Simulation step responses of V_{dc} are shown in Figure 2.15, confirming the active damping using the $\mathrm{V_q}$FF control.

2.6. EXPERIMENTAL RESULTS

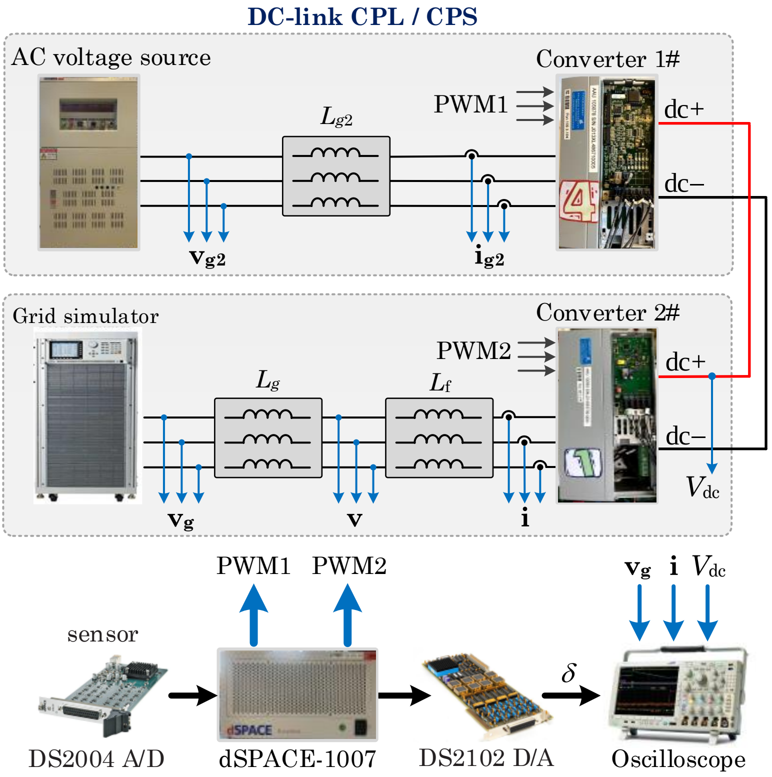

DC-link CPL / CPS
AC voltage source
Converter 1#
PWM1
L_{g2}
dc+
dc−
$\mathbf{v_{g2}}$
$\mathbf{i_{g2}}$
Grid simulator
Converter 2#
PWM2
L_g
L_f
dc+
dc−
V_{dc}
$\mathbf{v_g}$
$\mathbf{v}$
$\mathbf{i}$
PWM1
PWM2
$\mathbf{v_g}$
$\mathbf{i}$
V_{dc}
sensor
δ
DS2004 A/D
dSPACE-1007
DS2102 D/A
Oscilloscope

Figure 2.16. Experimental Setup. Source: [J1].

The experimental setup depicted in Figure 2.16 is based on a back-to-back system. Converter 1# serves as a CPS or CPL, which is interconnected with Converter 2# through the dc link. Converter 2# implements the GFM control strategy. The ac grid consists of the grid simulator and series inductors. The control principles for Converters 1# and 2# are implemented using the dSPACE platform. Waveforms of frequency f, dc-link voltage V_{dc}, PCC voltage $\mathbf{v}$, ac current $\mathbf{i}$, and power angle δ are demonstrated. Note that δ is the phase angle different of $\mathbf{v_g}$ and $\mathbf{E}$, i.e., $\delta = \theta_g - \theta$, where θ_g is obtained using a fast PLL.

Figure 2.17 to Figure 2.19 demonstrate the enhanced performance with the DVSC+PFF method. Figure 2.17 compares the dynamics between the DVSC+PFF and single-loop DVSC methods. The GFM-VSC remains stable with the DVSC+PFF method, while it becomes unstable when switching to the single-loop DVSC method at $\boldsymbol{t_1}$. Waveforms of f, V_{dc} and $\mathbf{i}$ demonstrate oscillations within low frequencies, subsequently tripping the VSC. The results validate the LFO issue of GFM-VSCs using the single-loop DVSC method, which can be mitigated using the DVSC+PFF method.

Figure 2.18 compares the system stability between proportional controller-based and notch-filtered PFF controls. When employing the proportional-based PFF control, the GFM-VSC becomes unstable as K_{pp} of the PFF control is increased to 0.15p.u. Waveforms of f and V_{dc} manifest oscillations with fundamental frequencies, while the waveform of $\mathbf{i}$ features significant dc components. In contrast, when the PFF control is equipped with a notch filter, the GFM-VSC always keeps stable during the increase of K_{pp}. The comparative results confirm that the PFF control employed notch filter minimizes its adverse impacts on the SO issue.

Figure 2.19 illustrates the step response of V_{dc} utilizing the DVSC+PFF method. As V_{dcref} shifts to 420V (1.05 p.u.), V_{dc} precisely follows this change, with the measured rise time under 35ms. Moreover, the overshoot of V_{dc} is effectively dampened.

Figure 2.20 and Figure 2.21 demonstrate the enhanced performance with the DVSC+$\mathrm{V_q}$FF method. Figure 2.20 compares the dynamics between the DVSC+$\mathrm{V_q}$FF and single-loop DVSC methods. The GFM-VSC remains stable with the DVSC+$\mathrm{V_q}$FF method, while it becomes unstable as the $\mathrm{V_q}$FF control is deactivated at $\boldsymbol{t_1}$. Waveforms of V_{dc}, $\mathbf{i}$, and δ demonstrate divergent oscillations within low frequencies, subsequently tripping the VSC. The results validate that the DVSC+$\mathrm{V_q}$FF method can effectively mitigate the LFO issue.

Figure 2.21 illustrates the step response of V_{dc}, employing the DVSC+$\mathrm{V_q}$FF method for synchronization. As V_{dcref} shifts to 1.05 p.u., V_{dc} accurately tracks this change, with the measured rise time under 40ms. Meanwhile, the overshoot of V_{dc} is lower than 1.06 p.u.

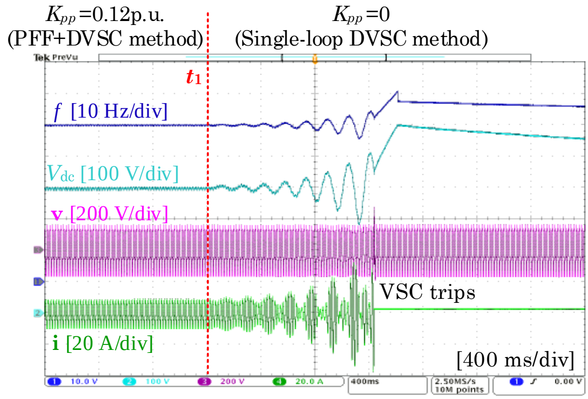
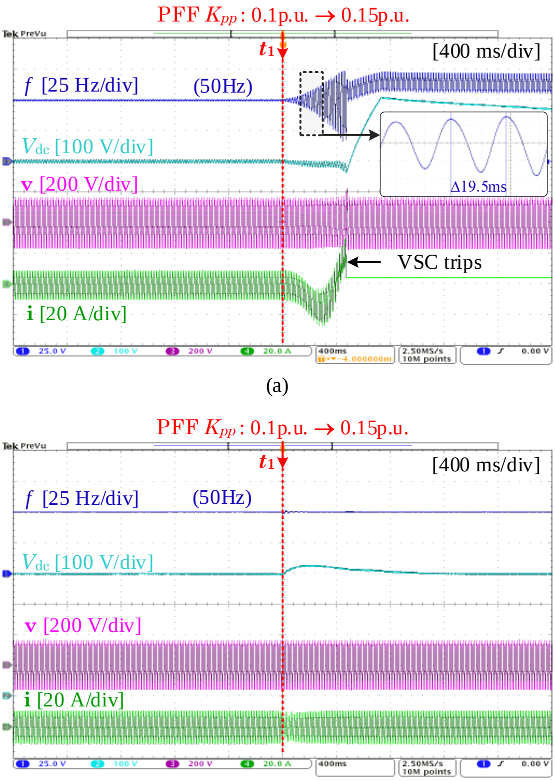


Figure 2.17. Dynamics comparison between the DVSC+PFF and single-loop DVSC methods. Source: [J1].



(a)

(b)

Figure 2.18. Dynamics with the DVSC+PFF method. (a) With proportional controller in the PFF loop. (b) With cascaded proportional controller and notch filter in the PFF loop. Source: [J1].

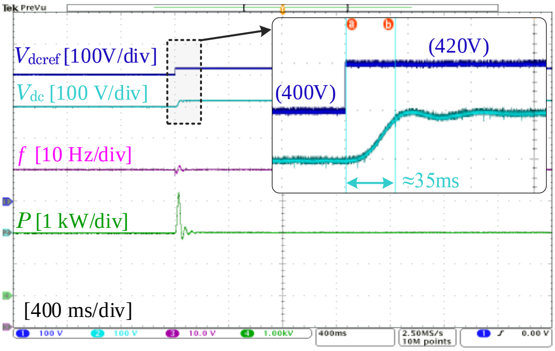


Figure 2.19. Step response of V_{dc} with the DVSC+PFF method. Source: [J1].

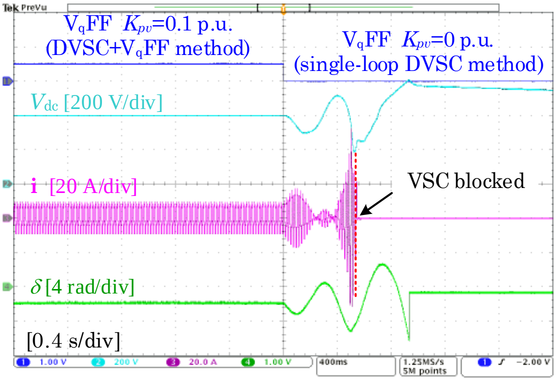


Figure 2.20. Dynamics comparison between the DVSC+V_qFF and single-loop DVSC methods. Source: [J2].

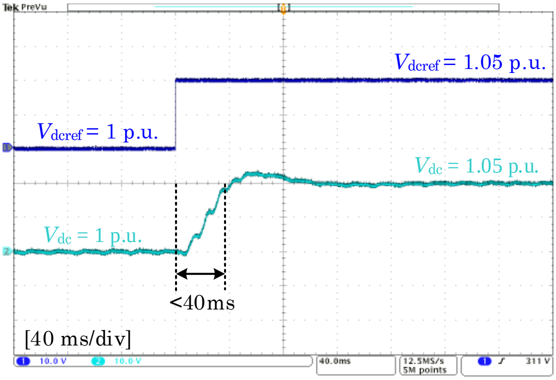


Figure 2.21. Step response of V_{dc} with the DVSC+V_qFF method. Source: [J2].

2.7. SUMMARY

This chapter has analyzed the small-signal synchronization stability of GFM-VSCs employing different DVSC approaches.

1) A SISO model is developed to analyze the small-signal synchronization stability. It reveals that the GFM-VSC using the single-loop DVSC approach encounters the LFO issue when connecting to a CPS or CPL through the dc link.

2) A flexible synchronization control is proposed, which comprises a paralleled configuration of DVSC, PFF, and V_qFF control loops. Both the PFF and V_qFF controls form feedback loops from the phase angle dynamics to the frequency deviations, functioning as active dampers against the constant-power dynamics exhibited on the dc link.

3) Methods for loop gain shaping and parameter tuning for the proposed synchronization control are developed, which effectively mitigate the LFO issue without aggravating the SO issue. The GFM-VSC, employing the proposed synchronization control, demonstrates stable operation across a range of grid strengths and in both inverter and rectifier modes.

CHAPTER 3. DAMPING EFFECTS OF INNER CONTROL LOOPS

The content of this chapter is based on publications [J3], [C2], and [C3].

3.1. INTRODUCTION

The control architecture of GFM-VSCs includes the outer and inner control loops, as illustrated in Figure 1.2. Besides the outer-loop DVSC methods that are discussed in Chapter 2, the inner control loops are also of critical concern.

GFM-VSCs with omitted inner control loops exhibit a simple control architecture [18], [43], [44]. Yet, this configuration may introduce the risk of instability under stiff ac grids and the overcurrent issue under large disturbances [18], [45], [46]. Therefore, it is crucial to assess how inner control loops influence the damping of the system.

Different types of inner-loop control strategies are reported in [8] [18], [47]-[56], which are illustrated in Figure 1.3. The SO and SSO issues, arising from the interactions between outer and inner loops, are reported with various inner-loop controller forms [9], [18], [49], [50], [52], [57]-[59]. However, most of those studies rely on numerical approaches, which, however, cannot shed analytical insight into the impact of inner-loop control dynamics on the outer-loop control dynamics and associated instability issues.

To fill the research gaps, this Chapter develops an analytical approach to characterize the impact of inner control loops on the dynamics of GFM-VSCs [J3], [C3]. The approach comprises two steps and can be extended to different controller forms. First, the dynamics of inner control loops are described using an impedance model. On the basis of the impedance model, the complex torque coefficient method is employed in GFM-VSCs to characterize the interactions between inner and outer control loops under different ac grid conditions. Case studies are conducted based on the virtual admittance and vector current control, including the analyses of impedance profiles and complex torque plots. Parameter tuning guidelines for inner control loops are finally developed to enhance the stability, which is validated by experimental results.

3.2. IMPEDANCE-BASED DYNAMICS CHARACTERIZATION

3.2.1. PRINCIPLE AND DERIVATION

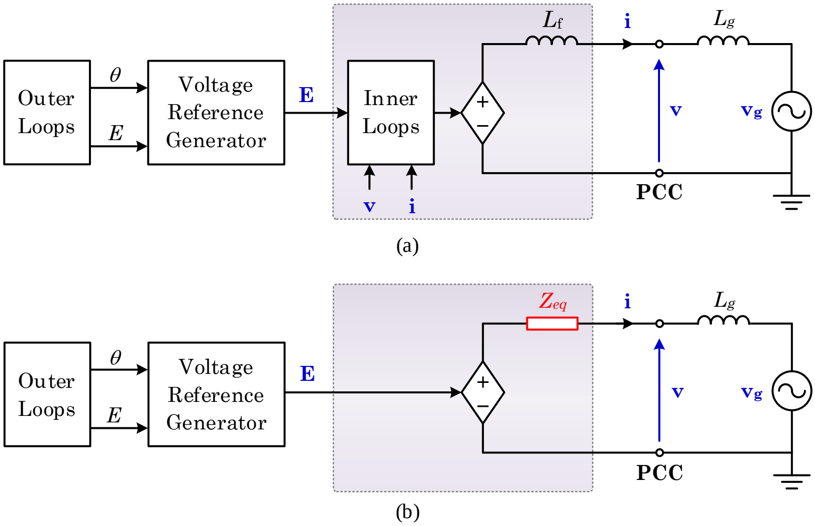

Outer Loops
θ
E
Voltage Reference Generator
E
Inner Loops
v
i
Lf
i
Lg
v
vg
PCC
(a)
Outer Loops
θ
E
Voltage Reference Generator
E
Zeq
i
Lg
v
vg
PCC
(b)

Figure 3.1. Principle of the impedance-based characterization. (a) Using original inner control loops. (b) Using impedance representation for inner control loops. Source: [J3], [C3].

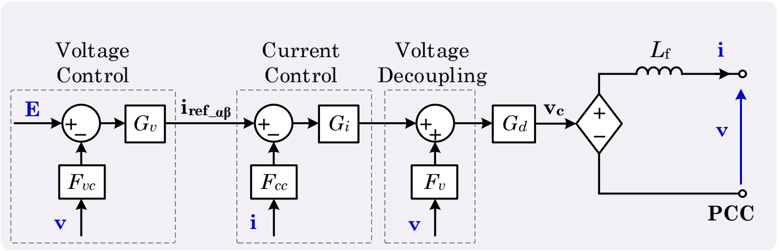

Voltage Control
Current Control
Voltage Decoupling
Lf
i
E
iref_αβ
Gv
Gi
Gd
vc
Fvc
Fcc
Fv
v
i
v
v
PCC

Figure 3.2. General configuration of inner control loops. Source: [J3], [C3].

Three types of inner control loops are depicted in Figure 1.3 [J3], which are listed as follows:

1) Virtual impedance control [47]-[49], as depicted in Figure 1.3(a).
2) Vector voltage and vector current control [8], [50], as depicted in Figure 1.3(b).
3) Virtual admittance and vector current control [54], [55], as shown in Figure 1.3(c).

Figure 3.1 shows the principle of impedance representation for inner control loops [C3], where the circuit and control variables are clarified in Chapter 2.2. It can be observed from Figure 3.1(a) to Figure 3.1(b) that the inner control loops are omitted while their dynamics are integrated into an ac-output impedance Z_{eq}. Therefore, compared to GFM-VSCs without inner control loops, the inclusion of inner control loops essentially shapes the inductor filter L_f into the impedance Z_{eq}, thereby affecting the system dynamics.

Figure 3.2 demonstrates a general configuration of inner control loops that can cover different inner-loop schemes. This configuration is realized in the $\alpha\beta$-frame. F_{vc} represents the flag of the vector voltage control. F_{cc} represents the flag of the vector current control. F_v represents the flag of the voltage decoupling control. G_v represents the vector voltage controller or the virtual admittance. G_i represents the vector current controller. G_d represents the time delay.

Figure 3.3 presents the derivation of Z_{eq}. In Stage 1, GFM-VSC's terminal voltage $\mathbf{v_c}$ is decomposed into three controlled voltage sources according to Superposition theorem [77], i.e., $\mathbf{v_{c1}}$, $\mathbf{v_{c2}}$, and $\mathbf{v_{c3}}$. The loop gains from three input variables, internal EMF $\mathbf{E}$, PCC voltage $\mathbf{v}$, and ac current $\mathbf{i}$, to three controlled voltage sources, are derived according to Block diagram algebra [74]. They are expressed as

$$\begin{cases} \mathbf{v_{c1}} = \left(G_d \cdot G_i \cdot G_v\right) \cdot \mathbf{E} \\ \mathbf{v_{c2}} = \left(-G_d \cdot G_i \cdot G_v \cdot F_{vc} + G_d \cdot F_v\right) \cdot \mathbf{v} \\ \mathbf{v_{c3}} = \left(-G_d \cdot G_i \cdot F_{cc}\right) \cdot \mathbf{i} \end{cases} \tag{3.1}$$

In Stage 2, a virtual impedance Z_1 is employed to represent the dynamics of the current-controlled voltage source $\mathbf{v_{c3}}$ [77], represented as

$$Z_1 = G_d \cdot G_i \cdot F_{cc} \tag{3.2}$$

In Stage 3, controlled voltage sources $\mathbf{v_{c1}}$ and $\mathbf{v_{c2}}$ in series with impedances are transformed into controlled current sources $\mathbf{i_{o1}}$ and $\mathbf{i_{o2}}$ in parallel with admittances according to Norton's theorem [77]. The controlled current sources $\mathbf{i_{o1}}$ and $\mathbf{i_{o2}}$ are represented as

$$\begin{cases} \mathbf{i_{o1}} = \dfrac{\mathbf{v_{c1}}}{sL_f + Z_1} = \dfrac{G_d \cdot G_i \cdot G_v}{sL_f + Z_1} \cdot \mathbf{E} \\ \mathbf{i_{o2}} = \dfrac{\mathbf{v_{c2}}}{sL_f + Z_1} = \dfrac{-G_d \cdot G_i \cdot G_v \cdot F_{vc} + G_d \cdot F_v}{sL_f + Z_1} \cdot \mathbf{v} \end{cases} \tag{3.3}$$

In Stage 4, a virtual admittance Y_1 is employed to represent the dynamics of voltage-controlled current source $\mathbf{i_{o2}}$ [77], represented as

$$Y_1 = \frac{G_d \cdot G_i \cdot G_v \cdot F_{vc} - G_d \cdot F_v}{sL_f + Z_1}. \tag{3.4}$$

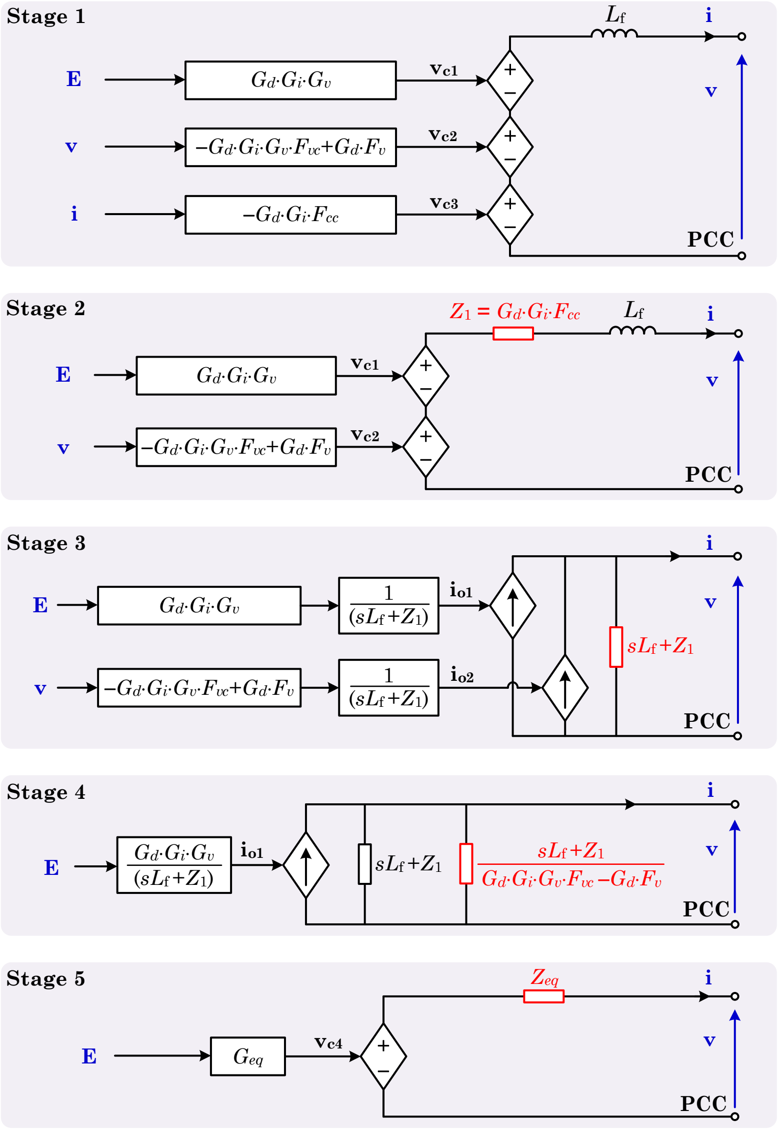

Stage 1
E
v
i
Gd·Gi·Gv
−Gd·Gi·Gv·Fvc+Gd·Fv
−Gd·Gi·Fcc
vc1
vc2
vc3
Lf
i
v
PCC
Stage 2
Z1 = Gd·Gi·Fcc
Lf
E
v
Gd·Gi·Gv
−Gd·Gi·Gv·Fvc+Gd·Fv
vc1
vc2
i
v
PCC
Stage 3
E
v
Gd·Gi·Gv
−Gd·Gi·Gv·Fvc+Gd·Fv
1/(sLf+Z1)
1/(sLf+Z1)
io1
io2
sLf+Z1
i
v
PCC
Stage 4
E
Gd·Gi·Gv/(sLf+Z1)
io1
sLf+Z1
(sLf+Z1)/(Gd·Gi·Gv·Fvc−Gd·Fv)
i
v
PCC
Stage 5
E
Geq
vc4
Zeq
i
v
PCC

Figure 3.3. Derivation of the impedance-based representation. Source: [J3], [C3].

In Stage 5, the controlled current source $\mathbf{i}_{o1}$ with paralleled admittances is transformed into a controlled voltage source $\mathbf{v}_{c4}$ connected in series with an impedance Z_{eq} according to Norton's theorem [77]. The transfer function model of Z_{eq} and the loop gain from $\mathbf{E}$ to $\mathbf{v}_{c4}$ are given by

$$Z_{eq} = \frac{sL_f + G_d \cdot G_i \cdot F_{cc}}{G_d \cdot G_i \cdot G_v \cdot F_{vc} - G_d \cdot F_v + 1}, \tag{3.5}$$

$$G_{eq} = \frac{G_d \cdot G_i \cdot G_v}{G_d \cdot G_i \cdot G_v \cdot F_{vc} - G_d \cdot F_v + 1}. \tag{3.6}$$

3.2.2. CASE STUDY

The case study employs the virtual admittance and vector current control realized in the $\alpha\beta$-frame. Parameters depicted in Figure 3.2 are set as F_{vc}=1 and F_{cc}=1. G_v denotes the virtual admittance control and is expressed as

$$G_v = \frac{1}{sL_v + G_R \cdot R_v}, \tag{3.7}$$

where L_v represents the virtual inductance, and R_v represents the virtual resistance. Note that R_v incorporates a notch filter denoted as G_R, which functions at the fundamental frequency to reduce the R/X ratio of the power transmission impedance [18]. The notch filter can be replaced with an HPF for the dq-frame realization of virtual admittance control [49]. G_i refers to the current controller and is expressed as

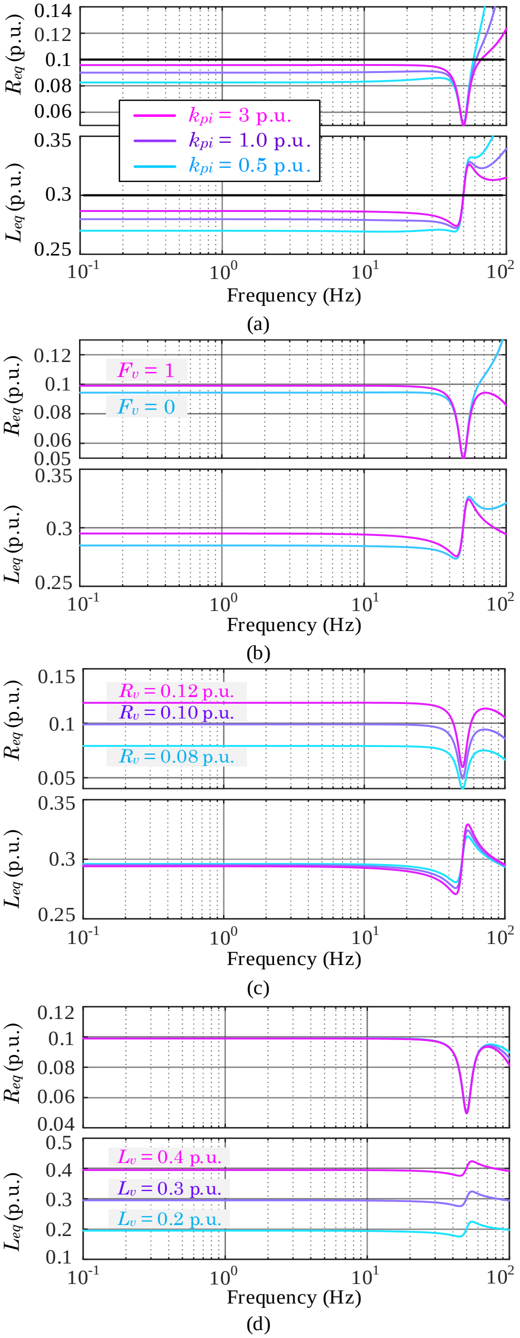
$$G_i = k_{pi} + \frac{k_{ri}\, s}{s^2 + 2\omega_r s + \omega_1^2}, \tag{3.8}$$

where a quasi-proportional-resonant controller is employed. k_{pi} represents the proportional gain, while k_{ri} and ω_r denote the resonant gain and cut-off frequency, respectively. Moreover, the time delay is assumed to be unity gain when analyzing the dynamics within synchronous and sub-synchronous frequencies, which is expressed as G_d=1. Given this assumption, the loop gain G_{eq} equals 1.

The transfer function model of Z_{eq} can be represented as a complex space vector in the frequency domain by substituting s=$j\omega$, given by

$$Z_{eq} \quad \leftrightarrow \quad \mathbf{Z_{eq}} = R_{eq} + j\omega \cdot L_{eq}. \tag{3.9}$$

The real component denotes the equivalent resistance R_{eq}, while the imaginary component denotes the equivalent inductance L_{eq}. In ac circuits, the resistance component of a power transmission impedance can mitigate the dc bias of ac voltage and current [18]. Those issues manifest as the SOs in active and reactive power [77]. Therefore, the low-frequency component of R_{eq} indicates the damping impacts of inner control loops on the SO issue.



(a)

(b)

(c)

(d)

Figure 3.4. Frequency responses of $\mathbf{Z_{eq}}$ with various inner-loop parameters. (a) Different k_{pi}. (b) Different F_v. (c) Different R_v. (d) Different L_v. Source: [J3].

Figure 3.4 demonstrates the frequency-domain profiles of $\mathbf{Z_{eq}}$, where various inner-loop parameters are tested. Figure 3.4(a) shows impedance plots with different k_{pi} of the vector current control, with R_v set to 0.1p.u., L_v set to 0.3p.u., k_{ri} set to 0.4p.u., and F_v set to 0. It can be observed that R_{eq} exhibits an increase as k_{pi} varies from 0.5p.u. to 3p.u. Yet, its value is always lower than that of R_v, unless under the assumption of infinite k_{pi}, i.e.

$$Z_{eq}\Big|_{k_{pi}\to+\infty} = sL_v + R_v \cdot G_R \tag{3.10}$$

Therefore, it can be observed that the reduced component of R_{eq} compared to R_v is due to the interaction between vector current control and virtual admittance. Further, Figure 3.4(b) compares the impedance plots with disabled (F_v=0) and enabled (F_v=1) voltage decoupling control. It is evident that when employing the voltage decoupling control, R_{eq} is increased and approaches 0.1p.u. within low frequencies. The findings from Figure 3.4(a)-(b) indicate that the interaction between vector current control and virtual admittance results in a negative component in R_{eq}. Employing the voltage decoupling control and increasing k_{pi} of the vector current control can mitigate such negative-resistance impacts.

Figure 3.4(c) and (d) show impedance plots with different R_v and L_v, respectively. It is shown that R_{eq} is increased significantly as R_v switches from 0.08p.u. to 0.1p.u. and further to 0.12p.u., which indicates that R_v contributes a positive resistance effect to $\mathbf{Z_{eq}}$. In contrast, the variation of L_v has little influence on the low-frequency R_{eq}, but it mainly contributes to the inductance component of $\mathbf{Z_{eq}}$. Moreover, the impedance measurement results have validated the accuracy of $\mathbf{Z_{eq}}$, which are detailed in [J3].

3.3. CONTROL INTERACTION ANALYSIS

3.3.1. COMPLEX TORQUE COEFFICIENT BASICS

The complex torque coefficient method was originally proposed in the torsional interaction analysis for synchronous machines [78], [79]. In a single synchronous machine infinite-bus system, the mechanical torque represents the electromechanical dynamics (rotor), whereas the electrical torque characterizes the dynamics of the electrical subsystem (stator and ac infinite bus) [78]. Figure 3.5 depicts the complex space representations of mechanical and electrical torques. $\mathbf{T_m}$ denotes the mechanical torque, and $\mathbf{T_e}$ denotes the electrical torque. They are mathematically expressed as

$$\begin{cases} \mathbf{T_m}(j\omega) = K_m(\omega) + j\omega \cdot D_m(\omega) \\ \mathbf{T_e}(j\omega) = K_e(\omega) + j\omega \cdot D_e(\omega) \end{cases}. \tag{3.11}$$

The real components align with phase angle θ, indicative of mechanical synchronizing torque K_m and electrical synchronizing torque K_e. The imaginary components align with the frequency ω, referring to mechanical damping torque D_m and electrical damping torque D_e.

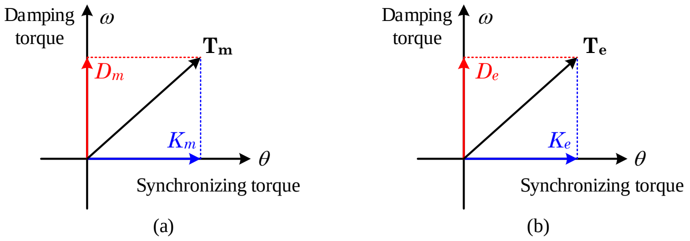


Figure 3.5. Complex space representations of mechanical and electrical torques. (a) Mechanical torque. (b) Electrical torque. Source: [J3].

According to the power balance between the electrical subsystem and the mechanical subsystem, the interaction can be represented through the equation shown as

$$K_m(\omega) + K_e(\omega) + j\omega \cdot \left[D_m(\omega) + D_e(\omega)\right] = 0\,. \tag{3.12}$$

The real components $K_m + K_e$ refer to the net synchronizing torques. Given $K_m + K_e = 0$, the frequencies of oscillation modes can be identified [80]. Further, the imaginary components denote the net damping torques, i.e., $D_m + D_e$, which determine the stability at the identified oscillation modes [81], given by

$$\begin{cases} D_m + D_e > 0 & \Rightarrow \quad \text{Stable} \\ D_m + D_e < 0 & \Rightarrow \quad \text{Unstable} \end{cases}. \tag{3.13}$$

It is clear that the complex torque coefficient-based analytical method can quantify the contribution of each subsystem to the damping [80].

3.3.2. INTERACTION ANALYSIS FOR GFM-VSCS

Figure 3.6 presents the circuit and control diagrams of the studied GFM-VSC [J3]. The variables are clarified in Chapter 2.2. The grid synchronization is implemented using the PSC, with the control law

$$\omega = G_{PSC} \cdot \left(P_{\text{ref}} - P\right) + \omega_1, \quad G_{PSC} = K_{psc}\frac{\omega_p}{s+\omega_p}, \quad \theta = \frac{\omega}{s}\,. \tag{3.14}$$

G_{PSC} denotes the PSC controller, consisting of a proportional controller K_{psc} and an LPF with cut-off frequency ω_p. The AVC is adopted to maintain the magnitude of PCC voltage, denoted as V_{mag}, around 1p.u. The control law is expressed as

$$E = \left(V_{\text{ref}} - V_{\text{mag}}\right) \cdot K_{iv}/s\,. \tag{3.15}$$

where K_{iv} represents the integral gain.

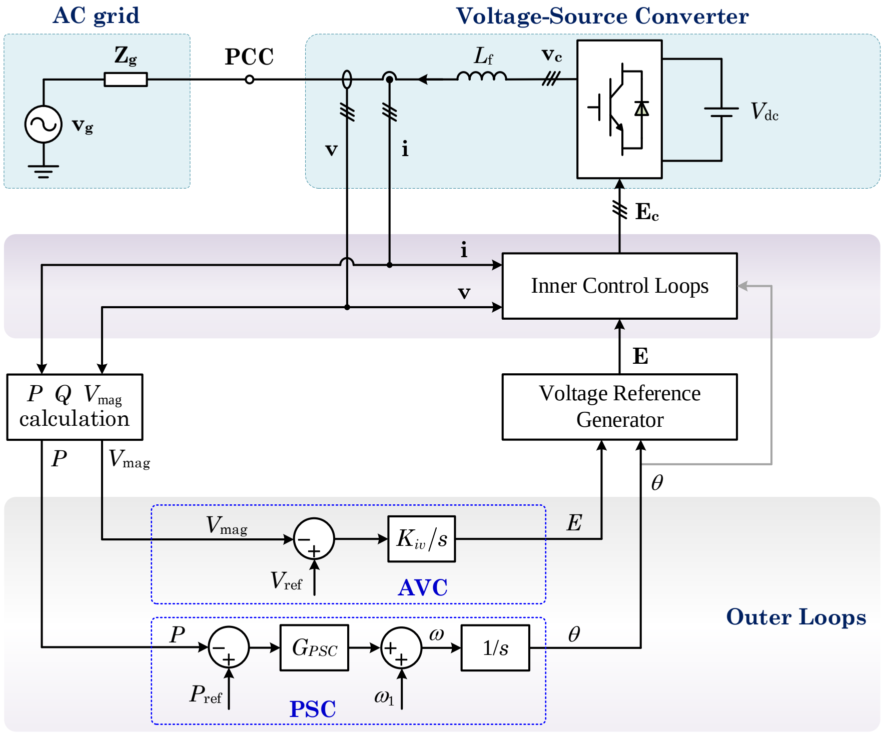

AC grid
Voltage-Source Converter
Zg
PCC
Lf
vc
vg
v
i
Vdc
Ec
i
v
Inner Control Loops
E
P Q Vmag calculation
Voltage Reference Generator
P
Vmag
θ
Vmag
Kiv/s
E
Vref
AVC
Outer Loops
P
GPSC
ω
1/s
θ
Pref
PSC
ω1

Figure 3.6. Main circuit and control diagrams of the studied GFM-VSC. Source: [J3].

To employ the complex torque coefficient approach for GFM-VSCs, the mechanical and electrical torques need to be identified. Figure 3.7 shows the equivalent circuit diagram in the dq-frame, where the inner-loop dynamics are represented by impedance Z_{eq_dq}. The dq-frame impedance Z_{eq_dq} can be obtained from $\alpha\beta$-frame impedance Z_{eq} using the frequency translation [73], given by

$$\mathbf{Z_{eq\_dq}}\left(s\right)=Z_{eq}\left(s+j\omega_{1}\right). \tag{3.16}$$

The complex vector and the corresponding impedance matrix are expressed as

$$\mathbf{Z_{eq\_dq}}\left(s\right)=Z_{\mathrm{d}}\left(s\right)+jZ_{\mathrm{q}}\left(s\right) \quad \leftrightarrow \quad Z_{eq\_dq}\left(s\right)=\begin{bmatrix} Z_{\mathrm{d}}\left(s\right) & -Z_{\mathrm{q}}\left(s\right) \\ Z_{\mathrm{q}}\left(s\right) & Z_{\mathrm{d}}\left(s\right) \end{bmatrix}. \tag{3.17}$$

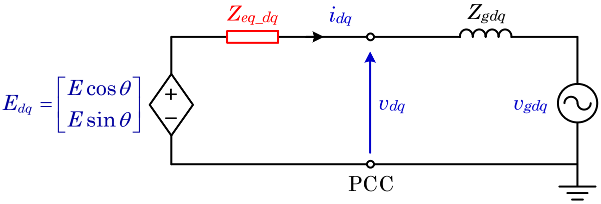

$E_{dq}=\begin{bmatrix}E\cos\theta\\E\sin\theta\end{bmatrix}$
+
−
Z_{eq_dq}
i_{dq}
Z_{gdq}
v_{dq}
v_{gdq}
PCC

Figure 3.7. Equivalent circuit diagram using *dq*-frame impedance representation for inner control loops. Source: [J3].

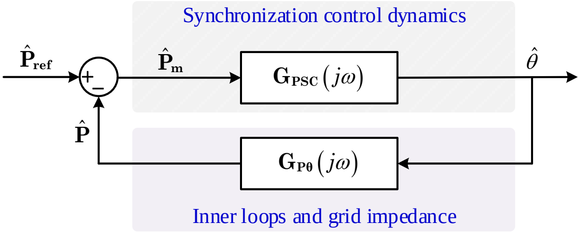

Synchronization control dynamics
$\hat{\mathbf{P}}_{\mathbf{ref}}$
+
−
$\hat{\mathbf{P}}_{\mathbf{m}}$
$\mathbf{G}_{\mathbf{PSC}}(j\omega)$
$\hat{\theta}$
$\hat{\mathbf{P}}$
$\mathbf{G}_{\mathbf{P\theta}}(j\omega)$
Inner loops and grid impedance

Figure 3.8. Closed-loop active power control for GFM-VSCs. Source: [J3].

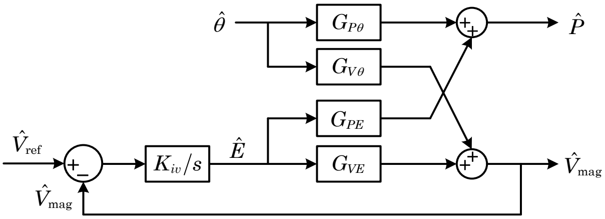

$\hat{\theta}$
$G_{P\theta}$
$G_{V\theta}$
G_{PE}
G_{VE}
+
+
$\hat{P}$
$\hat{V}_{\text{ref}}$
+
−
K_{iv}/s
$\hat{E}$
$\hat{V}_{\text{mag}}$
$\hat{V}_{\text{mag}}$

Figure 3.9. Plants of the active power and voltage magnitude controls. Source: [J3].

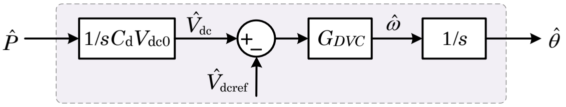

$\hat{P}$
$1/sC_{\text{d}}V_{\text{dc0}}$
$\hat{V}_{\text{dc}}$
+
−
$\hat{V}_{\text{dcref}}$
G_{DVC}
$\hat{\omega}$
$1/s$
$\hat{\theta}$

Figure 3.10. Small-signal model of the dc-link CPS/CPL and the single-loop DVSC. Source: [J1].

The active power at the PCC can be derived based on the equivalent circuit, given by

$$P=\frac{EV_g\sin\theta\left(Z_{\text{q}}+Z_{\text{gq}}\right)+\left(E^2-EV_g\cos\theta\right)\left(Z_{\text{d}}+Z_{\text{gd}}\right)}{\left(Z_{\text{d}}+Z_{\text{gd}}\right)^2+\left(Z_{\text{q}}+Z_{\text{gq}}\right)^2}. \tag{3.18}$$

The transfer function model from phase angle $\hat{\theta}$ to active power $\hat{P}$, under small perturbations, is derived as

$$\hat{P} = \underbrace{E_0 V_{\mathrm{g}0} \frac{\left(Z_{\mathrm{q}} + Z_{\mathrm{gq}}\right)\cos\theta_0 + \left(Z_{\mathrm{d}} + Z_{\mathrm{gd}}\right)\sin\theta_0}{\left(Z_{\mathrm{d}} + Z_{\mathrm{gd}}\right)^2 + \left(Z_{\mathrm{q}} + Z_{\mathrm{gq}}\right)^2}}_{G_{P\theta}} \cdot \hat{\theta}, \tag{3.19}$$

Figure 3.8 presents the closed-loop control of the active power for GFM-VSCs. $\mathbf{G_{PSC}}$ denotes the PSC dynamics. $\mathbf{G_{P\theta}}$ denotes the dynamics of the inner control loops and the grid impedance. Mapping $\mathbf{G_{PSC}}$ and $\mathbf{G_{P\theta}}$ with the complex torque equation (3.11), the frequency-domain power-angle relationships are expressed as

$$\begin{cases} \hat{\mathbf{P}}_{\mathbf{m}} = \dfrac{1}{\mathbf{G_{PSC}}\left(j\omega\right)} \cdot \hat{\theta} = K_m(\omega) \cdot \hat{\theta} + j\omega \cdot D_m(\omega) \cdot \hat{\theta} \\ \hat{\mathbf{P}} = \mathbf{G_{P\theta}}\left(j\omega\right) \cdot \hat{\theta} = K_e(\omega) \cdot \hat{\theta} + j\omega \cdot D_e(\omega) \cdot \hat{\theta} \end{cases}. \tag{3.20}$$

The control interactions and the damping for specific oscillation modes can be characterized through the analysis of 1/$\mathbf{G_{PSC}}$ and $\mathbf{G_{P\theta}}$ in the frequency domain, as indicated in (3.12).

Moreover, the complex torque coefficient-based analytical method can be extended to different controller forms of GFM-VSCs.

1) When considering the AVC dynamics, plants of the active power and the voltage magnitude controls are depicted in Figure 3.9. Transfer function models $G_{P\theta}$, $G_{V\theta}$, G_{PE}, and G_{VE} can be obtained from the equivalent circuit diagram in Figure 3.7 [82]. The transfer function model from $\hat{\theta}$ to $\hat{P}$ in Figure 3.8 is thus reformulated as

$$\hat{P} = \left(G_{P\theta} - G_{PE} \cdot \frac{K_{iv}/s}{1 + K_{iv}/s \cdot G_{VE}} \cdot G_{V\theta} \right) \cdot \hat{\theta} \tag{3.21}$$

2) When considering the dc-link dynamics, the small-signal model of the dc-link CPS/CPL and the single-loop DVSC is depicted in Figure 3.10 [J1]. The transfer function model G_{PSC} in Figure 3.8 can be replaced by

$$\hat{\theta} = \left(\frac{1}{s C_{\mathrm{d}} V_{\mathrm{dc}0}} \cdot G_{DVC} \cdot \frac{1}{s} \right) \cdot \hat{P} \tag{3.22}$$

3.3.3. CASE STUDY

The case study employs the virtual admittance and vector current control as inner control loops and the PSC as the outer control loop. The PSC incorporates a proportional controller K_{psc} and an LPF. K_{psc} is set to 0.1p.u. in this study, while the 3Hz and 100Hz LPFs are employed as two scenarios.

Figure 3.11 compares the complex torque plots under stiff (L_g=0.05p.u.) and weak grids (L_g=0.8p.u.), with R_v set to 0.1p.u., L_v set to 0.1p.u., k_{pi} set to 2p.u., and PSC employing a 3Hz LPF. The electrical damping torque D_e under the stiff grid is significantly lower than that under the weak grid. It indicates that the GFM-VSC exhibits a lower net damping when connecting to a stiff ac grid, thereby posing a higher risk of instability. As a result, subsequent case studies are conducted with L_g set to 0.05p.u.

Figure 3.12 presents the complex torque plots with various inner-loop parameters, where the damping for the SO and SSO issues are investigated. Figure 3.12(a) illustrates the impact of R_v on damping torques of the SO mode, with k_{pi} set to 2p.u., L_v set to 0.1p.u., and PSC using a 100Hz LPF. The mechanical complex torques are depicted by black lines, while blue and red lines represent electrical complex torques with R_v set to 0.05p.u. and 0.1p.u., respectively. It is shown that the condition $K_m + K_e = 0$ arises around the fundamental frequency, corresponding to the SO mode. In the case of R_v set to 0.05p.u., the net damping torque at the fundamental frequency is negative, i.e., $D_m + D_e < 0$, indicating the occurrence of the SO issue. In contrast, as R_v transitions to 0.1p.u., the net damping torque exhibits a positive value, i.e., $D_m + D_e > 0$, which thus means that the SO issue is mitigated.

Figure 3.12(b) illustrates the impact of R_v on the SSO-mode damping torques, with k_{pi} set to 2p.u., L_v set to 0.1p.u., and PSC adopting a 3Hz LPF. In this scenario, $K_m + K_e = 0$ is observed within sub-synchronous frequencies, corresponding to the SSO mode. The net damping torque is positive when R_v is set to 0.05p.u., i.e., $D_m + D_e > 0$. However, it turns negative as R_v transitions to 0.1p.u., indicating the occurrence of the SSO issue. The analysis of Figure 3.12(a)-(b) reveals that R_v enhances the damping of SO issue while compromising the damping of SSO issue.

Figure 3.12(c) depicts complex torque plots with different L_v, with k_{pi} set to 2p.u., R_v set to 0.1p.u., and PSC adopting a 3Hz LPF. Blue and red lines represent the electrical complex torques with L_v set to 0.2p.u. and 0.1p.u., respectively. It is evident that as L_v shifts from 0.2p.u. to 0.1p.u., the electrical damping torque D_e is diminished within sub-synchronous frequencies, while D_e at the fundamental frequency remains little affected. As a result, the net damping torque $D_m + D_e$ becomes negative at the SSO-mode frequency, implying the occurrence of the SSO issue. The analysis reveals that L_v enhances the damping of the SSO issue while exhibiting negligible influence on the damping of the SO issue.

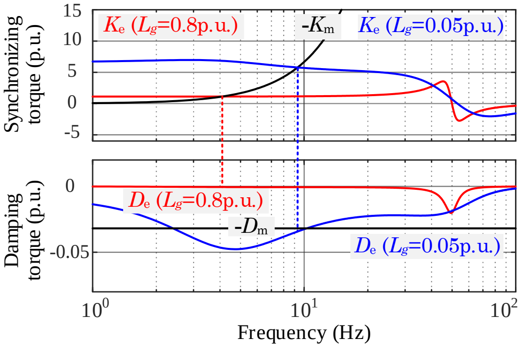
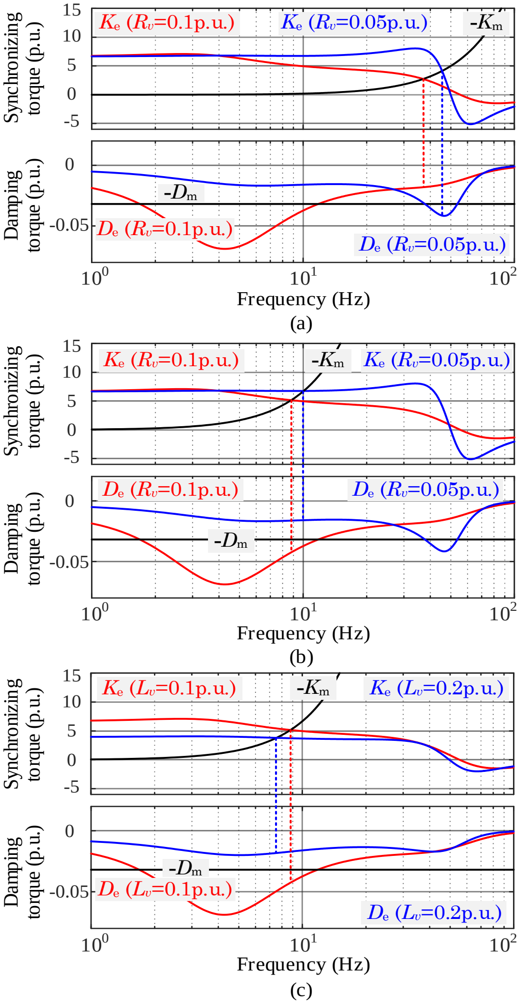


Figure 3.11. Complex torque plots under stiff and weak grids. Source: [J3].



(a)

(b)

(c)

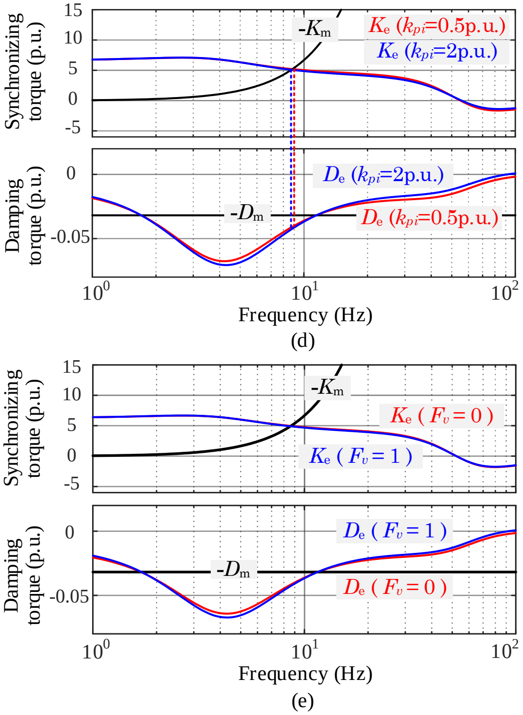


Figure 3.12. Complex torque plots with various inner-loop parameters. (a) Different R_v, with PSC employing a 100Hz LPF. (b) Different R_v, with PSC employing a 3Hz LPF. (c) Different L_v. (d) Different k_{pi}. (e) Different F_v. Source: [J3].

Figure 3.12(d)-(e) illustrate the complex torque plots with different k_{pi} and F_v, with L_v set to 0.1p.u., R_v set to 0.1p.u., and PSC employing a 3Hz LPF. It is demonstrated that when increasing k_{pi} from 0.5 p.u. to 2 p.u., the electrical damping torque D_e of the SO mode increases, while D_e of the SSO mode exhibits a slight reduction. A similar effect can be obtained in the case of F_v set to 1. Nevertheless, it is noteworthy that the influences of k_{pi} and F_v are not as significant as the effects of R_v and L_v.

Moreover, the accuracy of the complex torque plots is validated through the measured complex torques using the frequency scan method. The measurement results are detailed in [J3].

Based on the analytical results of impedance profiles and complex torque profiles, parameter tuning guidelines for the inner control loops are developed as follows:

1) Setting a high bandwidth for the vector current controller and utilizing the voltage decoupling control are recommended. Those measures aim to mitigate the undesired interaction between virtual admittance and vector current control.

2) The tuning of R_v is intended to provide active damping for the SO mode. It is evident that R_v has an adverse effect on the SSO-mode damping, while it can be addressed by tuning L_v.

3) The tuning of L_v aims to provide active damping for the SSO mode. Meanwhile, the adverse impact of R_v can be compensated.

Following the above guidelines, the parameters of inner control loops in this study are set as k_{pi}=2p.u., F_v=1, R_v=0.1p.u., and $L_v \geq$0.2p.u. With those settings, the GFM-VSC can effectively dampen the SSO and SO issues. Notably, the instability issues are affected by both outer and inner loops. The well-tuned inner control loops essentially provide a stable operation range within which the outer-loop parameters can be regulated.

3.4. EXPERIMENTAL RESULTS

The experimental tests are performed based on the setup in Figure 2.16, while a constant dc-link voltage is provided by Converter 1#. The parameters of the studied GFM-VSC and their values are detailed in Table 3.1. Waveforms of PCC voltage $\mathbf{v}$, ac current $\mathbf{i}$, active power P, and reactive power Q are demonstrated.

Table 3.1. Circuit and Control Parameters of the Studied GFM-VSC. Source: [J3].

Symbol	Description	Value (p.u.)
P_0	Rated power	3kW (1 p.u.)
v_g	RMS value of grid voltage	110V/50Hz (1 p.u.)
V_{ref}	Rated voltage reference	110V (1 p.u.)
ω_1	Nominal angular frequency	100π rad/s (1 p.u.)
L_{g}	Grid impedance	0.05 p.u.
L_{f}	Filter inductor	0.078 p.u.
R_v	Virtual resistance	0.05-0.12 p.u.
L_v	Virtual inductance	0.1-0.3 p.u.
K_{PSC}	PSC proportional gain	0.1 p.u.
K_{iv}	AVC integral gain	50 p.u.
k_{pi}	Proportional gain of vector current control	0.5-3 p.u.
k_{ri}	Resonant gain of current vector control	0.4 p.u.
ω_r	Resonant cut-off frequency of vector current control	2π rad/s
T_d	Control time delay	150 μs

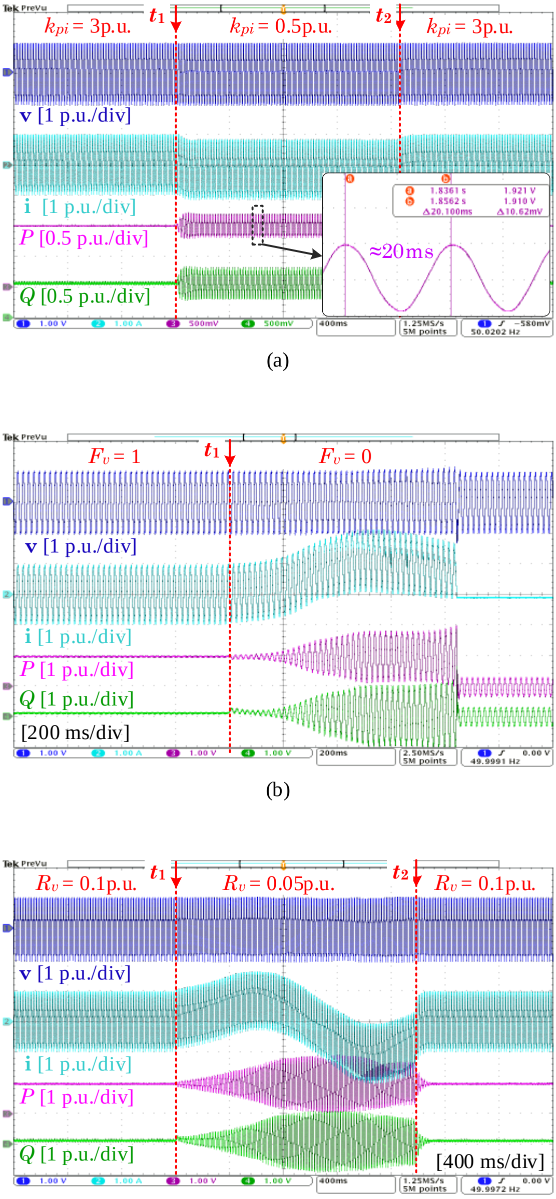


Figure 3.13. Dynamics of the SO mode with different inner-loop parameters. (a) Different k_{pi}. (b) Different F_v. (c) Different R_v. Source: [J3], [C3].

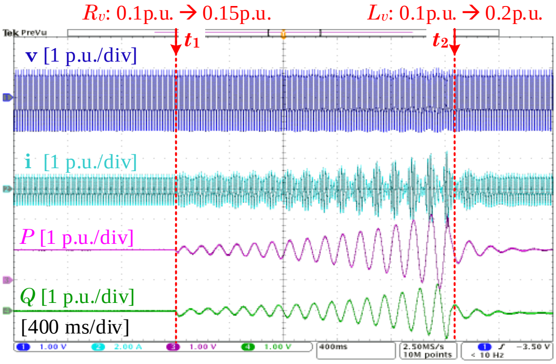


Figure 3.14. Dynamics of the SSO mode with different inner-loop parameters. Source: [J3].

Figure 3.13 shows the SO-mode dynamics of the GFM-VSC with different inner-loop parameters. Figure 3.13(a) illustrates the dynamic effect of k_{pi}. It is shown that the GFM-VSC remains stable when k_{pi} is set to 3p.u., while it experiences the SO issue as k_{pi} switches to 0.5p.u. at $\boldsymbol{t_1}$. The SO issue manifests as dc components in the waveform of $\mathbf{i}$, along with fundamental-frequency resonances in waveforms of P and Q. The results validate that increasing k_{pi} of the vector current control enhances the damping for the SO mode.

Figure 3.13(b) demonstrates the dynamic effect of F_v. Note that K_{psc} in this test is set at 0.17p.u., which results in a worse damping impact for the SO issue [18], [57]. It is shown that the GFM-VSC suffers from the SO issue after F_v switching to 0 at $\boldsymbol{t_1}$. DC components arise in the waveform of $\mathbf{i}$, whereas the resonances at the fundamental frequency occur in waveforms of P and Q. The results confirm the enhanced SO-mode damping with the voltage decoupling control.

Figure 3.13(c) illustrates the dynamic effect of R_v. It is shown that the SO issue arises in the GFM-VSC as R_v is decreased to 0.05p.u. The waveform of $\mathbf{i}$ exhibits ultra-low-frequency oscillations, while waveforms of P and Q demonstrate fundamental-frequency oscillations. Subsequently, such instability issue is mitigated when R_v is set back to 0.1p.u. The results confirm the enhanced SO-mode damping with a large R_v.

Figure 3.14 demonstrates the SSO-mode dynamics with different inner-loop parameters. It is shown that the GFM-VSC experiences the SSO issue as R_v shifts from 0.1p.u. to 0.15p.u., where waveforms of $\mathbf{v}$, $\mathbf{i}$, P, and Q exhibit divergent oscillations within sub-synchronous frequencies. Subsequently, the SSO issue is effectively mitigated by increasing L_v from 0.1p.u. to 0.2p.u. The results confirm that the damping of the SSO issues is jeopardized by R_v, while it is enhanced by L_v.

3.5. SUMMARY

In this chapter, an analytical approach is proposed to assess the influence of inner control loops on the damping of GFM-VSCs.

1) The characteristics of inner control loops are described by an impedance model. The low-frequency resistance component of the impedance model serves as the indicator of the damping effect on the SO issue.

2) The complex torque coefficient method employed for GFM-VSCs identifies the oscillation modes via synchronizing torques and assesses the stability through the net damping torque. Inner-loop control dynamics influence the damping torque, thereby establishing a stable operational range within which the outer-loop parameters can be regulated.

3) Analyses of the virtual admittance and vector current control illustrate that R_v improves the damping of the SO issue while simultaneously compromising the damping of the SSO issue. L_v, conversely, enhances the damping of the SSO issue with negligible impact on the SO issue. Moreover, increasing the proportional gain of vector current control and utilizing the voltage decoupling control enhances the damping of the SO issue. Parameters of inner control loops are tuned to mitigate both SO and SSO issues.

CHAPTER 4. IMPEDANCE-BASED EXTERNAL INTERACTIONS ANALYSIS

The content of this chapter is based on publications [J4] and [C1].

4.1. INTRODUCTION

Chapters 2-3 have discussed both the outer and inner control loops of GFM-VSCs. Besides the control strategies, the external interactions of GFM-VSCs with both ac networks and dc-link sources/loads are of critical concern. Table 1.1 lists different sources and loads that are commonly interconnected with VSCs on the dc bus [41], [42], [60]-[64]. It is evident that those sources and loads can influence the dynamics of the GFM-VSC, which, however, have not been revealed.

The impedance method characterizes the dynamics of VSCs at their ac or dc terminals, which serves as a promising approach for analyzing external interactions. The dc-link impedance can reveal the interaction between GFM-VSCs and their dc-link connections [65]. It is reported that the CPL exhibits a negative-resistance characteristic and negatively affects the system stability [41], whereas the CRL demonstrates a positive resistance. However, the dynamics of the GFM-VSC, when interacting with different dc-link connections, remains unclear.

In addition to interactions via the dc link, GFM-VSCs also interface with ac systems through the PCC. The ac impedance matrix can characterize the interactions between VSCs and ac systems [66]-[68]. It is reported in [36] and [37] that when the GFM-VSC incorporates the dc-link voltage regulation, its ac impedance matrix demonstrates a negative real part in the *d-d* channel, making the GFM-VSC exhibit CPL behavior at the ac side. Yet, those studies primarily emphasize the DVSC strategies while overlooking the diversity of the dc-link connections. Consequently, the influences of sources and loads interconnected via the dc link on the ac impedance characteristics and their stability impact remain unresolved issues.

To fill the research gaps, this Chapter analyzes the external interactions of GFM-VSCs with dc and ac subsystems [J4]. Firstly, dc-link impedances reveal the interactions between different dc-link loads and the GFM-VSC. Subsequently, ac impedance-based analyses are conducted to assess the effects of dc-link sources and loads on ac impedance characteristics and their interaction with ac grids. Finally, the worst-case operation scenarios for different dc-link connections are identified under both rectifier and inverter modes.

4.2. DESCRIPTION OF MAIN CIRCUIT AND CONTROL SYSTEM

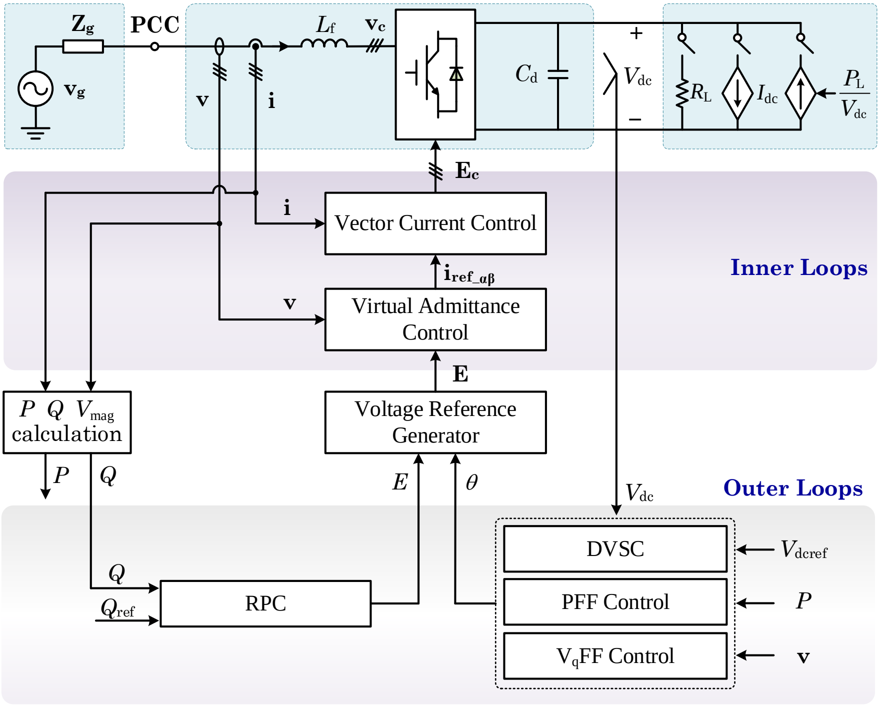

Zg
PCC
Lf
vc
vg
v
i
Cd
+
Vdc
−
RL
Idc
PL / Vdc
Ec
i
Vector Current Control
iref_αβ
Inner Loops
v
Virtual Admittance Control
E
P Q Vmag calculation
Voltage Reference Generator
P
Q
E
θ
Vdc
Outer Loops
DVSC
Vdcref
Q
Qref
RPC
PFF Control
P
VqFF Control
v

Figure 4.1. Main circuit and control diagrams of the studied GFM-VSC. Source: [J4].

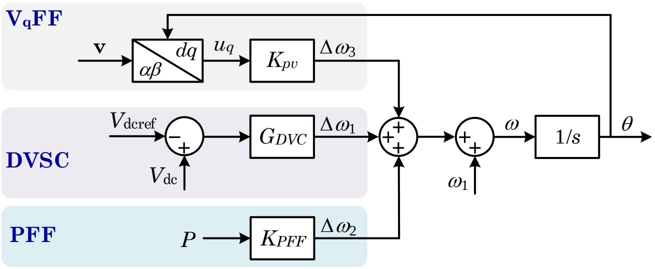

VqFF
v
dq
αβ
uq
Kpv
Δω3
Vdcref
−
+
GDVC
Δω1
DVSC
Vdc
ω
1/s
θ
ω1
PFF
P
KPFF
Δω2

Figure 4.2. Block diagram of the flexible synchronization control. Source: [C1].

Figure 4.1 depicts the diagrams of the studied GFM-VSC [J4]. The variables are clarified in Chapter 2.2. Different dc-link sources and loads are illustrated in Table 1.1. The parameters of the studied GFM-VSC are presented in Table 4.1.

Figure 4.2 shows the flexible synchronization control that is proposed in Chapter 2 [C1], which consists of paralleled DVSC, PFF, and V_qFF loops. Different types of

DVSC methods can be derived by enabling and disabling specific control loops, leading to the following options:

1) Single-loop DVSC method [J1], as shown in Figure 2.2.
2) DVSC+PFF method [J1], as shown in Figure 2.6.
3) DVSC+V_qFF method [J2], as shown in Figure 2.12.

Table 4.1. Circuit and Control Parameters of the Studied GFM-VSC. Source: [J4].

Symbol	Description	Value (p.u.)
P_0	Rated power	3kW (1 p.u.)
v_g	RMS value of grid voltage	110V (1 p.u.)
ω_1	Nominal angular frequency	100π rad/s (1 p.u.)
V_{dcref}	DC-link voltage reference	400V (3.64 p.u.)
L_{f}	Filter inductor	3mH (0.078 p.u.)
C_{d}	DC-link capacitor	1.45mF (5.7 p.u.)
K_p	Proportional gain of DVSC	0.25 p.u.
K_i	Integral gain of DVSC	0.5 p.u.
Q_{ref}	Reactive power reference	0
E_0	Rated magnitude of EMF	1 p.u.
k_q	RPC droop coefficient	0.1 p.u.
R_v	Virtual resistance	0.1 p.u.
L_v	Virtual inductance	0.15 p.u.
k_{pi}	Proportional gain of vector current control	1.5 p.u.
k_{ri}	Resonant gain of vector current control	0.5 p.u.
T_d	Control time delay	150 μs

4.3. DC-LINK IMPEDANCE-BASED DYNAMICS ANALYSIS

4.3.1. DC-LINK IMPEDANCE ANALYSIS BASICS

Figure 4.3 illustrates the interconnected system represented by dc-link impedances. The system includes the load subsystem and the source subsystem, which are interconnected through the dc link [65]. The load subsystem refers to dc-link sources and loads, with Z_{Source} and Z_{Load} representing their dynamics. The source subsystem refers to the ac grid and the GFM-VSC, with the dc-link impedance Z_{dc} representing their dynamics. The dc-link voltage of this interconnected system is expressed as

$$V_{\mathrm{dc}} = \frac{V}{1 + Z_{\mathrm{dc}} / Z_{\mathrm{Load}}} \quad \text{or} \quad V_{\mathrm{dc}} = \frac{V}{1 + Z_{\mathrm{dc}} / Z_{\mathrm{Source}}}. \tag{4.1}$$

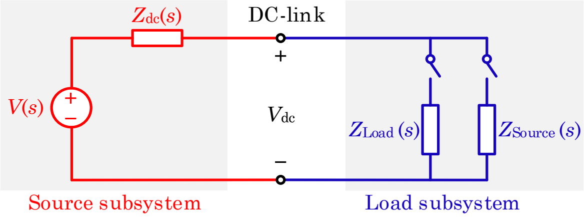

$Z_{\mathrm{dc}}(s)$
DC-link
$V(s)$
+
V_{dc}
−
$Z_{\mathrm{Load}}(s)$
$Z_{\mathrm{Source}}(s)$
Source subsystem
Load subsystem

Figure 4.3. Interconnected system represented by dc-link impedances. Source: [J4].

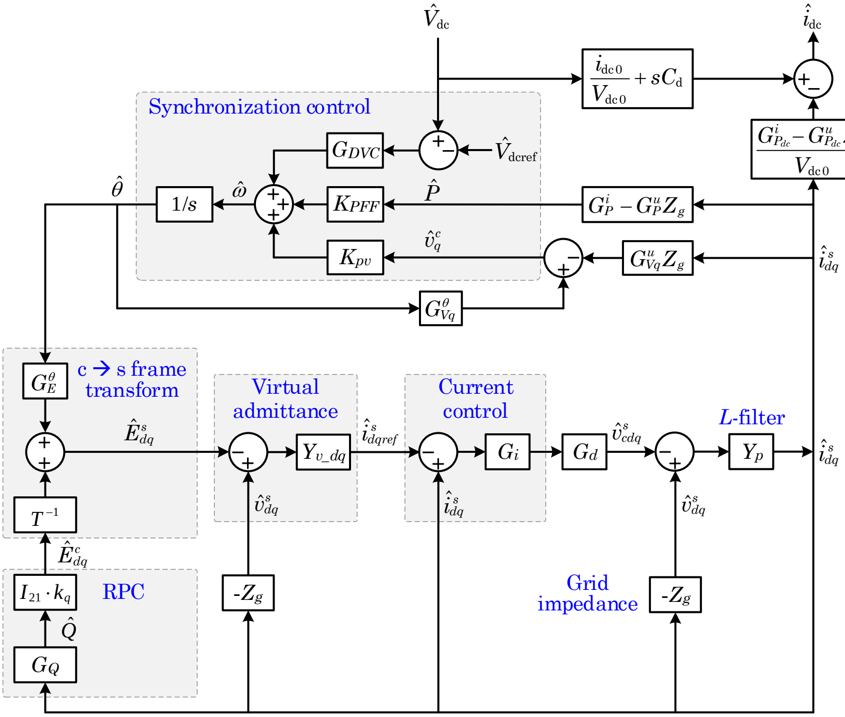

$\hat{V}_{\mathrm{dc}}$
$\hat{i}_{\mathrm{dc}}$
$\frac{i_{\mathrm{dc}0}}{V_{\mathrm{dc}0}}+sC_{\mathrm{d}}$
Synchronization control
G_{DVC}
$\hat{V}_{\mathrm{dcref}}$
$\frac{G^{i}_{P_{dc}}-G^{u}_{P_{dc}}Z_g}{V_{\mathrm{dc}0}}$
$\hat{\theta}$
$1/s$
$\hat{\omega}$
K_{PFF}
$\hat{P}$
$G^{i}_{P}-G^{u}_{P}Z_g$
K_{pv}
$\hat{v}^{c}_{q}$
$G^{u}_{Vq}Z_g$
$\hat{i}^{s}_{dq}$
G^{θ}_{Vq}
G^{θ}_{E}
c → s frame transform
$\hat{E}^{s}_{dq}$
Virtual admittance
Y_{v_dq}
$\hat{i}^{s}_{dqref}$
Current control
G_i
G_d
$\hat{v}^{s}_{cdq}$
L-filter
Y_p
$\hat{i}^{s}_{dq}$
$\hat{v}^{s}_{dq}$
$\hat{i}^{s}_{dq}$
$\hat{v}^{s}_{dq}$
T^{-1}
$\hat{E}^{c}_{dq}$
$I_{21}\cdot k_q$
RPC
$\hat{Q}$
G_Q
$-Z_g$
Grid impedance
$-Z_g$

Figure 4.4. DC-link impedance model of the studied GFM-VSC. Source: [J4].

The minor loop gains, expressed as $Z_{\mathrm{dc}}/Z_{\mathrm{Load}}$ and $Z_{\mathrm{dc}}/Z_{\mathrm{Source}}$, refer to the impedance ratios between source and load subsystems. Those impedance ratios can reflect the system stability using the Nyquist stability criterion [65].

Figure 4.4 illustrates the impedance model of the studied GFM-VSC on the dc side. Modeling of the control system and main circuit is detailed in Section 2.3. The transfer function model of Z_{dc} is derived as

$$Z_{\mathrm{dc}} = -\frac{\hat{V}_{\mathrm{dc}}}{\hat{i}_{\mathrm{dc}}} = \left(\frac{i_{\mathrm{dc}0}}{V_{\mathrm{dc}0}} + sC_{\mathrm{d}} + Y_{\mathrm{dc}1} \right)^{-1} \tag{4.2}$$

$$\begin{cases} Y_{\mathrm{dc}1} = \left(G^{i}_{P_{dc}} - G^{u}_{P_{dc}} Z_g \right) \Big/ V_{dc0} \cdot T_1 G_d Y_{v\_dq} G^{\theta}_{E} \left(s - G^{\theta}_{Vq} \right)^{-1} \cdot G_{DVC} \\ T_1 = \left[Z_p + Z_g + G_d T_2 + G_d G_i Y_{v\_dq} G^{\theta}_{E} \left(s - G^{\theta}_{Vq} \right)^{-1} \cdot \left(G^{i}_{P} - G^{u}_{P} Z_g - G^{u}_{Vq} Z_g \right) \right]^{-1} \\ T_2 = G_i + G_i Z_g + G_i Y_{v\_dq} T^{-1} I_{21} k_q \left(G^{i}_{Q} - G^{u}_{Q} Z_g \right) \end{cases} \tag{4.3}$$

4.3.2. DYNAMICS WITH DIFFERENT DC-LINK LOADS

The dc-link loads considered in this study are listed as follows.

1) CPL, where the impedance model is derived as

$$\left(V_{\mathrm{dc}0} + \hat{V}_{\mathrm{dc}} \right) \cdot \left(i_{\mathrm{dc}0} + \hat{i}_{\mathrm{dc}} \right) = P_{\mathrm{L}} \quad \Rightarrow \quad Z_{\mathrm{CPL}} = \frac{\hat{V}_{\mathrm{dc}}}{\hat{i}_{\mathrm{dc}}} = -\frac{V_{\mathrm{dc}0}}{i_{\mathrm{dc}0}} \tag{4.4}$$

with P_{L} denoting the CPL. $V_{\mathrm{dc}0}$ and $i_{\mathrm{dc}0}$ represent the operating points of the dc-link voltage and current, respectively.

2) CRL, where the impedance model is expressed as

$$V_{\mathrm{dc}0} + \hat{V}_{\mathrm{dc}} = \left(i_{\mathrm{dc}0} + \hat{i}_{\mathrm{dc}} \right) \cdot R_{\mathrm{L}} \quad \Rightarrow \quad Z_{\mathrm{CRL}} = \frac{\hat{V}_{\mathrm{dc}}}{\hat{i}_{\mathrm{dc}}} = R_{\mathrm{L}} = \frac{V_{\mathrm{dc}0}}{i_{\mathrm{dc}0}}, \tag{4.5}$$

with R_{L} denoting the CRL.

3) CIL, where the impedance model is expressed as

$$Z_{\mathrm{CIL}} = \left. \frac{\hat{V}_{\mathrm{dc}}}{\hat{i}_{\mathrm{dc}}} \right|_{\hat{i}_{\mathrm{dc}}=0} = \infty \tag{4.6}$$

By comparing (4.4) and (4.5), it is observed that $Z_{\mathrm{CPL}} = -Z_{\mathrm{CRL}}$ can be achieved when the operating points $V_{\mathrm{dc}0}$ and $i_{\mathrm{dc}0}$ for CRL and CPL are the same. Consequently, when a CRL and a CPL are configured in parallel, their dc link impedance can be expressed as

$$Z_{\mathrm{CRL}} \,//\, Z_{\mathrm{CPL}} = \infty \quad \leftrightarrow \quad Z_{\mathrm{CIL}} , \tag{4.7}$$

which is an infinite value and thus equals Z_{CIL}. This impedance relationship indicates that the same behavior can be demonstrated with the CIL and the paralleled CPL+CRL, given the same operating points $i_{\mathrm{dc}0}$ and $V_{\mathrm{dc}0}$. Consequently, the dynamics of the GFM-VSC loaded by a CIL fall between those loaded by a CPL and a CRL.

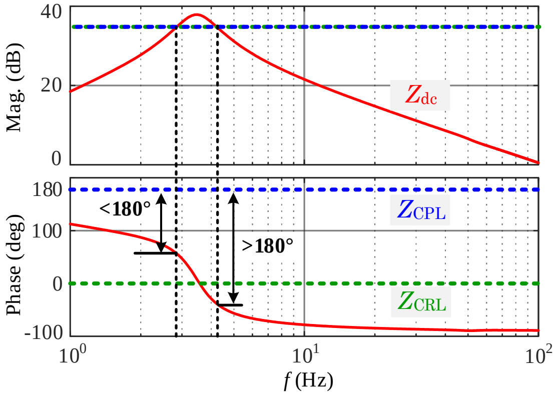


Figure 4.5. Bode plots of Z_{dc}, Z_{CPL}, and Z_{CRL}. Source: [J4].

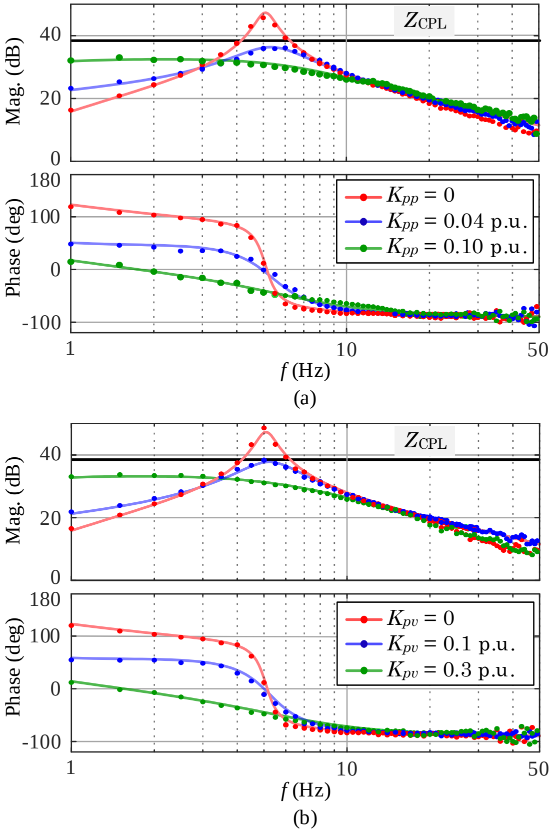


Figure 4.6. Bode plots of Z_{dc} with different synchronization methods. (a) With the DVSC+PFF method. (b) With the DVSC+V_qFF method. Source: [J4].

Figure 4.5 shows Bode plots of Z_{dc}, Z_{CPL}, and Z_{CRL}, where the GFM-VSC employs the single-loop DVSC method. Red lines refer to Z_{dc}, while blue and green dot lines refer to Z_{CPL} and Z_{CRL}, respectively. Both the theoretical and the experimentally measured dc-link impedance profiles are presented, thus confirming the effectiveness of the impedance model. It is illustrated that the magnitude Bode plots of Z_{dc}, Z_{CPL}, and Z_{CRL} intersect at low frequencies. The stability is determined by the phase differences in the frequency range where $\left|Z_{\mathrm{dc}}\right| > \left|Z_{\mathrm{CRL}}\right|$ and $\left|Z_{\mathrm{dc}}\right| > \left|Z_{\mathrm{CPL}}\right|$. Specifically, the phase difference between Z_{dc} and Z_{CPL} surpasses 180° in the frequency range where $\left|Z_{\mathrm{dc}}\right| > \left|Z_{\mathrm{CPL}}\right|$, thereby indicating the existence of RHP poles. The LFO issue thus arises with the GFM-VSC. Conversely, the phase difference between Z_{dc} and Z_{CRL} remains below 180° in the frequency range where $\left|Z_{\mathrm{dc}}\right| > \left|Z_{\mathrm{CRL}}\right|$, thus denoting a stable operation. The comparative analyses thus illustrate that the CPL poses the highest risk of instability among dc-link loads, whereas the CRL demonstrates the most favorable behavior.

To mitigate the LFO issues arising from the interaction between GFM-VSC and CPL, the flexible synchronization control is employed to shape the dc-link impedance. Figure 4.6 illustrates Bode plots of Z_{dc} using the DVSC+PFF and DVSC+$\mathrm{V_q}$FF methods. Experimental impedance measurements confirm the theoretical impedance profiles. It is shown that those two synchronization methods exhibit comparable impedance-shaping effects. When increasing K_{pp} of the PFF control and K_{pv} of the $\mathrm{V_q}$FF control, the peak value of Z_{dc} in the magnitude plots is reduced significantly, subsequently preventing intersections with the magnitude plot of Z_{CPL}. Therefore, the DVSC+PFF and the DVSC+$\mathrm{V_q}$FF methods stabilize the GFM-VSC loaded by a CPL.

4.4. AC IMPEDANCE-BASED DYNAMICS ANALYSIS

4.4.1. AC IMPEDANCE ANALYSIS BASICS

Figure 4.7 illustrates the interconnected system that is represented by ac impedance matrices. The system includes the load subsystem and the source subsystem, which are interconnected at the PCC [68], [83]. The load subsystem refers to the GFM-VSC and dc-link sources and loads, with ac impedance matrix Z_{ac} characterizing their dynamics. The source subsystem refers to the ac grid, with Z_g representing its dynamics. The PCC voltage of this interconnected system is expressed as

$$v_{dq} = \frac{Z_{ac} \cdot Z_g^{-1}}{I + Z_{ac} \cdot Z_g^{-1}} \cdot v_{gdq} + \frac{I}{I + Z_{ac} \cdot Z_g^{-1}} \cdot V_o \,, \tag{4.8}$$

where I denote the identity matrix. The minor loop gains, expressed as $Z_{ac} \cdot Z_g^{-1}$, refer to the impedance ratio between load and source subsystems [68]. The system stability can be assessed through closed-loop poles by solving

$$L = \det\left(I + Z_{ac} \cdot Z_g^{-1}\right) = 0 \,. \tag{4.9}$$

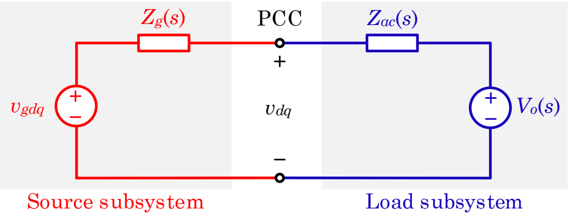


Figure 4.7. Interconnected system represented by ac impedance model. Source: [J4].

4.4.2. DYNAMICS WITH DIFFERENT DC-LINK LOADS

When GFM-VSCs operate in the rectifier mode, the dynamics of different loads connected at the dc link are represented as follows.

1) CPL, where the transfer function model from $\hat{P}_{\mathrm{dc}}$ to $\hat{V}_{\mathrm{dc}}$ is given by

$$P_{\mathrm{dc}} = C_{\mathrm{d}} \cdot V_{\mathrm{dc}} \cdot \frac{dV_{\mathrm{dc}}}{dt} + P_{\mathrm{L}} \quad \Rightarrow \quad G_{dc\_\mathrm{CPL}} = \frac{\hat{V}_{\mathrm{dc}}}{\hat{P}_{\mathrm{dc}}} = \frac{1}{s C_{\mathrm{d}} V_{\mathrm{dc}0}}, \tag{4.10}$$

with P_{L} representing the CPL.

2) CIL, where the transfer function model from $\hat{P}_{\mathrm{dc}}$ to $\hat{V}_{\mathrm{dc}}$ is given by

$$P_{\mathrm{dc}} = C_{\mathrm{d}} \cdot V_{\mathrm{dc}} \frac{dV_{\mathrm{dc}}}{dt} + V_{\mathrm{dc}} \cdot I_{\mathrm{L}} \quad \Rightarrow \quad G_{dc\_\mathrm{CIL}} = \frac{\hat{V}_{\mathrm{dc}}}{\hat{P}_{\mathrm{dc}}} = \frac{1}{s C_{\mathrm{d}} V_{\mathrm{dc}0} + I_{\mathrm{L}}}, \tag{4.11}$$

with I_{L} representing the CIL.

3) CRL, where the transfer function model from $\hat{P}_{\mathrm{dc}}$ to $\hat{V}_{\mathrm{dc}}$ is given by

$$P_{\mathrm{dc}} = C_{\mathrm{d}} V_{\mathrm{dc}} \frac{dV_{\mathrm{dc}}}{dt} + \frac{V_{\mathrm{dc}}^2}{R_{\mathrm{L}}} \quad \Rightarrow \quad G_{dc\_\mathrm{CRL}} = \frac{\hat{V}_{\mathrm{dc}}}{\hat{P}_{\mathrm{dc}}} = \frac{1}{s C_{\mathrm{d}} V_{\mathrm{dc}0} + 2 V_{\mathrm{dc}0} / R_{\mathrm{L}}}, \tag{4.12}$$

with R_{L} representing the CRL.

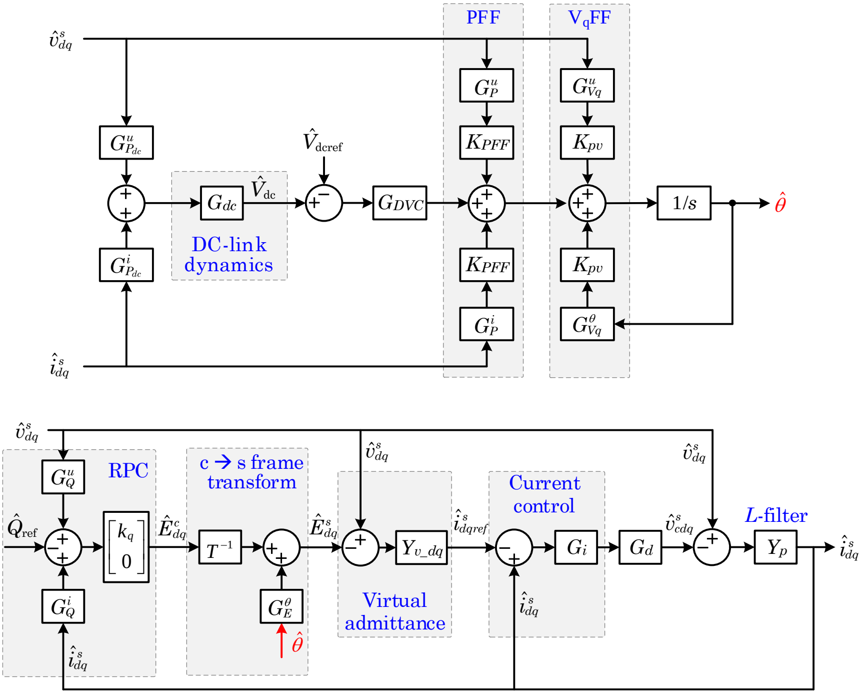

PFF
V$_q$FF
$\hat{v}^s_{dq}$
$G^u_{P_{dc}}$
$G^i_{P_{dc}}$
$\hat{i}^s_{dq}$
G_{dc}
$\hat{V}_{dc}$
DC-link dynamics
$\hat{V}_{dcref}$
G_{DVC}
G^u_P
K_{PFF}
G^i_P
G^u_{Vq}
K_{pv}
G^θ_{Vq}
1/s
$\hat{\theta}$
RPC
G^u_Q
$\hat{Q}_{ref}$
k_q
0
G^i_Q
$\hat{E}^c_{dq}$
c → s frame transform
T^{-1}
G^θ_E
$\hat{E}^s_{dq}$
Y_{v_dq}
Virtual admittance
$\hat{i}^s_{dqref}$
Current control
G_i
G_d
$\hat{v}^s_{cdq}$
L-filter
Y_p
$\hat{i}^s_{dq}$

Figure 4.8. AC impedance model of the studied GFM-VSC. Source: [J4].

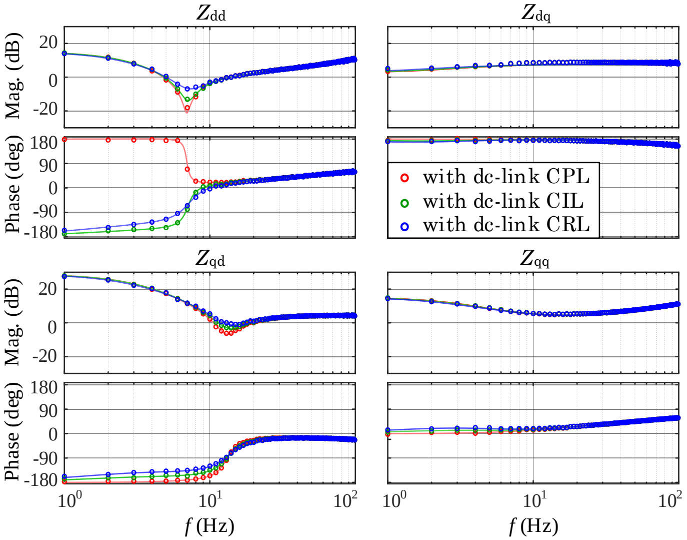


Figure 4.9. Bode plots of Z_{ac} with different dc-link loads. Source: [J4].

Figure 4.8 depicts the ac impedance model of the GFM-VSC. Modeling of the control system and main circuit is detailed in Section 2.3. The transfer function matrix of Z_{ac} is derived as

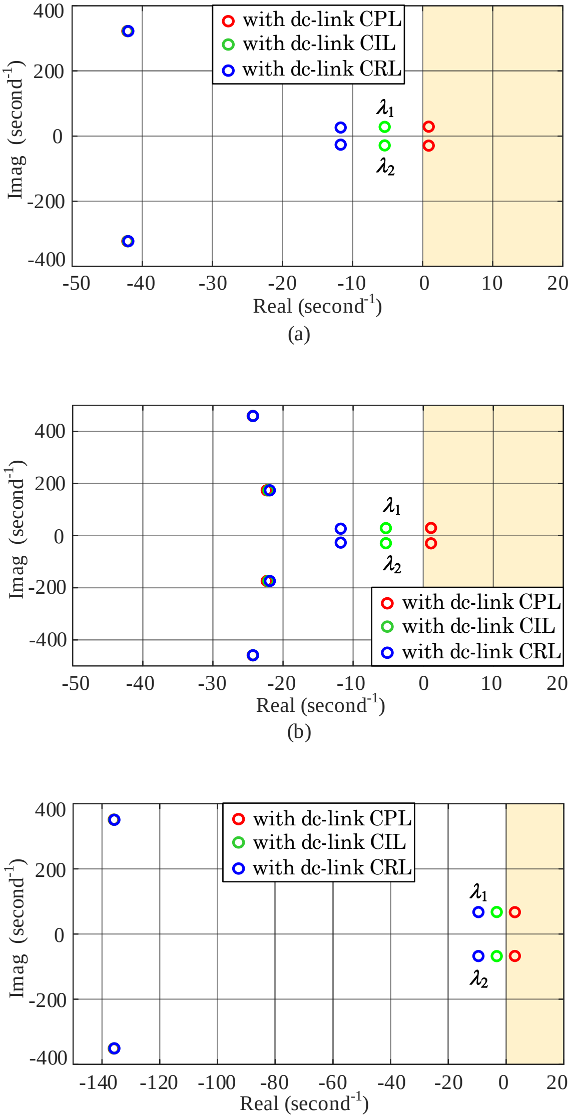
$$\begin{cases} Z_{ac}=\begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix}=\dfrac{\hat{v}_{dq}^{s}}{\hat{i}_{dq}^{s}}=T_3^{-1}\left(Z_p+T_4\right) \\ T_3=I_2-G_dG_iY_{v\_dq}\left[T^{-1}I_{21}k_qG_Q^u+G_E^\theta\Big/\left(s-G_{Vq}^\theta\right)\left(G_P^u+G_{Vq}^u-G_{DVC}G_{dc}G_{P_{dc}}^u\right)-I_2\right] \\ T_4=G_dG_i\left[I_2+Y_{v\_dq}T^{-1}I_{21}k_qG_Q^i+Y_{v\_dq}G_E^\theta\cdot\left(s-G_{Vq}^\theta\right)^{-1}\left(G_P^i-G_{DVC}G_{dc}G_{P_{dc}}^i\right)\right] \end{cases} \tag{4.13}$$

where Z_{dd}, Z_{dq}, Z_{qd}, and Z_{qq} denote the *d-d* channel, *d-q* channel, *q-d* channel, and *q-q* channel impedances of the ac impedance matrix, respectively.

Figure 4.9 shows the Bode plots of Z_{ac} with different loads connected through the dc link, where the GFM-VSC employs the single-loop DVSC method. The red lines represent Z_{ac} of the GFM-VSC loaded by CPL, the blue lines correspond to Z_{ac} with dc-link CIL, and the green lines refer to Z_{ac} with dc-link CRL. Both the theoretically calculated and experimentally measured ac impedance profiles are presented, thereby validating the effectiveness of the impedance model. It is shown that Z_{dd} exhibits a negative real component within low frequencies, which is due to the incorporated dc-link voltage regulation with GFM-VSCs [69], [70]. Yet, as the load connected through the dc link transitions from CPL to CIL and subsequently to CRL, the frequency range where Z_{dd} exhibits a negative real part becomes narrower. Meanwhile, the initially inductive imaginary part of Z_{dd} transforms into capacitive behavior with load variations. Additionally, Z_{qd} demonstrates a decreased frequency range of negative real parts during the load transition of CPL, CIL, and CRL.

The presence of a negative real part exhibited in Z_{ac} may result in instability issues when GFM-VSCs interact with ac grids. To assess the system stability associated with the ac-side interactions, closed-loop poles obtained from (4.9) are analyzed. Different ac grid conditions are considered in this study, listed as follows:

1) Inductive stiff grid, where the inductor L_g is set to 0.15p.u.
2) Inductive weak grid, where L_g is set to 0.85p.u.
3) Series-compensated weak grid [84], where L_g is set to 1p.u., and the capacitor C_g is set to 5p.u.

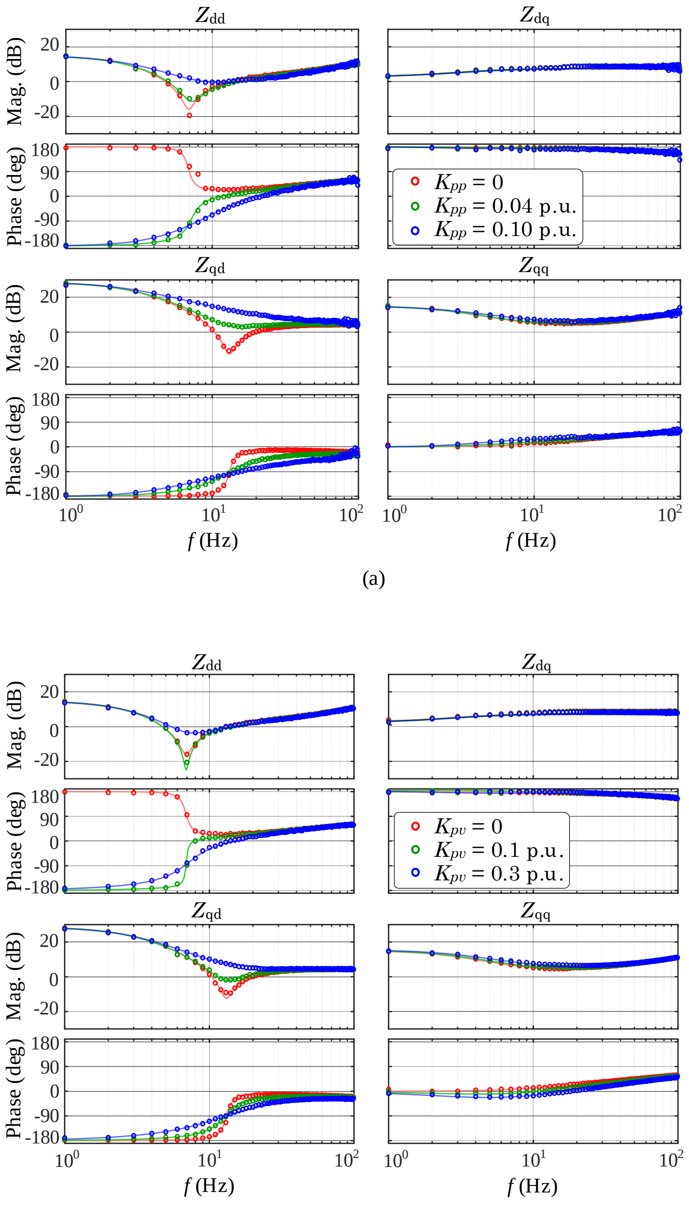


(a)

(b)

(c)

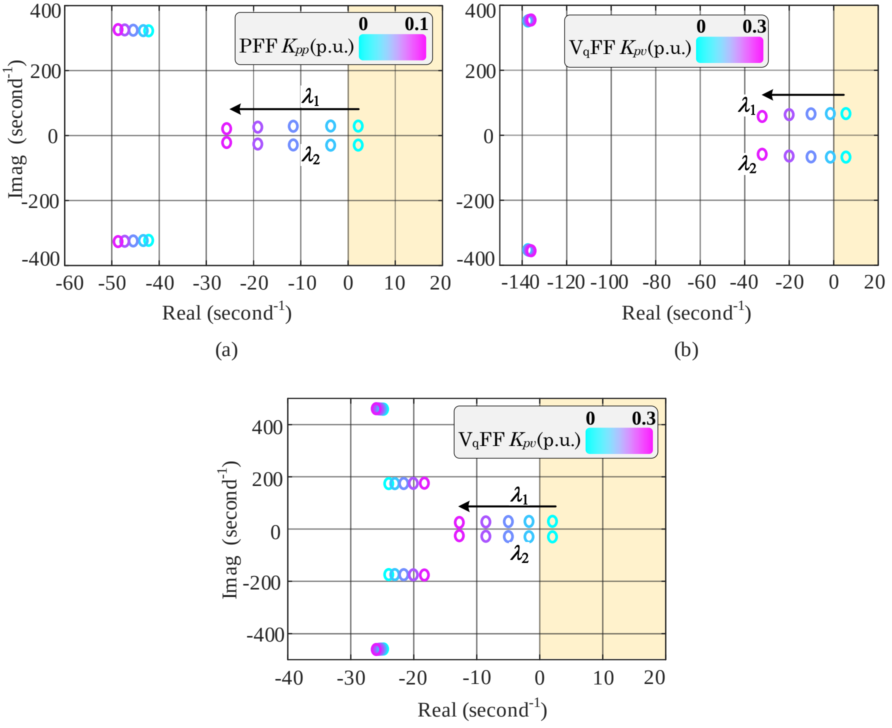
Figure 4.10. Closed-loop poles with different dc-link loads. (a) Inductive stiff grid. (b) Inductive weak grid. (c) Series-compensated weak grid. Source: [J4].



(a)

(b)

Figure 4.11. Bode plots of Z_{ac} with flexible synchronization control. (a) With DVSC+PFF method. (b) With DVSC+V$_q$FF method. Source: [J4].



(a)

(b)

(c)

Figure 4.12. Closed-loop poles with flexible synchronization control. (a) With DVSC+PFF method under the inductive weak grid. (b) With DVSC+V$_q$FF method under the inductive stiff grid. (c) With DVSC+V$_q$FF method under the series-compensated weak grid. Source: [J4].

Figure 4.10 presents the closed-loop poles under different ac grid conditions, reflecting the dynamic effect of ac impedance characteristics depicted in Figure 4.9. Despite the closed-loop poles being located at different frequencies, the load variations mainly influence the low-frequency poles, denoted as λ_{1-2}. It is shown that when a CPL is connected to the GFM-VSC through the dc link, poles λ_{1-2} are situated in the RHP, indicating that the LFO issue arises. Such phenomena can be found under different ac grid conditions. In contrast, poles λ_{1-2} transition to the LHP as the dc link is connected to CIL and CRL, which thus denotes a stable operation of the GFM-VSC. Figure 4.9 and Figure 4.10 emphasize that the dc-link CPL results in the broadest frequency range in which Z_{dd} exhibits a negative real part, thereby posing the highest risk of instability.

To alleviate the risk of instability associated with the dc-link CPL, the flexible synchronization control is employed to shape the characteristics of Z_{ac}. Figure 4.11 shows the Bode plots of Z_{ac} using the DVSC+PFF and DVSC+V$_q$FF methods, which are confirmed by experimental impedance measurement. It is shown that those two synchronization methods exhibit comparable impedance-shaping effects. When increasing K_{pp} of the PFF control and K_{pv} of the V_qFF control, the range of frequencies where Z_{dd} exhibits a negative real part becomes narrower. Meanwhile, the initially inductive imaginary part of Z_{dd} transforms into a capacitive behavior with parameter variations.

Figure 4.12 presents the closed-loop poles with the flexible synchronization control under different ac grid conditions, which reflects the dynamic effect of ac impedance characteristics depicted in Figure 4.11. It is apparent that poles $\lambda_{1\text{–}2}$ shift towards the LHP when increasing K_{pp} of the PFF control and K_{pv} of the V_qFF control. Such effects can be observed under different ac grid conditions. The GFM-VSC thus transitions from unstable to stable operations. As a result, Figure 4.11 and Figure 4.12 reveal that the DVSC+PFF and DVSC+V_qFF methods narrow the frequency range where Z_{dd} exhibits a negative real part, thereby stabilizing the GFM-VSC loaded by a CPL.

4.4.3. DYNAMICS WITH DIFFERENT DC-LINK SOURCES

GFM-VSCs can be connected to CPS and CIS in the inverter mode. Dynamics of CPS and CIS are the same as CPL and CIL, as illustrated in (4.10) and (4.11), with P_L and I_L exhibiting negative values.

Figure 4.13 depicts the Bode plots of Z_{ac} with different dc-link sources. The DVSC+V_qFF method is employed in the study, with K_{pv} set to 0.1p.u. The red lines represent Z_{ac} with dc-link CIS, while the blue lines correspond to Z_{ac} with dc-link CPS. It is shown that the GFM-VSC demonstrates a negative real part in Z_{qq} when operating in the inverter mode, while Z_{dd} remains passive. In the case of GFM-VSC connected to a CIS, Z_{qq} demonstrates a negative real part within low frequencies, whereas the imaginary part is inductive. Yet, as a CPS is employed at the dc link, Z_{qq} demonstrates a negative real part with a reduced frequency range and a capacitive imaginary part. Furthermore, similar transitions of the impedance characteristics are also demonstrated in Z_{qd}.

Figure 4.14 illustrates the Bode plots of Z_{ac} using the DVSC+V_qFF method, with a CIS connected through the dc link. Those impedance profiles are confirmed by experimental impedance measurement. It is shown that when increasing K_{pv} of the V_qFF control from 0.1p.u. to 0.4p.u., the range of frequencies within which Z_{qq} exhibits a negative real part becomes narrower. Meanwhile, the initially inductive imaginary part of Z_{qq} transforms into a capacitive behavior with parameter variations.

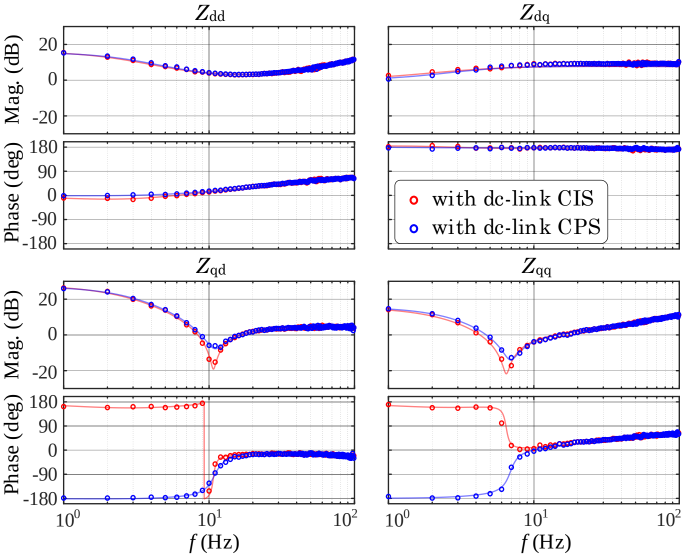


Figure 4.13. Bode plots of Z_{ac} with different dc-link sources. Source: [J4].

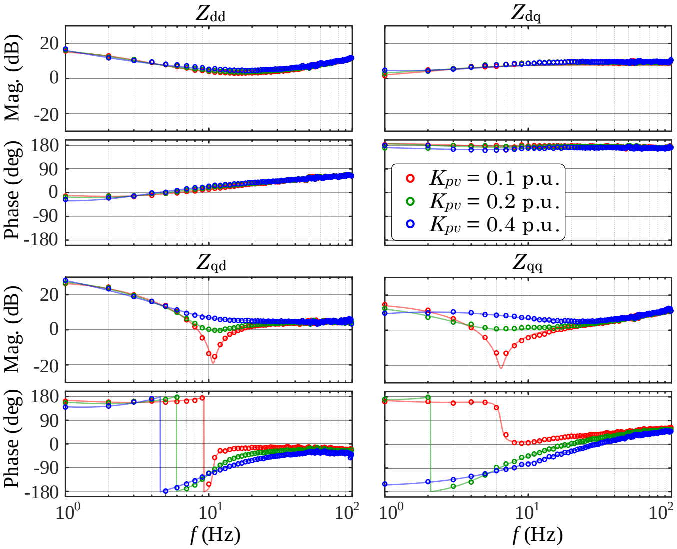
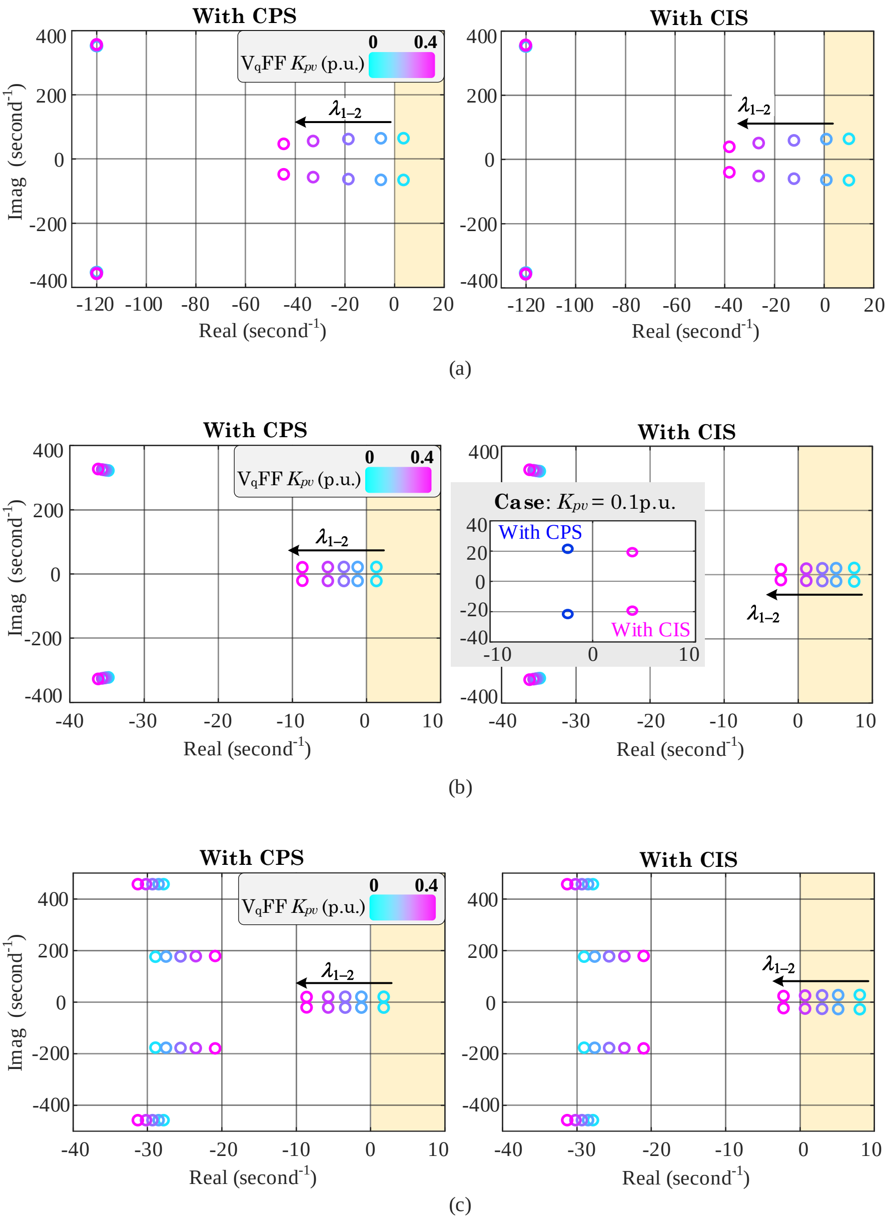


Figure 4.14. Bode plots of Z_{ac} with the DVSC+$\mathrm{V_q}$FF method. Source: [J4].



(a)

(b)

(c)

Figure 4.15. Closed-loop poles with different dc-link sources. (a) Inductive stiff grid. (b) Inductive weak grid. (c) Series-compensated weak grid. Source: [J4].

Figure 4.15 presents the closed-loop poles under different ac grid conditions, reflecting the dynamic effects of ac impedance characteristics demonstrated in Figure 4.13 and Figure 4.14. It is shown that poles $\lambda_{1\text{–}2}$ move towards the LHP when increasing K_{pv} of the V$_q$FF control, which can be observed under different ac grid conditions. Specifically, under the inductive weak grid with K_{pv} set to 0.1p.u., the GFM-VSC demonstrates a stable operation when connected to a CPS. Conversely, it suffers from instability when connected to a CIS. The comparative results in Figure 4.13 and Figure 4.15 indicate a higher risk of instability with the CIS than with the CPS. Moreover, Figure 4.14 and Figure 4.15 demonstrate that the DVSC+V$_q$FF method effectively narrows the frequency range where Z_{qq} exhibits a negative real part, thereby resulting in the enhanced stability of the GFM-VSC.

4.5. EXPERIMENTAL RESULTS

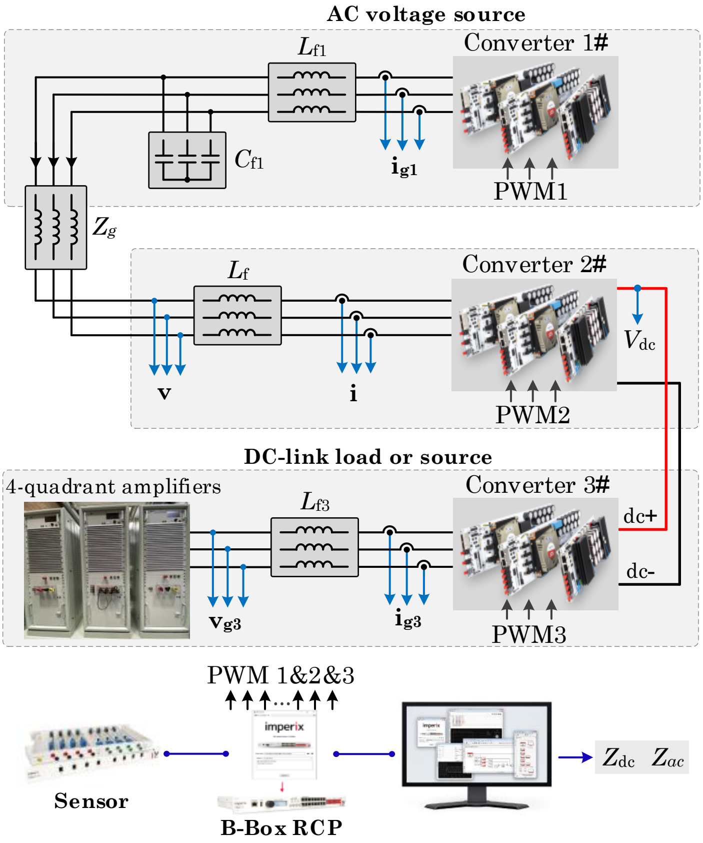
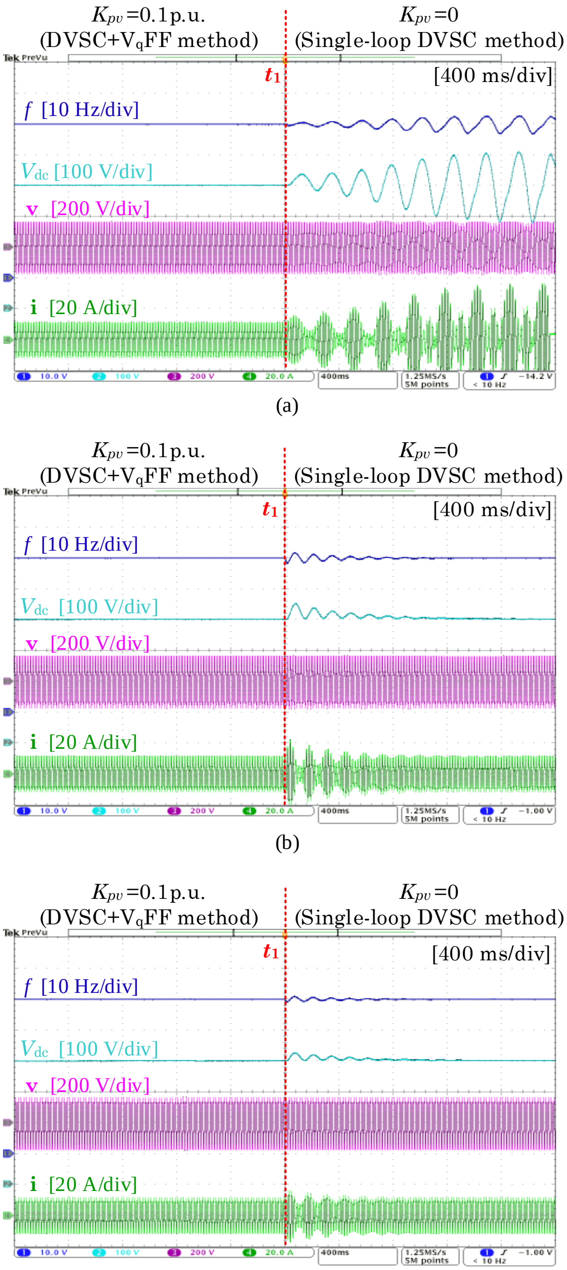

AC voltage source
L_{f1}
Converter 1#
C_{f1}
$\mathbf{i}_{g1}$
PWM1
Z_g
L_f
Converter 2#
V_{dc}
v
i
PWM2
DC-link load or source
4-quadrant amplifiers
L_{f3}
Converter 3#
dc+
dc-
$\mathbf{v}_{g3}$
$\mathbf{i}_{g3}$
PWM3
PWM 1&2&3
imperix
Z_{dc} Z_{ac}
Sensor
B-Box RCP

Figure 4.16. Experimental setup. Source: [J4].

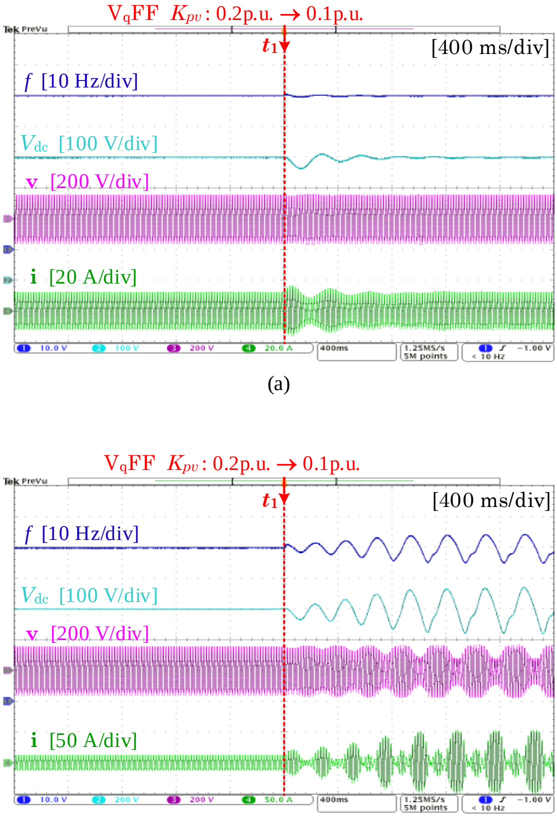


(a)

(b)

(c)

Figure 4.17. Dynamics comparison of the GFM-VSC connected to different loads. (a) With CPL. (b) With CIL. (c) With CRL. Source: [J4].



(a)

(b)

Figure 4.18. Dynamics comparison of the GFM-VSC connected to different sources. (a) With CPS. (b) With CIS. Source: [J4].

The experimental setup depicted in Figure 4.16 is implemented based on Imperix power electronics systems [J4]. Converter 1# generates an ac voltage source to act as the grid voltage and can inject voltage perturbations to measure Z_{ac}. Converter 2# acts as the GFM-VSC, while Converter 3# serves as a dc-link source or load with different characteristics [85].

Figure 4.17 presents the dynamics comparison of the GFM-VSC connected to different loads, with L_g set to 0.85p.u. The GFM-VSC, employing the single-loop DVSC method, encounters the LFO issue when connected to a CPL. In contrast, it maintains operational stability when connected to a CRL and CIL. Moreover, the GFM-VSC, using the DVSC+V$_q$FF method, exhibits a stable operation even loaded by a CPL. The results confirm that the CPL imposes a higher risk of instability than

CRL and CIL. Moreover, the DVSC+V_qFF method is validated to mitigate the risk of instability associated with the CPL.

Figure 4.18 illustrates the dynamics comparison of the GFM-VSC connected to different sources, with L_g set to 0.85p.u. The DVSC+V_qFF method is employed in this test. It is shown that as K_{pv} of the V_qFF control switches from 0.2p.u. to 0.1p.u., the GFM-VSC maintains operational stability when connected to a CPS. In contrast, it experiences the LFO issue when connected to a CIS. The results confirm that the CIS imposes a higher risk of instability than the CPS. Moreover, the DVSC+V_qFF method is also validated to mitigate the risk of instability associated with dc-link sources.

4.6. SUMMARY

This chapter has performed an external interaction analysis for GFM-VSCs, using the dc-link and ac impedance-based analytical methods.

1) DC-link impedances reveal that the CPL poses the highest risk of instability compared to CRL and CIL. Employing the DVSC+PFF and DVSC+V_qFF methods can alleviate the adverse effect of interactions between GFM-VSC and CPL.

2) AC impedance matrices reveal that in the rectifier operation mode, the CPL leads to a wider frequency range for Z_{dd} to exhibit a negative real part compared to the CIL and CRL. In the inverter operation mode, the CIS results in a wider frequency range for Z_{qq} to exhibit a negative real part compared to the CPS. The CIS poses a higher risk of instability than the CPS.

3) The DVSC+PFF and DVSC+V_qFF methods narrow the frequency range of negative real parts exhibited in Z_{dd} and Z_{qq}, thereby mitigating the risk of instability.

CHAPTER 5. CONCLUSIONS AND FUTURE WORK

5.1. CONCLUSIONS

This Ph.D. thesis has conducted studies on analytical modeling, dynamic analysis, and enhanced control strategies for GFM-VSCs with dc-link voltage regulation. The studies include the outer-loop DVSC methods, the inner control loops, and the external interactions with both ac grids and dc-link sources and loads. The major conclusions are summarized as follows.

- The small-signal synchronization stability of GFM-VSCs varies with different DVSC methods. The GFM-VSC using the single-loop DVSC method encounters the LFO issue when connected to a CPS or CPL at the dc link. The proposed flexible synchronization control, comprising paralleled configurations of DVSC, PFF, and V_qFF loops, can address the LFO issue. The PFF and V_qFF controls form feedback loops from the phase angle dynamics to the frequency deviations, functioning as active dampers against the dynamics of CPS and CPL. GFM-VSCs with proposed synchronization methods exhibit stable operations across a wide range of grid strengths and in both inverter and rectifier modes.

- An analytical approach is proposed to evaluate the impact of inner control loops on the damping. The impedance model uniformly characterizes the inner-loop control dynamics using equivalent resistance and inductance. Based on the impedance model, the complex torque coefficient method reveals the effect of inner-loop dynamics on the outer-loop dynamics. It identifies oscillation modes via synchronizing torques and assesses the stability through net damping torque. Inner control loops shape the damping torque, thereby providing a stable operational range within which the outer control loops can be tuned. Case studies with the virtual admittance and the vector current control exemplify the proposed analytical approach.

- External interactions of GFM-VSCs with both dc and ac systems are investigated using impedance-based analytical methods. Among different sources and loads connected via the dc link, the CPL poses the highest risk of instability compared to CIL and CRL in the rectifier mode, whereas the CIS poses a higher risk of instability than the CPS in the inverter mode. The low-frequency negative real part is exhibited in Z_{dd} of ac impedance matrix in the rectifier mode, while in Z_{qq} in the inverter mode. Different sources and loads affect the frequency range within which Z_{dd} and Z_{qq} exhibit negative real parts, thereby influencing the ac-side interactions. Furthermore, the proposed flexible synchronization control effectively narrows the frequency range of negative real parts, thereby mitigating the associated risks of instability.

5.2. FUTURE WORK

Based on the findings and outcomes of this Ph.D. project, there remain several open questions and potential directions that merit further investigation in future work.

- Besides the small-signal stability investigated in this Ph.D. thesis, the transient performance of GFM-VSCs under large disturbances is also a critical concern. The ac-side current-limiting control and dc-link voltage protection will be triggered during large disturbances, while different implementations of those measures can affect the system dynamics. Moreover, VSCs are required to have fault ride-through capability and provide GFM services to ac systems, thereby necessitating enhanced control strategies. Those issues will be thoroughly explored in future research.

- The studies in this Ph.D. thesis are conducted based on a single converter infinite-bus system. This setting is applicable for the stability analysis of a single converter, while the interactions among multiple power converters are neglected. Notably, real-world ac systems are characterized by the presence of SGs, converter-based resources with GFM or GFL control strategies, and local loads. Therefore, the interactions between the studied GFM-VSC and multiple power devices on the ac side, as well as strategies for stability enhancement of ac systems, could be investigated in future research.

- The dc-link sources and loads in this Ph.D. thesis generally refer to converter-based resources, which are assumed to exhibit specific characteristics (constant-power, constant-current, or constant-resistance behaviors) with idealized control performance. However, the control dynamics of converter-based resources cannot be neglected especially under large disturbances; and the physical output current/power limiting of converter-based resources may affect the instantaneous power response of GFM-VSCs. Therefore, the dc-link interactions between GFM-VSCs and converter-based resources, considering their control dynamics, remain a subject for further investigation.

- Converter-based resources recently employ wide-bandgap devices for hardware improvement, resulting in higher switching frequencies and minimized inductor and capacitor filters. Meanwhile, the trend towards a reduced dc-link capacitor is observed in some application scenarios, such as electric vehicle chargers. The control performance and potential risks of instabilities of GFM-VSCs, using the above hardware configurations, remain open issues for further exploration.

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Appended Publications

[J1] **Liang Zhao**, Zheming Jin, and Xiongfei Wang, “Analysis and damping of low-frequency oscillation for dc-link voltage-synchronized VSCs,” *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8177-8189, July 2023.

[J2] **Liang Zhao**, Zheming Jin, and Xiongfei Wang, “Small-signal synchronization stability of grid-forming converters with regulated dc-link dynamics,” *IEEE Trans. Ind. Electron.*, vol. 70, no. 12, pp. 12399-12409, Dec. 2023.

[J3] **Liang Zhao**, Xiongfei Wang, and Zheming Jin, “Exploring damping effect of inner control loops for grid-forming VSCs,” *IEEE Trans. Power Electron.*, under review.

[J4] **Liang Zhao**, Xiongfei Wang, and Zheming Jin, “Impedance-based dynamics analysis for dc-link voltage-synchronized voltage-source converters,” *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 10829-10844, Sept. 2023.

[C1] **Liang Zhao**, Xiongfei Wang, and Zheming Jin, “Flexible synchronization control for grid-forming converters with regulated dc-link dynamics,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1-8.

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