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Figures-of-Merit Study for Thermal Transient Measurement of SiC MOSFETs

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***Abstract*—Thermal transient measurement (TTM) utilizes temperature-sensitive electrical parameters (TSEP) to analyze the thermal structure of power semiconductor devices. However, the measured physical quantities are essentially electrical parameters rather than direct temperatures. Determining whether these measurements reflect correct temperature or thermal structure of the tested device remains unclear. This limitation becomes more pronounced with emerging silicon carbide (SiC) devices. To address this issue, this paper provides a figures-of-merit (FOM) study for the TTM applied to SiC MOSFETs. The FOM comprises three static and two dynamic factors. The proposed FOM is employed to evaluate ten plausible testing circuits of a SiC MOSFET, where four of them are identified as providing reproducible thermal structures. A high-fidelity finite-volume method simulation is also used as a benchmark to validate the result. This study highlights some important facts, notably that successful TSEP calibration does not guarantee reproducible TTM, and compliance with current standards may also yield incorrect results. These insights hold significant implications for the field of SiC MOSFETs and the future development of the TTM method.**

***Index Terms*—Silicon carbide (SiC) MOSFETs, thermal characterization, transient thermal measurement, temperature-sensitive electrical parameters (TSEP).**

I. Introduction

THERMAL characterization plays a critical role in the design and operation of power electronics [1]–[3]. This is particularly true for emerging silicon carbide (SiC) devices, which are rapidly gaining popularity in various applications such as renewable energy [4], automotive [5], and more. Given the reduced chip size, elevated power density, and higher cost compared to silicon (Si) devices, accurate thermal characterization of SiC devices is of utmost importance.

Thermal transient measurement (TTM) is a widely accepted technique to characterize the thermal properties of semiconductors, as recognized by standards such as JEDEC JESD 51-1 [6] and JESD 51-14 [7]. As shown in Fig. 1(a), the standard TTM involves three steps:

- *Calibration:* put a low sensing current I_{sense} on the device under test in a thermostat and calibrate the **static** temperature-sensitive electrical parameters (TSEP);
- *Cooling curve measurement:* add a high heating current I_{heat} to heat the device up, subsequently switch off I_{heat} and measure the **time-resolved** TSEP voltage at I_{sense} to obtain a cooling curve;
- *Post-processing:* convert the cooling curve into thermal structure properties, such as thermal impedance, structure function, etc. Details of these conversions should refer to [6]–[8].

However, the TTM method was primarily developed based on Si devices, and applying this approach to SiC MOSFETs presents following three challenges.

To begin with, existing studies lack quantitative metrics for evaluating the static calibration result. Specifically for SiC MOSFETs, multiple testing conditions, such as sensing currents and gate voltages, significantly impact the calibration results. Setting these parameters for SiC MOSFETs based on empirical rules developed for Si devices often results in misleading results. For instance, to mitigate self-heating effects, references [9], [10] suggest using a sensing current approximately 1/1000 of the nominal current, which is the empirical rule for Si devices [10]. Meanwhile, other studies argue for lower sensing currents [11] or higher sensing currents [12] for SiC MOSFETs. Similarly, the selection of gate voltages remains a topic of discussion in [13]–[15]. The lack of consensus in existing research for setting these conditions stems from a lack of quantitative criteria to guide the trade-off among different performances, such as minimizing self-heating, ensuring measuring accuracy, and achieving optimal resolution. As calibration is a prerequisite for TTM, the existing empirical criteria developed for Si devices limit the achievement of reproducible TTM for SiC MOSFETs.

Next, existing studies lack adequate considerations of the dynamic performance of the calibration results. The standard calibration process establishes a static relationship between junction temperatures and TSEPs. The feasibility of applying the static result to time-resolved (dynamic) cooling curve measurements remains unclear. Herold et al. [15] emphasize the significance of considering the dynamic behavior of TSEPs. Furthermore, our preliminary studies [16], [17] reveals that different dynamic behaviors impact the obtained thermal structure and noise immunity. These issues necessitate an effective scheme to evaluate the dynamic behaviors of TSEPs.

In addition, the assumption that complying with existing standards ensures obtaining accurate thermal structure may not

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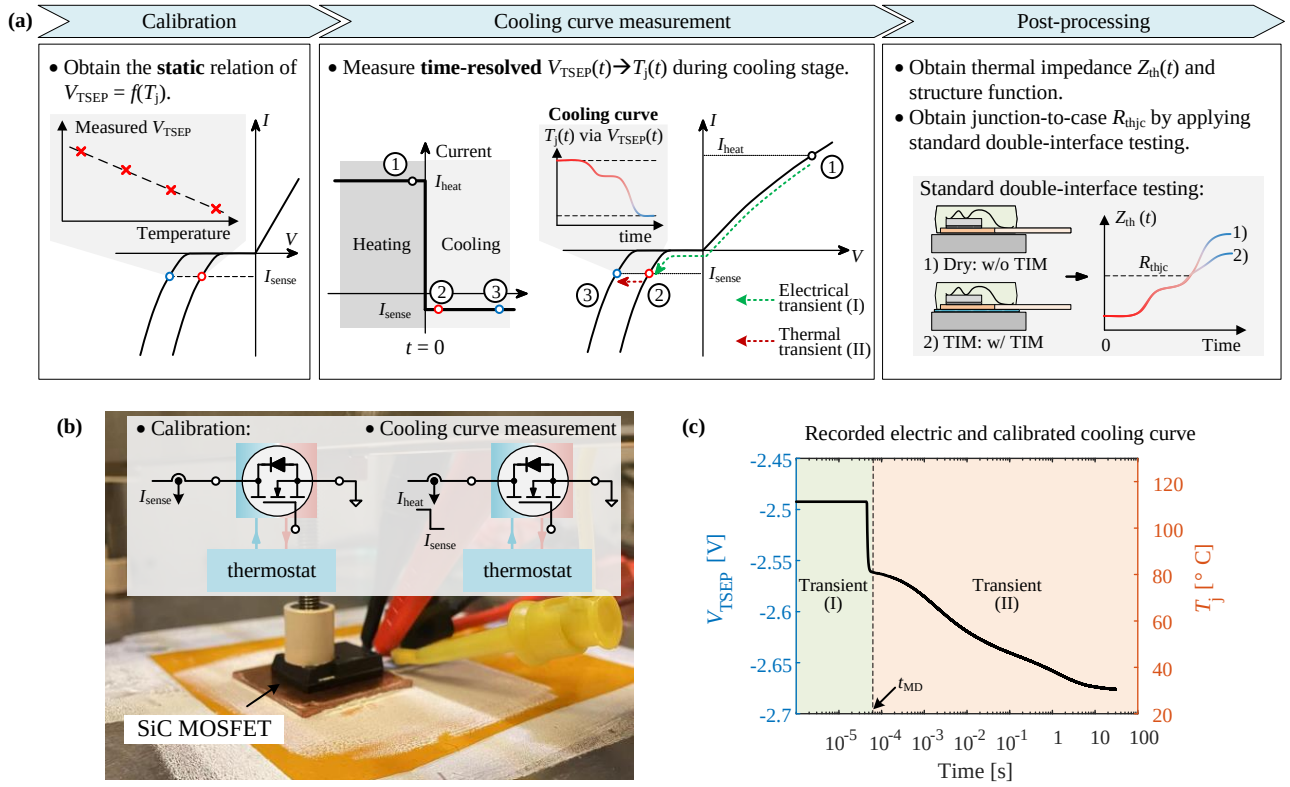


Fig. 1. (a) Main procedure of the standard thermal transient measurement (TTM), (b) the photo of the testing setup, and (c) an example of recorded electric and calibrated cooling curve. (TSEP: temperature sensitive electrical parameters, I_{sense}: sensing current for measuring TSEPs, I_{heat}: heating current to heat up the device, TIM: thermal interface material, t_{MD}: a delay time in cooling curve.)

always hold true, especially for SiC MOSFETs. Our previous studies [16], [17] has revealed that strict adherence to existing standards does not always guarantee the correctness of the obtained thermal structure. In this paper, further demonstrations are provided, indicating that the obtained thermal structure may still be incorrect, despite achieving perfect calibration in terms of static and dynamic performances and even seemingly perfect thermal impedance and structure function curves. These discrepancies are difficult to identify within the scope of the existing standard process. Thus, it is crucial to go beyond the limits of existing standards and conduct comprehensive investigations to ensure reproducible TTM for SiC MOSFETs.

The aforementioned three issues underscore an essential gap in the absence of quantitative figures-of-merit (FOM) studies to achieve reproducible TTM for SiC MOSFETs. This problem becomes increasingly intricate when addressing SiC MOSFETs with multiple TSEPs, various testing circuits, and different device structures. For instance, SiC MOSFETs have multiple TSEPs, and they can be evaluated by a variety of testing circuits. Funaki et al. [14] assessed two TSEPs and four potential testing circuits, concluding that the TTM approach is no longer applicable for SiC MOSFETs due to their imperfect structures. In contrast, Sarkany et al. [18] did a similar study in the same year, but reached opposite conclusions. Although subsequent studies [9], [11], [15], [19]–[23] have investigated various TSEPs for SiC MOSFETs, their reliance on empirical rules limits the development of a more general effort to ensure reproducible TTM for SiC MOSFETs. Furthermore, SiC MOSFETs with different structures, such as the incorporation of additional anti-parallel Schottky Barrier Diodes (SBDs), introduce different challenges when applying the TTM approach [24], [25]. All these issues highlight the need for an in-depth FOM study to establish a more general foundation for achieving reproducible TTM for SiC MOSFETs.

To address the above challenges, this paper presents a systematic investigation of the TTM approach in SiC MOSFETs, with an emphasis on obtaining reproducible thermal structure properties. The contributions are summarized as follows:

1) This paper provides a quantitative FOM study to ensure reproducible TTM for SiC MOSFETs. It compromises three static and two dynamic factors to evaluate the performances of the calibration and the measured cooling curve. The FOM not only offers a quantitative way to determine testing conditions, but also provides a validation protocol to address potential invisible electrical interference during transient measurements.
2) Ten plausible testing circuits and three TSEPs are evaluated by using the proposed FOM and four of them are identified as feasible for the tested SiC MOSFET. Experimental results are also benchmarked by high-fidelity finite-volume method (FVM) simulation.
3) For SiC MOSFETs with an SBD, a feasible method for obtaining TTM results without damaging the power devices is identified, with potential limitations discussed.

The structure of this paper is outlined as follows. Section II provides a FOM study to ensure reproducible TTM for SiC

MOSFETs, along with introducing the ten plausible testing circuits based on three TSEPs. Sections III to VII comprehensively evaluate the ten plausible testing circuits, utilizing the proposed FOMs. Section VIII presents a comparative study of all feasible testing methods, with a FVM simulation serving as a benchmark to validate their performances. Additionally, the evaluation of a device with an additional SBD is included. The conclusions are summarized at last.

II. The Proposed FOM and Plausible Test Methods

This section presents a FOM study to ensure reproducible TTM for SiC MOSFETs. It compromises three static and two dynamic factors to quantitatively evaluate the performances of the calibration and the measured cooling curve. Moreover, ten plausible testing circuits based on three different TSEPs of the SiC MOSFET are introduced. The subsequent Section III to VII will apply the proposed FOM to evaluate these different testing methods based on a selected SiC MOSFET C2M0160120D [26]. The testing setup is SIEMENS Simcenter Micred Power Tester 1800 A [27] as shown in Fig. 1(b). This standardized platform ensures the reproducibility of the test results presented in this paper.

A. Three Static Calibration FOMs

Calibration is the prerequisite of TTM. Thus, the FOM with three static factors is proposed to assess the calibration results, namely linearity ρ_{linear}, sensitivity S_{VT}, and self dissipation ratio η_{sd}, which are given by

$$FOM_1 = \rho_{\text{linear}} = \left| \frac{\text{cov}\left(V_{\text{TSEP}}, T_{\text{j}}\right)}{\sigma_{V_{\text{TSEP}}} \cdot \sigma_{T_{\text{j}}}} \right|, \tag{1}$$

$$FOM_2 = S_{\text{VT}} = \left| \frac{\Delta V_{\text{TSEP}}\ [\text{mV}]}{\Delta T_{\text{j}}\ [\text{K}]} \right|, \tag{2}$$

$$FOM_3 = \eta_{\text{sd}} = \frac{P_{\text{sense}}}{P_{\text{rate}}} = \frac{I_{\text{sense}} \times V_{\text{TSEP@}I_{\text{sense}}}}{P_{\text{rate}}}. \tag{3}$$

The ρ_{linear} quantifies the linearity between the measured TSEP (e.g., a TSEP voltage V_{TSEP}) and the junction temperature T_{j}, where cov denotes covariance, and σ represents standard deviation. A perfect linearity has $\rho_{\text{linear}} = 1$. Our previous work [16] showed that perfect linearity is more desirable. It not only simplifies temperature estimation for uncalibrated data points but also indicates that the measurement is primarily influenced by the device's temperature-sensitive characteristics rather than parasitic elements.

The sensitivity factor S_{VT} quantifies the ease of the temperature measurement by TSEPs. A so-called K factor is often used in engineering, which has $K = 1/S_{\text{VT}}$. In the case of typical SiC MOSFETs, the TSEP voltages are around 3 V (see Sections III to VII). $S_{\text{VT}} = 1\ \text{mV/K}$ implies that maintaining a temperature resolution of 1 K necessitates that the noise level of the measurement must be less than 1 mV, namely around 1/3000 of the nominal reading. Considering the practical constraints of acquisition systems, this paper adopts a threshold of S_{VT} above 1 mV/K for the subsequent evaluation.

Minimizing self-dissipation due to the sensing current is important in TTM. The self-dissipation ratio η_{sd} offers a quantitative means to justify the negligibility. Here, P_{sense} represents the dissipation of the sensing current, and P_{rate} corresponds to the nominal power dissipation as provided in the datasheet. Typically, P_{rate} is known to cause a substantial increase in junction temperature, often exceeding 100 K, as indicated by datasheets, e.g., [26], [28]. An η_{sd} value below 1% indicates that the temperature rise caused by the sensing current is less than 1 K, thus deeming it negligible. It should be noted that more stringent requirements can be applied, but the three factors are not entirely independent. For instance, a stricter demand for minimal self-dissipation may negatively affect linearity or sensitivity. Thus, the three quantified factors help to achieve a trade-off among the three static performances.

B. Two Dynamic FOMs for the Cooling Curve Measurement

In addition to assessing static performance, evaluating cooling curves requires a thorough consideration of dynamic behavior. The current-voltage characteristic in the middle of Fig. 1(a) exhibits two transients: transient I from ① to ② and transient II from ② to ③. Fig. 1(c) exemplifies a recorded electric and calibrated cooling curve, representing measurement either in the original TSEP voltage (left ordinate) or calibrated junction temperature (right ordinate).

Transient I, mainly electrical, is easily identified although it can also be converted into temperature. Standard JESD 51-1 [6] deals with this transient by excluding measurements during the time from $t = 0$ to ②, referred to as a delay time t_{md}. Subsequently, it employs a linear extrapolation to estimate the temperature at $t = 0$. However, it is vital to recognize that the validity of this linear extrapolation is based on a semi-infinite plate model [29]. A prolonged t_{md} violates this critical assumption, potentially leading to a significant decrease in the accuracy of the obtained thermal structure. Thus, this paper utilizes t_{md} as a dynamic FOM, which is limited by a maximum acceptable short period t_{valid} [29] as

$$FOM_4 = t_{\text{md}} \leq d_{\text{chip}}^2 \cdot \frac{c\rho}{2\lambda}, \tag{4}$$

with d_{chip} being the chip thickness, λ, c, and ρ being the thermal conductivity, specific heat capacity, and density of the material, respectively. For the tested SiC MOSFET chip, the thickness is 180 µm, $\lambda = 370\ \text{W/m K}$, $c = 750\ \text{J/kg K}$, and $\rho = 3100\ \text{kg/m}^3$. Thus, this paper opts for $t_{\text{md}} \leq 100$ µs in the subsequent testing condition settings.

Transient II is often considered purely thermal. However, one significant but long-overlooked issue involves that transient II is also susceptible to electrical interference, which, moreover, is often invisible and challenging to detect. Our previous study [17] revealed that Transient II exhibits different electrical noise under various testing condition settings. Subsequent analysis in this paper will further demonstrate that Transient II does not always respond correctly to thermal transients. Hence, this paper introduces an additional validation process. It compares thermal impedance curves from multiple TTM results at different currents. The underlying mechanism is that the correct thermal impedance should remain unaffected by heating current variations. For instance, the two thermal impedance curves under different heating currents are denoted

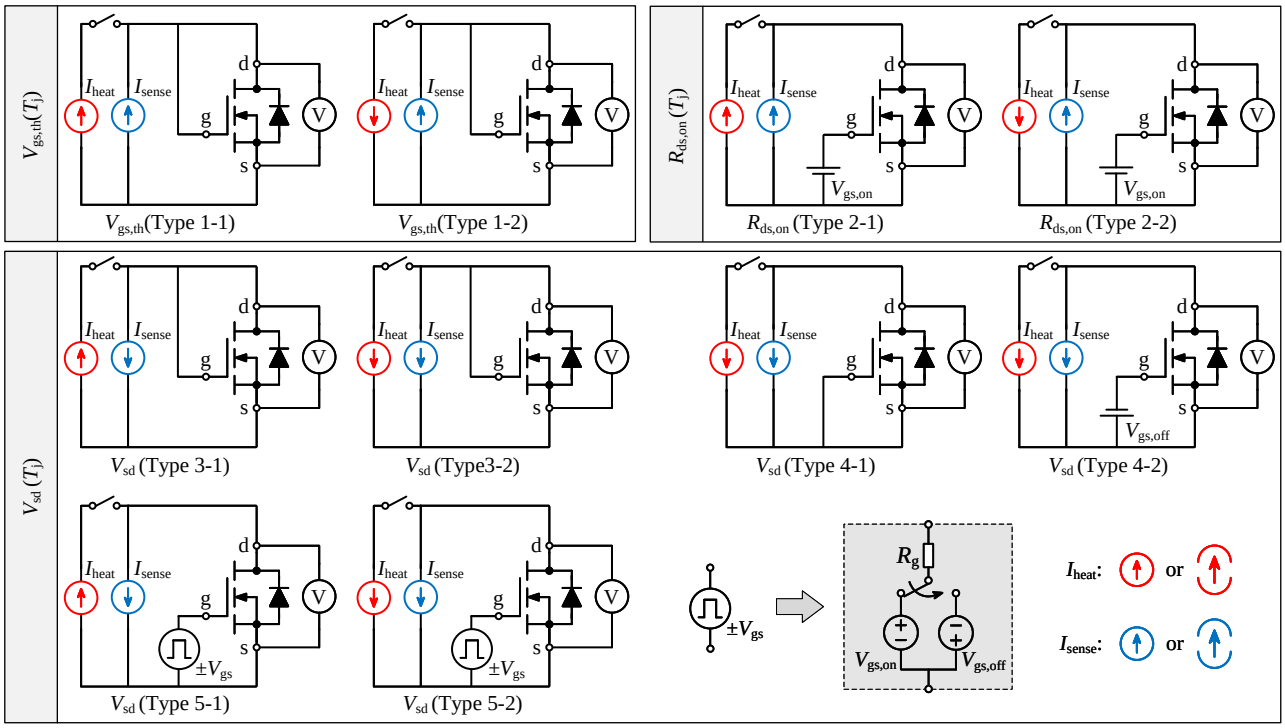


Fig. 2. Ten plausible testing circuits to perform TTM for SiC MOSFETs, which consist of three TSEPs including gate threshold voltage $V_{gs,th}$ (Type 1-1 and 1-2), on-state resistance $R_{ds,on}$ (Type 2-1 and 2-2), and voltage drop of the intrinsic body diode V_{sd} (from Type 3-1 to 5-2).

as Z_{th1} and Z_{th2}. An Euclidean distance $d(Z_{th1}, Z_{th2})$ quantifies their similarity as

$$FOM_5 = d(Z_{th1}, Z_{th2}) = \sqrt{\sum (Z_{th1} - Z_{th2})^2}. \quad (5)$$

Two completely identical thermal impedance curves will yield a distance of $d(Z_{th1}, Z_{th2}) = 0$. Considering some non-ideal issues, e.g., temperature-dependent material properties, the temperature rise differences generated by the two heating currents should not be too large to minimize the non-ideal impacts. The lowest possible FOM_5 value indicates the lowest possible influence of electrical influences. Implementing this validation protocol provides a factor to know the invisible electrical interference.

C. Ten Plausible Test Circuits for SiC MOSFETs

The above-established FOMs will be applied for evaluating the ten plausible testing circuits for the TTM of SiC MOSFETs as shown in Fig. 2, which are based on three typical TSEPs and classified into five categories (Type 1 to Type 5). Although some of these testing methods have been discussed in previous studies [9], [11], [14], [15], [18]–[23], the existing research primarily focuses on temperature estimation for power cycling or condition monitoring. The TTM method to obtain thermal structure properties has not been adequately studied. To the best of our knowledge, this is the first study in the public literature to systematically study all these circuits and perform cross-comparisons among results from different testing methods. By comprehensively exploring the feasibility and limitations of these testing methods, this paper offers valuable insights into the thermal characterization of SiC MOSFETs and the future development of the TTM method.

III. Type 1 Circuits Based on Gate Threshold Voltage

This section introduces two testing circuits of Type 1 that utilize the gate threshold voltage ($V_{gs,th}$) as the TSEP as shown in Fig. 2. To measure this voltage, the gate and drain of the MOSFET are shorted. A small sensing current is injected through the device, and the gate-source voltage is slightly higher than the threshold gate voltage, which has

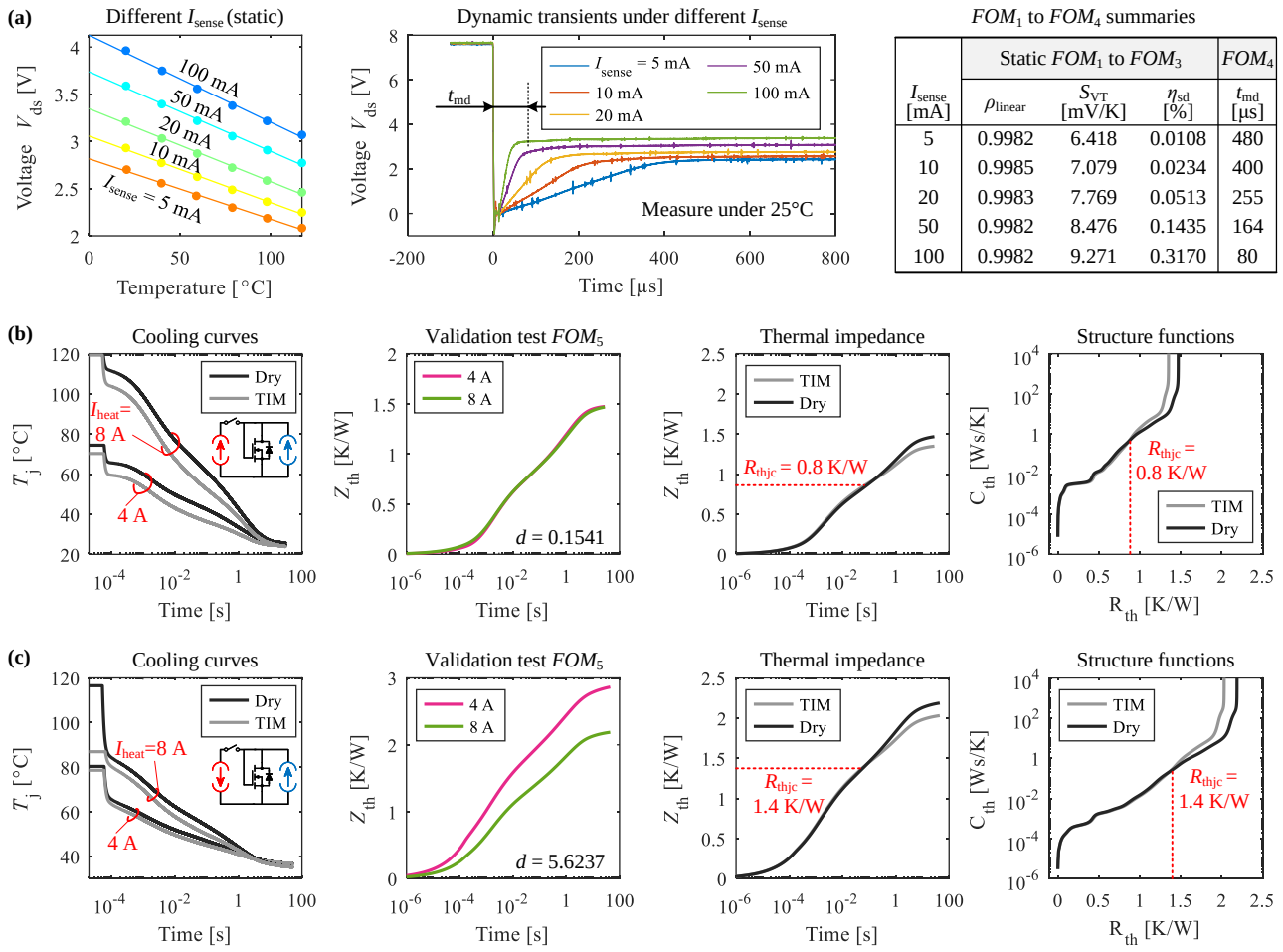
$$I_D = \frac{\beta}{2}(V_{gs} - V_{gs,th})^2, \quad (6)$$

where β is a parameter related to the effective channel [10]. With connecting the gate and drain terminals, the SiC MOSFET has $V_{gs} = V_{ds}$, which enables to obtain $V_{gs,th}$ by simply measuring V_{ds}. The difference between Type 1-1 and 1-2 lies in the direction of the heating current. With applying the proposed FOMs, the following part will initially discuss calibrations and subsequently present the obtained TTM results of both circuits.

A. Calibration of Type 1 based on $V_{gs,th}$

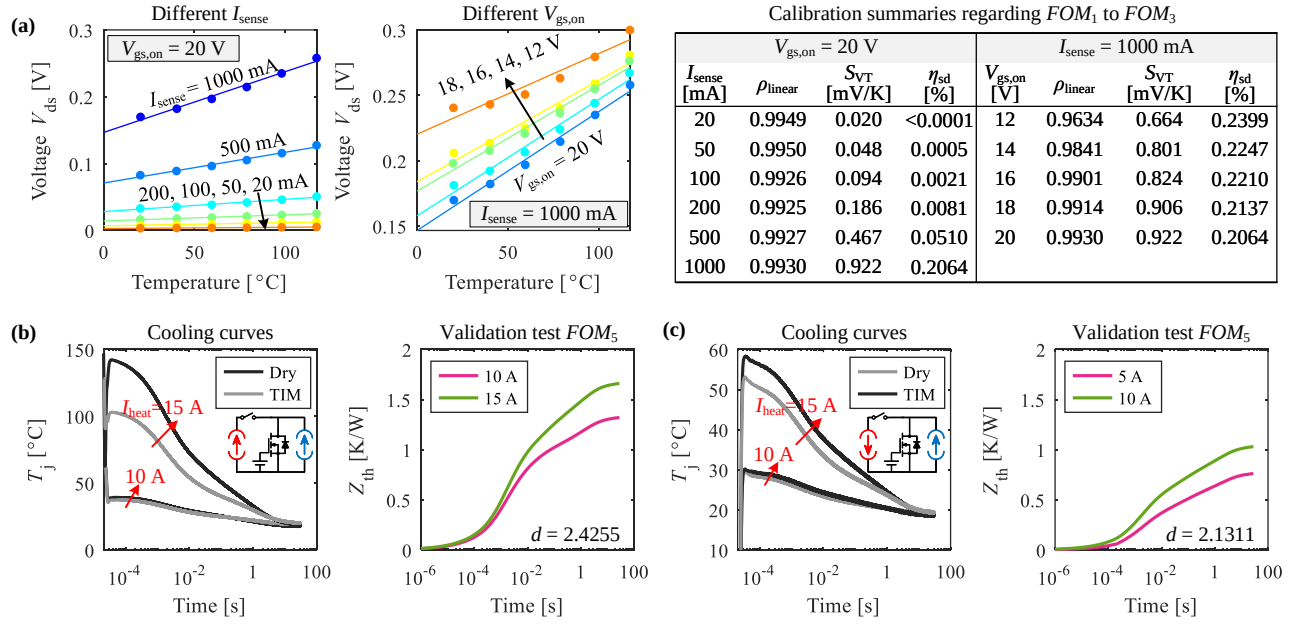
The static calibration results and their summaries for Type 1 circuits are shown on the left and the right of Fig. 3(a), respectively. $V_{gs,th}(T)$ provides high sensitivity for temperature measurement. For instance, at a sensing current from 5 to 100 mA, the sensitivity of $V_{gs,th}(T)$ ranges from 6.418 to 9.217 mV/K. Meanwhile, the linearity remains almost constant and the self-dissipation ratios are all less than 1%. All three static FOMs indicate that $V_{gs,th}(T)$ is an excellent TSEP.

However, the dynamic FOM determined by t_{md} is slow as shown in the middle of Fig. 3(a). The measured t_{md} is



I_{sense} [mA]	Static FOM_1 to FOM_3 ρ_{linear}	S_{VT} [mV/K]	η_{sd} [%]	FOM_4 t_{md} [µs]
5	0.9982	6.418	0.0108	480
10	0.9985	7.079	0.0234	400
20	0.9983	7.769	0.0513	255
50	0.9982	8.476	0.1435	164
100	0.9982	9.271	0.3170	80

Fig. 3. Type 1 test via the TSEP of gate threshold voltage. (a) Static calibrations (left), dynamic transients (middle), and their summaries (right). (b) Type 1-1 testing results: cooling curves, the validation test, double-interface thermal impedance curves, and the structure functions. (c) Type 1-2 testing results. ($Z_{th}(t)$: thermal impedance, C_{th}: thermal capacitance, R_{th}: thermal resistance, Dry: test without applying thermal grease, TIM: test applying thermal grease.)



$V_{gs,on}$ = 20 V I_{sense} [mA]	ρ_{linear}	S_{VT} [mV/K]	η_{sd} [%]	I_{sense} = 1000 mA $V_{gs,on}$ [V]	ρ_{linear}	S_{VT} [mV/K]	η_{sd} [%]
20	0.9949	0.020	<0.0001	12	0.9634	0.664	0.2399
50	0.9950	0.048	0.0005	14	0.9841	0.801	0.2247
100	0.9926	0.094	0.0021	16	0.9901	0.824	0.2210
200	0.9925	0.186	0.0081	18	0.9914	0.906	0.2137
500	0.9927	0.467	0.0510	20	0.9930	0.922	0.2064
1000	0.9930	0.922	0.2064				

Fig. 4. Type 2 test based on the TSEP of on-state resistance. (a) Calibration results under different I_{sense} (left), various $V_{gs,on}$ (middle), and their summaries (right). (b) Type 2-1 testing results: cooling curves and the proposed validation test of thermal impedance under different heating currents, (c) Type 2-2: cooling curves and the validation test.

strongly correlated to the sensing current, and this dynamic performance is influenced by various factors [30], such as the acquisition system, parasitic output capacitance, and device transients. Specifically, for the tested device, the unwanted electrical transient lasts around 480 µs with $I_{\text{sense}} = 5$ mA. Although 5-mA sensing current has good static performances, a sensing current of 100 mA is minimum to achieve the dynamic target of $t_{\text{md}} \leq 100$ µs. Considering both the static and dynamic performances, a sensing current of 100 mA is desirable. It reveals that the first four factors of the FOM (i.e., FOM_1 to FOM_4) can guide a trade-off for setting test conditions.

B. TTM Results of Type 1-1 and Type 1-2

The TTM results of Type 1-1 are shown in Fig. 3(b), including cooling curves, the proposed validation tests, double-interface thermal impedance[1], and their structure functions. Due to the large voltage drop of $V_{\text{gs,th}}$, the cooling curves exhibit a significant temperature change with heating currents only 4 A to 8 A. Meanwhile, the validation test shows that the two impedance curves have good consistency. The Euclidean distance is near zero, indicating that the obtained thermal structure is independent of the heating current change. Additionally, by applying the standard double-interface measurement, both the thermal impedance and structure function are obtained, yielding a junction-to-case thermal resistance of 0.8 K/W.

Similarly, the corresponding results of Type 1-2 are shown in Fig. 3(c). The temperature change in the cooling curve becomes smaller since the heating current conducts through the body diode partially. The proposed validation test shows significant inconsistency, which means the measured cooling curve contains non-negligible electrical interference. However, it is difficult to find any abnormal behaviors from the cooling curves alone. This invisible electrical interference has severe consequences on the final obtained thermal structure properties. For instance, the further provided double-interface thermal impedance and structure functions seem to be perfect, but the divergent points give $R_{\text{thjc}} = 1.4$ K/W which is almost double that of Type 1-1. A further FVM simulation will further validate this in Section VIII. This incorrect result reveals a potential risk that simply complying with the current standard does not guarantee a reproducible result.

IV. Type 2 Circuits based on On-State Resistance

The two testing circuits of Type 2 utilize the on-state resistance $R_{\text{ds,on}}$ as the TSEP as shown in Fig. 2. To measure $R_{\text{ds,on}}$, a positive gate voltage $V_{\text{gs,on}}$ is applied, and a sensing current is injected to measure the drain-to-source voltage drop V_{ds}. In both circuits, the sensing current and gate voltage affect the voltage drop and impact the temperature measurement.

First, the calibrated results based on different sensing currents and gate voltages are shown in Fig. 4(a). The primary limiting factor for $R_{\text{ds,on}}$ as the TSEP is the weak sensitivity. For instance, with a fixed gate voltage (i.e., 20 V), the sensitivity is only 0.020 mV/K for $I_{\text{sense}} = 20$ mA. Lowering the gate voltage can increase the value of the TSEP voltage but leads to a decrease in both sensitivity and linearity. However, the dynamic t_{md} is fast and all cases are shorter than 50 µs, which are easily read from the cooling curves in Figs. 4(b) and (c). Considering these trade-offs, the testing conditions are set with $I_{\text{sense}} = 1000$ mA and $V_{\text{gs,on}} = 20$ V.

Next, the cooling curves and the thermal impedance of Type 2-1 and 2-2 are presented in Figs. 4(b) and (c), respectively. However, for the validation test, the thermal impedance curves under different heating currents do not coincide with each other. Since the thermal structure of a power semiconductor should be independent of the heating currents, the observed inconsistency indicates that the two circuits do not provide correct TTM results. It reveals again that a successful calibration cannot guarantee reproducible TTM results.

V. Type 3 Circuits based on Source-Drain Voltage

Type 3 testing utilizes the voltage drop of the body diode as the TSEP. As the circuits depicted in Fig. 2, Type 3 connects the gate and drain terminals directly, resulting in $V_{\text{gs}} = V_{\text{ds}}$. When a sensing current flows in the reverse direction, the voltage drop of the body diode induces a negative gate voltage of $V_{\text{gs}} = -V_{\text{f}}$ around -2 to -3 V, however, the exact voltage value of the body diode is varied with different conditions, e.g., temperatures, leading to an unstable gate voltage.

The calibrations and dynamics under different sensing currents are evaluated in Figs. 5(a) and (b), respectively. All calibrations exhibit good linearity, but slower dynamics require a sensing current of at least 200 mA to achieve $t_{\text{MD}} \leq 100$ µs. The validation tests for Type 3-1 and 3-2 show significant inconsistency as shown in Figs. 5(c) and (d), indicating that Type 3 does not provide reproducible thermal structure. This underperformance is possibly caused by the unstable gate state, which will be studied in the next section.

VI. Type 4 Circuits based on Source-Drain Voltage with Constant Gate State

Type 4 is introduced as a solution to address the unstable gate state of Type 3. Specifically, the gate and source terminals are directly connected in Type 4-1, while a negative gate voltage is applied in Type 4-2. Both configurations provide a constant gate voltage to the SiC MOSFET and utilize the voltage drop of the body diode for heating and temperature measurement.

A. Calibrations of Type 4

The calibration results with different gate voltages, different sensing currents, dynamic behaviors, and their summaries are shown in Figs. 6(a)-(c). With different gate voltages, a strong relation between the calibrated body diode voltage and the gate voltage is shown in the left of Fig. 6(a). However, the forward voltage of an ideal diode should be independent of the gate voltage, which suggests that the different gate voltages affect the conduction characteristics of the body diode. This issue may not be common in Si devices but happens frequently in SiC MOSFETs. Our preliminary work [17] has provided the physical mechanism of this issue in detail. To ensure that the sensing current only flows through the body diode, the

[1]The standard double-interface testing [7] involves two measurements with and without applying thermal interface materials, which are denoted as "TIM" and "Dry" in this paper, respectively.

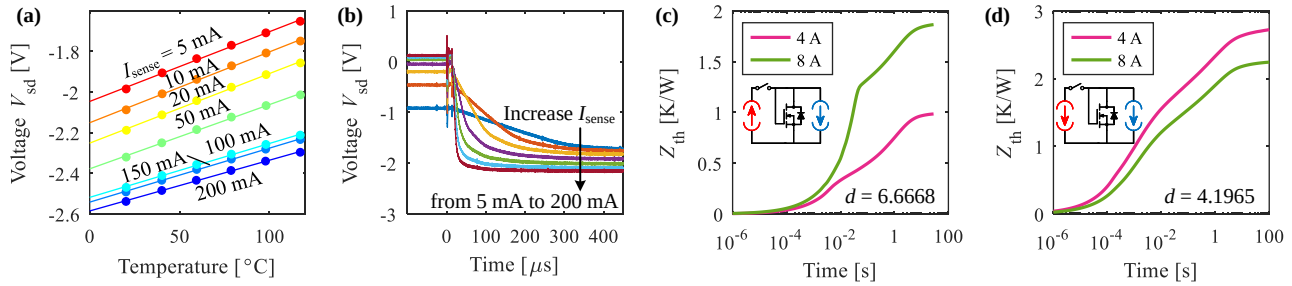
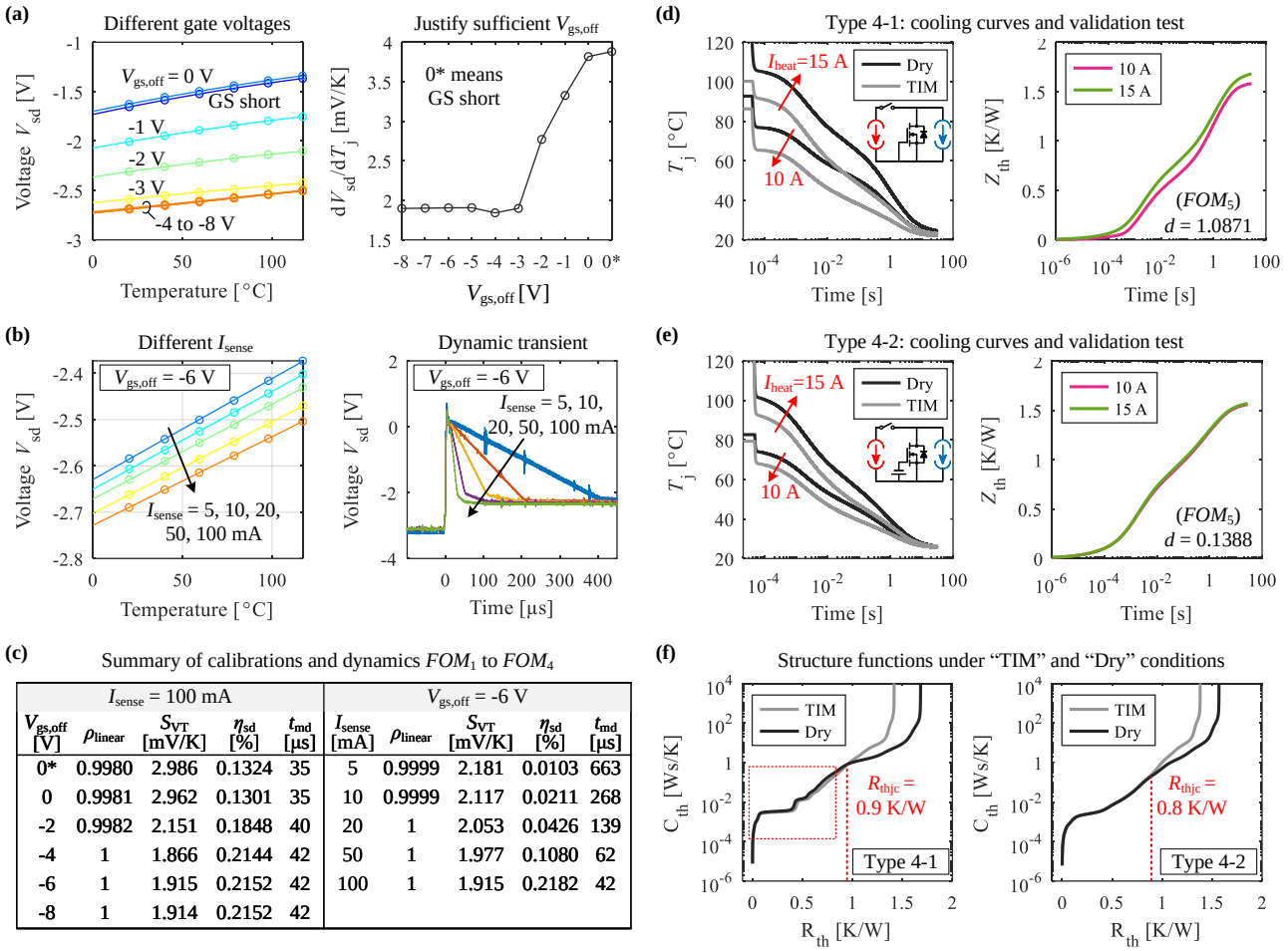


Fig. 5. Type 3 test: (a) calibration and (b) dynamic transient behaviors under different sensing currents, (c) the validation tests of Type 3-1 and (d) Type 3-2.



(c) Summary of calibrations and dynamics FOM_1 to FOM_4

I_{sense} = 100 mA					$V_{gs,off}$ = -6 V				
$V_{gs,off}$ [V]	ρ_{linear}	S_{VT} [mV/K]	η_{sd} [%]	t_{md} [µs]	I_{sense} [mA]	ρ_{linear}	S_{VT} [mV/K]	η_{sd} [%]	t_{md} [µs]
0*	0.9980	2.986	0.1324	35	5	0.9999	2.181	0.0103	663
0	0.9981	2.962	0.1301	35	10	0.9999	2.117	0.0211	268
-2	0.9982	2.151	0.1848	40	20	1	2.053	0.0426	139
-4	1	1.866	0.2144	42	50	1	1.977	0.1080	62
-6	1	1.915	0.2152	42	100	1	1.915	0.2182	42
-8	1	1.914	0.2152	42					

Fig. 6. Type 4 test. (a) Calibration under different gate voltages and its slope against temperature. (b) Calibration under different gate voltages and their dynamic transients. (c) Calibration summaries. (d) Cooling curves and validation test of Type 4-1. (e) Cooling curves and validation test of Type 4-2. (f) Structure functions of Type 4-1 and 4-2.

following equation is applied to justify a sufficient negative gate voltage, which is

$$\frac{\partial}{\partial V_{\mathrm{gs}}}\left[\frac{\partial V_{\mathrm{sd}}\left(T_{\mathrm{j}}\right)}{\partial T_{\mathrm{j}}}\right]=0, \tag{7}$$

where the mechanism is that when the entire sensing current flows through the body diode, the slope of the source-drain voltage against temperature is constant. The right of Fig. 6(a) shows the relationship of $\mathrm{d}V_{\mathrm{sd}}/\mathrm{d}T_{\mathrm{j}}$ as a function of $V_{\mathrm{gs,off}}$, where the curve becomes constant for $V_{\mathrm{gs,off}} < -5$ V. Considering a certain margin, $V_{\mathrm{gs,off}} = -6$ V can be selected.

Moreover, the calibration under different sensing currents is shown in the left of Fig. 6(b). The varied sensing currents slightly affect the linearity and sensitivity. The further dynamic transient [see the right of Fig. 6(b)] indicates that $I_{\mathrm{sense}} = 100$ mA is desirable. All details are summarized in Fig. 6(c).

B. TTM Results of Type 4-1 and Type 4-2

The cooling curves and the validation test of Type 4-1 are shown in Fig. 6(d). Although Type 4-1 provides a constant gate state, the inconsistent thermal impedance curves in the validation test indicate that simply shorting the gate-source terminals is not enough to turn off the channel of the SiC MOSFET, and thus it yields an incorrect TTM result. On the other hand, with a negative gate voltage of $V_{\mathrm{gs,off}} = -6$ V, the

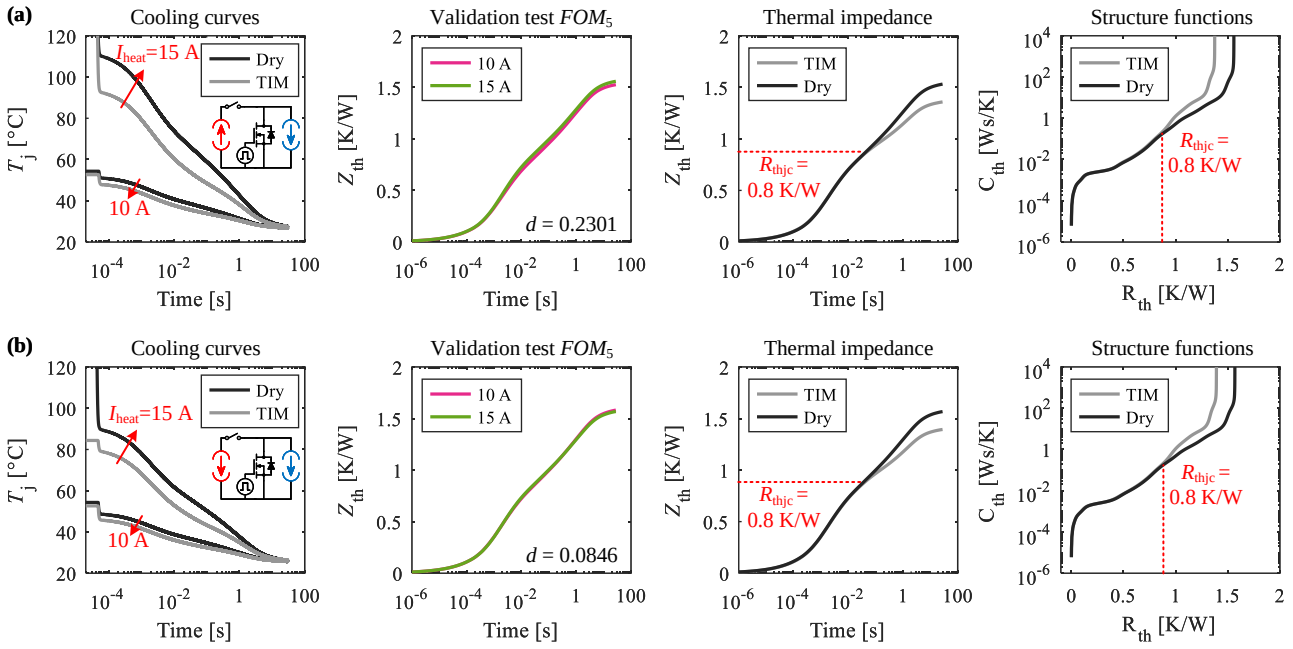


Fig. 7. Type 5 test. (a) Type 5-1: cooling curves, validation test, thermal impedance, and structure functions. (b) Type 5-2 results.

MOSFET channel is fully turned off, and the sensing current only conducts through the body diode. The cooling curves and the validation test for Type 4-2 are shown in Fig. 6(e), which exhibit excellent consistency. Furthermore, as shown in Fig. 6(f), Type 4-1 and Type 4-2 methods provide the obtained structure functions and junction-to-case thermal resistance, respectively. Their obtained junction-to-case thermal resistances R_{thjc} exhibit slight variations. Moreover, the dashed-box area as shown in the left of Fig. 6(f) has multiple minor differences. These underperformances are difficult to be identified by complying the current standard [7].

VII. Type 5 Circuits Based on Source-Drain Voltage with Switching Gate States

Type 5 features a switching gate state. During the heating stage, a positive gate voltage is applied. Subsequently, the heating current is switched off and a sensing current flows through the body diode to measure the junction temperature. The detailed working principle of Type 5 should refer to [17]. Since the TSEP is identical to that of Type 4, the calibration study is not repeated here. A sensing current of $I_{\text{sense}} = 100$ mA and a gate voltage of $V_{\text{gs,off}} = -6$ V are selected directly.

The performances of Type 5-1 and 5-2 are shown in Figs. 7(a) and (b), respectively. The good consistency of both validation tests indicates the reproducibility of their measured thermal structure properties. Moreover, the application of the standard double-interface testing in both thermal impedance and structure functions also demonstrates consistent $R_{\text{thjc}} = 0.8$ K/W.

VIII. Cross-Comparison of Different Testing Methods

A. Summary of the FOM based on All the Testing Methods

As shown in Fig. 8, all five factors of the FOM are summarized. Among them, Type 3 to 5 using the body diode as TSEP provide the best linearity; Type 1 with $V_{\text{gs,th}}$ has the highest sensitivity; and Type 2 with $R_{\text{ds,on}}$ has the quickest dynamic transient. It should be noted that while all TSEPs can provide successful calibrations, not all of them are capable of extracting reproducible thermal structures. This finding challenges a common assumption that successful calibration ensures obtaining the correct thermal structure. Therefore, the first four factors from FOM_1 to FOM_4 only guide a trade-off to select testing conditions and achieve better calibration. FOM_5 validates the reproducibility of the obtained result.

B. Comparison of the Four Feasible Methods

The comparison of the transient recovery of the four feasible circuits is shown in Fig. 9(a). Type 4-2 and Type 5-2 exhibit the quickest dynamic since they both utilize the body diode for both heating and sensing. Type 5-1, which uses the forward channel for heating and the body diode with reverse direction for measurement, shows a slower transient. Type 1-1 exhibits the slowest transient speed, which is consistent with the aforementioned FOM study.

Meanwhile, the comparison of the measured thermal impedance is shown in Fig. 9(b). The results indicate that Type 4-2, Type 5-1, and Type 5-2 have highly similar thermal impedance curves, diverging at around $R_{\text{th}} = 0.8$ K/W. The thermal impedance curve of Type 1-1 is slightly shifted downward. To validate them, we compared them with the datasheet-provided thermal impedance, which is more consistent with Type 4-2, Type 5-1, and Type 5-2. This observation suggests that the obtained results of Type 4-2, Type 5-1, and Type 5-2 may be more accurate. A further validation using FVM simulation will be applied to verify it again.

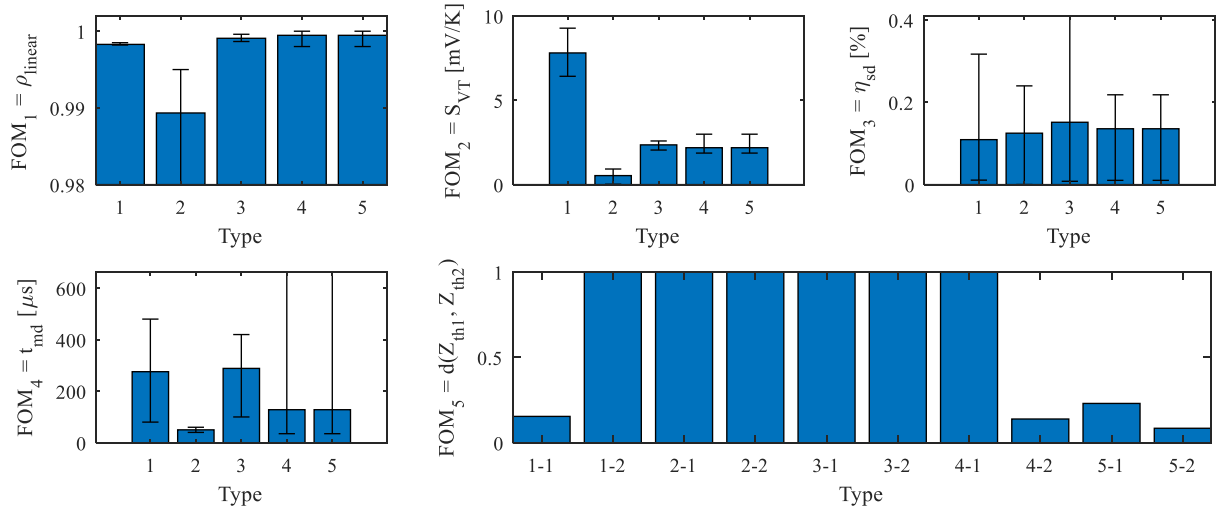


Fig. 8. Comparison of all the ten plausible testing circuits based on the proposed FOM. (Data from Figs. 3-7, where histograms represent mean values, and error bars show their minimum and maximum values. For instance, considering Type 1 test shown in Fig. 3(a), the device is tested under five different sensing current, and the resulted outcomes are unbiased summarized here.)

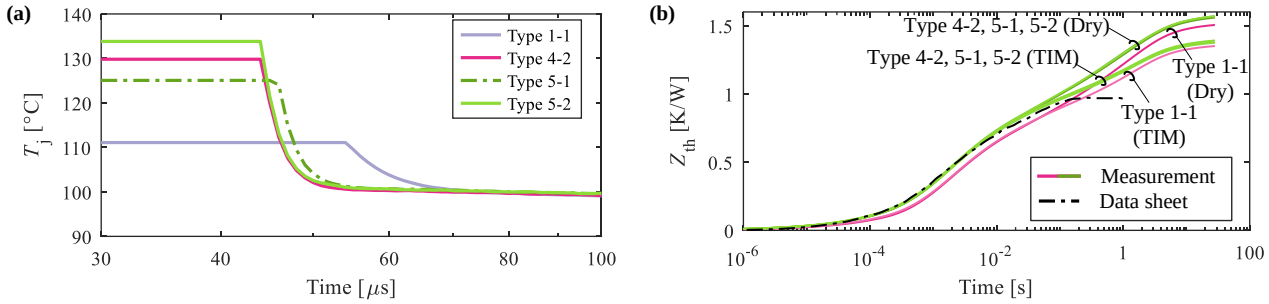
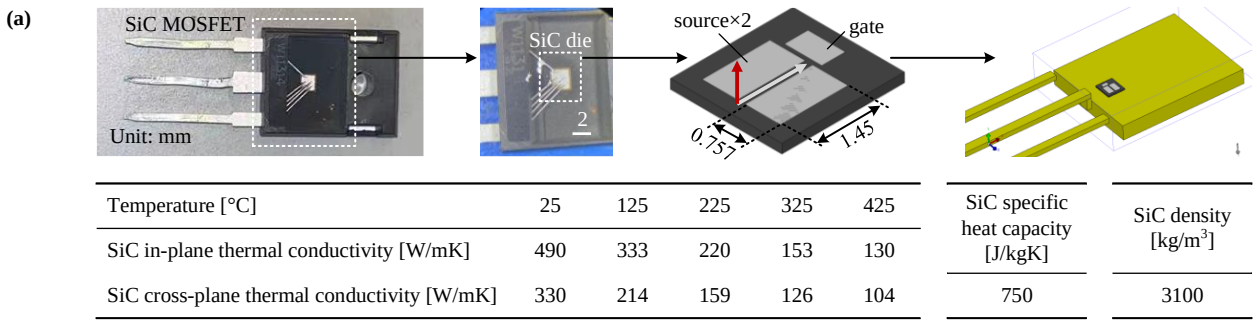


Fig. 9. Comparison of the four feasible testing circuits. (a) the transient speed and (b) thermal impedance curves and comparing to the data sheet (The data sheet provides junction-to-case thermal impedance. This work measures the junction-to-ambient thermal impedance complying with the standard [7]).



Temperature [°C]	25	125	225	325	425	SiC specific heat capacity [J/kgK]	SiC density [kg/m^3]
SiC in-plane thermal conductivity [W/mK]	490	333	220	153	130		
SiC cross-plane thermal conductivity [W/mK]	330	214	159	126	104	750	3100

Fig. 10. Building a high-fidelity simulation model to verify the accuracy of the obtained thermal structure. (a) Open the package of the device and build a virtual model: the figure contains measured dimensions of the SiC chip and the used material properties, where the thermal conductivity considers temperature dependence and anisotropy of the SiC. (b) and (c) compare the measuring results to the simulation results (within the chip area) under two different power losses.

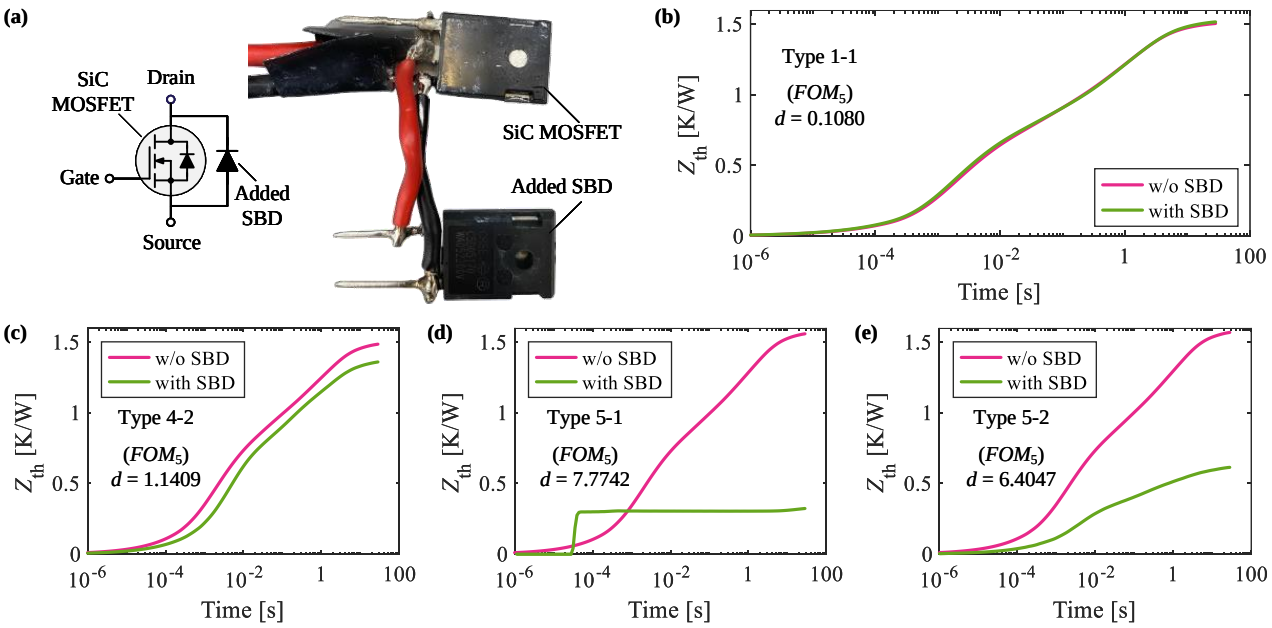


Fig. 11. Feasibility of the SiC MOSFET with an anti-parallel Schottky barrier diode (SBD). (a) Circuit of the SiC MOSFET with SBD and the experimental photo, (b) Obtained thermal impedance with and without the added SBD via Type 1-1, (c)-(e) the corresponding results by Type 4-2, Type 5-1, and Type 5-2.

TABLE I
SUMMARY OF FIGURES-OF-MERIT FOR THERMAL TRANSIENT MEASUREMENT.

FOM	Testing process	Purposes	Definition	Expected value
FOM_1	Calibration	Help to determine proper testing conditions: • FOM_1 to FOM_3 consider the impact of the testing condition settings on the static performances of calibration results; • FOM_4 considers the dynamic impact of testing conditions.	ρ_{linear} in (1)	The closer to 1, the better. A perfect linearity is 1.
FOM_2			S_{VT} in (2)	The larger the value, the better. $S_{\text{VT}} \geq 1$ mV/K is adopted in this paper.
FOM_3			η_{sd} in (3)	The smaller the value, the better. $\eta_{\text{sd}} \leq$ 1% is adopted in this paper.
FOM_4			t_{md} in (4)	The smaller the value, the better. $t_{\text{md}} \leq 100$ µs is selected via the calculation of (4).
FOM_5	Cooling curve measurement	Justify the electrical interference during the thermal transient measurement.	d in (5)	The smaller the value, the better. An ideal case has $d = 0$.

C. Verification of Measurement through FVM Simulation

To further validate the accuracy of the obtained results from different testing circuits, a FVM simulation is employed. While the thermal impedance curve provided in the datasheet appears to be more consistent with Type 4-2, Type 5-1, and Type 5-2 in the aforementioned discussion, it is still challenging to conclusively determine which testing circuits provide the most accurate results. To verify this, a high-fidelity simulation is conducted, as shown in Fig. 10. The MOSFET is opened exposing the internal details of the package. The measured die dimensions and the established 3D simulation model in Simcenter Flotherm [31] are shown in Fig. 10(a). The used material properties are also provided in the figure, where the temperature-dependence and anisotropic thermal conductivity have also been fully considered in the simulation model. The simulation primarily focuses on the chip to avoid intensive material and geometrical uncertainties in terms of multiple packaging layers.

The results of the subsequent analysis comparing the measured thermal structure with the calibrated model is shown in Figs. 10(b) and (c). Note that since Type 5-1 and Type 5-2 are consistent with Type 4-2, only the results of Type 4-2 are illustrated here. As depicted in Fig. 10(b), the structure function given by Type 1-1 indicates a higher thermal capacitance in the chip area, but the simulation result aligns more closely with Type 4-2. Furthermore, with increased power losses, the simulation result still agrees with Type 4-2. Thus, these findings suggest that the thermal impedance obtained from the testing circuits of Type 4-2, Type 5-1, and Type 5-2 is more accurate.

D. Comparative Analysis of Testing Circuit Feasibility in the Presence of Anti-Parallel Schottky Barrier Diode

Some SiC MOSFETs have anti-parallel SBDs, which pose challenges in using the body diode for temperature measurement. As shown in Fig. 11(a), the added SBD creates an additional path for the sensing current, potentially leading to inaccurate temperature measurements. Previous literature suggests cutting off the SBD's path, but it damages devices.

In this study, an additional SBD is intentionally connected to the tested SiC MOSFET to evaluate the feasibility of the different testing circuits. The TSEPs are recalibrated for each circuit, and the obtained thermal impedance curves are presented in Figs. 11(b)-(e). Among the four circuits, only Type 1-1 is not affected by the presence of the additional SBD. In contrast, the other three circuits are significantly disturbed and cannot produce accurate results. Therefore, although Type 1-1 was deemed less accurate in the aforementioned study, it is still a feasible method for temperature measurement in SiC MOSFETs with SBDs without damaging the devices.

IX. Conclusion

This study systematically investigates the thermal transient measurement of SiC MOSFETs, offering a comparison and verification of ten plausible testing circuits and three TSEPs through simulations and experiments. The purposes, definitions, and expected values of the proposed FOM are summarized in Table I. The key conclusions are summarized as follows:

1) A FOM study is provided for reproducible TTM of SiC MOSFETs, which comprises three static and two dynamic factors. The first four factors offer a quantitative way to guide a trade-off of testing conditions. The last factor provides a validation protocol to address potential electrical interference in measured thermal transients. Notably, this study reveals that electrical interference is not limited to the initial moment of the cooling curve (transient I) but can extend to the commonly regarded thermal transient (transient II), which is often overlooked in previous literature.
2) Four testing methods are identified as feasible for the tested SiC MOSFET. Type 4-2, Type 5-1, and Type 5-2 are recommended when the device does not have an SBD. Type 1-1 is feasible for the MOSFET with an SBD but it provides less accurate thermal structure.
3) The common assumption that successful calibration guarantees reproducible TTM results is incorrect. It is crucial to recognize that some erroneous tests (e.g., Type 1-2) can provide seemingly perfect thermal impedance and structure functions, but actually yield incorrect thermal structure properties. The proposed validation test with FOM_5 can help to identify this potential risk.
4) The existing standards developed for Si devices have certain limitations when applied to SiC devices. Based on the findings of this study, the authors suggest the inclusion of necessary validation protocols and quantified guidelines for setting testing parameters in future standards. Ignoring these conditions may result in the incomparability of different testing results and could lead to misleading thermal characterization of SiC devices.

References

[1] Y. Zhang, H. Wang, Z. Wang, F. Blaabjerg, and M. Saeedifard, "Mission profile-based system-level reliability prediction method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6916–6930, Jul. 2020.

[2] M. Janicki, J. Banaszczyk, G. De Mey, M. Kaminski, B. Vermeersch, and A. Napieralski, "Application of structure functions for the investigation of forced air cooling," in *Proc. 13th Int. Workshop Therm. Invest. ICs Syst. (THERMINIC)*, 2007, pp. 2–5.

[3] G. Farkas, Z. Sarkany, and M. Rencz, "Structural analysis of power devices and assemblies by thermal transient measurements," *Energies*, vol. 12, no. 14, p. 2696, 2019.

[4] T. Yin, L. Lin, C. Xu, D. Zhu, and K. Jing, "A hybrid modular multilevel converter comprising SiC MOSFET and Si IGBT with its specialized modulation and voltage balancing scheme," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11 272–11 282, Nov. 2021.

[5] K. Hamada, M. Nagao, M. Ajioka, and F. Kawai, "SiC—emerging power device technology for next-generation electrically powered environmentally friendly vehicles," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 278–285, Feb. 2015.

[6] JEDEC, "EIA/JESD 51-1: Intergrated circuits thermal measurement method-electrical test method (single semiconductor device)," 1995.

[7] ——, "JESD51-14: Transient dual interface test method for the measurement of the thermal resistance junction-to-case of semiconductor devices with heat flow through a single path," 2010.

[8] V. Szekely, "A new evaluation method of thermal transient measurement results," *Microelectronics J.*, vol. 28, pp. 277–292, 1997.

[9] T. Kestler and M.-M. Bakran, "Junction temperature measurement of SiC MOSFETs: Straightforward as it seems?" in *Proc. Int. Exhibition Conf. Power Electron., Intell. Motion, Renewable Energy Manage. (PCIM Europe)*, 2018, pp. 1–6.

[10] G. Zeng, H. Cao, W. Chen, and J. Lutz, "Difference in device temperature determination using pn-junction forward voltage and gate threshold voltage," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2781–2793, Mar. 2019.

[11] F. Yang, E. Ugur, and B. Akin, "Design methodology of DC power cycling test setup for SiC MOSFETs," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 4, pp. 4144–4159, Dec. 2020.

[12] F. Hoffmann, S. Rugen, D. Silber, and N. Kaminski, "Impact of the sensing current density on pn-junction based temperature estimation methods for Si and SiC power devices," *Microelectron. Reliab.*, vol. 114, no. 113834, 2020.

[13] F. Wagner, G. Reber, M. Rittner, M. Guyenot, M. Nitzsche, and B. Wunderle, "Power cycling of SiC-MOSFET single-chip modules with additional measurement cycles for life end determination," in *Proc. 11th Int. Conf. Integrated Power Electron. Systems (CIPS)*, 2020, pp. 1–6.

[14] T. Funaki and S. Fukunaga, "Difficulties in characterizing transient thermal resistance of SiC MOSFETs," in *Proc. 22nd Int. Workshop Therm. Invest. ICs Systems (THERMINIC)*, 2016, pp. 141–146.

[15] C. Herold, J. Sun, P. Seidel, L. Tinschert, and J. Lutz, "Power cycling methods for SiC MOSFETs," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, 2017, pp. 367–370.

[16] Y. Zhang, Y. Zhang, Z. Xu, Z. Wang, H. Wong, Z. Lu, and A. Caruso, "A guideline for silicon carbide MOSFET thermal characterization based on source-drain voltage," in *Proc. IEEE Appli. Power Electron. Conf. Expo. (APEC)*. IEEE, 2023, pp. 378–385.

[17] Y. Zhang, Y. Zhang, Z. Xu, Z. Wang, V. H. Wong, Z. Lu, and A. Caruso, "Guideline for reproducible SiC MOSFET thermal characterization based on source-drain voltage," *IEEE Trans. Ind. Appli.*, Early Access.

[18] Z. Sarkany, W. He, and M. Rencz, "Temperature change induced degradation of SiC MOSFET devices," in *Proc. 15th IEEE Int. Conf. Therm. Thermomech. Phenom. Electron. Systems (ITherm)*, 2016, pp. 1572–1579.

[19] J. O. Gonzalez and O. Alatise, "Impact of the gate driver voltage on temperature sensitive electrical parameters for condition monitoring of SiC power MOSFETs," *Microelectron. Reliab.*, vol. 76, pp. 470–474, 2017.

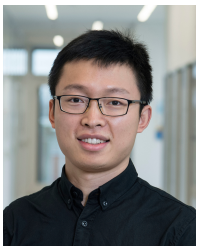
[20] T. Ziemann, U. Grossner, and J. Neuenschwander, "Power cycling of commercial SiC MOSFETs," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, 2018, pp. 24–31.

[21] F. Gothner, O. C. Spro, M. Herncs, and D. Peftitsis, "Challenges of SiC MOSFET power cycling methodology," in *Proc. 20th Eur. Conf. Power Electron. Appl. (EPE'18 ECCE Europe)*, 2018.

[22] F. Hoffmann and N. Kaminski, "Evaluation of the Vsd-method for temperature estimation during power cycling of SiC-MOSFETs," *IET Power Electronics*, vol. 12, no. 15, pp. 3903–3909, 2019.

[23] F. Yang, E. Ugur, and B. Akin, "Evaluation of aging's effect on temperature-sensitive electrical parameters in SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6315–6331, Jun. 2020.

[24] H. Guo, C. Guo, L. Wei, and Y. Liu, "Junction temperature measurement method for thermal resistance testing of SiC MOSFET module," in *Journal of Physics: Conference Series*, vol. 1907, no. 1, 2021.
[25] M.-K. Kim and S. W. Yoon, "Thermal impedance characterization using optical measurement assisted by multi-physics simulation for multi-chip SiC MOSFET module," *Micromachines*, vol. 11, no. 12, p. 1060, 2020.
[26] "C2M0160120D," https://assets.wolfspeed.com/uploads/2020/12/C2M0160120D.pdf, accessed: 23-07-2023.
[27] "SIEMENS Simcenter Micred Power Tester," https://plm.sw.siemens.com/en-US/simcenter/physical-testing/powertester/, accessed: 10-01-2024.
[28] "C3M0060065K," https://assets.wolfspeed.com/uploads/2020/12/C3M0060065K.pdf, accessed: 23-07-2023.
[29] M. Glavanovics and H. Zitta, "Thermal destruction testing: an indirect approach to a simple dynamic thermal model of smart power switches," in *Pro. 27th Eur. Solid-State Circuits Conf.*, 2001, pp. 221–224.
[30] K. M. Baron, K. Sharma, and I. Kallfass, "Virtual junction temperature estimation during dynamic power cycling tests," in *Proc. 11th Int. Conf. Power Electron. ECCE Asia*, 2023, pp. 3193–3199.
[31] "Simcenter flotherm software," https://plm.sw.siemens.com/en-US/simcenter/fluids-thermal-simulation/flotherm/, accessed: 2023-05-02.



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