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Optimal Modulation Method for Reducing Ripple Current and Power Loss of DC-link Capacitor in Multi-drive Systems

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***Abstract*-- This paper proposes a modulation method that can significantly reduce the ripple current and power loss of the DC-link capacitor of multi-drive systems. It is based on a derived analytical model for capacitor ripple current with an arbitrary number of drives connected in parallel at the DC-link side. Both the low-frequency and high-frequency current components are minimized by the optimal phase shift of modulation and carrier signals. Benchmark studies of multi-drive systems with 2 to 20 drives reveal that the total capacitor Root Mean Square (RMS) current is reduced to 34.3%~15.9%. Proof-of-concept experimental results from multi-drives with identical and different individual loading conditions verify the theoretical analysis and effectiveness of the proposed method.**

***Index Terms*-- Modulation method, DC-link capacitor, multi-drive systems, ripple current**

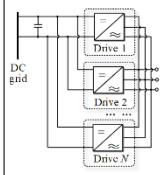
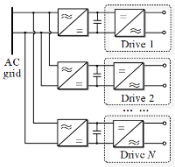
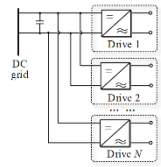
I. INTRODUCTION

Recently, multi-drive system concepts have been used in industrial and residential applications [1] [2]. There are three typical configurations of multi-drive systems: DC side parallel with single AC load [3], [4]; grid-side parallel with multiple AC loads [5], [6]; and DC-link parallel with multiple AC loads [7]–[9], as shown in Table I.

The common DC-link system has been advocated as a possibility for future integration of drives to reduce the number of conversion stages, improve reliability, and optimize the cost and volume, as shown in Fig.1 [10]. One of the concerns in such a system is the ripple current generated by multiple drives, which affects the long-term performance of the DC-link capacitor [11] [12].

In the multi-drive system, the method in [13] considers the phase shifts of modulation signals to reduce the low-order harmonics of the capacitor current. However, the derived model in this method has mandatory conditions to configure the individual rectifiers for the DC-link of each drive. A method is proposed to reduce the ripple current of the DC link capacitors by extracting the switching signals of the drives [14], which need the shared single AC load for multiple drives. Although a modulation method using phase shifts of carrier signals is given in [15], it can not deal with the effects of low-order harmonics superimposed by the individual loads in multi-drive systems. A method is presented to suppress DC link current harmonics by phase shifts of the carrier and the modulation signals [10]. However, this method cannot be used to quantitatively analyze the optimal phase shift in systems with more than two drives.

TABLE I
THREE CONFIGURATIONS OF THE MULTI-DRIVE SYSTEMS.

	Configuration 1	Configuration 2	Configuration 3
Definition	DC-side parallel with one AC load	Grid-side parallel with multiple AC loads	DC-link parallel with individual AC loads
Structure			
Application	On-board ships, electric vehicle (EV)	Paper, metal, mining, marine, and production lines applications	
Advantage	High power drives for AC load	Configurable individual AC loads	Lightweight of the system
Limitations	Single AC load application	Multiple rectifiers for the DC link of each drive	High ripple currents in DC link

This paper proposes a modulation scheme to minimize the DC-link capacitor current ripple for multi-drive systems with DC-side parallel and individual AC loads. The contribution lies in two aspects: 1) the DC-link capacitor ripple current is analytically derived applicable for systems with different number of drives connected in parallel; 2) the modulation scheme features with optimal phase-shifts of both the low-frequency modulation signals and switching-frequency carrier signals among the drives.

The structure of this paper is as follows: Section II presents the proposed optimal modulation modeling; Section III gives the case study; Section IV discusses the experimental verification, followed by the conclusions.

II. PROPOSED OPTIMAL MODULATION MODELING

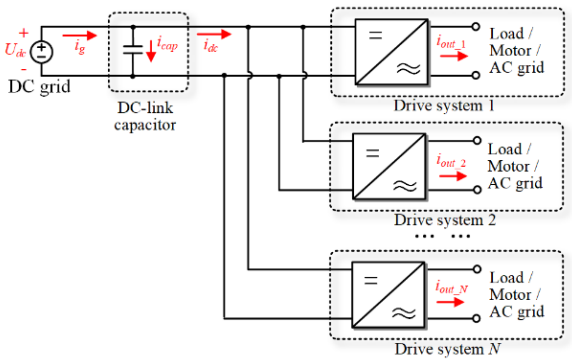
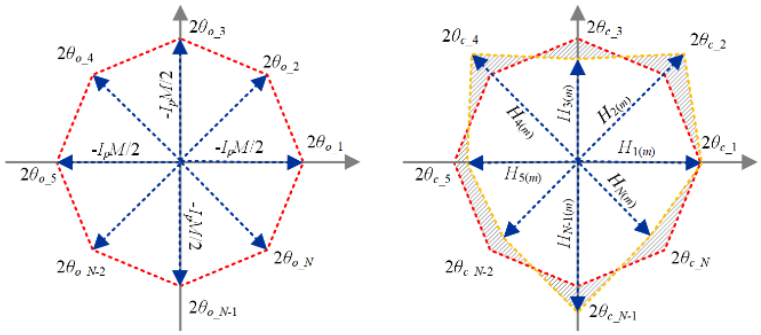


Fig. 1: Configuration of a multi-drive system.



(a) Optimal phase shift for modulation signals (b) Optimal phase shift for carrier signals

Fig. 2: Optimal phase shift of modulation and carrier signals.

The DC-link current of a drive consists of the DC component, low-frequency harmonic, and high-frequency harmonic [16]. The DC component i_{dc_DC}, the low-frequency harmonic component (double-fundamental frequency) i_{dcl}, and the high-frequency harmonic component (m^{th}-order harmonic of the carrier frequency) i_{dch} can be given as:

$$\begin{cases} i_{dc\_DC} = \dfrac{I_p M}{2} \\ i_{dcl} = -\dfrac{I_p M}{2}\cos\left(2\left(\omega_0 t + \theta_0\right)\right) \\ i_{dch} = \displaystyle\sum_{m=2,4,\ldots}^{\infty}\left[\begin{array}{l}(-1)^{\frac{m}{2}}\dfrac{8 I_p M}{\pi m} \\ \times\sin\left(\omega_0 t+\theta_0\right)\cos\left(m\left(\omega_c t+\theta_c\right)\right) \\ \times\displaystyle\sum_{n=1,3,\ldots}^{\infty}\left[J_n\left(\frac{\pi m M}{2}\right)\sin\left(n\left(\omega_0 t+\theta_0\right)\right)\right]\end{array}\right] \end{cases} \quad (1)$$

where I_P and M represent the amplitude of the AC current and the modulation ratio, respectively. ω_o, ω_c, θ_o, and θ_c represent the angular velocity of the modulation signal and the carrier signal, the phase angle of the modulation signal and the carrier signal, respectively. $J_n(\pi mM/2)$ is the Bessel function.

Multiple drives share a common DC bus in Fig.1. The i_{dcl} for multiple drives can be given as:

$$i_{dcl} = -\frac{1}{2} I_p M \sum_{i=1}^{N}\left[\cos\left(2\left(\omega_0 t + \theta_{0\_i}\right)\right)\right] \quad (2)$$

where θ_{o_i} is the shift phase angles of the modulation signals of the i^{th} drive, and N is the number of drives.

The magnitude of the low-frequency harmonic current I_{dcl_mag} can be simplified as:

$$I_{dcl\_mag} = -\frac{I_p M}{2} \times\sqrt{\left[\sum_{i=1}^{N}\sin\left(2\theta_{0\_i}\right)\right]^2+\left[\sum_{i=1}^{N}\cos\left(2\theta_{0\_i}\right)\right]^2} \quad (3)$$

The high-frequency harmonic current of the m^{th}-order

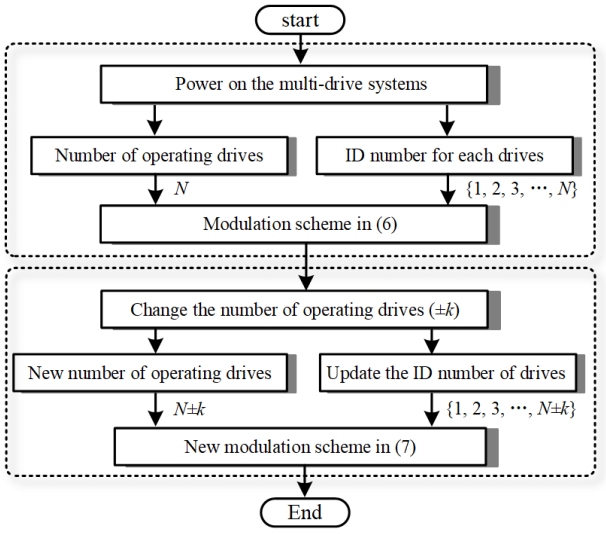


Fig. 3. Proposed optimal modulation scheme.

carrier frequency $i_{dch(m)}$ can be expressed as:

$$\begin{cases} i_{dch(m)} = \displaystyle\sum_{i=1}^{N} H_{i(m)}\cos\left(m\left(\omega_c t+\theta_{c\_i}\right)\right) \\ H_{i(m)} = \dfrac{(-1)^{\frac{m}{2}} 8 I_p M}{\pi m}\sin\left(\omega_0 t+\theta_{0\_i}\right) \\ \quad \times\displaystyle\sum_{n=1,3,\ldots}^{\infty}\left[J_n\left(\frac{\pi m M}{2}\right)\sin\left(n\left(\omega_0 t+\theta_{0\_i}\right)\right)\right] \end{cases} \quad (4)$$

where θ_{c_i} represents the phase shift angles of the carrier signals of the i^{th} drive.

The magnitude of the m^{th}-oder harmonic of the carrier frequency $I_{dch(m)\_mag}$ can be simplified as:

$$I_{dch(m)\_mag} = \sqrt{\left[\sum_{i=1}^{N} H_{i(m)}\sin\left(m\theta_{c\_i}\right)\right]^2+\left[\sum_{i=1}^{N} H_{i(m)}\cos\left(m\theta_{c\_i}\right)\right]^2} \quad (5)$$

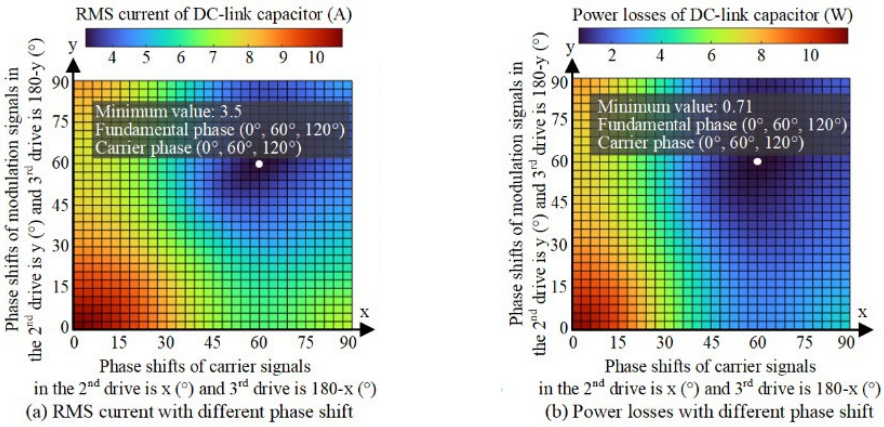


Fig. 4. RMS current and power losses of DC-link capacitor by the analytical equations. (The numerical results are specific to the system with the specifications shown in Table I discussed later in Section IV; results in Fig. 4(b) is calculated based on the frequency-dependent equivalent series resistance (ESR) values and DC-link capacitor ripple current spectrum.)

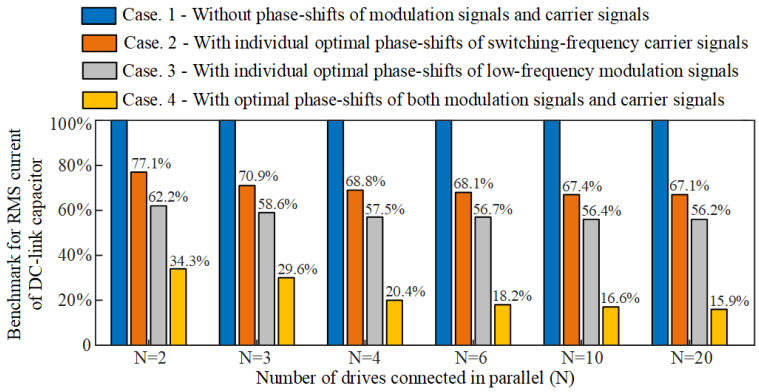


Fig. 5. Benchmark for the RMS value of DC-link capacitor ripple current

According to (3), when the $2\theta_{o\_i}$ in multi-drive systems is equally divided into 360°, thus low-frequency current harmonics can be completely canceled, as shown in Fig. 3(a). According to (5), the $2\theta_{c\_i}$ can also be equally divided into 360°, which can significantly reduce the high-frequency current harmonic components. It should be noted that the above phase-shifting method cannot eliminate all the high-frequency harmonics since $H_{i(m)}$ magnitudes are unequal in different drives. The remaining high-frequency current components can be represented by the shaded area in Fig. 3(b).

Since the selection of the phase shift of carrier signals or modulation signals depends on the number of running drives. The implementation of the proposed optimal modulation scheme is described in Fig. 3.

When the number of drives is N, the θ_{o_i} and θ_{c_i} of the i^{th} drive are:

$$i \in \{1,2,\cdots,N\} \qquad \theta_{0\_i} = \theta_{c\_i} = \left\{\frac{180}{N}\times(i-1)\right\} \tag{6}$$

When the number of drives changes (increased or decreased by k), it is only necessary to update the currently operating drives to 1 ~ (N ± k). At this time, the θ_{o_i} and θ_{c_i} of the i^{th} drive are:

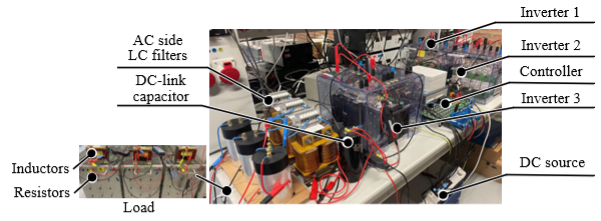
$$i \in \{1,2,\cdots,N\pm k\} \qquad \theta_{0\_i} = \theta_{c\_i} = \left\{\frac{180}{N\pm k}\times(i-1)\right\} \tag{7}$$

The number of operating drives can be judged by monitoring their output AC side current $iout_1$, $iout_2$, ..., $iout_N$. This is common practice in commercial drives to have output current measurement for control and protection purpose.

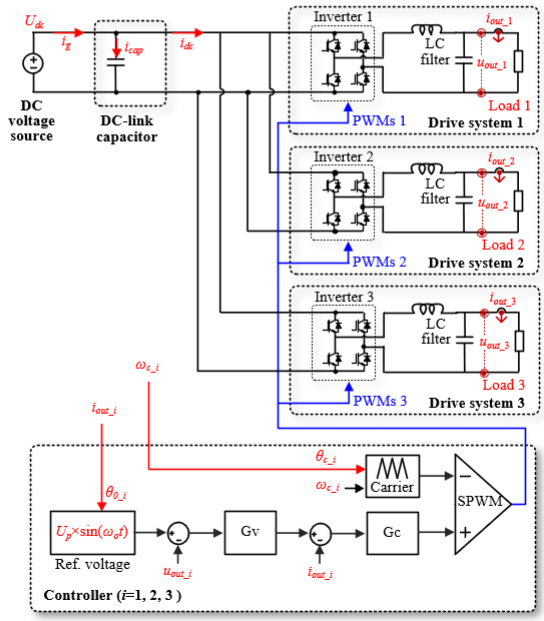
III. DC-LINK CAPACITOR CURRENT AND BENCHMARK

Fig. 4 shows the RMS current and power loss of the DC-link capacitors with different carrier and modulation phase shifts by the analytical equations with three drives. Both optimal phase shift angles of carrier signals and modulation signals are 0°, 60, and 120° when N=3, which agrees well with (6).

The benchmark of the DC-link capacitor RMS current is further analyzed in Fig. 5. The RMS current ratios of DC-link capacitors, including four phase shift cases of carrier signals and modulation signals are compared. The RMS current of the DC-link capacitor with the proposed modulation method is only 34.3% to 15.9% of that without phase shift from 2 to 20 drives, respectively.



(a) Experimental prototype of the multiple drives



(b) Schematic diagram of the experimental prototype

Fig. 6. Prototype of the multi-drive system.

IV. EXPERIMENTAL VERIFICATION

The experimental platform and the control schematic are shown in Fig. 6, where three drives are connected in parallel. Each drive applies a full-bridge inverter, which consists of four IGBTs (with antiparallel diodes). In addition, each drive is configured with an LC-type filter and a load. The control schematic is presented in Fig. 5(b), where a double-loop control method is adopted. Firstly, the reference voltage $U_P \times \sin(\omega_0 t)$ is given, in which the voltage amplitude U_P is 110 V, and the frequency ω_0 can be changed along with different motor speed. Compared to the reference voltage and the measurement voltage u_{out_i}, the voltage error goes through a PI voltage controller (Gv) to generate the reference current. Similarly, the current error, generated by comparing the reference current and the feedback current i_{out_i}, passes through a PI current controller Gc to generate modulation ratios of full-bridge inverters. Finally, the triangular carrier (switching frequency is ω_{c_i}) and the modulation ratios can generate the PWM signals through modulation methods, where the pulse signal PWMs 1-3 are set for drive system 1-3, respectively. It should be noted that a dead time of 200 *ns* is set in the SPWM.

TABLE II
SYSTEM PARAMETERS.

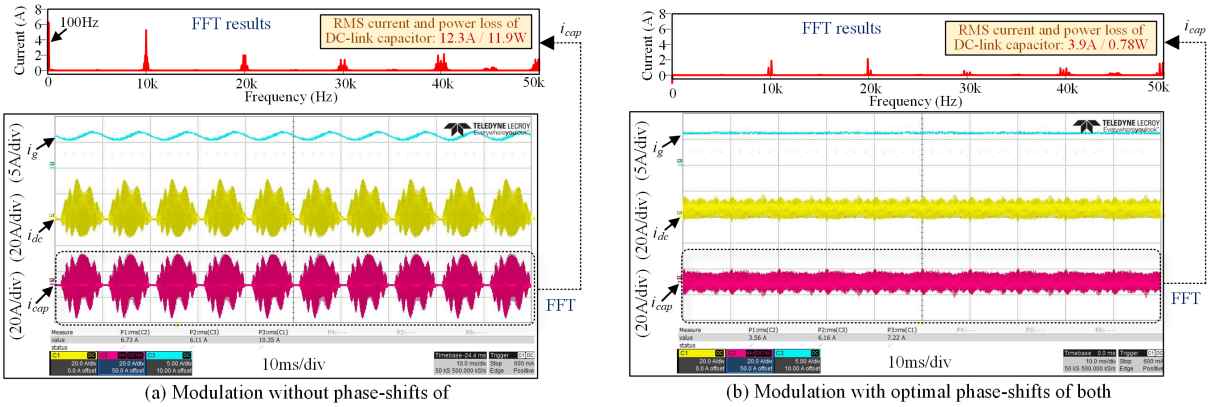
DC source output voltage	150 V
AC side output voltage	110 V
Capacitance of DC-link capacitor	2.75 mF (100 Hz)
ESR of DC-link capacitor	122 mΩ (100 Hz)
LC filters on the AC side	2 mH / 40 μF
AC side loading of three drives	Condition 1: 20 Ω / 20 Ω / 20 Ω
	Condition 2: 20 Ω / 25 Ω / 33 Ω
Switching frequency	5000 Hz
Fundamental frequency	50 Hz
Modulation ratio	0.8
PWM dead time	5×10^{-7} s

The specifications are shown in Table II, including two conditions for the same loading (20Ω) and individual loading (20Ω 25Ω 33Ω) in three drives.

Fig. 7 shows the waveforms of the DC-side supply current i_g, the DC bus current i_{dc}, and the capacitor ripple current i_{cap} with the same loading in three drives. The FFT analysis verifies the results that when the phase shifts of the modulation signal angles are 0°, 60°, and 120° in Fig. 7(b), the low-frequency harmonics can be eliminated. When the phase shifts of the carrier signal angles are 0°, 60°, and 120° in Fig. 7(b), the high-frequency harmonic current can be reduced. The calculation shows that the RMS current and power loss of the DC-link capacitor in the proposed optimized modulation scheme are 31.3% and 6.5% in without optimized modulation.

In addition, Fig. 8 shows the waveforms of the capacitor ripple current with individual loading in three drives. Through the calculation, the RMS current and power loss of the DC-link capacitor in the proposed optimized modulation scheme are 34.2% and 13.1% of that in without optimized modulation, which indicates that the proposed method is still effective with individual loading in multiple drive systems.

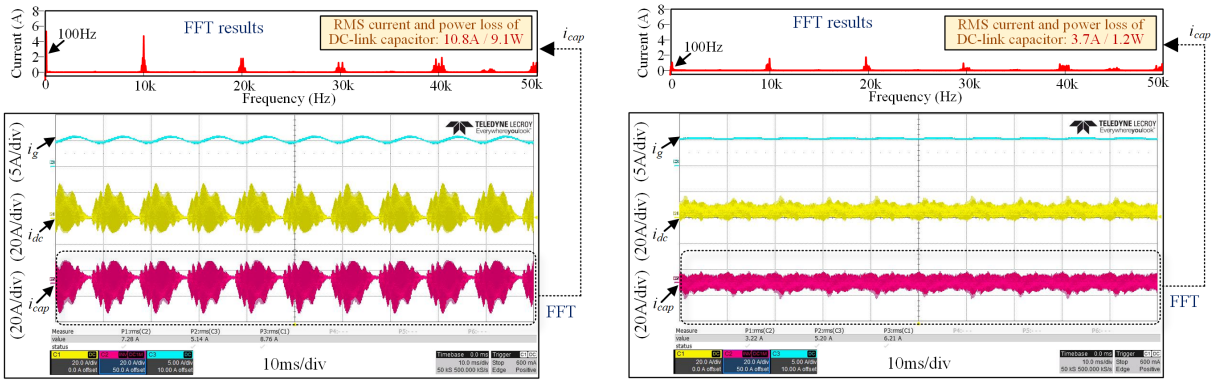
Fig. 9 shows the results under a dynamic change of the number of drives in operation with three modes. Before the change, Mode 1 is three drives with optimal phase shifts. Mode 2 is when the 1st drive is turned off, the 2nd and the 3rd drives keep the same phase shifts. In Mode 2, the DC-side supply current i_g reduces from 6.6 A to 4.4 A since the loading of each drive in operation remains the same. Mode 3 is when the phases shifts of the 2nd and the 3rd drives are updated to the optimal ones according to (8). Comparing the results without and with the update of the phase shifts wtih two drives in Mode 2 and Mode 3, the DC-link capacitor RMS current is 3.8 A and 2.5 A, respectively. Accordingly, its power loss of DC link capacitor is 1.4 W and 0.56 W, respectively. The results imply that the performance can be maintained by updating to the optimal phase shifts according to the number of drives in operation.



(a) Modulation without phase-shifts of low-frequency modulation signals and switching-frequency carrier signals.

(b) Modulation with optimal phase-shifts of both low-frequency modulation signals and switching-frequency carrier signals.

Fig. 7. Measured current waveforms and DC-link capacitor ripple current spectrum with identical loads (20Ω) of the three drives



(a) Modulation without phase-shifts of low-frequency modulation signals and switching-frequency carrier signals.

(b) Modulation with optimal phase-shifts of both low-frequency modulation signals and switching-frequency carrier signals.

Fig. 8. Measured current waveforms and DC-link capacitor ripple current spectrum with different loads (20Ω, 25Ω, 33Ω) of the three drives

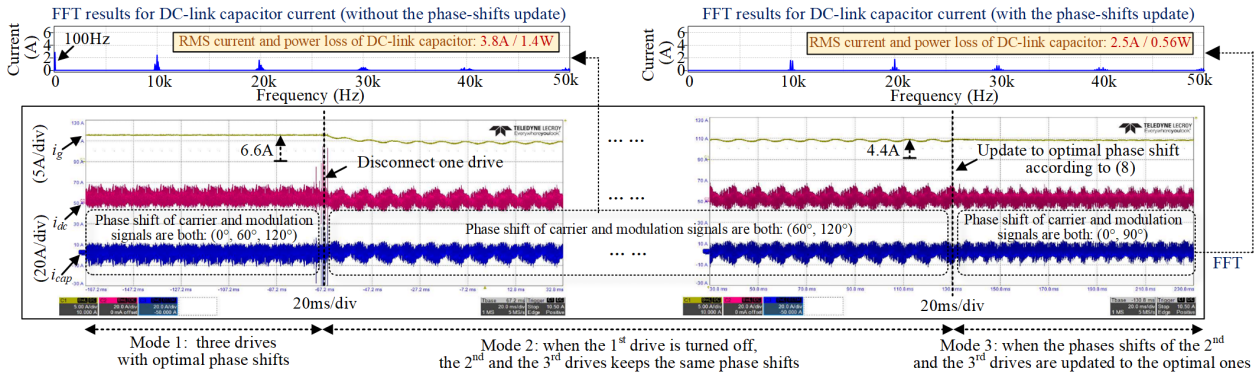


Fig. 9. Experimental current waveforms with switching from three drives to two drives. (ig - DC-side supply current, idc - DC bus current; icap – capacitor ripple current; the corresponding power losses are based on the capacitors used in the experiment.)

V. Conclusions

This digest proposes an optimal modulation method for minimizing the ripple current of DC-link capacitors in multi-drive systems. Based on the derived analytical model, the method can concurrently reduce the low- and high-frequency harmonics of DC-link capacitors and applicable for systems with different number and different loading of drives. The RMS current and power loss of the DC-link capacitor are reduced to 31.3% and 6.5% (with same identical loading condition), 34.2% and 13.2% (with different loading condition), respectively, compared to that of no phase shift, for an experimental setup with three drives based on the proposed method.

References

[1] D. Kumar, F. Zare, and A. Ghosh, “DC microgrid technology: System architectures, AC grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects,” IEEE Access, vol. 5, pp. 12 230–12 256, Jun. 2017.

[2] A. K. Kaviani, B. Hadley, and B. Mirafzal, “A time-coordination approach for regenerative energy saving in multiaxis motor-drive systems,” IEEE Trans. Power Electron., vol. 27, no. 2, pp. 931–941, Feb. 2012.

[3] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "Impact of interleaving on ac passive components of paralleled three-phase voltage source converters," IEEE Trans. Ind. Appl., vol. 46, no. 3, pp. 1042–1054, May-Jun. 2010.
[4] "Slimline IGBT Stacks." Semikron, https://www.semikron.com/products/product-lines/air-cooled-igbt-stacks/ semikube-slimline-igbt-stacks.html, 2022.
[5] H. M. Delpino and D. Kumar, "Line harmonics on systems using reduced DC-link capacitors," in Proc. 39th Annu. Conf. IEEE Ind. Electron., Nov. 2013, pp. 961–966.
[6] H.Wang, S. Huang, D. Kumar, Q.Wang, X. Deng, G. Zhu, and H.Wang, "Lifetime prediction of DC-link capacitors in multiple drives system based on simplified analytical modeling," IEEE Trans. Power Electron., vol. 36, no. 1, pp. 844–860, Jan. 2021.
[7] D. Kumar, P. W. Wheeler, J. C. Clare, and T.-W. Kim, "Weight/volume effective multi-drive system based on two-stage matrix converter," in Proc. 34th Annu. Conf. IEEE Ind. Electron., Nov 2008, pp. 2782–2787.
[8] "The benefits of DC-sharing—focus on drives." Danfoss, https://www.focusondrives.com/the-benefits-of-dc-sharing/, 2015.
[9] "Vacon nxp common DC bus utilize and redistribute energy efficiently."VACON, https://files.danfoss.com/download/DrivesDKDDPB911A122 NXP Common DC Bus LR.pdf, 2016.
[10] S. Baburajan, H. Wang, F. Mandrile, B. Yao, Q. Wang, D. Kumar, and F. Blaabjerg, "Design of common DC-link capacitor in multiple-drive system based on reduced DC-link current harmonics modulation," *IEEE Trans. Power Electron*., vol. 37, no. 8, pp. 9703–9717, Aug. 2022.
[11] H. M. Delpino and D. Kumar, "Line harmonics on systems using reduced DC-link capacitors," in *Proc. Annual Conf. of the IEEE Ind. Electron*. Society, 2013, pp. 961–966.
[12] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—an overview," *IEEE Trans. Ind. Appl*., vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.
[13] Y. Yang, P. Davari, F. Zare, and F. Blaabjerg, "Enhanced phase-shifted current control for harmonic cancellation in three-phase multiple adjustable speed drive systems," *IEEE Trans. Power Del*., vol. 32, no. 2, pp. 996–1004, Apr. 2017.
[14] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt activepower- filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron*., vol. 55, no. 3, pp. 1175–1189, Mar. 2008.
[15] X. Lyu, Y. Li, and D. Cao, "DC-link RMS current reduction by increasing paralleled three-phase inverter module number for segmented traction drive," *IEEE J. Emerg. Sel. Topics in Power Electron*., vol. 5, no. 1, pp. 171–181, Mar. 2017.
[16] F. Vasca and L. Iannelli, *Dynamics and control of switched electronic systems*. London, U.K.: Springer, 2012.