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Advantages and Challenges of a Type-3 PLL

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***Abstract*—A phase-clocked loop (PLL) is a closed-loop feedback control system which synchronizes its output signal in frequency as well as in phase with an input signal. The phase detector, the loop filter, and the voltage controlled oscillator are the key parts of almost all PLLs. Within the areas of power electronics and power systems, which are focused on in this paper, the PLLs typically employ a proportional-integral controller as the loop filter, resulting in a type-2 control system (a control system of type-N has N poles at the origin in its open-loop transfer function). Recently, some attempts have been made to design type-3 PLLs, either by employing a specific second-order controller as the loop filter, or by implementing two parallel tracking paths for the PLL. For this type of PLLs, however, the advantages and limitations are not clear at all, as the results reported in different literature are contradictory, and there is no detailed knowledge about their stability and dynamic characteristics. In this paper, different approaches to realize a type-3 PLL are examined first. Then, a detailed study of dynamics and analysis of stability, followed by comprehensive parameters design guidelines for a typical type-3 PLL are presented. Finally, to get insight into the advantages/limitations of this type of PLLs, the performance of a well-tuned type-3 PLL is compared with a conventional synchronous reference frame PLL (which is a type-2 PLL) through extensive experimental results and some theoretical discussions.**

***Index Terms*—Phase-locked loop (PLL), synchronization, type-3 systems, synchronous reference frame PLL (SRF-PLL).**

I. Introduction

PHASE-LOCKED loops (PLLs) are widely used in different applications within the areas of power electronics and power systems, particularly for synchronization and control purposes in distributed generation systems, custom power equipment, flexible AC transmission systems (FACTS), uninterruptible power supplies (UPS), HVDC transmission systems, etc. [1]-[3]. The PLLs have also found widespread applications in synchronized phasor measurement units (PMUs), power quality instruments, sensorless control of AC machines, and estimation of harmonics, inter-harmonics, sequence components, and peak values [4]-[6].

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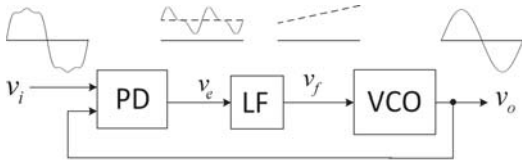


Fig. 1. Basic scheme of a typical PLL.

Generally speaking, a PLL is a closed-loop feedback control system which synchronizes its output signal in frequency as well as in phase with an input signal. Three building blocks are common to most PLL designs: 1) a phase detector (PD), a loop filter (LF), and a voltage controlled oscillator (VCO). Fig. 1 shows the block diagram of a typical PLL.

Within the areas of power electronics and power systems, which are focused on in this paper, the PLLs typically employ a proportional-integral (PI) controller as the LF, resulting in a type-2 control system [7]. A control system of type-N has N poles at the origin in its open-loop transfer function. There are a large number of publications that cover the study of dynamics and properties of these PLLs, among which [8]-[10] are the most recent ones.

Recently, some attempts have been made to design the type-3 PLLs for different areas of application, like synchrophasor measurement units, grid connected power converters, speed motor control systems, etc. [4], [11], [13]-[17]. As reviewed in section II, these approaches can be broadly classified into two categories as single-loop methods, in which the PLL has a single tracking loop and uses a second-order transfer function, with a double pole at the origin and a pair of zeros, as LF, and the dual-loop methods, in which the PLL uses two parallel tracking paths. For this type of PLLs, however, the advantages and limitations are not clear at all, as the reported results are contradictory, and there is no detailed information about their stability and dynamic characteristics.

In this paper, different approaches to realize a type-3 PLL are examined first. Then, based on its small-signal model, a detailed study of dynamics and stability of a typical type-3 PLL is performed, and comprehensive design guidelines are proposed. Finally, through extensive experimental results and some theoretical discussions, the performance of the well-tuned type-3 PLL is compared with a conventional synchronous reference frame PLL (SRF-PLL), which is a typical type-2 PLL.

II. Different Approaches To Realize A Type-3 PLL

In this section, different approaches to realize a type-3 PLL are investigated. In each case, the general structure

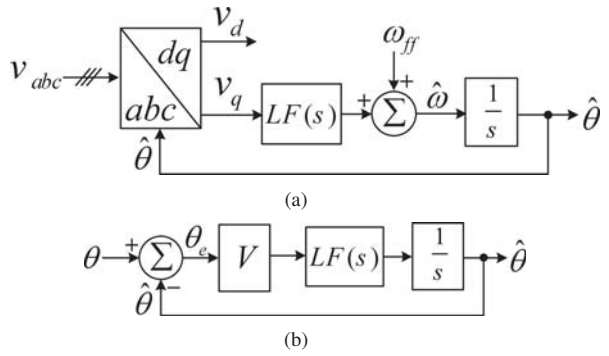


Fig. 2. (a) Basic scheme of a conventional SRF-PLL, and (b) its small-signal model.

is presented, and its advantages and limitations are briefly discussed.

Fig. 2(a) illustrates the basic scheme of a conventional SRF-PLL, in which $LF(s)$ is the LF transfer function. Supposing that, the three-phase input voltages are balanced and undistorted, the small-signal model of the SRF-PLL can be obtained as shown in Fig. 2(b), where θ and $\hat{\theta}$ are the input and estimated phases, respectively, θ_e is the phase error, and V is the input voltage amplitude [7]. It is shown in [7] and [9] that, considering the LF as a proportional-integral (PI) controller (i.e., $LF(s) = k_p + k_i/s$, where k_p and k_i are the proportional and integral gains, respectively) results in a type-2 PLL. The question is: what form of $LF(s)$ is required to realize a type-3 PLL? It is known that, the type-3 PLLs are able to track a frequency ramp input with zero steady-state phase-error [18]. So, to realized a type-3 PLL, $LF(s)$ should be designed such that, for $\theta(s) = \Delta\dot{\omega}/s^3$, where $\Delta\dot{\omega}$ is the frequency ramp rate in $\mathrm{rad/s^2}$, we obtain $\lim_{t\to\infty} \theta_e(t) = 0$.

From Fig. 2(b), the phase-error Laplace transform in response to a frequency ramp input is

$$\theta_e(s) = \frac{s}{s + LF(s)V}\theta(s) = \frac{1}{s^2}\frac{\Delta\dot{\omega}}{s + LF(s)V}. \quad (1)$$

Applying the final value theorem to (1), yields the steady-state phase error, $\theta_{e,ss}$, as

$$\theta_{e,ss} = \lim_{t\to+\infty}\theta_e(t) = \lim_{s\to 0} s\theta_e(s) = \lim_{s\to 0}\frac{1}{s}\frac{\Delta\dot{\omega}}{s + LF(s)V}. \quad (2)$$

For $\theta_{e,ss}$ to be zero, it is required that, LF have a transfer function as $LF(s) = n(s)/s^2$, $n(0) \neq 0$, where $n(s)$ is a polynomial of order smaller than or equal to 2. Based on this, the open-loop transfer function can be obtained, from Fig. 2(b), as

$$G_{ol}(s) = \frac{\hat{\theta}(s)}{\theta_e(s)} = V \times LF(s)\frac{1}{s} = \frac{n(s)V}{s^3}. \quad (3)$$

From (3), it is obvious that, the asymptotic plot of $G_{ol}(s)$ has a phase of $-270°$ at zero-frequency and a slope of -60 dB/dec at low frequency. Therefore, to stabilize the system, the LF must have a pair of zeros before the gain-crossover frequency, ω_c. Notice that, presence of two zeros before ω_c, break the asymptotic slope to -20 dB/dec and push the phase up $180°$

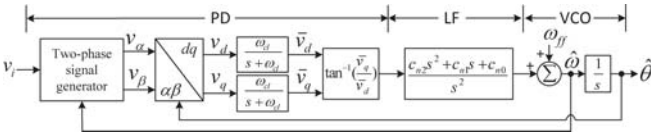


Fig. 3. Basic scheme of the RPLL.

of negative phase and, consequently, stabilize the system. So, to realize a type-3 PLL, the LF transfer function should be of the form

$$LF(s) = \frac{n(s)}{s^2} = \frac{c_{n2}s^2 + c_{n1}s + c_{n0}}{s^2} \quad (4)$$

where c_{n0}, c_{n1}, and c_{n2} are non-zero positive constants.

Based on Fig. 2(b), and considering the LF transfer function as that given in (4), the characteristic polynomial of the type-3 SRF-PLL can be obtained as

$$s^3 + Vc_{n2}s^2 + Vc_{n1}s + Vc_{n0} = 0. \quad (5)$$

Applying the Routh-Hurwitz stability criterion to (5), yields

$$V > \frac{c_{n0}}{c_{n1}c_{n2}} \quad (6)$$

which means, to ensure the stability, the input voltage amplitude should be greater than $c_{n0}/(c_{n1}c_{n2})$. So, the possibility of instability under severe voltage sags or faults is a serious drawback associated with the type-3 SRF-PLL.

To the best of the authors' knowledge, Shinnaka [11], for the first time, proposed a type-3 PLL for power grid applications. This PLL, referred to as the robust-PLL (here, called RPLL), is shown in Fig. 3, in which the LF transfer function is the same as that given in (4). To further improve the filtering capability of this PLL, two first-order low pass filters (LPFs) are also included within the control loop. As discussed briefly before, and will be covered with more details in the following sections, a LF of form of (4) in and of itself may cause stability problems. Therefore, including additional LPF(s) in the control loop of a type-3 PLL (which causes extra phase roll-off) may not be a good idea, unless its (their) cut-off frequency is (are) far above the gain-crossover frequency of the PLL. The experimental results presented in [11] show that, the RPLL transient response is highly oscillatory, which implies it suffers from very limited stability margins.

In [4], Karimi-Ghartemani has suggested a type-3 version of his well-known PLL, i.e., the enhanced PLL (EPLL), for the computation of synchrophasors. The basic scheme of this PLL, here called the type-3 EPLL, is shown in Fig. 4. It can be observed that, the type-3 EPLL as well, uses the same LF as that given in (4). The results presented in [4] show that, this PLL can be useful in the computation of synchrophasors.

A different approach to realize a type-3 PLL is that proposed by Kamata *et al.* [12]. A simple block diagram description of this approach, referred to as the dual-loop type-3 PLL, designed for the wireless communications, is shown in Fig. 5 (see [12, Fig. 1] for the original form). As shown, the PLL has two tracking loops, each of which has its own LF and VCO. The LF in the second loop is a simple gain, and its output is

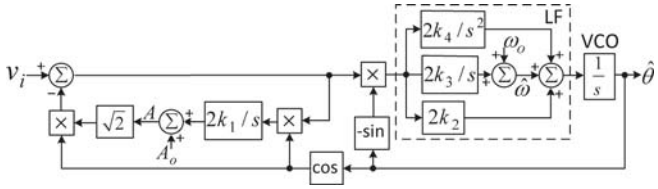


Fig. 4. Basic scheme of the type-3 EPLL.

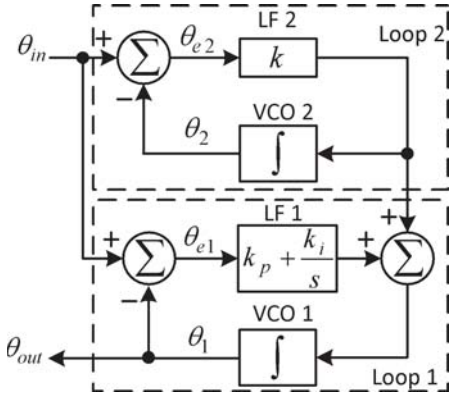


Fig. 5. Block diagram description of the dual-loop type-3 PLL.

directly added to the output of the LF (here PI controller) of the first loop. The open loop transfer function of this PLL is as given in (7).

$$G_{ol}(s) = \frac{\theta_{out}}{\theta_{in} - \theta_{out}} = \frac{(k + k_p)s^2 + (k_i + k_p k)s + k_i k}{s^3}. \tag{7}$$

An adaptation of the dual-loop type-3 PLL for grid connected applications has been proposed by Indu Rani *et al.* [13]. Fig. 6(a) illustrates the basic scheme of this PLL, which is referred to as the FPLL. The FPLL, similar to its counterpart, includes two loops: a conventional SRF-PLL, which constitutes the main loop, and a frequency feedforward loop. Fig. 6(b) illustrates the small-signal model of the FPLL (see Appendix A for how to obtain the model).

The question that may arise here is: what is the advantage of a dual-loop type-3 PLL (e.g., the FPLL) over a single-loop one (e.g., the type-3 SRF-PLL)? To answer this question, let us first determine the open-loop transfer function of the FPLL. Considering that, the LF is a PI controller, and the LPF block in the feedforward path is a first-order LPF with transfer function $LPF(s) = \omega_p/(s + \omega_p)$, where, ω_p is the cutoff frequency, then the FPLL open-loop transfer function can be obtained as

$$G_{ol}(s) = \frac{\hat{\theta}(s)}{\theta_e(s)} = \frac{(Vk_p + \omega_p)s^2 + V(k_i + k_p\omega_p)s + Vk_i\omega_p}{s^3} \tag{8}$$

From (8) it can be observed that, any decrease in the input voltage amplitude, V, changes both open-loop gain and zeros. Fortunately, these changes act against each other from the stability point of view. As a consequence, a dual-loop type-3 PLL, contrary to a single-loop one, can remain stable at

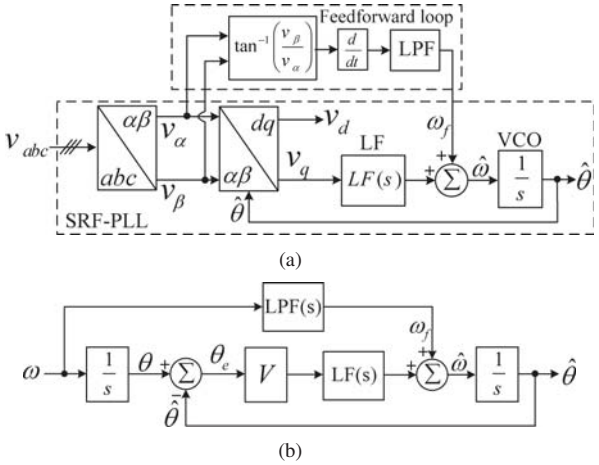


Fig. 6. (a) Basic scheme of the FPLL, and (b) its small-signal model.

low loop gains. This conclusion can also be verified by applying the Routh-Hurwitz stability criterion to the characteristic polynomial of the FPLL,

$$s^3 + (Vk_p + \omega_p)s^2 + V(k_i + k_p\omega_p)s + Vk_i\omega_p = 0 \tag{9}$$

which yields the stability conditions as

$$\begin{cases} V > 0 \\ k_i > 0 \\ k_p > 0 \\ \omega_p > 0. \end{cases}$$

Regarding the FPLL performance, there are two further issues that need to be addressed: 1) The FPLL employs a differentiator in the feedforward loop, which may degrade its performance under noisy grid conditions. 2) For $c_{n0} = k_i\omega_p$, $c_{n1} = k_i + k_p\omega_p$, and $c_{n2} = k_p + \omega_p/V$, the type-3 SRF-PLL and the FPLL have the same closed-loop transfer functions, and as a result, the same dynamics.

Another type-3 PLL for grid applications is that proposed by Liccardo *et al*. [14]. Fig. 7 illustrates the basic scheme of this PLL, which is referred to as the FFqPLL. The FFqPLL, similar to other dual-loop type-3 PLLs, includes two loops: a qPLL which constitutes the main loop, and a feedforward loop. So, stability at low loop gains (which is a characteristic of the dual-loop type-3 PLLs) is the characteristic of this PLL. The FFqPLL also has a more noise immunity than the FPLL, as it does not use the differentiator in the feedforward loop.

Application of dual-loop type-3 PLLs for the motor speed control purposes has been suggested in [15]-[17]. The experimental results presented in those articles show that, with some modifications, the dual-loop type-3 PLL shown in Fig. 5 can be desirable in the speed control of electric motors, particularly when the motor speed reference changes linearly with time.

III. Dynamics Assessment, Stability Analysis, and Design Guidelines

The aim of this section is threefold: study of dynamics, stability analysis, and parameters design guidelines for a typical type-3 PLL. A type-3 SRF-PLL, shown in Fig. 8,

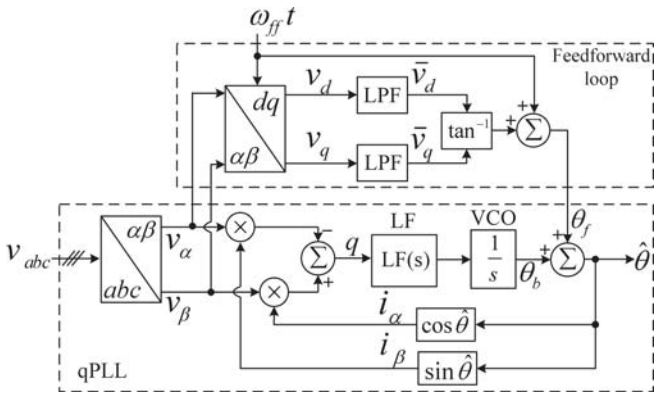


Fig. 7. Basic scheme of the FFqPLL.

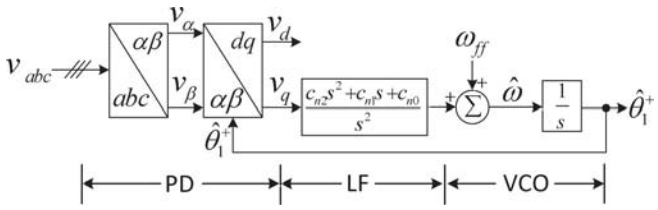


Fig. 8. The type-3 SRF-PLL.

is considered for this study. Before starting the study, the PLL small-signal model under unbalanced and harmonically distorted grid conditions is derived.

A. Small-Signal Modeling

The three-phase input voltages of the PLL are assumed to be unbalanced and harmonically distorted, expressed in (10), where V_h^+ (V_h^-) and θ_h^+ (θ_h^-) are the amplitude, and angle of the h^{th} harmonic component of the positive- (negative-) sequence of the input voltages, respectively.

$$\begin{aligned} v_a(t) &= \sum_{h=1}^{+\infty}\left[V_h^+\cos\left(\theta_h^+\right)+V_h^-\cos\left(\theta_h^-\right)\right] \\ v_b(t) &= \sum_{h=1}^{+\infty}\left[V_h^+\cos\left(\theta_h^+-\frac{2\pi}{3}\right)+V_h^-\cos\left(\theta_h^-+\frac{2\pi}{3}\right)\right] \\ v_c(t) &= \sum_{h=1}^{+\infty}\left[V_h^+\cos\left(\theta_h^++\frac{2\pi}{3}\right)+V_h^-\cos\left(\theta_h^--\frac{2\pi}{3}\right)\right] \end{aligned} \tag{10}$$

By applying the Clarke (abc-to-$\alpha\beta$) transformation, and subsequently, the Park ($\alpha\beta$-to-dq) transformation to the three-phase input voltages, the LF input signal (i.e., v_q) can be obtained as

$$v_q(t)=\sum_{h=1}^{+\infty}\left[V_h^+\sin\left(\theta_h^+-\hat{\theta}_1^+\right)-V_h^-\sin\left(\theta_h^-+\hat{\theta}_1^+\right)\right] \tag{11}$$

Under a quasi-locked state, i.e. when $\hat{\theta}_1^+\approx\theta_1^+$ and $\hat{\omega}=\omega$, (11) can be rewritten as

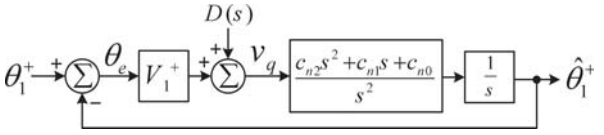


Fig. 9. Small-signal model of the type-3 SRF-PLL.

$$\begin{aligned} v_q(t) &= \underbrace{V_1^+(\theta_1^+-\hat{\theta}_1^+)}_{\text{dc term}} \\ &+\underbrace{\sum_{h=2}^{+\infty}\left[V_h^+\sin\left(\theta_h^+-\hat{\theta}_1^+\right)\right]-\sum_{h=1}^{+\infty}\left[V_h^-\sin\left(\theta_h^-+\hat{\theta}_1^+\right)\right]}_{\text{disturbance terms}} \end{aligned} \tag{12}$$

Based on (12), the small-signal model of the type-3 SRF-PLL can be obtained, as shown in Fig. 9, where $D(s)$ is the Laplace transform of the disturbance terms in (12).

B. Stability Margin

From Fig. 9, the open loop transfer function can be obtained as

$$G_{ol}(s)=\left.\frac{\hat{\theta}_1^+}{\theta_e}\right|_{D(s)=0}=V_1^+\frac{c_{n2}s^2+c_{n1}s+c_{n0}}{s^3}. \tag{13}$$

For the sake of simplicity in the analysis, let us rewrite the transfer function (13) as

$$G_{ol}(s)=k\frac{(s+\omega_{z1})(s+\omega_{z2})}{s^3} \tag{14}$$

where, $k=V_1^+c_{n2}$, and $\omega_{z1,2}=\frac{c_{n1}}{2c_{n2}}\pm\frac{1}{2}\sqrt{\left(\frac{c_{n1}}{c_{n2}}\right)^2-4\frac{c_{n0}}{c_{n2}}}$. From (14), the PLL phase margin can be determined as

$$PM=-90^\circ+\underbrace{\tan^{-1}\left(\frac{\omega_c}{\omega_{z1}}\right)}_{\phi_{z1}}+\underbrace{\tan^{-1}\left(\frac{\omega_c}{\omega_{z2}}\right)}_{\phi_{z2}} \tag{15}$$

where, ω_c is the crossover frequency, and is determined by

$$\omega_c=\frac{k}{\sin(\phi_{z1})\sin(\phi_{z2})}. \tag{16}$$

It is shown in Appendix B that, the coincident zeros (i.e., $\omega_{z1}=\omega_{z2}$) are better than the spread zeros in terms of the stability margin. The coincident zeros also has been suggested as a optimal choice in [19]. Therefore, considering $\omega_{z1}=\omega_{z2}=\omega_z$, (14), (15), and (16) are rewritten as

$$G_{ol}(s)=k\frac{(s+\omega_z)^2}{s^3} \tag{17}$$

$$PM=-90^\circ+\underbrace{2\tan^{-1}\left(\frac{\omega_c}{\omega_z}\right)}_{\phi_z} \tag{18}$$

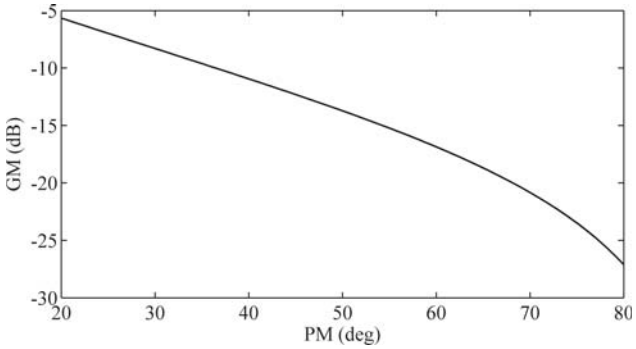


Fig. 10. GM as a function of PM.

$$\omega_c = \frac{k}{\sin^2(\phi_z)}. \tag{19}$$

Based on (18) and (19), and after some simple mathematical manipulations, we can obtain

$$\omega_z = \frac{\omega_c}{\tan(PM) + \sec(PM)} \tag{20}$$

$$k = \omega_c \frac{\sin(PM)+1}{2}. \tag{21}$$

Notice that, (20) and (21) determine the LF parameters (i.e., k, and ω_z) based on ω_c and PM. Therefore, by selecting appropriate values for ω_c and PM, all PLL parameters will be determined.

Based on (20) and (21), and the open loop transfer function of (17), the PLL gain margin can be obtained as

$$GM = 20\log\left(\frac{\cos(PM)}{[1+\sin(PM)]^2}\right). \tag{22}$$

An interesting observation from (22) is that, the GM only depends on the PM. Fig. 10 illustrates GM as a function of PM. As shown, the GM is negative, which means, the PLL may become unstable, if the loop gain decreases too much. Such systems are said to be conditionally stable. This behavior is in contrast to the performance of the type-2 PLLs, which are unconditionally stable [18].

According to Fig. 9, the amplitude of the fundamental frequency positive sequence component, $\hat{V}_1^+$, appears as a gain in the forward path of the PLL small-signal model. So, the possibility of instability under severe voltage sags or faults is a serious drawback associated with a type-3 SRF-PLL. The possible solutions to this problem will be discussed in detail in section III-E.

C. Transient Response

Substituting (20) and (21) into (17), and performing some mathematical manipulations, the open-loop transfer function (17) can be rewritten as

$$G_{ol}(s) = \frac{P(s)}{s^3} \tag{23}$$

where $P(s) = 0.5\left[1+\sin(PM)\right]\omega_c s^2 + \cos(PM)\omega_c^2 s + 0.5\left[1-\sin(PM)\right]\omega_c^3$. Based on Fig. 9 and using (23), the error transfer function can be obtained as

$$G_e(s) = \left.\frac{\theta_e(s)}{\theta_1^+(s)}\right|_{D(s)=0} = \frac{1}{1+G_{ol}(s)} = \frac{s^3}{s^3+P(s)}. \tag{24}$$

Based on (24), the phase error Laplace transform, when a phase step ($\Delta\phi/s$), a frequency step ($\Delta\omega/s^2$), and a frequency ramp ($\Delta\dot{\omega}/s^3$) input is applied, can be obtained as

$$\theta_e^{\Delta\phi}(s) = \frac{\Delta\phi s^2}{s^3+P(s)} \tag{25a}$$

$$\theta_e^{\Delta\omega}(s) = \frac{\Delta\omega s}{s^3+P(s)} \tag{25b}$$

$$\theta_e^{\Delta\dot{\omega}}(s) = \frac{\Delta\dot{\omega}}{s^3+P(s)} \tag{25c}$$

respectively. Applying the final value theorem to (25), yields

$$\lim_{t\to\infty}\theta_e^{\Delta\phi}(t) = \lim_{s\to 0} s\theta_e^{\Delta\phi}(s) = \lim_{s\to 0}\frac{\Delta\phi s^3}{s^3+P(s)} = 0 \tag{26a}$$

$$\lim_{t\to\infty}\theta_e^{\Delta\omega}(t) = \lim_{s\to 0} s\theta_e^{\Delta\omega}(s) = \lim_{s\to 0}\frac{\Delta\omega s^2}{s^3+P(s)} = 0 \tag{26b}$$

$$\lim_{t\to\infty}\theta_e^{\Delta\dot{\omega}}(t) = \lim_{s\to 0} s\theta_e^{\Delta\dot{\omega}}(s) = \lim_{s\to 0}\frac{\Delta\dot{\omega} s}{s^3+P(s)} = 0 \tag{26c}$$

which confirms the zero steady-state phase error, after a phase step, a frequency step, as well as a frequency ramp. Table I provides a comparison between the type-2 and type-3 SRF-PLLs in terms of the steady-state phase-error for different types of inputs.

TABLE I
STEADY-STATE PHASE-ERROR FOR DIFFERENT INPUTS.

input	Type-3 SRF-PLL	Type-2 SRF-PLL
Phase step	0	0
Frequency step	0	0
Frequency ramp	0	$\Delta\dot{\omega}/k_i$

For a given value of PM, a higher ω_c results in a faster dynamic response after line disturbances such as a phase jump, a frequency step, a frequency ramp, etc. Thus, in the sequel, just the effect of PM on the dynamic performance of the PLL is studied. A PM within the range of $30^\circ - 60^\circ$ is considered in this study, since it is the recommended range for the stability [18].

Figs. 11(a), (b), and (c) illustrate the PLL transient-response to a phase step, a frequency step, and a frequency ramp input, respectively, for different values of PM. As can be seen, a low value for PM makes the PLL transient response oscillatory, while a high value makes it too damped. To further support this conclusion, the closed-loop Bode magnitude plots of the PLL for different values of PM are illustrated in Fig. 12. As expected, the lower the PM value, the larger the magnitude

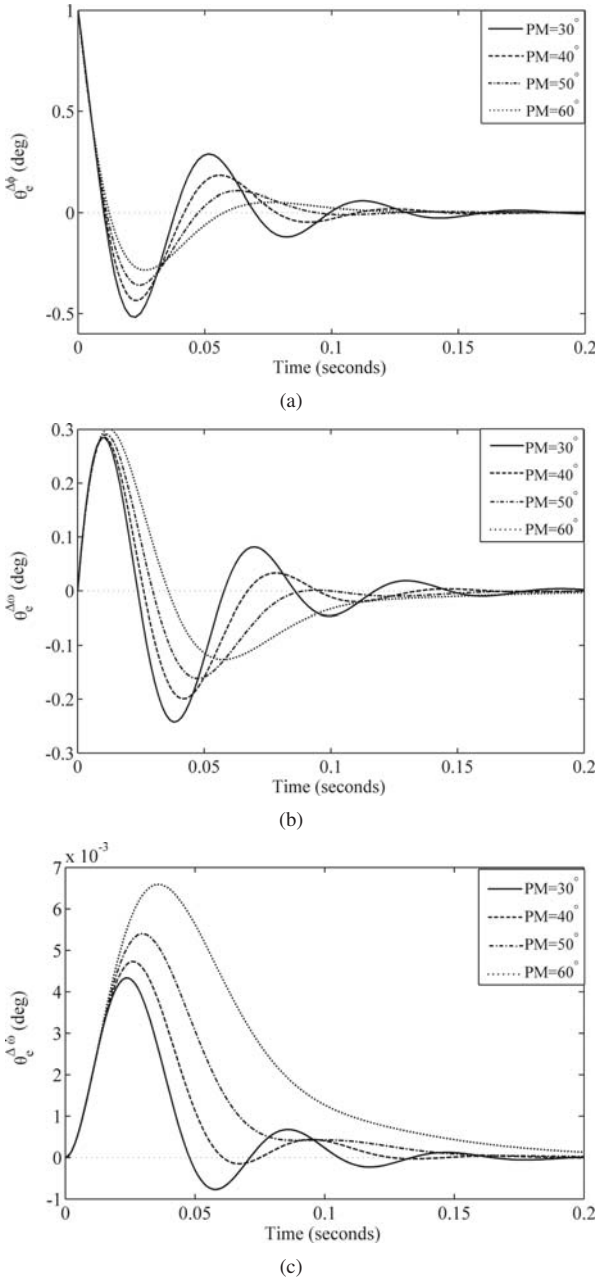


Fig. 11. Phase-error transient response for different values of PM: (a) phase step input, (b) frequency step input, and (c) frequency ramp input.

of the resonant peak and, therefore, the more oscillatory the PLL transient-response is. On the other hand, as shown in Fig. 11, both high and low values for PM are inappropriate in terms of the settling time. Thus, to achieve a satisfactory transient response in terms of both settling time and oscillation damping, a PM within the range of $40°$ to $50°$ is recommended in this paper.

It is shown in Appendix C that, for a given value of ω_c, a PM of about $47°$ results in the minimum settling time (2% criterion) in response to a phase jump. Therefore, in this study, the phase margin is selected equal to $47°$. Substituting $PM = 47°$ into (22), yields $GM = -12.86\,\text{dB}$, which means that the PLL remains stable under voltage sags up to $1 - 10^{(GM/20)} \approx 0.77$ pu.

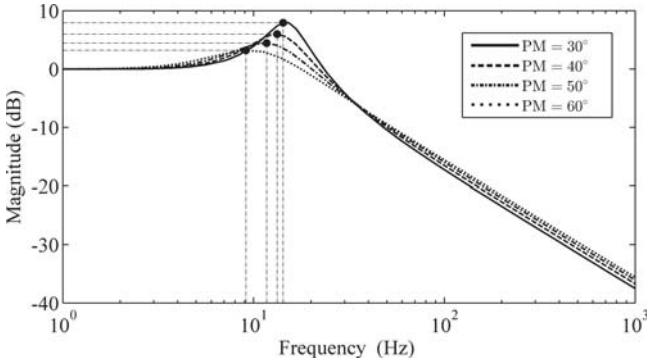


Fig. 12. Closed-loop Bode magnitude plots for different values of PM.

D. Disturbance Rejection

From (12), it is observed that, the fundamental negative sequence component in the input voltage, appears as a disturbance input to the PLL linearized model, pulsating at twice the input voltage fundamental frequency. In the same way, the input voltage harmonics, which dominantly are non-triplen odd harmonics (i.e. 5th, 7th, 11th, 13th, etc.), are sensed by the linearized model as even harmonic components (i.e., 6th, 12th, etc.). Thus, the disturbance input to the PLL linearized model (i.e., $D(s)$) can be considered as $D(s) = L\left[f(2\omega, 6\omega, 12\omega, ...)\right]$, where L denotes the Laplace operator.

From Fig. 9, the disturbance transfer function, relating $\hat{\theta}_1^+$ to $D(s)$, can be obtained as

$$G_d(s) = \left.\frac{\hat{\theta}_1^+(s)}{D(s)}\right|_{\theta_1^+(s)=0} = \frac{1}{V_1^+}\frac{G_{ol}(s)}{1+G_{ol}(s)}. \qquad (27)$$

By substituting (23) into (27), the disturbance transfer function G_d can be rewritten as

$$G_d(s) = \frac{1}{V_1^+}\frac{P(s)}{s^3 + P(s)}. \qquad (28)$$

Fig. 13 illustrates the Bode magnitude plots of the disturbance transfer function of (28) (solid lines) and the open loop transfer function of (23) (dashed lines) for the selected value of PM (i.e., $PM = 47°$) and three different values of ω_c. As it can be observed, for a given value of ω_c, the open-loop and disturbance transfer functions have well-matched amplitudes at disturbance frequencies. Therefore, instead of using the disturbance transfer function $G_d(s)$, the open-loop transfer function $G_{ol}(s)$ can be used to design the crossover frequency ω_c.

Fig. 14 illustrates the logarithmic magnitude plot of the open-loop transfer function, in which ω_d is the lowest-order disturbance frequency of concern (here, 2ω), and $\text{atten}_{\omega_d} = |G_{ol}(j\omega_d)| \approx |G_d(j\omega_d)|$ is the attenuation provided by the PLL at this frequency. Notice that, providing a sufficient attenuation at the lowest disturbance frequency guarantees a high attenuation at higher disturbance frequencies.

From Fig. 14, the crossover frequency, ω_c, can be expressed based on ω_d and atten_{ω_d} as

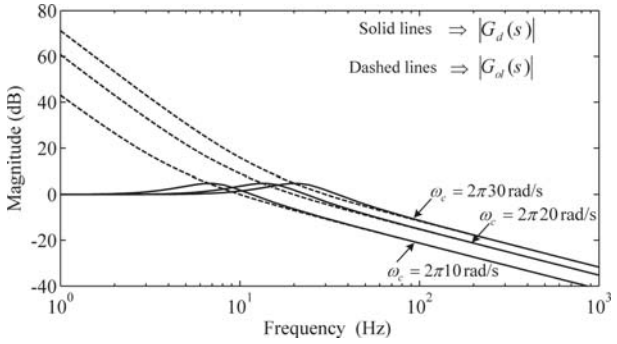


Fig. 13. Bode magnitude plots of $G_d(s)$ (solid lines) and $G_{ol}(s)$ (dashed lines) for three different values of ω_c.

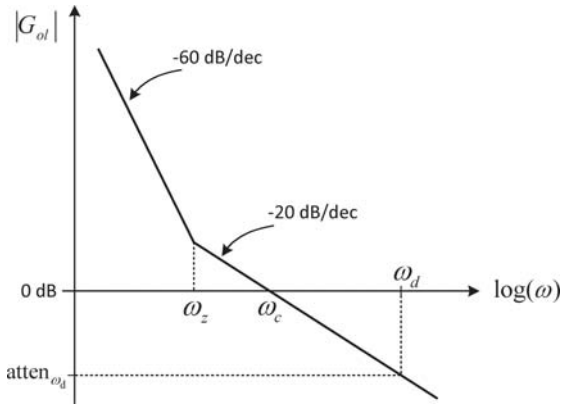


Fig. 14. Logarithmic magnitude plot of the open-loop transfer function.

$$\omega_c = \omega_d \times 10^{(\text{atten}_{\omega_d}/20)}. \tag{29}$$

Based on (29), the crossover frequency ω_c can be simply determined by selecting an appropriate value for atten_{ω_d}. Fig. 15 illustrates ω_c as a function of atten_{ω_d}. Obviously, providing a high attenuation requires a small ω_c, which degrades the PLL dynamic response. So, there is a trade-off between the speed of response and disturbance rejection capability. To deal with this problem, we recommend to select ω_c according to the minimum requirements of the disturbance rejection capability, which itself depends on the degree of grid voltage unbalance and distortion. In this paper, atten_{ω_d} is selected to be -15 dB. This selection yields the crossover frequency equal to $\omega_c = 2\pi 17.78\,\text{rad/s}$.

Once ω_c and PM are determined, the LF parameters can be simply calculated as

$$\begin{cases} c_{n0} = \dfrac{k\omega_z^2}{V_1^+} = \dfrac{\omega_c^3}{V_1^+}\dfrac{1-\sin(PM)}{2} = 187277.5 \\ c_{n1} = \dfrac{2k\omega_z}{V_1^+} = \dfrac{\cos(PM)\omega_c^2}{V_1^+} = 8511.5 \\ c_{n2} = \dfrac{k}{V_1^+} = \dfrac{\omega_c}{V_1^+}\dfrac{1+\sin(PM)}{2} = 96.7. \end{cases} \tag{30}$$

Notice that, to calculate the LF parameters, V_1^+ was assumed to be unity.

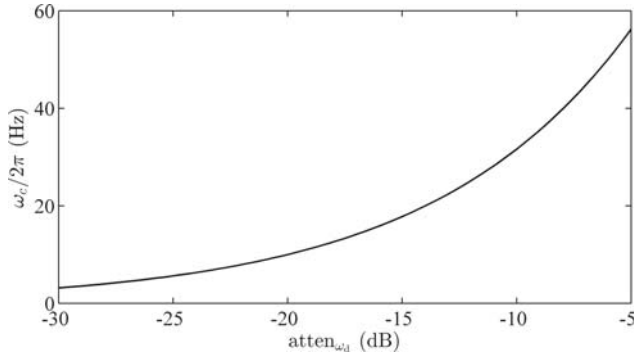


Fig. 15. ω_c as a function of atten_{ω_d}.

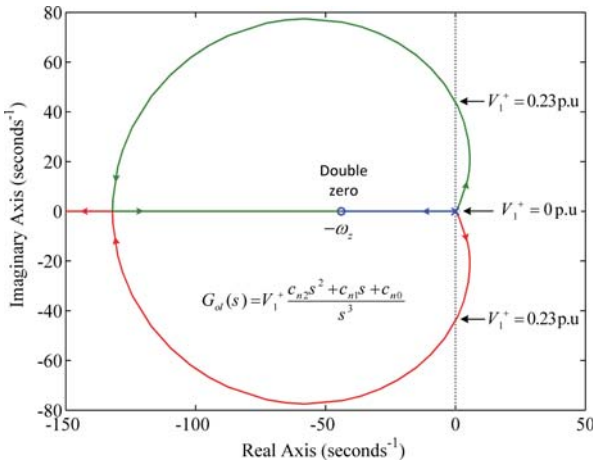


Fig. 16. Root locus of the designed type-3 SRF-PLL with the amplitude V_1^+ as the variable parameter.

E. Low Voltage and Interruption Ride-Through

In recent years, with ever increasing use of power-converter based distributed generation (DG) systems in the utility grid, and consequently their increasing influence on the grid stability, the low voltage ride through (LVRT) capability (i.e., the ability to remain connected to the grid in the presence of severe voltage sags or faults) has become an issue of great importance. Therefore, it can be concluded that the LVRT capability is also a requirement of high importance for the PLLs, since they play an important role in the control of almost all grid-interfaced DG systems.

It was discussed in section III-C that, the designed parameters for the type-3 SRF-PLL leads to a $GM = -12.86\,\text{dB}$. It means that, the PLL remains stable under voltage sags up to $1 - 10^{GM/20} = 0.77\,\text{pu}$, however, under more severe voltage sags, the PLL may become unstable. This conclusion can be verified graphically by the root-locus of the PLL system with the amplitude V_1^+ as the variable parameter (see Fig. 16). Notice that, the closed-loop poles enter to the right half plan for $V_1^+ < 0.23\,\text{pu}$.

In order to overcome this limitation, one can simply select a higher value for PM, and in this way, obtain a more negative value for GM (see Fig. 10). For example, selecting a PM equal to 68° yields a GM around -20 dB, which guarantees the PLL stability under voltage sags up to 0.9 pu. However, as discussed

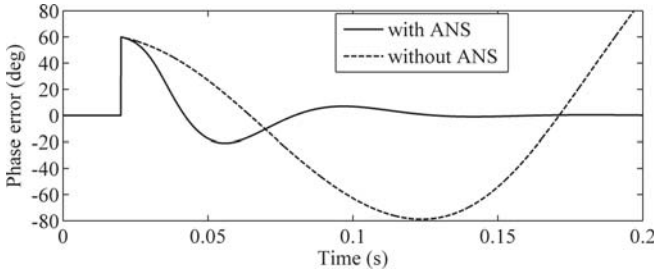


Fig. 17. PLL phase-error response to a voltage sag of 0.9 pu associated with a phase-angle jump of 60°.

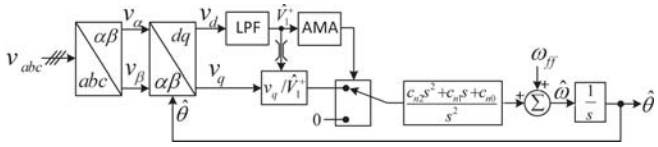


Fig. 18. Modified structure of the type-3 SRF-PLL to assure the low voltage and interruption ride-through capability.

before, selecting such a high value for PM slows down the PLL dynamic response. Another approach is to use an in-loop/pre-loop amplitude normalization system (ANS) to prevent the loop gain fall into the unstable region in the presence of severe voltage sags. For example, Fig. 17 illustrates the PLL phase-error response to a voltage sag of 0.9 pu associated with a phase-angle jump of 60°. As shown, when the ANS is used, the PLL remains stable. Another possible approach is to use the dual-loop structures to implement the type-3 PLL, but at the cost of more complexity.

In the case of line outages, or when the grid faults reduce the input voltage amplitude to almost zero, the type-3 SRF-PLL would be unstable. Therefore, to provide the interruption ride-through capability as well for the type-3 SRF-PLL, the structure shown in Fig. 18 is recommended [1], [20], in which the input voltage is monitored by an amplitude monitoring algorithm (AMA). Once an interruption is detected, the LF is disconnected from the PD so that the output signal of the PLL remains on its nominal condition.

IV. Evaluation Results

In this section, the performance of the designed type-3 PLL is evaluated through experiments based on a TMS320F28335 DSP from Texas Instruments. Throughout the experiments, the nominal frequency is set to $2\pi 50$ rad/s, and the sampling frequency is fixed to 10 kHz.

In experimental verifications, the three-phase input signals are generated internally in DSP. They are then fed to the external digital-to-analogue (D/A) converter via the serial peripheral interfaces (SPI) to generate the analog test signals. These signals are acquired by the DSP to perform the PLL algorithm [see Fig. 19]. In addition to offering high flexibility in experiments, this approach provides internal information (such as the instantaneous fundamental phase angle) which simplifies the model validation and the performance evaluation [1], [21].

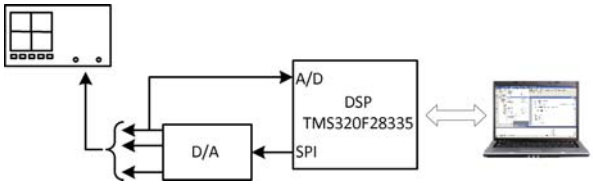


Fig. 19. Experimental setup.

To provide a means of comparison, a conventional SRF-PLL (which is a type-2 system) is also implemented. In this PLL, the LF parameters (i.e., k_p and k_i) are designed such that a damping ratio of 0.7, and a same bandwidth as that of the designed type-3 PLL is achieved. Accordingly the values of k_p and k_i are

$$\begin{cases} k_p = 114 \\ k_i = 6634.6 \end{cases} \tag{31}$$

Fig. 20(a) and (b) illustrate the open-loop and closed-loop Bode plots of the designed type-2 and type-3 SRF-PLLs, respectively. These plots will be used to justify the experimental results.

A. Grid Fault (Voltage Sag with Phase Jump)

Fig. 21 illustrates the experimental results, when the grid voltage undergoes a voltage sag of 0.5 pu with a phase jump of +40° simultaneously. A simple ANS is used for both PLLs in this test scenario. It can be seen that, the type-2 SRF-PLL yields a more damped transient response than the type-3 SRF-PLL. The 2% settling time (i.e., the time after which the phase error reaches and remains within a 0.8° neighborhood of zero) is about 62 and 95 ms for the type-2 and type-3 SRF-PLLs, respectively. These results can also be justified theoretically, through the closed-loop Bode plots of Fig. 20(b). As shown, the type-3 SRF-PLL has a higher resonant peak than the type-2 one, which justifies its more oscillatory transient response.

B. Frequency Step

Fig. 22 illustrates the experimental results, when the grid voltage undergoes a frequency step change of +5 Hz. Again, the type-2 SRF-PLL yields a more damped transient response with a shorter settling time. The 2% settling time (i.e., the time after which the estimated frequency reaches and remains within 0.1 Hz of its final value) is about 60 ms for the type-2 SRF-PLL, while it is about 93 ms for the type-3 SRF-PLL. This result can be theoretically justified with same the reason as mentioned in the previous test.

C. Unbalanced and Distorted Grid Condition

Figs. 23 illustrates the experimental results, when the grid voltage is unbalanced and harmonically distorted ($\vec{V}_1^+ = 1\angle 0°$, $\vec{V}_1^- = 0.1\angle 0°$, $\vec{V}_5^- = 0.05\angle 90°$, $\vec{V}_7^+ = 0.05\angle 0°$). It is observed that, the type-3 SRF-PLL exhibits a bit better performance than the type-2 SRF-PLL. These results can also be verified theoretically, through the closed loop Bode plots of Fig. 20(b). It can be observed that, the type-3 SRF-PLL provides a bit higher attenuation at disturbance frequencies.

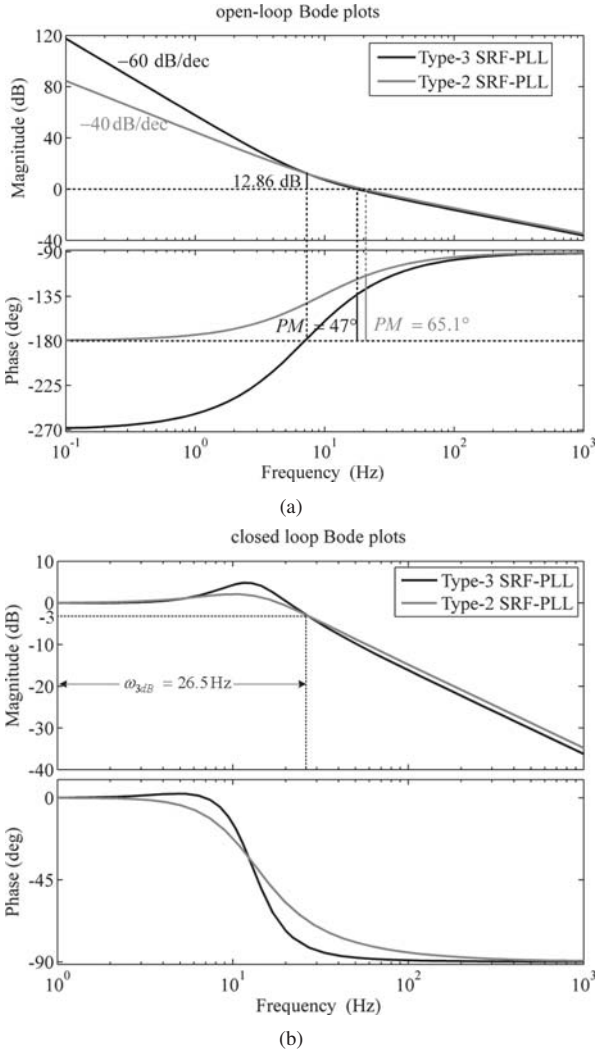


Fig. 20. (a) Open-loop and (b) closed-loop Bode plots of the type-2 and type-3 SRF-PLLs.

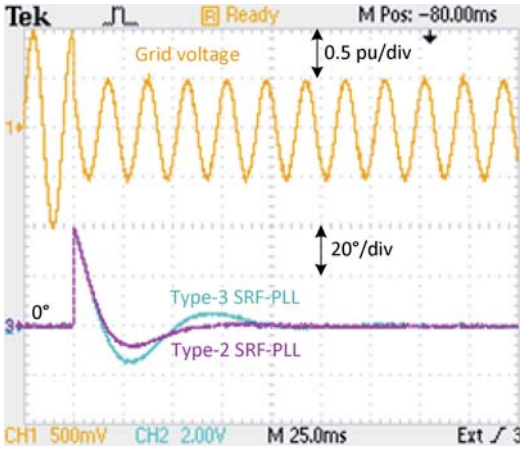


Fig. 21. Experimental results when the grid voltage undergoes a voltage sag of 0.5 pu with a phase jump of $+40°$: Ch1 denotes the grid voltage (0.5 pu/div), and Ch2 and Ch3 denote the phase error ($20°/\text{div}$).

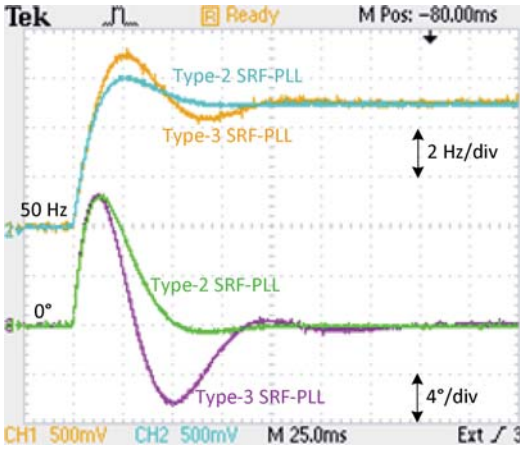


Fig. 22. Experimental results when the grid voltage undergoes a frequency step change of +5 Hz: Ch1 and Ch2 denote the estimated frequency (2 Hz/div), and Ch3 and Ch4 denote the phase error ($4°/\text{div}$).

D. Frequency Ramp

Fig. 24 illustrates the experimental results, when the grid voltage frequency changes linearly with time at a rate of $\Delta\dot{\omega} = 2\pi 30\ \text{rad/s}^2$. It is observed that, during the frequency ramping interval, the type-3 SRF-PLL yields a zero steady-state phase error, while the type-2 SRF-PLL has a tracking error of about $1.6°$. These results are consistent with those predicted theoretically , i.e., $\theta_{e,ss} = \Delta\dot{\omega}/k_i = 1.627°$ and $\theta_{e,ss} = 0$ for the type-2 and type-3 SRF-PLLs, respectively.

E. Sinusoidal Frequency Variation

Fig. 25 illustrates the experimental results, when the grid voltage frequency undergoes sinusoidal variations around its nominal value as

$$\omega = \omega_{ff}(1 + 0.1 \sin 15t). \tag{32}$$

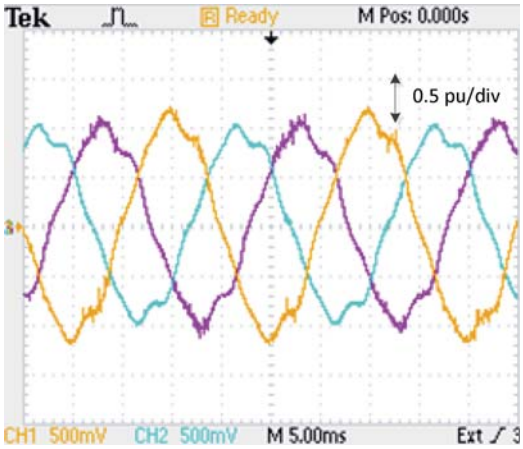
The peak-to-peak phase error is about $3.9°$ for the type-3 SRF-PLL, while it is about $8.1°$ for the type-2 SRF-PLL.

The obtained results along with some information about the PLLs stability margins are summarized in Table II.

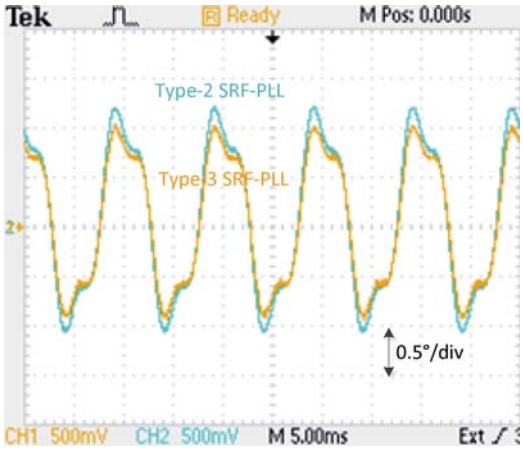
V. Conclusion

The contradictory results, reported in some recent literature, about properties of type-3 PLLs, and also a lack of deep knowledge about the stability and dynamic characteristics of these PLLs, were the main motivations to perform this study. The study was started with an overview of different approaches that have been proposed to realize a type-3. It was shown that, these approaches can be broadly classified into two categories: the single-loop and the dual loop methods. For each category, the available structures were shown, and their advantages and limitations were briefly discussed.

Considering a type-3 SRF-PLL as the case study, a detailed study of dynamics and stability analysis were performed, and comprehensive design guidelines were proposed. The well-tuned type-3 SRF-PLL was then compared with a conventional SRF-PLL, through extensive experiments. The results indicate that, in the case of the frequency and phase-angle jumps,



(a)



(b)

Fig. 23. Experimental results under unbalanced and harmonically distorted grid condition: (a) grid voltage (0.5 pu/div), and (b) phase error (0.5°/div).

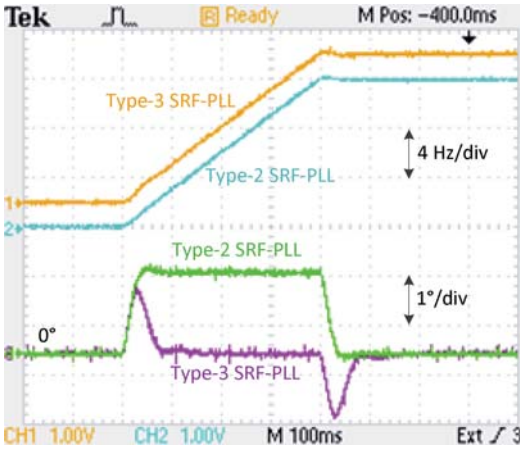


Fig. 24. Experimental results when the grid voltage frequency changes linearly with time at a rate of $\Delta\dot{\omega} = 2\pi 30$ rad/s^2: Ch1 and Ch2 denote the estimated frequency (4 Hz/div), and Ch3 and Ch4 denote the phase error (1°/div).

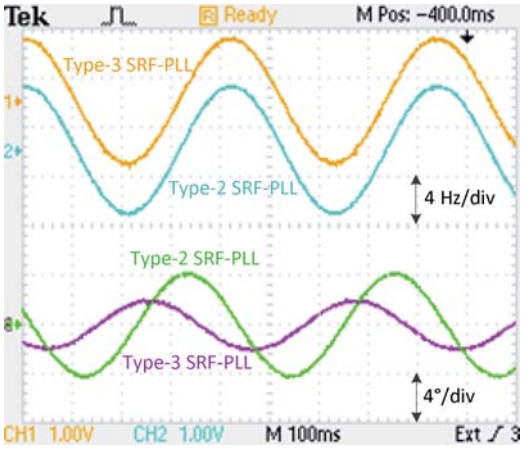


Fig. 25. Experimental results when the grid voltage frequency undergoes sinusoidal variations: Ch1 and Ch2 denote the estimated frequency (4 Hz/div), and Ch3 and Ch4 denote the phase error (4°/div).

the type-2 SRF-PLL provides better performance in terms of the settling time and the overshoot than the type-3 one. On the contrary, in the case of the frequency ramp or cyclic frequency variations, the type-3 SRF-PLL provides better performance. Both PLLs have almost the same disturbance rejection capability. Based on these results, it can be concluded that, a type-3 PLL can be attractive just in applications where the frequency varies continuously over time and the presence of distortions and noises in the measured signals limits the PLL bandwidth.

APPENDIX A
SMALL-SIGNAL MODELING OF THE FPLL

In order to determine the small-signal model of the FPLL, the three-phase input voltages are assume to be balanced and undistorted, as follows

$$\begin{aligned} v_a(t) &= V\cos(\overbrace{\omega t+\phi}^{\theta}) \\ v_b(t) &= V\cos(\omega t+\phi-2\pi/3) \\ v_c(t) &= V\cos(\omega t+\phi+2\pi/3) \end{aligned} \tag{A-1}$$

where, V, ω, and ϕ are the input voltages amplitude, angular frequency, and phase-angle, respectively.

Based on Fig. 6(a), the feedforward loop output signal, ω_f, can be expressed in the Laplace domain as

$$\omega_f(s) = LPF(s)\times L\left(\frac{d\left\{\tan^{-1}\left(v_\beta(t)/v_\alpha(t)\right)\right\}}{dt}\right) \tag{A-2}$$

where L is the Laplace operator, and

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V\cos(\theta) \\ V\sin(\theta) \end{bmatrix}. \tag{A-3}$$

Substituting (A-3) into (A-2), gives

$$\omega_f(s) = LPF(s)\times \underbrace{L\left(\frac{d\theta}{dt}\right)}_{\omega} = LPF(s)\omega(s). \tag{A-4}$$

TABLE II
COMPARISON SUMMARY.

	Type-3 SRF-PLL	Type-2 SRF-PLL
0.5 pu voltage sag with +40° phase-angle jump		
Settling time	95 ms (4.75 cycles)	62 ms (3.1 cycles)
Phase overshoot	14.8°	8.2°
+5 Hz frequency jump		
Settling time	93 ms (4.65 cycles)	60 ms (3 cycles)
Frequency overshoot	1.9 Hz	1 Hz
Unbalanced and distorted grid condition		
peak-to-peak phase error	1.86°	2.2°
30 Hz/s frequency ramp		
steady-state phase error	0°	1.6°
Sinusoidal frequency variation		
peak-to-peak phase error	3.9°	8.1°
Phase margin	47°	65.1°
Gain margin	−12.86 dB	Inf
3 dB bandwidth	$2\pi 26.5$ rad/s	$2\pi 26.5$ rad/s
Crossover frequency	$2\pi 17.78$ rad/s	$2\pi 20$ rad/s
Resonant peak	4.8 dB	2.1 dB

Based on (A-4) and the small-signal model of the conventional SRF-PLL shown in Fig. 2(b), the small-signal model of the FPLL can be obtained as shown in Fig. 6(b).

APPENDIX B
OPTIMUM LOCATING THE LF ZEROS

It is shown in this section that, the coincident zeros are better than the spread zeros in terms of the stability margin. In what follows, superscript "c" corresponds to the coincident zeros case, and the superscript "s" corresponds to the spread zeros case.

From (15), it is easy to conclude that, for a given value of ω_c, the lower the values of ω_{z1} and ω_{z2} are, the higher the PLL phase margin is. Therefore, to have a fair comparison between the coincident and spread zeros cases, let us assume the following condition on the zeros position:

$$\omega_z^c = \sqrt{\omega_{z1}^s \omega_{z2}^s} \tag{B-1}$$

where, $\omega_z^c = \omega_{z1}^c = \omega_{z2}^c$.

From (15), the phase margin for the coincident and spread zeros cases can be obtained as

$$PM^c = -90^\circ + 2\tan^{-1}(\frac{\omega_c}{\omega_z^c}) \tag{B-2a}$$

$$PM^s = -90^\circ + \tan^{-1}(\frac{\omega_c}{\omega_{z1}^s}) + \tan^{-1}(\frac{\omega_c}{\omega_{z2}^s}). \tag{B-2b}$$

In the following it is proved that, for a given value of ω_c, $PM^c \geq PM^s$.

For any values of $\omega_{z1,2}^s$, we can write

$$(\omega_{z1}^s - \omega_{z2}^s)^2 \geq 0 \;\; \Rightarrow \;\; (\omega_{z1}^s)^2 + (\omega_{z2}^s)^2 - 2\omega_{z1}^s\omega_{z2}^s \geq 0. \tag{B-3}$$

Adding $4\omega_{z1}^s\omega_{z2}^s$ to both sides of (B-3), yields

$$(\omega_{z1}^s + \omega_{z2}^s)^2 \geq 4\omega_{z1}^s\omega_{z2}^s \;\; \Rightarrow \;\; (\omega_{z1}^s + \omega_{z2}^s) \geq 2\sqrt{\omega_{z1}^s\omega_{z2}^s}. \tag{B-4}$$

Multiplying both sides of (B-4) by $\omega_c/(\omega_{z1}^s\omega_{z2}^s)$, yields

$$\frac{\omega_c}{\omega_{z1}^s} + \frac{\omega_c}{\omega_{z2}^s} \geq \frac{2\omega_c}{\sqrt{\omega_{z1}^s\omega_{z2}^s}}. \tag{B-5}$$

Multiplying both sides of (B-5) by $1/\left[1-\omega_c^2/(\omega_{z1}^s\omega_{z2}^s)\right]$ (which is a negative term), gives

$$\frac{\frac{\omega_c}{\omega_{z1}^s} + \frac{\omega_c}{\omega_{z2}^s}}{1-\frac{\omega_c^2}{\omega_{z1}^s\omega_{z2}^s}} \leq \frac{\frac{2\omega_c}{\sqrt{\omega_{z1}^s\omega_{z2}^s}}}{1-\frac{\omega_c^2}{\omega_{z1}^s\omega_{z2}^s}}. \tag{B-6}$$

Substituting (B-1) into (B-6), yields

$$\frac{\frac{\omega_c}{\omega_{z1}^s} + \frac{\omega_c}{\omega_{z2}^s}}{1-\frac{\omega_c^2}{\omega_{z1}^s\omega_{z2}^s}} \leq \frac{\frac{2\omega_c}{\omega_z^c}}{1-\left(\frac{\omega_c}{\omega_z^c}\right)^2} \tag{B-7}$$

which is equivalent to

$$\tan\left[\tan^{-1}(\frac{\omega_c}{\omega_{z1}^s}) + \tan^{-1}(\frac{\omega_c}{\omega_{z2}^s})\right] \leq \tan\left[2\tan^{-1}(\frac{\omega_c}{\omega_z^c})\right]. \tag{B-8}$$

Taking the inverse tangent from both sides of (B-8), and then adding -90° to both sides, yields

$$\underbrace{-90^\circ + \tan^{-1}(\frac{\omega_c}{\omega_{z1}^s}) + \tan^{-1}(\frac{\omega_c}{\omega_{z2}^s})}_{PM^s} \leq \underbrace{-90^\circ + 2\tan^{-1}(\frac{\omega_c}{\omega_z^c})}_{PM^c} \tag{B-9}$$

APPENDIX C
MINIMIZING THE PHASE-ERROR SETTLING-TIME

Fig. 26 illustrates the phase-error settling time (2% criterion) of the type-3 SRF-PLL versus the PM (for three different values of ω_c) in response to a phase-angle jump of $\Delta\phi = 1^\circ$. It is observed that, for all values of ω_c, the minimum settling time happens around $PM = 47^\circ$. Therefore, from the settling time point of view, a $PM = 47^\circ$ is optimal. Notice that, using different settling time criteria will give different results. For example, the minimum settling time happens around $PM = 40^\circ$ for the 5% criterion, while it happens around $PM = 50^\circ$ for the 1% criterion.

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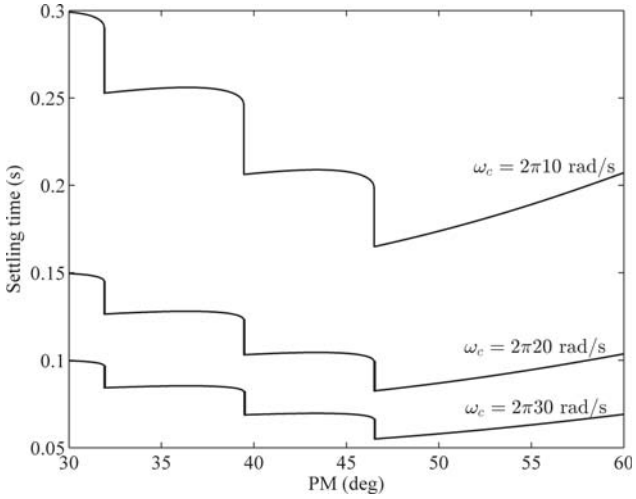

Fig. 26. Phase-error settling time versus the PM value in response to a phase-angle jump.

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