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Published in:
I E E E Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2013.2238878

Publication date:
2014

Document Version
Early version, also known as pre-print

Analysis, Design, and Experimental Verification of A Synchronous Reference Frame Voltage Control for Single-Phase Inverters

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***Abstract*—Control of three-phase power converters in the synchronous reference frame is now a mature and well developed research topic. However, for single-phase converters, it is not as well-established as three-phase applications. This paper deals with the design of a synchronous reference frame multi-loop control strategy for single phase inverter-based islanded distributed generation (DG) systems. The proposed controller uses a synchronous reference frame PI (SRFPI) controller to regulate the instantaneous output voltage, a capacitor current shaping loop in the stationary reference frame to provide active damping and improve both transient and steady-state performances, a voltage decoupling feedforward to improve the system robustness, and a multi-resonant harmonic compensator to prevent low-order load current harmonics to distort the inverter output voltage. Since, the voltage loop works in the synchronous reference frame, it is not straightforward to fine-tune the control parameters and evaluate the stability of the whole closed loop system. To overcome this problem, the stationary reference frame equivalent of the voltage loop is derived. Then, a step-by-step systematic design procedure based on a frequency response approach is presented. Finally, the theoretical achievements are supported by experimental results.**

***Index Terms*—Single-phase inverter, stand-alone mode, multi-loop, synchronous reference frame (SRF).**

I. Introduction

Distributed generation (DG), mainly from renewable energy sources has increased during recent years [1]-[4]. Small-scale electricity generation units, such as microturbines, roof-mounted photovoltaic and wind generation systems, and commercially available fuel cells are being widely utilized at the distribution level. Almost all these systems utilize some kind of power electronic converters to provide a controlled and high quality power exchange with the single-phase grid or local loads. A voltage source inverter (VSI) is the most common topology which can operate either in grid-connected or stand-alone mode. In stand-alone or island operation mode, i.e., when the grid is not present, the local loads should be supplied by the DG system, which now acts as a controlled voltage source. Thus, the essential requirement is to control the system voltage parameters such as amplitude and frequency with fast dynamic response and zero steady-state error.

Various control techniques for single-phase VSIs in stand-alone mode have been presented in literature. Thanks to availability and low-cost of advanced digital signal processors (DSPs), digital control strategies based on repetitive control [5]-[8], dead-beat control [9]-[11], and discrete-time sliding mode control [12]-[15] have been proposed recently. Digital repetitive control is proposed to reduce harmonic distortions of the output voltage produced by nonlinear loads, with its excellent ability in eliminating periodic disturbances. However, in practical applications, slow dynamics, poor tracking accuracy, a large memory requirement, and poor performance to non-periodic disturbances are the main limitations of this technique. Dead-beat and sliding mode controllers exhibit excellent dynamic performance in direct control of the instantaneous inverter output voltage. A unique feature is that even with their fast response, if wisely designed, they prevent overshoot and ringing. Despite the advantages they offer, these techniques suffer from some drawbacks, such as complexity, sensitivity to parameter variations and loading conditions, and steady-state errors. The proportional-resonant (PR) control has shown superiority in eliminating the steady-state error associated to the tracking problem of ac signals. This technique has also attracted increasing interests in instantaneous voltage control of single-phase VSIs [16]-[18]. Although simple to implement, PR control has certain disadvantages, the mains being exponentially decaying response to step changes, and great sensitivity and possibility of instability to the phase shift of sensed signals [19]. The synchronous reference frame proportional-integral (SRFPI) controller is widely used for three-phase converter systems to obtain a zero steady-state error. The adoption of this technique to single-phase applications is also proposed in [20]-[22]. In the SRFPI control, electrical signals are all transformed to the synchronous reference frame, where quantities are dc and, as a consequence the zero steady-state error is ensured by using a conventional PI regulator. This transformation requires at least two orthogonal signals, thus a fictitious second phase must be generated to allow emulation of a two phase system.

In industrial applications, usually, LC smoothing filters are used to effectively mitigate the harmonic contents of the

Manuscript received September 11, 2012; revised November 15, 2012; accepted for publication December 30, 2012. This work was supported in part by the Ferdowsi University of Mashhad.

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inverter output waveforms. However, an ideally loss-less LC circuit is highly susceptible to resonances with harmonic components generated by the inverter. Yet, it is possible to employ a single loop instantaneous voltage regulator along with a damping resistor in the filter circuit, it is more advantageous to use a multi-loop control to improve the system stability and dynamic performance and at the same time actively damp the resonance oscillations. Depending on the inner loop feedback variable and the type of controllers, several multi-loop control schemes have been proposed [8], [12], [23]-[28], which all are implemented in the stationary reference frame and suffer from limited gain of PI regulators at the fundamental frequency resulting in steady-state error and poor disturbance rejection capability. Multi-loop structure with SRFPI controllers for single-phase islanded inverters is proposed in [20]. This method uses the current of the filter inductor as the feedback signal to compensate the load disturbances and actively damp the resonances while an outer voltage loop regulates the output voltage and ensures zero steady-state error and stability over a wide range of operating conditions. [23] and recently [22] have shown that regardless of the controller type, in multi-loop techniques, the capacitor current feedback brings better disturbance rejection capability than the inductor current feedback. On the other hand, it is simpler and definitely more cost effective to sense the capacitor current instead of the higher ampere inductor current.

In this paper, a SRFPI controller is proposed to regulate the instantaneous output voltage. While the use of SRFPI controller in three phase systems is a mature topic, in single phase systems, it has not been yet properly investigated. The proposed multi-loop structure employs a simple inner capacitor current shaping loop to provide active damping and improve both transient and steady-state performances. Also, a voltage decoupling feedforward is utilized to improve the system robustness and at the same time simplify the system modeling and controller design. Finally, a multi-resonant harmonic compensator is added to the suggested scheme which prevents low-order load current harmonics to distort the inverter output voltage, especially under distorted and nonlinear loads. Combining the multi-loop control, the harmonic resonators and the voltage feedforward with the SRFPI in single phase systems has not been yet explored. The SRFPI control algorithm involves several reference frame transformations, therefore, the classical control techniques cannot be simply applied to evaluate the performance of the closed loop system. So, the single-phase equivalent of the SRFPI regulator is obtained, which, significantly simplifies the controller design and stability analysis. A detailed design procedure with consideration of the practical implementation issues, such as the effect of loading conditions and the control delay is then proposed. Detailed design criteria, derived from a frequency response approach and based on the desired bandwidth of inner and outer control loops, are presented. Experimental results are reported, which confirm the satisfactory steady-state and transient performance, particularly under highly distorting loads.

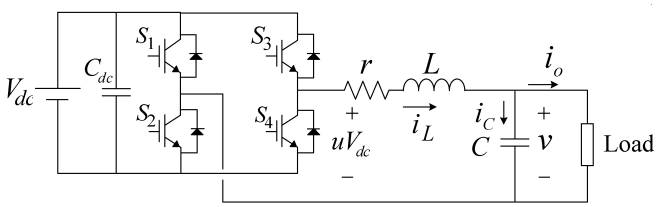

Fig. 1. Power stage of a single-phase VSI.

TABLE I
SYSTEM PARAMETERS.

parameter	value
switching frequency, f_s	20 kHz
fundamental frequency, ω_f	$2\pi 60\,\mathrm{rad/s}$
filter inductance, L	$500\,\mu\mathrm{H}$
filter capacitance, C	$22\,\mu\mathrm{F}$
ESR of the inductance, r	$0.2\,\Omega$
dc-link voltage, V_{dc}	300 V

II. SYSTEM MODELING

The power stage of a single-phase voltage source inverter (VSI), consisting of an IGBT full bridge configuration followed by a LC filter, is illustrated in Fig. 1. Throughout this paper, the dc-link voltage is assumed to be constant. This assumption can be simply realized by using a sufficiently large capacitance at the dc-link. The system parameters are listed in Table I

From Fig. 1, the differential equations describing the dynamics of the VSI can be obtained as

$$L\frac{di_L}{dt} = uV_{dc} - v - ri_L \tag{1a}$$

$$C\frac{dv}{dt} = i_C = i_L - i_o \tag{1b}$$

where, u is the control variable.

Based on (1), and considering that, the switching frequency is much higher than the fundamental frequency, the average switching model (ASM) of the VSI can be obtained as shown in Fig. 2. Notice that, in the ASM model, the control input u is replaced by a function (referred to as the modulating signal, $\tilde{m}$) representing its average value over one cycle of the switching frequency.

III. CONTROL OF SINGLE-PHASE CONVERTERS IN DQ REFERENCE FRAME

Control of three-phase power converters in the DQ rotating reference frame is now a mature and well developed research topic. However, for single-phase converters, it is not as well-established as three-phase applications. The main reason behind this, lies partly in its more complex structure than the conventional stationary reference frame controller, and also a secondary orthogonal signal that is needed to implement a single-phase controller in the DQ reference frame.

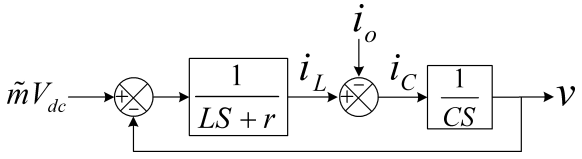

Fig. 2. ASM model of VSI.

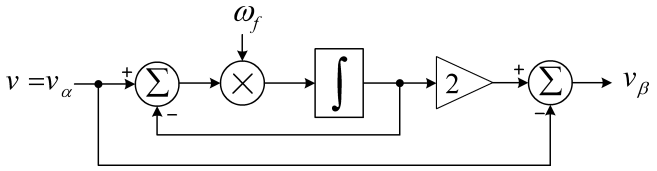

Fig. 3. Structure of a first-order APF.

In this section, the different orthogonal signal generation (OSG) techniques are reviewed first, and their advantages and limitations are examined. Then, the most suitable OSG technique for this study is selected. The structure of the suggested DQ reference frame control is introduced afterwards. Finally, based on a mathematical analysis, the stationary reference frame equivalent of the suggested control system is derived, which significantly simplifies the stability analysis and the controller parameters design.

A. Different OSG techniques

To create an orthogonal signal from an original single-phase signal, different OSG techniques have been proposed in literature. The earliest OSG technique is a transfer delay block [29]. This technique is simple to implement, however degrades the dynamic performance of the system. The reason is that, due to a quarter of cycle delay in the second phase, the controller can not respond to any changes in the system immediately. In [21], the orthogonal signal is generated by differentiating the original signal. The noise amplification caused by derivative function is the main drawback of this approach. A Hilbert transform based OSG is presented in [30]. The high complexity and computational burden are the main drawbacks of this approach. Ciobotaru et al. [31] suggest a second order generalized integrator (SOGI) based OSG. This approach prevents harmonics/noises from reaching the controller, therefore is not suitable for this study. Brabandere et al. [32] propose a Kalman filter method. Similar to Hilbert transform method, this approach suffers from high complexity and computational burden. An all-pass filter (APF) based OSG is suggested by Kim et al. [33]. This technique is easy to achieve, and does not attenuate the higher order components. Therefore, in this study, the APF method is selected. Fig. 3 illustrates the structure of a first-order APF. The input-to-output transfer function describing the dynamics of APF is shown in (2), where w_f is the fundamental angular frequency.

$$\frac{v_\beta(s)}{v_\alpha(s)} = \frac{\omega_f - s}{\omega_f + s} \tag{2}$$

B. Suggested control structure

Fig. 4 illustrates the suggested control scheme, which includes a SRFPI controller to regulate the instantaneous output voltage, an inner current shaping loop to provide active damping and improve both transient and steady-state performances, and a voltage-feedforward path to improve the system robustness. The capacitor current is selected as the feedback signal in the inner current loop, since it brings better disturbance rejection capability than the inductor current feedback. Indeed, because the capacitor current is directly proportional to the time rate of change of output voltage, it gives some kind of prediction about output voltage distortions caused by nonlinear load currents and allows the inner control loop to compensate in advance. On the other hand, it is simpler and definitely more cost effective to sense the capacitor current instead of the higher ampere inductor current. It should be noted here that a practical difficulty in accurately measuring the filter capacitor current, especially for high capacitances, is that the low frequency current information is immersed by switching frequency currents. So, a low pass filter in the current feedback loop may be required. In practice and to reduce the filtering requirements and the resultant phase

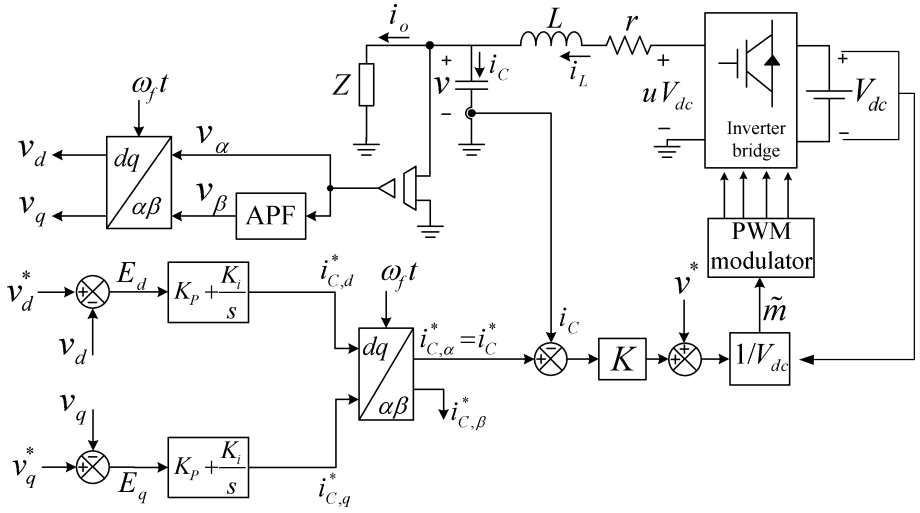

Fig. 4. Suggested control structure.

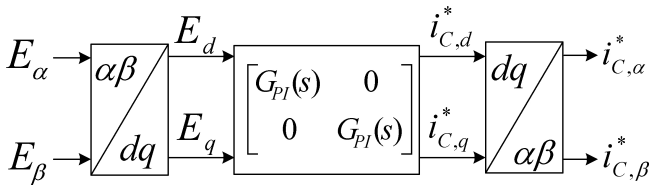

Fig. 5. Stationary ($\alpha\beta$) reference frame representation of the SRFPI controller.

delays, the LC filter capacitor should be chosen as small as possible. It is also noteworthy that the current ripple highly depends on the capacitor equivalent series resistance (ESR). In practice, to reduce the ESR effect, several low ESR capacitors are connected in parallel for the LC filter. The reference current for the inner current loop is generated by applying the inverse Park transformation to the output signals of the voltage loop i.e., $i^*_{C,dq}$. Since, in a pseudo two phase system, only α-axis quantities belong to the real system, just the real reference $i^*_{C,\alpha}$ is fed to the inner loop.

C. Stationary reference frame equivalent of SRFPI

Because, the voltage loop works in the synchronous reference frame, it is not straightforward to fine-tune the control parameters and evaluate the stability of the whole closed loop system. To overcome this problem, using the technique suggested in [34], the stationary reference frame equivalent of the voltage loop is derived in the sequel, which significantly simplifies the stability analysis and control parameters design.

Fig. 5 illustrates the stationary ($\alpha\beta$) reference frame representation of the SRFPI controller, where $G_{PI}(s) = K_p + K_i/s$.

In control system terms, the structure shown in Fig. 5 is a two-inputs two-outputs system, which can be described in the time domain as expressed in (3), where $*$ is the convolution operator.

Taking the Laplace transform from both sides of (3), and performing some mathematical manipulations, yields (4). Substituting $G_{PI}(s) = K_p + K_i/s$ into (4), and performing some mathematical simplifications, gives (5). Finally, by substituting $E_\beta(s) = \frac{\omega_f - s}{\omega_f + s} E_\alpha(s)$ into (5), the transfer function relating the real reference current $i^*_{C,\alpha}$ to the real voltage error E_α, can be obtained as

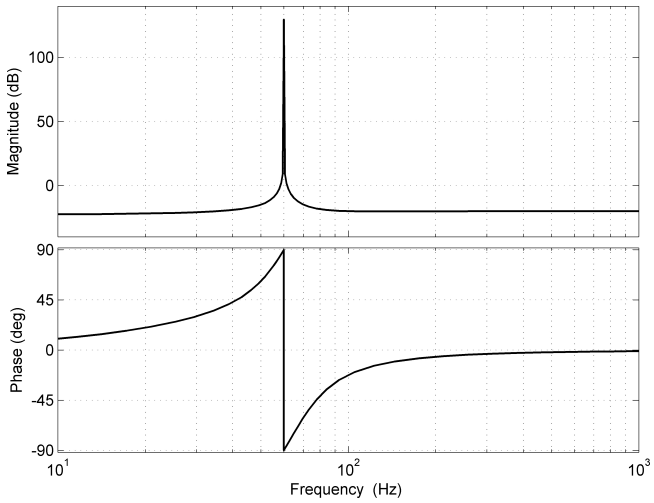

Fig. 6. Bode plot of transfer function $H(s)$.

$$i^*_{C,\alpha}(s) = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^3 + \omega_f s^2 + \omega_f^2 s + \omega_f^3} E_\alpha(s) = H(s) E_\alpha(s) \quad (6)$$

where $a_3 = K_P$, $a_2 = K_P\omega_f + K_i$, $a_1 = K_P\omega_f^2 + 2\omega_f K_i$, $a_0 = K_P\omega_f^3 - K_i\omega_f^2$.

From the control point of view, $H(s)$ is the stationary reference frame equivalent of the SRFPI. Fig. 6 illustrates the Bode plot of transfer function $H(s)$ for $K_P = 0.1$, $K_i = 10$, and $\omega_f = 2\pi 60\,\mathrm{rad/s}$. As expected, the transfer function $H(s)$ provides a very high gain at the fundamental frequency, which ensures a zero steady-sate error at this frequency.

IV. Controller Parameters Design

A. Inner current control loop

The simplified model of the inverter with the added inner capacitor current control loop is shown in Fig. 7. However it is possible to use a PI controller in the inner loop, it introduces undesirable phase delay to the sinusoidal reference and also complicates the controller design. By using a simple proportional controller, the phase delay problem is prevented and the system analysis and controller design is significantly

$$\begin{bmatrix} i^*_{C,\alpha}(t) \\ i^*_{C,\beta}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} cos(\omega_f t) & -sin(\omega_f t) \\ sin(\omega_f t) & cos(\omega_f t) \end{bmatrix}}_{\alpha\beta \leftarrow dq} \left\{ \underbrace{\begin{bmatrix} G_{PI}(t) & 0 \\ 0 & G_{PI}(t) \end{bmatrix}}_{\text{PI}} * \left\{ \underbrace{\begin{bmatrix} cos(\omega_f t) & sin(\omega_f t) \\ -sin(\omega_f t) & cos(\omega_f t) \end{bmatrix}}_{dq \leftarrow \alpha\beta} \begin{bmatrix} E_\alpha(t) \\ E_\beta(t) \end{bmatrix} \right\} \right\} \quad (3)$$

$$\begin{bmatrix} i^*_{C,\alpha}(s) \\ i^*_{C,\beta}(s) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \begin{pmatrix} G_{PI}(s+j\omega_f) \\ +G_{PI}(s-j\omega_f) \end{pmatrix} & \begin{pmatrix} -jG_{PI}(s+j\omega_f) \\ +jG_{PI}(s-j\omega_f) \end{pmatrix} \\ \begin{pmatrix} +jG_{PI}(s+j\omega_f) \\ -jG_{PI}(s-j\omega_f) \end{pmatrix} & \begin{pmatrix} G_{PI}(s+j\omega_f) \\ +G_{PI}(s-j\omega_f) \end{pmatrix} \end{bmatrix} \begin{bmatrix} E_\alpha(s) \\ E_\beta(s) \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} i^*_{C,\alpha}(s) \\ i^*_{C,\beta}(s) \end{bmatrix} = \begin{bmatrix} K_P + \dfrac{K_i s}{s^2+\omega_f^2} & -\dfrac{K_i\omega_f}{s^2+\omega_f^2} \\ \dfrac{K_i\omega_f}{s^2+\omega_f^2} & K_P + \dfrac{K_i s}{s^2+\omega_f^2} \end{bmatrix} \begin{bmatrix} E_\alpha(s) \\ E_\beta(s) \end{bmatrix} \quad (5)$$

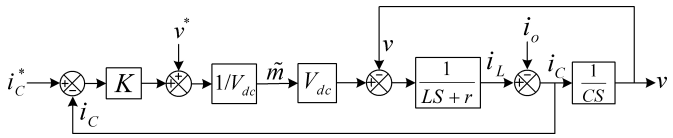

Fig. 7. Block diagram of inner current control loop.

simplified. Though, this needs a high proportional gain to reduce the steady-state error, the voltage-feedforward path in the proposed control scheme solves this problem and reduces the required control effort.

Assuming that the load impedance is Z, then in the block diagram of Fig. 7 we can replace $i_o = v/Z$ and, consequently, obtain the following closed-loop transfer function

$$G(s) = \frac{i_C}{i_C^*} = \frac{CZKs}{LCZs^2 + (CZ(r+K) + L)\,s + r}. \quad (7)$$

This clearly shows how the performance of the inner current control loop may be dependent on the load impedance. This effect can be different depending on the converter and controller parameters (values of C, r, L, and K). The corresponding Bode diagrams for the simple case of $K = 10$ and under different loading conditions are shown in Fig. 8. As it can be seen, the bandwidth as well as the gain of transfer function $G(s)$ is a little reduced by increasing the inverter load. In this work, the controller parameter K is selected according to the required bandwidth of the inner current control loop. As shown in Fig. 8, the lowest control bandwidth is expected at the nominal load. So, in order to guarantee the required bandwidth under all loading conditions, K should be tuned under nominal or maximum loading conditions. In such conditions and assuming that the expected bandwidth of the capacitor current controller is ω_{bi}, then the gain value can be calculated from (7), $|G(j\omega_{bi})|^2 = 1/2$, as

$$K = \frac{L + rCZ + \sqrt{2rCZ(RCZ + L) + L^2(2 + C^2Z^2\omega_{bi}^2)}}{CZ}. \quad (8)$$

Ideally, if the bandwidth of i_C/i_C^* (set by K) was infinite, then (7) would become $i_C/i_C^* \approx 1$, and therefore a perfect blocking of load disturbances and an instantaneous dynamic response would be achieved. Whereas this bandwidth can be selected up to the bandwidth limit of the voltage modulator (mainly set by the PWM frequency), in practice, it is chosen enough lower than the switching frequency to limit the current loop response to the switching noises. A satisfactory compromise is then a bandwidth as high as 1/5-1/4 of the switching frequency. Based on this selection criterion, and with $f_s = 20\,\text{kHz}$, the bandwidth is set as $\omega_{bi} = 2\pi(0.2 \times 20)\,\text{kHz} \approx 25\,\text{krad/s}$, and consequently K is determined from (8) to be about 16. However it is conservative, but to ensure that under all loading conditions, the bandwidth will not become less than the decided value, ω_{bi}, (8) is evaluated for the nominal load. This value for K will give a bandwidth of 5 kHz (32 krad/s) under no load condition.

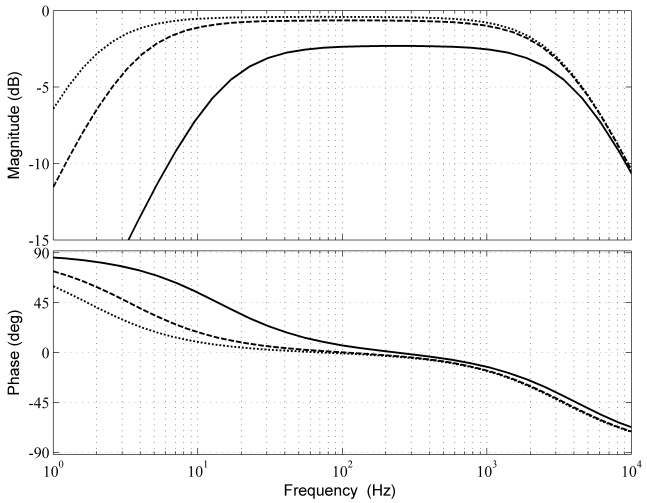

Fig. 8. Bode plots of $G(s)$ under nominal load (solid line), one-fifth of nominal load (dashed line), and one-tenth of nominal load (dotted line) with $K = 10$.

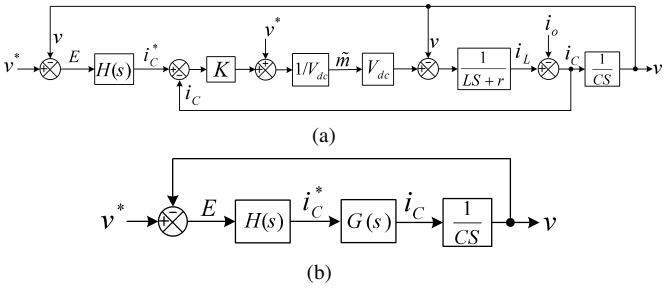

Fig. 9. (a) Block diagram of proposed control system, and (b) its simplified representation.

B. Outer voltage control loop

Once K is set by the inner current loop bandwidth criterion, the next step is to tune the parameters of the voltage feedback loop. Fig. 9 shows the block diagram of the proposed control system and its simplified representation, in which the SRFPI regulator and the inner current control loop are replaced by $H(s)$ and $G(s)$, respectively, and $v^* = v_\alpha^* = v_d^* cos(\omega_f t) - v_q^* sin(\omega_f t)$.

To investigate the effect of inverter load on the voltage regulation performance, the Bode plots of the open loop transfer function $T_{ol}(s) = v/E = H(s)G(s)/Cs$ under nominal load (solid line), one-fifth of nominal load (dashed line), and one-tenth of nominal load (dotted line) are depicted in Fig. 10 for the simple case of $K = 16$, $K_p = 0.15$, and $K_i = 0$.

From these plots it can be concluded that under light loads, the phase margin and the closed loop stability is slightly reduced. Physically, under no-load or light load conditions, the lightly damped characteristic of the output filter can cause a sharp reduction in the open loop phase and, consequently, reduce the phase margin. This effect is more considerable when the crossover frequency of the open loop system is near the resonant frequency of the LC filter, which holds for our case as both frequencies are around 1.5 kHz. Traditionally, a resistor in series or parallel with the filter capacitor or inductor

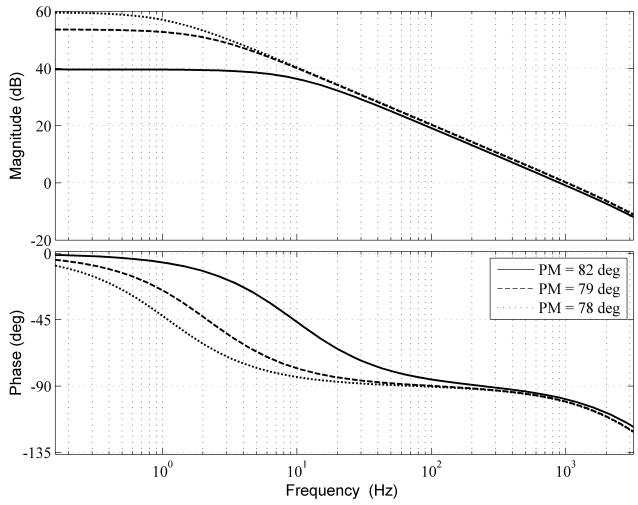

Fig. 10. Bode plots of $T_{ol}(s)$ under nominal load (solid line), one-fifth of nominal load (dashed line), and one-tenth of nominal load (dotted line) with $K = 16$, $K_p = 0.15$, and $K_i = 0$.

is used to damp the high-frequency resonances. However, as shown in Fig. 10, the capacitor current loop actively damps the LC resonance even under light loads and therefore enables an increase in the system bandwidth and avoids instability problems under light loads. According to these explanations, the voltage loop PI controller is designed under light load conditions. Besides it simplifies the analytical analysis, this simplification is conservative and ensures the stability for all inverter operating conditions. When the converter is under light loads (Z tends toward ∞), the transfer function of (7) can be approximated by

$$\frac{i_C}{i_C^*} \cong \frac{K}{Ls + r + K}. \tag{9}$$

From Fig. 9, the open loop and closed loop transfer functions of the inverter system under light load condition can be written as (10) and (11), respectively, where $b = (L\omega_f + r + K)C$.

The choice of the proportional gain of the PI compensator is a trade-off between the attainable voltage regulation bandwidth and the control loop stability. In this work, K_p is chosen to provide a desired bandwidth of ω_{bv} for v/v^* loop. A robust performance of the control system and a minimum steady-state error will be then ensured by means of proper selection of the integral gain of the compensator. For the sake of simplicity, the following analytical analysis to determine K_p is based on the assumption that the integral gain, K_i, has almost no effect on the voltage regulation dynamics. Zmood and Holmes, for the first time, showed that, a promising feature of PI controller implementation in the synchronous reference frame is the almost decoupled analysis and design of controller parameters [34]. In this way, K_p mainly determines the transient response and the steady-state response at the fundamental frequency is almost specified by K_i. Indeed, as shown in (5), the stationary reference frame equivalent of the integral term of a SRFPI controller is an ideal resonant term which theoretically affects the system performance in vicinity of the resonant frequency. Therefore, one can easily conclude that the crossover frequency as well as the dynamics performance is almost unaffected by the integral parameter. So, while tuning the proportional gain, we simply assume $K_i = 0$. However, when attending the system stability, the effect of K_i and K_p will be considered simultaneously. Using the aforementioned assumption, $H(s)$ will be simplified to K_p and the transfer function of the closed loop system in the frequency domain and under light load is obtained in (12).

$$\frac{v}{v^*} \cong \frac{K_p K}{K_p K - LC\omega^2 + j(r+K)C\omega} \tag{12}$$

After some simple manipulations on (12), one can find equation (13) for K_p to achieve a desired bandwidth of ω_{bv}.

$$K_p = \frac{C\omega_{bv}\left[\sqrt{2L^2\omega_{bv}^2 + K^2} - L\omega_{bv}\right]}{K} \tag{13}$$

In inverter applications, the choice of system bandwidth is a compromise between the transient response and the disturbance rejection requirements. In practice and depending on the application requirements, a value in the range of ten times the fundamental frequency and one-tenth the switching frequency may be chosen to get both fast dynamics and switching noise immunity. For the inverter under study, this range is between 600 Hz and 2 kHz and a value of 1.3 kHz is decided for the control bandwidth which is in the middle of this range. Evaluating equation (13) at $\omega_{bv} = 2\pi \times 1.3\,\mathrm{kHz} \approx 8\,\mathrm{krad/s}$ yields $K_p = 0.15$. The Bode plots of the closed loop transfer function $T_{cl}(s) = T_{ol}(s)/(1 + T_{ol}(s))$ under nominal load (solid line), one-fifth of nominal load (dashed line), and one-tenth of nominal load (dotted line) are depicted in Fig. 11 for $K = 16$, $K_p = 0.15$ and $K_i = 0$. Evidently the influence of loading condition on the system bandwidth is almost negligible. So, it is reasonable to conclude that equation (13) ensures the decided bandwidth under different loading conditions.

C. Stability analysis and determining the integrator gain

From (11), the system characteristic polynomial can be obtained as

$$\begin{aligned} LCs^5 + bs^4 + (b\omega_f + Ka_3)s^3 + (b\omega_f^2 + Ka_2)s^2 \\ +((r+K)C\omega_f^3 + Ka_1)s + Ka_0 = 0 \end{aligned} \tag{14}$$

$$\frac{v}{v^* - v} = \frac{K(a_3s^3 + a_2s^2 + a_1s + a_0)}{LCs^5 + bs^4 + b\omega_f s^3 + b\omega_f^2 s^2 + (r+K)C\omega_f^3 s} \tag{10}$$

$$\frac{v}{v^*} = \frac{K(a_3s^3 + a_2s^2 + a_1s + a_0)}{LCs^5 + bs^4 + (b\omega_f + Ka_3)s^3 + (b\omega_f^2 + Ka_2)s^2 + ((r+K)C\omega_f^3 + Ka_1)s + Ka_0} \tag{11}$$

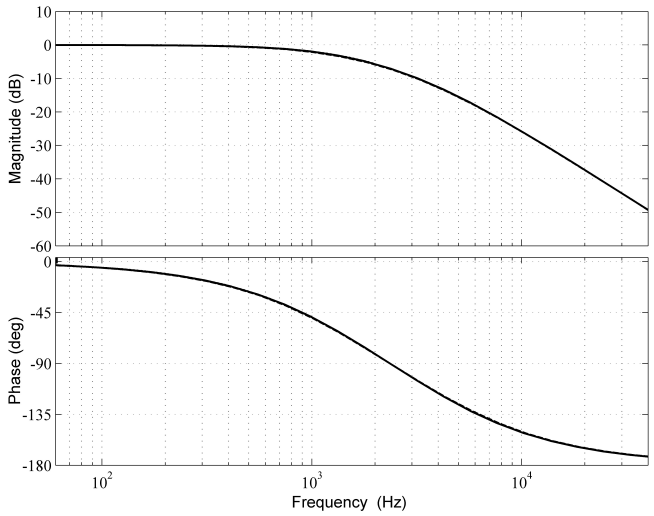

Fig. 11. Bode plots of $T_{cl}(s)$ under nominal load (solid line), one-fifth of nominal load (dashed line), and one-tenth of nominal load (dotted line) with $K = 16$, $K_p = 0.15$, and $K_i = 0$.

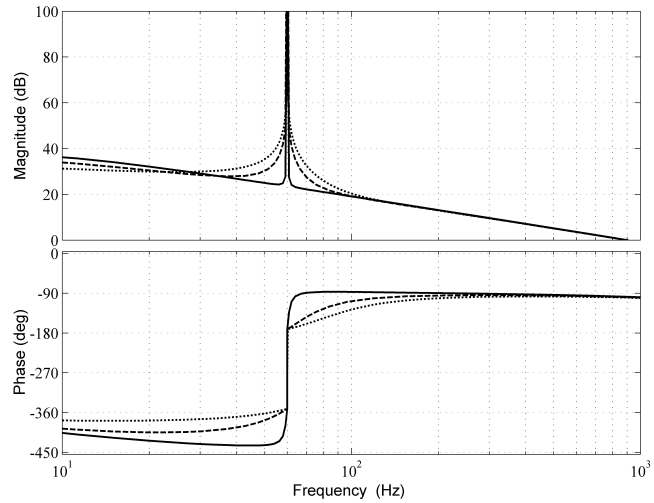

Fig. 12. Bode plots of $T_{ol}(s)$ for three different values of K_i: 1 (solid line), 15 (dashed line), and 30 (dotted line) with $K = 16$ and $K_p = 0.15$.

Applying the Routh-Hurwitz stability criterion to (14), yields the the system stability discriminant as

$$\begin{cases} K > 0 \\ K_p > 0 \\ K_i < K_p \times \omega_f. \end{cases} \tag{15}$$

This establishes an upper bound for K_i in terms of K_p (already determined) and ω_f (a grid related constant) which in our case is $K_p\omega_f = 55$.

After evaluating the system stability, it is important to examine its stability margin from the open loop transfer function $T_{ol}(s)$. The open loop Bode plots of Fig. 12, show that K_i, especially when small, just affects the controller performance in vicinity of ω_f and has almost no influence on the phase margin (PM). PM is about 80° and 70° under nominal and light load conditions, respectively, which translates to a perfect stability under all loading conditions.

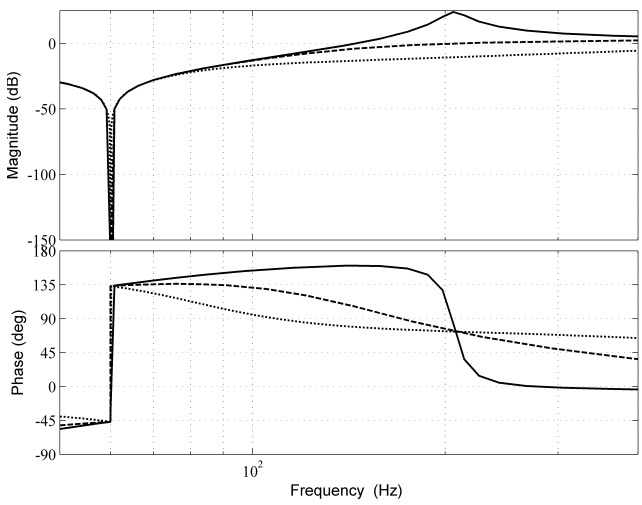

Fig. 13. Variation of harmonic impedance for three different values of K_p: 0.01 (solid line), 0.05 (dashed line), and 0.15 (dotted line).

On the other hand, the essence of the controller integral term is to eliminate the steady-state amplitude and phase errors. The open loop Bode plots of Fig. 12 show how K_i is responsible for providing a high gain at the fundamental frequency, ω_f. Ideally, the inverter control system can only track a sinusoidal reference with zero steady-state error, if the $T_{ol}(s)$ has a peak with infinite magnitude at ω_f. Based on this analysis, K_i should be chosen as high as possible, regarding the stability limitation $K_i < K_p\omega_f$, to essentially remove the steady-state error. On the other hand, the integral gain should be minimized to ensure that the integral term does not affect other frequencies. Practically, this gain is selected enough lower than the stability criterion and may be oversized in applications where variations of the fundamental frequency is expected, which may happen in the case of parallel connected inverters in stand-alone AC systems. Accordingly, in our work K_i is chosen to be 30, which is almost in the middle of its stable range ($k_i < 55$).

D. Harmonic impedance

Harmonic impedance is an effective criterion to assess the effect of harmonic load currents on the output voltage distortion. To limit the voltage distortion caused by harmonic currents the harmonic impedance should be ideally zero. So that, the parameters of the voltage loop compensator should be selected to have the lowest possible harmonic impedance, specially at low frequencies. From Fig. 9(a), the transfer function of the harmonic impedance can be derived as (16), where $d = L\omega_f + r$.

Fig. 13 compares the effect of K_p on the harmonic impedance magnitude and phase. Clearly, the magnitude of harmonic impedance, and consequently the inverter harmonic voltage distortion decreases as K_p increases. In our work, a value of $K_p = 0.15$ is already chosen based on the bandwidth selection of the voltage loop. This gain effectively damps the resonant peak as shown in Fig. 10. However, the attenuation at high-amplitude low-order harmonics may not be adequate, specially under highly distorted load conditions. To overcome

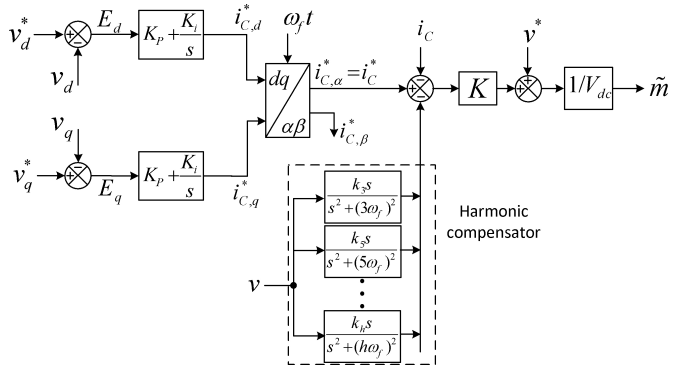

Fig. 14. Suggested control scheme with a multi-resonant harmonic compensator.

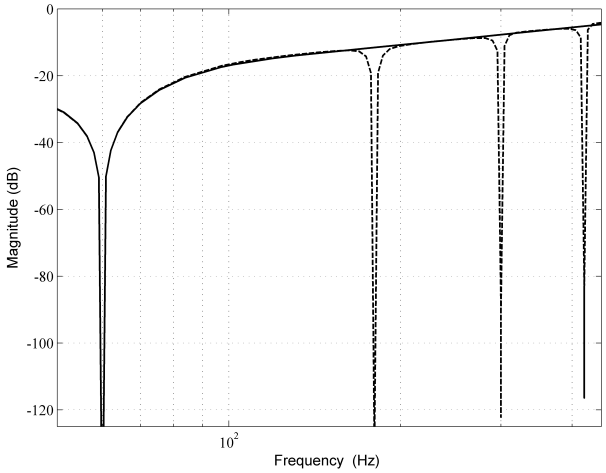

Fig. 15. Bode magnitude plots of the inverter harmonic impedance with (dashed line) and without (solid line) using the harmonic compensator for $k_p = 0.15$.

this problem, a multi-resonant harmonic compensator can be added to the suggested control scheme as depicted in Fig. 14. The transfer function of the harmonic compensator is

$$HC(s) = \sum_{n=3,\,5,\,\ldots,h} \frac{k_n s}{s^2 + (n\omega_f)^2} \tag{17}$$

where, k_n is the integrator gain for the n^{th} harmonic component, and h is the highest harmonic order that needs to be attenuated.

In order to better visualize the effect of the added multi-resonant harmonic compensator, the Bode magnitude plots of the inverter harmonic impedance with and without using the harmonic compensator are compared in Fig. 15 for $k_p = 0.15$. The dashed line indicates the harmonic impedance with using the harmonic compensator (including three modules tuned at the 3rd, 5th, and 7th harmonic frequencies), and the solid line indicates the harmonic impedance without using the harmonic compensator. It can be observed that, the harmonic compensator results in notches in the frequency response at the concern frequencies. As a consequence, using the multi-resonant harmonic compensator, the inverter output voltage harmonic distortion is significantly reduced.

The number of harmonic integrators in the harmonic compensator depends on the load characteristics and also the application where the inverter is used. In this paper, a harmonic compensator including three modules tuned at the 3rd, 5th, and 7th harmonic frequencies is suggested, since they are the most dominant harmonic components in the load current. It is worth mentioning that, the added resonant compensators have a very negligible effect on the dynamic performance of the inverter, since they only respond to the frequencies around their resonant frequencies.

E. Effect of control delay

Digital control systems impose an additional time delay in the control loop. This delay corresponds to the digital sampling, program computation time, and PWM register update and results in one or two PWM period delays in digital execution of the control algorithm.

A time delay of T_d in the Laplace domain, is described as $e^{-T_d s}$ which in the frequency domain becomes

$$\left|e^{-j\omega T_d}\right| = 1 \tag{18a}$$

$$\angle e^{-j\omega T_d} = -\omega T_d. \tag{18b}$$

Thus, the control delay does not affect the magnitude of the system transfer functions, however it introduces roll-off in the phase. In systems with limited PM, this extra loop phase lag may degrade the control performance or even cause instability. Replacing the cross-over frequency of the open loop system, ω_c, in (18b), it is convenient to determine how much the phase margin is reduced when a time delay of T_d contributes to the control loop.

$$\Delta PM = -\omega_c T_d. \tag{19}$$

However, it is not convenient to include the effect of control delay in the system modeling and control design, it is necessary to check the system stability in presence of delays in the system. In our work, $\omega_c \approx 5.6\,\mathrm{krad/s}$ which means that for one and two switching period delay, the new PM is 65° and 50°, respectively. The reduced PM is still adequate to ensure the system stability and avoid the oscillatory response.

F. Efficiency of proposed control structure

Fig. 16, shows the Bode plots of $T_{cl}(s)$ under nominal load for suggested control (solid line), without voltage feedforward path (dashed line), and without inner current loop (dotted line). These plots show how efficiently the output voltage

$$Z_o(s) = \frac{v}{i_o} = \frac{Ls^4 + ds^3 + d\omega_f s^2 + d\omega_f^2 s + r\omega^3}{LCs^5 + bs^4 + (b\omega_f + Ka_3)s^3 + (b\omega_f^2 + Ka_2)s^2 + ((r+K)C\omega_f^3 + Ka_1)s + Ka_0} \tag{16}$$

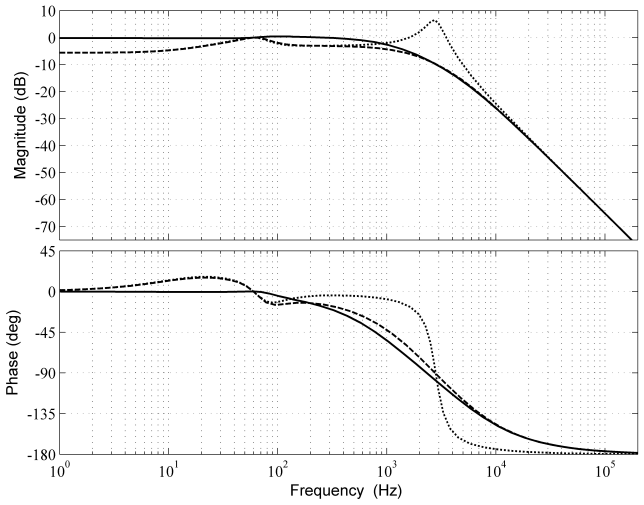

Fig. 16. Bode plots of $T_{cl}(s)$ under nominal load for suggested control (solid line), without voltage feedforward path (dashed line), and without inner current loop (dotted line).

feedforward reduces the steady-state error and the inner current control loop eliminates the resonant and increases the converter stability.

G. Effect of Parameters Uncertainty

In practice, the parameters of the LC filter may not be exact, or may vary as a consequence of varying operating conditions and aging. The performance of the control system, in terms of the PM and the control bandwidth, considering mismatches in the L and C values is investigated and the results are depicted in Fig. 17. Clearly, over a wide range of parameters mismatch, the variation of the PM, as a reliable stability measure, is insignificant and the closed loop system is far from instability. Fig. 17(b) shows that the ω_{bv} mainly remains unchanged with inductance variations; however, the capacitance uncertainties lead to large bandwidth variations. Especially, high positive values of ΔC limit the bandwidth and may deteriorate the dynamics performance.

V. Performance Evaluation

To confirm the effectiveness of the proposed control strategy, a single phase inverter system was set up, consisting of a high power DC source, a full bridge IGBT intelligent power module (IPM), a LC filter, gate drives, and sensors. The control algorithm was implemented in TMSF28335 floating point digital signal controller (DSC) from Texas Instruments. In principle, the proposed control scheme requires only one current sensor to measure the capacitor current. However, to include the overcurrent protection as an industrial feature to the developed inverter system, a relatively low cost current sensor is also utilized for the inductor current. The nominal power, frequency, and voltage of the experimental prototype are 2 kVA, 60 Hz, and 120 V_{rms}, respectively, and other parameters can be found in Table I. Measurements are done at 20 ksamples/s. To avoid noises at switching instants, all signals are sampled in the middle of each PWM period.

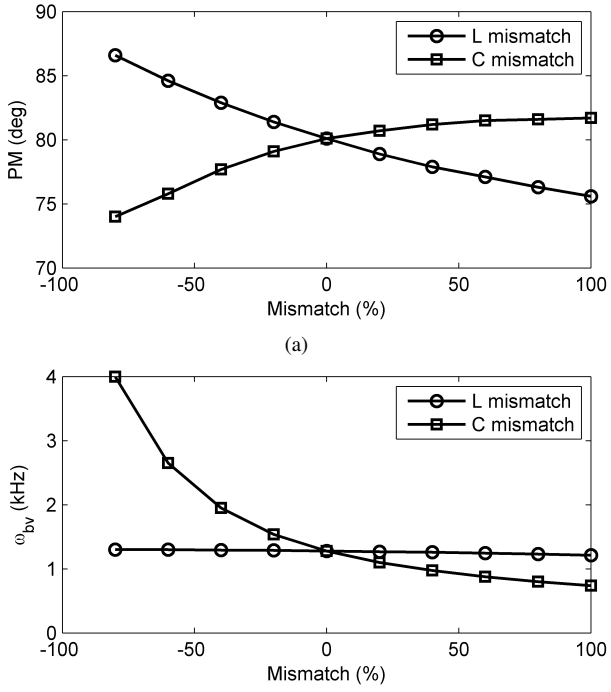

Fig. 17. Effect of L and C mismatch (%) on (a) PM, and (b) closed loop control bandwidth.

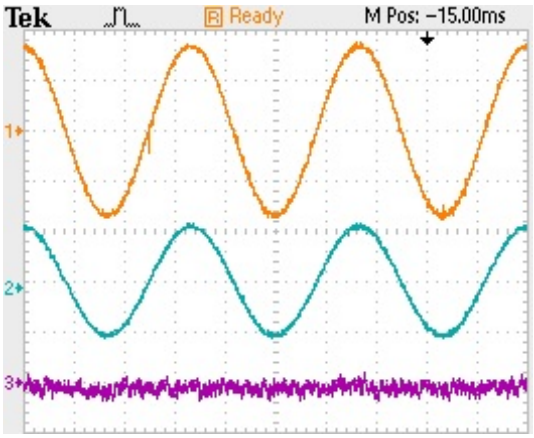

Fig. 18. Steady-state waveforms under nominal resistive load ($R = 8\,\Omega$): Ch1 denotes the output voltage (100 V/div), Ch2 denotes the load current (20 A/div), and Ch3 denotes the tracking error (10 V/div).

In the first study, the steady-state performance under the nominal resistive load is investigated. The output voltage and current as well as the tracking error waveforms are shown in Fig. 18, where the excellent reference tracking with the successful elimination of the steady-state error is obvious.

In the following, the tracking performance under a LC type load with no resistor in the circuit is also studied. It is the worst case with a high order linear load where the lack of damping may cause oscillations or even instability. The parameters of load are selected such that the load self-resonant frequency lies within the control bandwidth. The results are shown in Fig. 19. Due to the waveform regulation of the capacitor current, a stable operation is achieved.

In another study, the transient performance for a load step

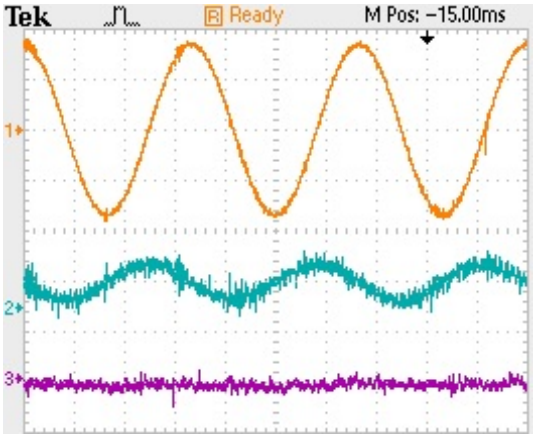

Fig. 19. Steady-state waveforms under LC load: Ch1 denotes the output voltage (100 V/div), Ch2 denotes the load current (4 A/div), and Ch3 denotes the tracking error (10 V/div).

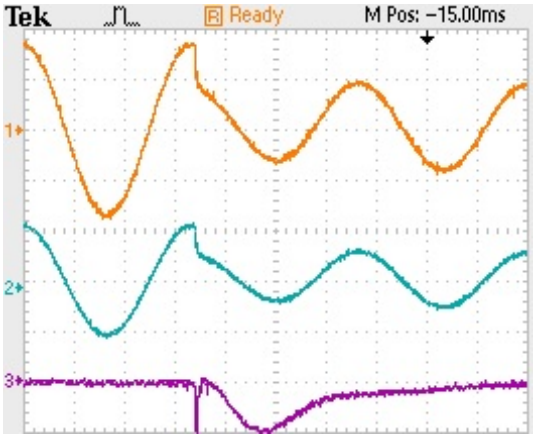

Fig. 21. Transient waveforms in response to -50% step change of reference voltage amplitude: Ch1 denotes the output voltage (100 V/div), Ch2 denotes the load current (20 A/div), and Ch3 denotes the tracking error (20 V/div).

Fig. 20. Transient waveforms in response to no load to nominal resistive load step change: Ch1 denotes the output voltage (100 V/div), Ch2 denotes the load current (20 A/div), and Ch3 denotes the tracking error (10 V/div).

Fig. 22. Steady-state waveforms under a highly distorting load without using the HC: Ch1 denotes the output voltage (100 V/div), Ch2 denotes the load current (20 A/div), and Ch3 denotes the tracking error (10 V/div).

from no load to the nominal resistive load is considered. Fig. 20 depicts that the current regulator dynamic is very fast. The output voltage recovers in less than 1 ms, while it undergoes very little variations during the transient.

Fig. 21 shows the inverter system response to a -50% step change of command voltage under nominal resistive load. Due to the excellent performance of the voltage regulator loop, the phase and amplitude errors are removed in about a cycle.

As a worst case operation, the performance of the proposed control scheme has been tested in presence of a highly distorting load consisting of a diode rectifier bridge feeding a 500 μF capacitor in parallel with a 30 Ω resistor. The converter current is highly distorted with sharp spikes and zero periods, as shown in Fig. 22. Yet the load voltage remains sinusoidal (THD = 3.18 %) with only a small distortion observable when the rectifier diodes start conducting. This promising behavior is a consequence of providing enough control bandwidth (about 1.3 kHz). As shown in Fig. 23, the output voltage quality can be more improved by using the harmonic compensation network including three modules tuned at the 3rd, 5th, and 7th harmonic frequencies. In this case, THD is reduced to 1.89%. For performance comparison, another commonly adopted capacitor current-regulated voltage-controlled strategy is implemented on the same experimental rig. The conventional technique uses stationary reference frame proportional controllers for both voltage and current control loops [26], [35]. For the sake of fair comparison, the voltage decoupling feedforward is also added to the conventional scheme. The gain of the inner current and output voltage control loops are chosen such that the same bandwidth as the proposed technique is achieved. This selection provides a PM of about 75°. As the proposed technique, the conventional strategy also benefits from the voltage variations prediction provided by the capacitor current feedback and consequently offers a very fast dynamic response. The quality of the sinusoidal voltage waveforms in terms of THD and the steady-state error between the output voltage and its reference for different test cases are compared in Table II. Both techniques can supply different load types with negligible harmonic distortions in the generated voltage, however, thanks to the harmonic compensator block, the proposed technique produced an output voltage with lower harmonic contents than the voltage produced by the conventional technique under a highly nonlinear load. The comparative performance results under identical loads clearly

Fig. 23. Steady-state waveforms under a highly distorting load with using the HC: Ch1 denotes the output voltage (100 V/div), Ch2 denotes the load current (20 A/div), and Ch3 denotes the tracking error (10 V/div).

TABLE II
PERFORMANCE COMPARISON UNDER DIFFERENT LOADS.

		Proposed technique		Conventional technique	
Load type	i_o (Arms)	THDv (%)	Peak Error (%)	THDv (%)	Peak Error (%)
No load	0	0.21	0.5	0.2	5
Nominal resistive load	15	0.2	0.5	0.2	5.5
LC load	1	0.21	0.5	0.2	5
Highly nonlinear load (without HC)	11	1.68 (3.18)	3 (4.5)	3.11	7.5

demonstrate that significant improvements in the voltage tracking performance can be achieved using the proposed control technique.

VI. CONCLUSIONS

This paper has proposed a synchronous reference frame PI (SRFPI) controller to regulate the instantaneous output voltage of the single phase inverter in stand-alone mode, which guarantees zero steady-state error at the fundamental frequency. Besides, an inner capacitor current regulating loop brings active damping and improves both transient and steady-state performances. A voltage feedforward path boosts the system robustness. A multi-resonant harmonic compensator actively prevents the low-order harmonic currents to distort the inverter output voltage. The single-phase equivalent of the SRFPI regulator was provided, which, significantly simplifies controller design and stability analysis. Based on this model, an step-by-step design procedure with consideration of the practical implementation aspects has been suggested. The performance of the proposed control strategy has been confirmed through extensive experiments.

ACKNOWLEDGMENT

This work was supported in part by Research Deputy of Ferdowsi University of Mashhad, under grant no. 2/19570 (dated 13 December 2011). This support is gratefully acknowledged.

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