Evaluation of Capacitor Voltage Balancing Control Strategies for Multilevel DAB Converters

Song, Chaochao; Wang, Ning; Sangwongwanich, Ariya; Yang, Yongheng; Blaabjerg, Frede

Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2024.3454961

Publication date:
2024

Document Version
Accepted author manuscript, peer reviewed version

Evaluation of Capacitor Voltage Balancing Control Strategies for Multilevel DAB Converters

Chaochao Song, *Member, IEEE*, Ning Wang, *Student Member, IEEE*, Ariya Sangwongwanich, *Senior Member, IEEE*, Yongheng Yang, *Senior Member, IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—Dual-active-bridge (DAB) converter with multilevel neutral-point-clamped (NPC) topology has shown potential to be a viable solution for medium-voltage DC (MVDC) systems. However, it will face a crucial challenge with regard to capacitor voltage balancing. In order to mitigate the negative effects caused by the voltage imbalance, e.g., overvoltage on certain devices, various control strategies for voltage balancing have been developed. To better design and implement the voltage balancing strategies, this paper evaluates several voltage balancing approaches, i.e., modified-duty-cycle (MDC) method, modified-phase-shift-and-duty-cycle (MPSDC) method, fixed-switching-state (FSS) method, and complementary-switching-state (CSS) method. These voltage balancing approaches have distinct characteristics in terms of dynamics, efficiency, robustness, applicability with modulation strategy, and implementation complexity. Evaluation results show that the MDC and MPSDC methods have advantage of extending to various control strategies. However, they are affected by current polarity identification, and have large current and power fluctuations. The FSS method is the most robust and the simplest one, but it also has poor dynamics. On the other hand, the CSS method can deliver smooth dynamics and high efficiency, but it relies on identifying the polarity of inductor current, and it cannot be used to the single-phase-shift (SPS) and triple-phase-shift (TPS) control strategies. Based on the evaluation results, the suitable applications of different voltage balancing methods are discussed.**

***Index Terms*—Dual-active-bridge converters, neutral-point-clamped topology, capacitor voltage balancing, evaluation.**

I. Introduction

MEDIUM voltage DC (MVDC) systems have attracted increasing attention in industry and academia with the growing adoption of DC generation plants (e.g., photovoltaic (PV)), DC loads (e.g., electrical vehicles), and energy storage systems [1]–[5]. Compared to the AC power-transfer networks, the MVDC systems can achieve higher power-transfer efficiency, capability, and flexibility, while lower control complexity [6]–[10]. However, as many key technologies are not fully developed and commercialized, the MVDC systems still remain in the testing and development phases [11]. The exploration of medium voltage (MV) DC-DC converters is crucial in the development of MVDC systems [12]–[14]. Among various DC-DC topologies, neutral-point-clamped (NPC)-based dual-active-bridge (DAB) converter, as shown in Fig. 1, is a promising solution thanks to its superiority of high power density, soft-switching capability, bidirectional power flow capability, galvanic isolation, and high voltage-blocking capability (compared to traditional two-level DAB converter) [15]–[19]. Moreover, the NPC topology has gained significant attraction as being the most widely adopted and commercialized multilevel topology. Two-level and three-level topology is applied to the primary side according to the voltage level. The two-three (2/3)-level DAB converter (i.e., two-level topology in the primary side) is suitable for the applications where the input and output voltage ratings are considerably different, e.g., between the battery and MVDC bus in the energy storage systems. On the other hand, the three-three (3/3)-level DAB converter can be employed to the MVDC scenarios where the input and output DC voltages are close.

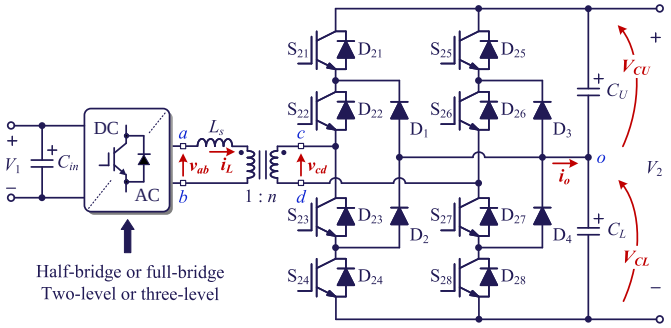


Fig. 1. A neutral-point-clamped (NPC)-based dual-active-bridge (DAB) converter: V_1 and V_2 are the DC-link voltages, v_{ab} and v_{cd} are the AC voltages of the two bridges, $1:n$ is the turns ratio of the transformer, L_s is the series inductor, i_L is the inductor current, i_o is the neutral-point current, V_{CU} and V_{CL} are the capacitor voltages of C_U and C_L.

Capacitor voltage balancing (also referred to as neutral-point voltage balancing) is an additional control challenge for the NPC-based DAB converters compared to the two-level DAB converter. Owing to the asymmetrical gate pulses (caused by the tolerances in the pulse generator or gate drivers), asymmetrical layout, and tolerances in the power devices (e.g., DC-link capacitors), the two capacitor voltages may become

Manuscript received February 22, 2024; revised July 23, 2024; accepted August 30, 2024. This work was supported by the research project Artificial Intelligence for Next-Generation Power Electronics (AI-Power) under Award 223431. (*corresponding author: Ning Wang*.)

Chaochao Song, Ning Wang, Ariya Sangwongwanich, and Frede Blaabjerg are with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (e-mail: chso@energy.aau.dk, nwa@et.aau.dk, ars@energy.aau.dk, fbl@energy.aau.dk).

Yongheng Yang is with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: yang_yh@zju.edu.cn).

Color versions of one or more figures in this article are available at xxxxxxxxxx

Digital Object Identifier xxxxxxx

unbalanced under certain conditions in practice [20]–[22]. This may cause overvoltage for certain power devices, which will affect their lifetime, and even damage these devices [23]–[28]. Moreover, a significant voltage imbalance can lead to distortion in the AC terminal voltage of the NPC bridge (i.e., v_{cd} in Fig. 1). This, in turn, can negatively impact the accuracy of the power model and further deteriorate an optimal control for DAB converters [27], [28]. Therefore, a method to achieve capacitor voltage balancing should be employed to the NPC-based DAB converters.

Capacitor voltage balancing control strategies have been discussed for various power electronic converters, e.g., modular multilevel converter (MMC), cascaded two-level DAB converters, and multilevel hybrid-clamped converters [29]–[32]. However, these voltage balancing methods cannot be applied to the NPC-based DAB converters owing to different topology and modulation schemes. The voltage balancing methods proposed for NPC-type inverter/rectifier can provide more inspiration for the research of the NPC-based DAB converters due to the same NPC topology [33], [34]. Nevertheless, the modulation of the NPC-type inverter/rectifier and DAB converter is different, making the characteristics related to voltage balancing different. For instance, identifying the current polarity in certain switching states online is challenging in the DAB converter due to non-sinusoidal current waveform and high variation frequency (e.g., tens of kHz to 1 MHz). In addition, different from the inverter/rectifier where the phase current frequency is much lower than the switching frequency, when certain switching states change within a switching cycle to balance the capacitor voltages, the inductor current of the DAB converter will be distorted severely under certain conditions as the current frequency is the same as the switching frequency, resulting in large current and power fluctuations. Consequently, when applying the voltage balancing control of NPC inverter/rectifier to the DAB converters, the above issues should be addressed.

Prior-art research has proposed various voltage balancing methods for the NPC-based DAB converters. Certain components, e.g., flying capacitors, are used to suppress capacitor voltage imbalance in [35], [36]. However, additional hardware components will cause higher cost and power losses. On the other hand, capacitor voltages are balanced by control strategies in most research [27], [28], [37]–[48]. The existing voltage balancing control can be mainly divided into four approaches: 1) modified-duty-cycle (MDC) method, 2) modified-phase-shift-and-duty-cycle (MPSDC) method, 3) fixed-switching-state (FSS) method, and 4) complementary-switching-state (CSS) method. A voltage balancing control proposed in [45], [46] regulates the duty cycles of gate pulses to increase the dwell time of the switching states which benefit the voltage balancing (i.e., the charges necessary for the neutral point). Thus, the difference between two capacitor voltages can be eliminated. In [38]–[44], the control strategies balance the capacitor voltages by dynamically modifying the phase-shift angles together with the duty cycles of gate pulses. The MDC and MPSDC methods rely on the inductor current polarity to identify the beneficial and adverse switching states, which requires heavy pre-calculations when the operating parameters change in a wide range. In order to decouple the voltage balancing from the inductor current polarity, the control strategies based on the FSS method were proposed in [27], [47]. Under the applied switching states in the FSS method, the direction of the neutral-point current can be controlled independently from the inductor current polarity. Therefore, the pre-calculation for current polarity is not required, which simplifies the implementation. However, the dynamics of DAB converters will be affected by the voltage distortion during the voltage balancing, especially when there is a frequent transition between the steady state and balancing state. Alternatively, a CSS method was proposed to suppress current and transferred power fluctuations during the voltage balancing [28], [48]. This method involves substituting the adverse switching states with their corresponding complementary switching states. Accordingly, the direction of the neutral-point current can be controlled in a way to assist the voltage balancing. At the same time, the voltage v_{cd} and inductor current i_L can be maintained unchanged. Hence, the CSS method can achieve smooth dynamics. However, it also depends on current polarity identification.

In addition to inductor current polarity identification and converter dynamics, other characteristics, e.g., efficiency and robustness, are also different among various voltage balancing approaches. However, due to the lack of a comprehensive comparison of these voltage balancing control strategies, it remains difficult to determine which approach is the most appropriate for specific applications and operating conditions. Therefore, this paper benchmarks various voltage balancing control methods based on a two-three (2/3)-level NPC-based DAB converter (i.e., a two-level full-bridge is applied to the primary side). It should be noted that the analysis and results can also be applied to the case where both sides are NPC bridges. The main contributions of this paper are:

- Certain comparison has been carried out among some capacitor voltage balancing methods in [27] and [28]. However, the comparison mainly focuses on dynamics with a large capacitor voltage error and robustness, while other crucial issues, e.g., dynamics with frequent transitions between steady and balancing states, transient switching conditions (zero-voltage-switching (ZVS) and hard-switching (HS)), applicability to various control schemes (e.g., single-phase-shift (SPS) control, and triple-phase-shift (TPS) control), and implementation complexity, have not been discussed. Thus, this paper gives a comprehensive comparison among various capacitor voltage balancing approaches in terms of dynamics, efficiency, robustness, applicability with modulation strategy, and implementation complexity based on experimental tests.
- Based on the evaluation results, the applications where each capacitor voltage balancing control strategy can be suitably used are discussed.

The rest of the paper is arranged as follows. The basic analysis of the switching states, and main demands on capacitor voltage balancing of the NPC-based DAB converters are analyzed in Section II. Different voltage balancing approaches are presented in Section III. The benchmarking based on experiments and simulations is detailed in Section IV. Finally, Section V presents the conclusions.

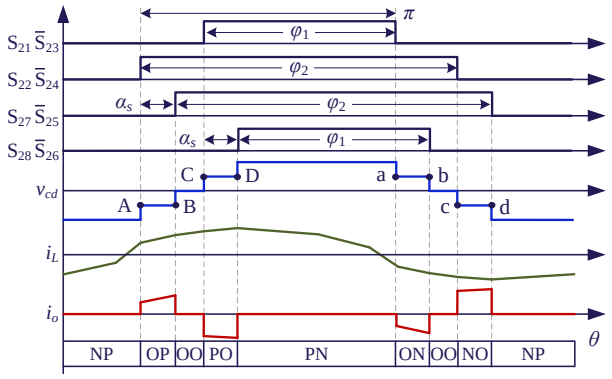


Fig. 2. Typical waveforms of the switching sequence, voltage v_{cd}, inductor current i_L, and neutral-point current i_o with a five-level control scheme.

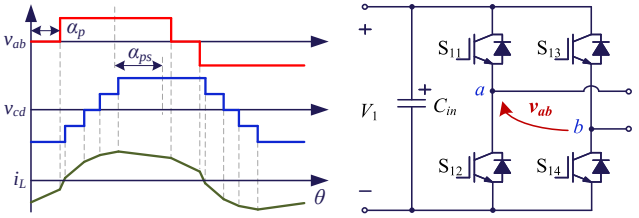


Fig. 3. Topology and waveforms of a two-three (2/3)-level DAB converter: (a) Waveforms of v_{ab}, v_{cd}, and i_L, and (b) a two-level H-bridge applied to the primary side.

II. Basic Analysis for Voltage Balancing

A. Switching State Analysis

Fig. 2 shows the gate pulses, AC terminal voltage v_{cd}, inductor current i_L, and neutral-point current i_o for the NPC bridge in the NPC-based DAB converters. φ_1 and φ_2 denote the duty cycles of the outer switches (i.e., S_{21}, S_{24}, S_{25}, and S_{28}) and inner switches (i.e., S_{22}, S_{23}, S_{26}, and S_{27}), respectively, satisfying $\varphi_1 + \varphi_2 = 2\pi$, and α_s is the phase-shift angle between the two legs of the NPC bridge. In addition to the above three control variables, the DAB converters are also controlled by the phase-shift angles/duty cycles of the primary-side bridge (i.e., the waveform of v_{ab}), and the phase-shift angle between the two-side bridges. With various topologies used to the primary side, the control variables and the waveform of v_{ab} are different. For instance, when a two-level bridge is applied to the primary side, the waveforms of the voltages and inductor current will be as shown in Fig. 3, where α_p is the phase-shift angle in the primary side, and α_{ps} is the phase-shift angle between the two bridges.

For convenience, the switching states are expressed by [P], [O], and [N], as shown in Table I. For instance, under such a definition, the switching state [PO] denotes that the gate pulses of S_{21} and S_{22} in the first leg, and S_{26} and S_{27} in the second leg, are ON, and the others are OFF. Among the five levels on the voltage v_{cd}, the current i_o will flow through the neutral point when $v_{cd} = \pm 0.5V_2$, i.e., under the four switching states [OP], [PO], [ON], and [NO]. In ideal operation, the two capacitor voltages V_{CU} and V_{CL} are balanced as the waveform of i_o is symmetrical in each switching period (see Fig. 2),

TABLE I
Switching States for NPC Bridge of the NPC-Based DAB

Switching State	ON Switches (first leg)	ON Switches (second leg)
[P]	$\{S_{21}, S_{22}\}$	$\{S_{25}, S_{26}\}$
[O]	$\{S_{22}, S_{23}\}$	$\{S_{26}, S_{27}\}$
[N]	$\{S_{23}, S_{24}\}$	$\{S_{27}, S_{28}\}$

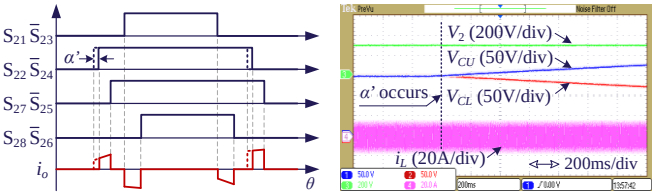


Fig. 4. Voltage imbalance caused by the asymmetrical gate pulses. (a) Disturbance phase-shift angle α' on S_{22} and S_{24}. (b) Experimental results of unbalanced capacitor voltages.

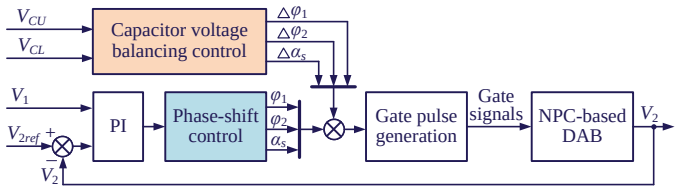


Fig. 5. Control structure of the NPC-based DAB converters with capacitor voltage balancing [38], [45]–[47].

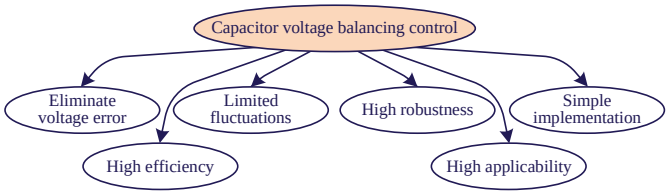


Fig. 6. Demands for capacitor voltage balancing control.

which means the charges drawn from and injected into the neutral point are equal. However, certain non-ideal factors, e.g., the asymmetrical gate pulses and layout, and tolerances in the capacitors, will deteriorate the voltage balance, and may cause overvoltage on certain devices. For example, Fig. 4 demonstrates the capacitor voltage imbalance caused by an error in the phase-shift angle α' (i.e., asymmetrical gate pulses). In order to avoid these negative effects, a voltage balancing control should be employed to the NPC-based DAB converters. Fig. 5 illustrates a generic control structure of NPC-based DAB converters, which is composed of a basic phase-shift control to achieve power-transfer management, and a voltage balancing control to avoid voltage imbalance.

B. Demands on Voltage Balancing Control

For a capacitor voltage balancing control, in addition to eliminating the difference between the two capacitor voltages, other demands should also be considered, as shown in Fig. 6, which are expressed as follows:

1) Limited current and power oscillation:

After the voltage balancing control is activated, the waveform of the voltage v_{cd} may be distorted caused by the variation of the duty cycles and/or phase-shift angles, and the inductor current will fluctuate due to

$$\frac{di_L(t)}{dt} = \frac{v_{ab}(t) - v_{cd}(t)/n}{L_s} \tag{1}$$

Furthermore, as the current changes, the transferred power will also fluctuate due to

$$P = \frac{1}{T_{hs}} \int_0^{T_{hs}} v_{ab}(t) i_L(t) dt \tag{2}$$

The current and power fluctuations will be more significant with a continuous imbalance factor, e.g., a disturbance phase-shift angle α' (see Fig. 4(a)), due to the frequent transitions between the balancing state and steady state. Thus, the oscillation should be suppressed by the voltage balancing control to achieve smooth dynamics and stable operation.

2) High efficiency:

While performing voltage balancing, fluctuations in the inductor current can increase the root-mean-square (RMS) values, leading to higher power losses in the DAB converters [49]. These fluctuations can also alter the phase relationships between the voltage v_{cd} and current i_L, which can impact soft-switching operation. Therefore, it is essential to design a voltage balancing control strategy that can effectively suppress the increment in power loss and prevent efficiency reduction.

3) Robust to parameter variations:

Variations in operating parameters during voltage balancing can cause the zero-crossing point of the inductor current to shift, potentially leading to a reversal of the neutral-point current direction for a specific switching state. This can increase the voltage balancing period, and in extreme cases, lead to further degradation of voltage imbalance due to incorrect identification of the inductor current polarity. Thus, the voltage balancing control requires high robustness against operating parameter variations.

4) Applicable to various control schemes:

In normal operating state (i.e., no capacitor voltage imbalance), the NPC-based DAB converters can be controlled by various phase-shift control schemes, e.g., SPS control (see Fig. 7(a)), TPS control (see Fig. 7(b)), and five-level control (see Fig. 2). It should be noted that the SPS and TPS control schemes are special cases of the five-level control. When the duty cycles φ_1 and φ_2 are π (ignoring dead time), and the phase-shift angle α_s is 0, the five-level control will be the converted to SPS control. On the other hand, when the duty cycles φ_1 and φ_2 are π, and the phase-shift angle α_s is not equal to 0, it will be converted to TPS control. With different optimization objectives, certain control schemes will be employed depending on the operating parameters and conditions. The capacitor voltage balancing control should be applicable to various control strategies, so that it does not need to be regulated when the operating conditions and parameters change.

5) Simple implementation:

When certain switching states are applied to capacitor voltage balancing control, e.g., [OP], [PO], [ON], and [NO]

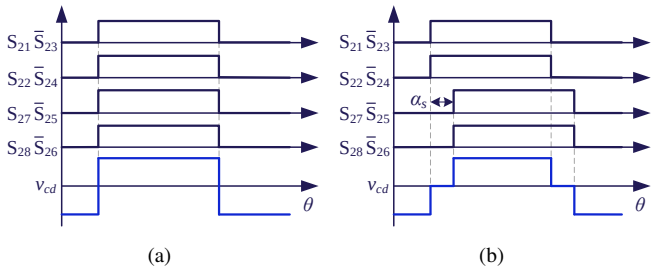


Fig. 7. Waveforms of the switching sequence and voltage v_{cd} with: (a) SPS control, and (b) TPS control.

in Fig. 2, the direction of the neutral-point current i_o should be identified based on inductor current polarity, because the neutral-point current will be opposite under the conditions when $i_L > 0$ and $i_L < 0$, as shown in Fig. 8. However, since the zero-crossing point of the inductor current is affected by various factors, such as the DC-link voltages, transferred power levels, and operating modes (divided by different relationships of the duty cycles and phase-shift angles), determining the inductor current polarity requires heavy pre-calculations based on the inductor current expression, especially when the operating parameters vary widely. A practical and feasible voltage balancing control strategy should be easily implemented after compromising the above demands, which means less pre-calculation, parameter regulation, and/or operating-mode transition is required.

By taking the above demands as the evaluation criteria, various capacitor voltage balancing approaches for the NPC-based DAB converters are discussed in the following.

III. Capacitor Voltage Balancing Control Strategies

A. Modified-Duty-Cycle (MDC) Method

As analyzed above, the capacitor voltages can be balanced when the dwell time of the four switching states [OP], [PO], [ON], and [NO] is regulated, which can be achieved by modifying the duty cycles of the gate pulses [45]. The MDC method applies an additional duty cycle φ_M to the original duty cycles to regulate the capacitor voltages, as shown in Fig. 9. Since the direction of the neutral-point current i_o is affected by the inductor current polarity (see Fig. 8), the regulation of the duty cycles will be different under various inductor current polarity during the four intervals. Fig. 9 illustrates four conditions under different combinations of current polarity, where $I_L[\mathrm{A,B}]$ and $I_L[\mathrm{C,D}]$ represent the average inductor current during [A, B] and [C, D], and $f\{i_L(t)\}$ represents the inductor current model, which is used for determining the polarity of the inductor current. Due to the symmetry of the inductor current in a switching period, the current polarity during [a, b] and [c, d] will be opposite to that of [A, B] and [C, D], respectively. Therefore, only the current polarity during [A, B] and [C, D] is analyzed. Under certain current polarity, the switching states which can assist the voltage balancing can be identified. For instance, for the condition of $V_{CU} > V_{CL}$, voltage balancing requires a current injection

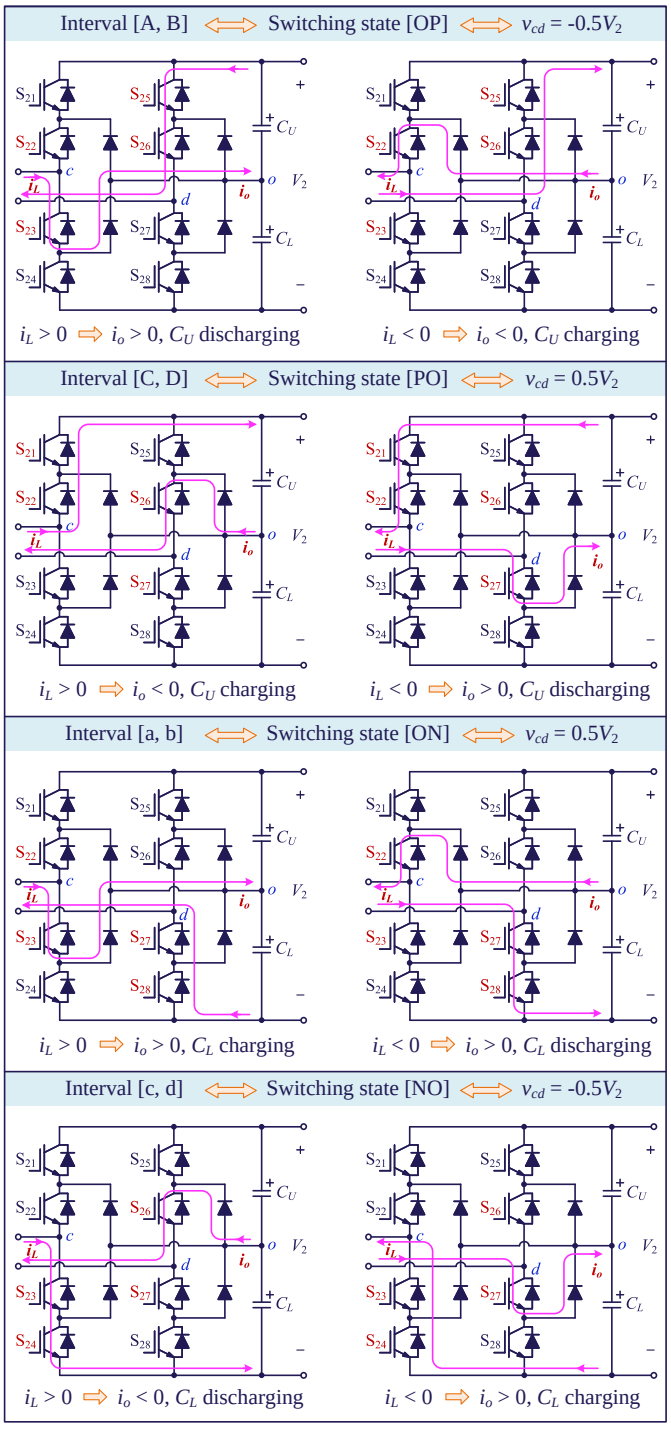


Fig. 8. Current conduction paths under the four switching states [OP], [PO], [NO], and [ON] when the inductor current i_L is positive and negative. Note that $i_L > 0$ means that i_L flows from the primary to the secondary side, $i_o > 0$ means that i_o is injected into the neutral point, and vice versa.

into the neutral point, i.e., $i_o > 0$. When $I_L[\mathrm{A,B}] > 0$ and $I_L[\mathrm{C,D}] > 0$ (which means $I_L[\mathrm{a,b}] < 0$ and $I_L[\mathrm{c,d}] < 0$), the required positive neutral-point current can be obtained under the switching states [OP] and [NO], which can be seen from Fig. 8. Therefore, these two switching states are defined as beneficial switching states. Conversely, [PO] and [ON] are considered adverse switching states, as the neutral-point

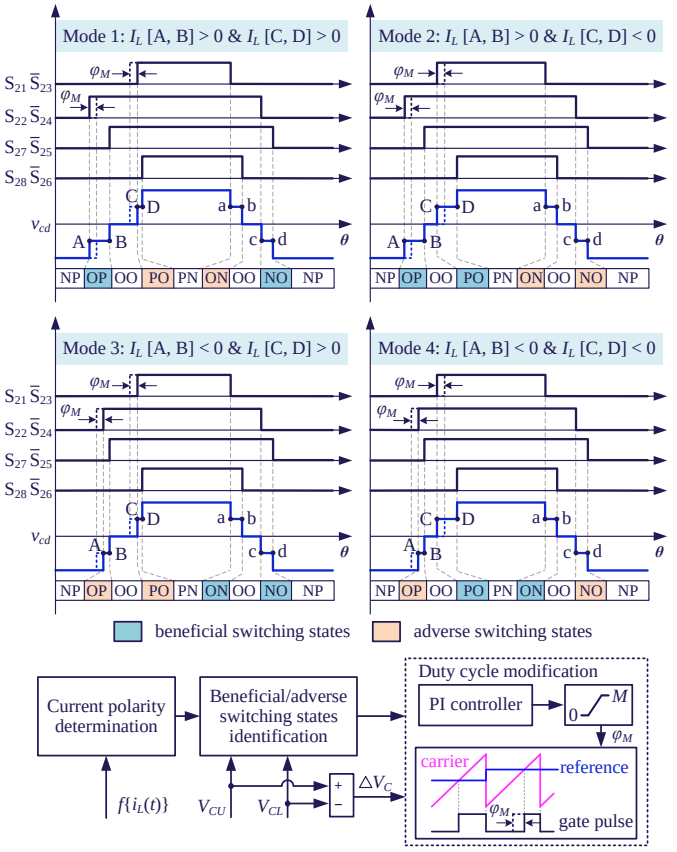


Fig. 9. Implementation of the modified-duty-cycle (MDC) voltage balancing method for the condition of $V_{CU} > V_{CL}$.

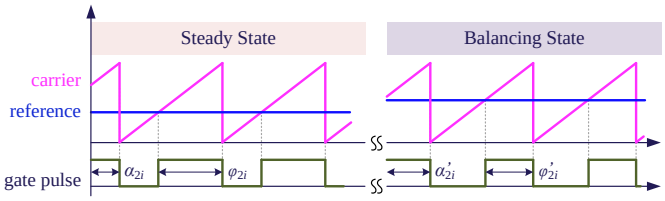


Fig. 10. Phase-shift angle and duty cycle of the gate pulse for each switch with capacitor voltage balancing control strategies.

current during these two switching states is negative. In Fig. 9 (as well as Figs. 11, 13, and 14), the beneficial and adverse switching states are marked in blue and yellow, respectively, and the dotted lines on the switching sequences and voltage v_{cd} denote the waveforms before the voltage balancing is enabled.

In order to increase the required charges to the neutral point, the dwell time of the beneficial switching states should be increased, while that of the adverse switching states should be decreased. In order to achieve this, the additional duty cycle φ_M is dynamically modified by a proportional-integral (PI) controller based on the error between the two capacitor voltages (i.e., $\triangle V_C = V_{CU} - V_{CL}$), and then, φ_M will be added to the original duty cycles of certain gate pulses to increase the required charges to the neutral point. Fig. 10 illustrates the gate pulse generation, where α_{2i} and φ_{2i}

($i = 1 \sim 8$) are the phase-shift angle and duty cycle of each switch during the steady state, and α'_{2i} and φ'_{2i} are that during the balancing state. In the MDC method, the phase-shift angles for all the switches are maintained unchanged while the duty cycles of S_{21} and S_{22} are modified (S_{23} and S_{24} are inverted by S_{21} and S_{22}, respectively). Therefore, the control variables in the MDC method during the capacitor voltage balancing state can be expressed as

$$\begin{aligned} &\alpha'_{2i} = \alpha_{2i}(i = 1 \sim 8), \varphi'_{2i} = \varphi_{2i}(i = 5 \sim 8) \\ &\begin{cases} \text{Mode 1}: \varphi'_{21} = \varphi_{21} - \varphi_M, \varphi'_{22} = \varphi_{22} + \varphi_M \\ \text{Mode 2}: \varphi'_{21} = \varphi_{21} + \varphi_M, \varphi'_{22} = \varphi_{22} + \varphi_M \\ \text{Mode 3}: \varphi'_{21} = \varphi_{21} - \varphi_M, \varphi'_{22} = \varphi_{22} - \varphi_M \\ \text{Mode 4}: \varphi'_{21} = \varphi_{21} + \varphi_M, \varphi'_{22} = \varphi_{22} - \varphi_M \end{cases} \end{aligned} \tag{3}$$

It should be noted that the duty cycle of the switches in the second bridge leg (i.e., $S_{25} \sim S_{28}$) can also be regulated for voltage balancing. However, the performance of the voltage balancing control will be similar to Fig. 9. Thus, this paper only analyze the condition when the duty cycles are modified for the switches in the first bridge leg (i.e., $S_{21} \sim S_{24}$) in the MDC method. In addition, M in Fig. 9 is the upper threshold for the output of PI controller, and is also the maximum value of φ_M, which will affect the dynamics of the NPC-based DAB converters in terms of current/power fluctuations and settling time during voltage balancing. In order to avoid voltage and current waveform distortion with constant switching sequence, the upper threshold M should be lower than $0.5(\pi - \varphi_1)$ [28].

On the other hand, for the other imbalance condition, i.e., $V_{CU} < V_{CL}$, $i_o < 0$ is required for voltage balancing. Consequently, the beneficial and adverse switching states will be opposite to the condition of $V_{CU} > V_{CL}$, and the duration of the four switching states [OP], [PO], [ON], and [NO] should also be regulated in an opposite way. For instance, when $I_L[\mathrm{A,B}] > 0$ and $I_L[\mathrm{C,D}] > 0$, the duty cycles will be adjusted as illustrated in Mode 4 of Fig. 9 for the condition of $V_{CU} < V_{CL}$. A similar condition applies also for the MPSDC method and CSS method.

B. Modified-Phase-Shift-and-Duty-Cycle (MPSDC) Method

Since the sawtooth carrier is used to generate the gate pulses of the power switches, when the reference is changed to regulate the duty cycle (see Fig. 9), the duration of the first two intervals [A, B] and [C, D] is modified by φ_M, while that of the other two intervals [a, b] and [c, d] is kept constant. If all the four intervals are required to change for a shorter balancing period, the phase-shift angles should be regulated together with the duty cycles. Fig. 11 shows a typical MPSDC method with different inductor current polarity, where α_M is used to modify the phase-shift angles and duty cycles. For Mode 1 and Mode 4, the duty cycles are not changed, and the phase-shift angles are increased or decreased by α_M. On the other hand, both the phase-shift angles and duty cycles should be regulated for Mode 2 and Mode 3. The control variables

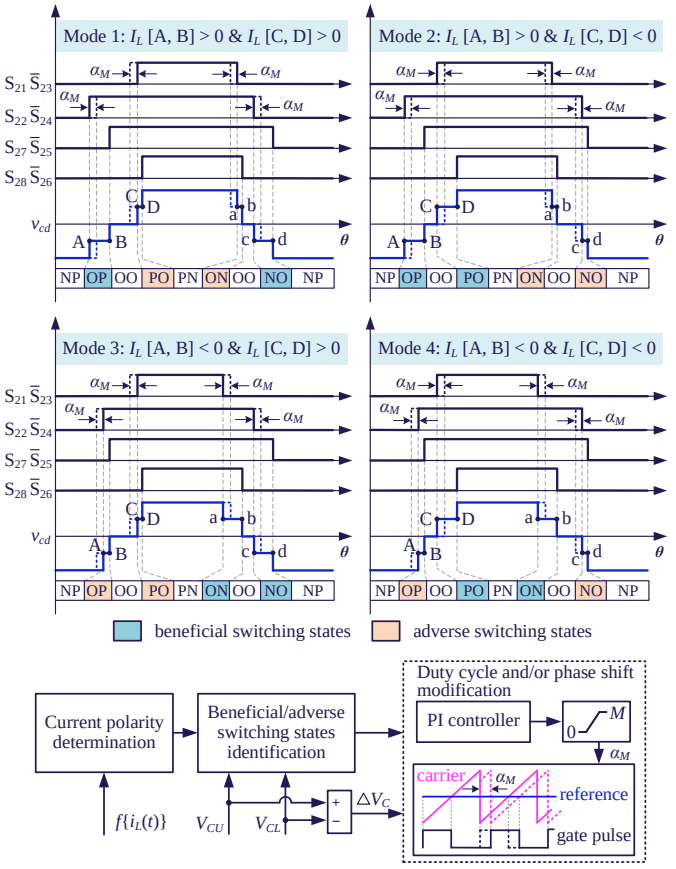


Fig. 11. Implementation of the modified-phase-shift-and-duty-cycle (MPSDC) voltage balancing method for the condition of $V_{CU} > V_{CL}$.

for the four modes during the voltage balancing are expressed as

$$\begin{aligned} &\alpha'_{2i} = \alpha_{2i}(i = 5 \sim 8), \varphi'_{2i} = \varphi_{2i}(i = 5 \sim 8) \\ &\begin{cases} \text{Mode 1}: \begin{cases} \alpha'_{21} = \alpha_{21} + \alpha_M, \alpha'_{22} = \alpha_{22} - \alpha_M, \\ \varphi'_{21} = \varphi_{21}, \varphi'_{22} = \varphi_{22} \end{cases} \\ \text{Mode 2}: \begin{cases} \alpha'_{21} = \alpha_{21} + \alpha_M, \alpha'_{22} = \alpha_{22} + \alpha_M, \\ \varphi'_{21} = \varphi_{21} + 2\alpha_M, \varphi'_{22} = \varphi_{22} + 2\alpha_M \end{cases} \\ \text{Mode 3}: \begin{cases} \alpha'_{21} = \alpha_{21} - \alpha_M, \alpha'_{22} = \alpha_{22} - \alpha_M, \\ \varphi'_{21} = \varphi_{21} - 2\alpha_M, \varphi'_{22} = \varphi_{22} - 2\alpha_M \end{cases} \\ \text{Mode 4}: \begin{cases} \alpha'_{21} = \alpha_{21} - \alpha_M, \alpha'_{22} = \alpha_{22} + \alpha_M, \\ \varphi'_{21} = \varphi_{21}, \varphi'_{22} = \varphi_{22} \end{cases} \end{cases} \end{aligned} \tag{4}$$

C. Fixed-Switching-State (FSS) Method

In the above two approaches, the capacitor voltages are balanced by regulating the original four switching states [OP], [PO], [ON], and [NO]. Thus, the beneficial and adverse switching states should be determined based on inductor current polarity, which requires heavy pre-calculations and potentially cause other issues (detailed in Section IV). In order to decouple the voltage balancing from the current polarity identification, the FSS method introduces two additional switching states [$N_{(+)}N_{(+)}$] and [$P_{(-)}P_{(-)}$] (as defined in Table II) [27], [47]. Under the two additional switching states, the direction of the neutral-point current i_o can be controlled

TABLE II
ADDITIONAL SWITCHING STATES FOR FSS METHOD

Switching State	ON Switches (first arm)	ON Switches (second arm)
$[P_{(+)}]$	$\{S_{21}\}$	$\{S_{25}\}$
$[P_{(-)}]$	$\{S_{22}\}$	$\{S_{26}\}$
$[N_{(+)}]$	$\{S_{23}\}$	$\{S_{27}\}$
$[N_{(-)}]$	$\{S_{24}\}$	$\{S_{28}\}$

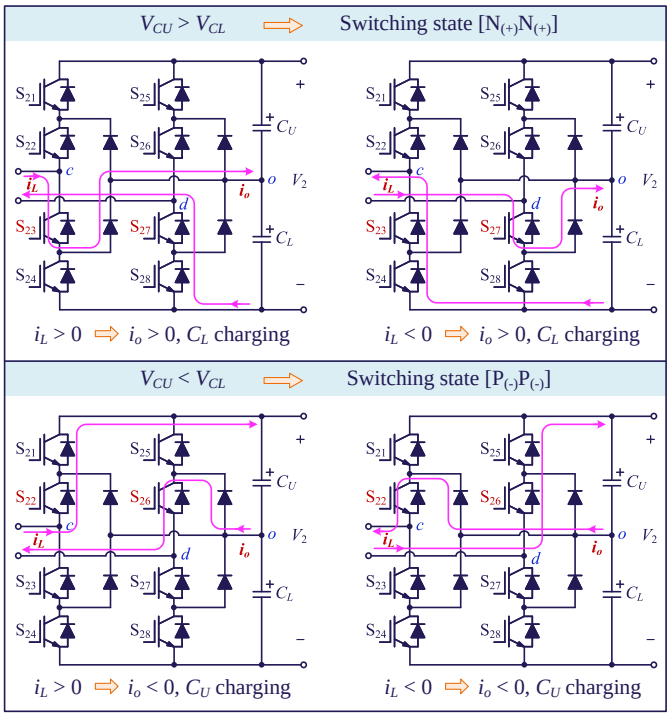


Fig. 12. Current flow paths for the switching state $[N_{(+)}N_{(+)}]$ and $[P_{(-)}P_{(-)}]$ for $V_{CU} > V_{CL}$ and $V_{CU} < V_{CL}$, respectively.

regardless of the inductor current polarity, as shown in Fig. 12. Therefore, a certain switching state, determined by the unbalanced condition, is employed during intervals [E, F] and [e, f], i.e., $[N_{(+)}N_{(+)}]$ when $V_{CU} > V_{CL}$, and $[P_{(-)}P_{(-)}]$ when $V_{CU} < V_{CL}$, as shown in Fig. 13, where V_{thr} is the threshold to activate the voltage balancing control. It can be seen from Fig. 13 that certain phase-shift angles and/or duty cycles should be regulated to obtain the fixed switching state $[N_{(+)}N_{(+)}]$ or $[P_{(-)}P_{(-)}]$. However, since the gate pulses for S_{21} and S_{24} are kept unchanged, they can be used as reference signals, and the other gate pulses can be obtained by

$$\begin{aligned} V_{CU} > V_{CL}: &\begin{cases} S_{22} = S_{21}, S_{23} = \overline{S}_{21}, S_{28} = S_{21} \\ S_{25} = S_{24}, S_{26} = S_{24}, S_{27} = \overline{S}_{24} \end{cases} \\ V_{CU} < V_{CL}: &\begin{cases} S_{26} = \overline{S}_{21}, S_{27} = S_{21}, S_{28} = S_{21} \\ S_{22} = \overline{S}_{24}, S_{23} = S_{24}, S_{25} = S_{24} \end{cases} \end{aligned} \tag{5}$$

By doing so, the phase-shift angles and duty cycles for certain switches are not required to calculate, which can simplify the implementation of the voltage balancing control.

D. Complementary-Switching-State (CSS) Method

During the voltage balancing with the MDC, MPSDC, and FSS methods, the voltage v_{cd} changes, as shown in Figs. 9, 11, and 13. Thus, the inductor current and transferred power will fluctuate. To avoid current overshoots and improve the DAB dynamics, the CSS method was proposed [28], [48]. In this method, the CSS pairs refer to two switching states that enable the neutral-point current i_o to flow in opposite directions while maintaining the same voltage v_{cd}. Accordingly, it can be obtained from Fig. 8 that [PO] and [ON], [OP] and [NO] are two CSS pairs.

Fig. 14 depicts the CSS method under different inductor current polarity. For instance, as earlier analyzed, [PO] and [ON] are the adverse switching states when $I_L[\text{A}, \text{B}] > 0$ and $I_L[\text{C}, \text{D}] > 0$. Thus, these two switching states should be replaced by their corresponding CSSs during the respective intervals, i.e., [PO] is replaced by [ON] during [C, D], and [ON] is replaced by [PO] during [a, b]. After the replacement, all the four switching states will be beneficial for voltage balancing due to the opposite direction of i_o. At the same time, the current and power fluctuations can be effectively suppressed due to the unchanged voltage v_{cd}. The control variables in the CSS method can be obtained by

$$\begin{cases} \text{Mode 1}: \begin{cases} \alpha'_{21} = \alpha_{21} + \alpha_s, \alpha'_{22} = \alpha_{22}, \\ \alpha'_{27} = \alpha_{27}, \alpha'_{28} = \alpha_{28} - \alpha_s, \\ \varphi'_{2i} = \varphi_{2i} (i = 1 \sim 8) \end{cases} \\ \text{Mode 2}: \begin{cases} \alpha'_{21} = \alpha_{21} + \alpha_s, \alpha'_{22} = \alpha_{22} + \alpha_s, \\ \alpha'_{27} = \alpha_{27} - \alpha_s, \alpha'_{28} = \alpha_{28} - \alpha_s, \\ \varphi'_{21} = \varphi_{21} + \alpha_s, \varphi'_{22} = \varphi_{22} + \alpha_s, \\ \varphi'_{27} = \varphi_{27} - \alpha_s, \varphi'_{28} = \varphi_{28} - \alpha_s \end{cases} \\ \text{Mode 3}: \begin{cases} \alpha'_{2i} = \alpha_{2i}, (i = 1 \sim 8) \\ \varphi'_{21} = \varphi_{21} - \alpha_s, \varphi'_{22} = \varphi_{22} - \alpha_s, \\ \varphi'_{27} = \varphi_{27} + \alpha_s, \varphi'_{28} = \varphi_{28} + \alpha_s \end{cases} \\ \text{Mode 4}: \begin{cases} \alpha'_{21} = \alpha_{21}, \alpha'_{22} = \alpha_{22} + \alpha_s, \\ \alpha'_{27} = \alpha_{27} - \alpha_s, \alpha'_{28} = \alpha_{28}, \\ \varphi'_{2i} = \varphi_{2i}, (i = 1 \sim 8) \end{cases} \end{cases} \tag{6}$$

The CSS method can achieve smooth dynamics without current and power fluctuations. However, since the beneficial and adverse switching states are determined by the inductor current polarity, the CSS method also requires the current polarity identification, which is similar to the MDC and MPSDC methods.

The main characteristics of the four capacitor voltage balancing methods have been summarized in Table III. The MDC, MPSDC, and CSS methods require current polarity identification to determine the beneficial and adverse switching states, as they apply the original switching states, i.e., [OP], [PO], [ON], and [NO], while the FSS method does not need due to applying two novel switching states $[N_{(+)}N_{(+)}]$ and $[P_{(-)}P_{(-)}]$. In addition, two of the four intervals [A, B], [C, D], [a, b], and [c, d] are regulated during each switching cycle for the MDC and CSS methods, while all the four intervals are modified for the MPSDC method. As for the FSS method, two novel intervals [E, F] and [e, f] are applied to regulate the

TABLE III
MAIN CHARACTERISTICS OF VARIOUS VOLTAGE BALANCING METHODS

Voltage balancing method	MDC	MPSDC	CSS	FSS
Current polarity identification	No need			Need
Applied switching states	Original switching states [OP], [PO], [ON], [NO]			Novel switching states [$N_{(+)}N_{(+)}$], [$P_{(-)}P_{(-)}$]
Number of modified intervals	2	4	2	2
Additional PI controller	Need		No need	

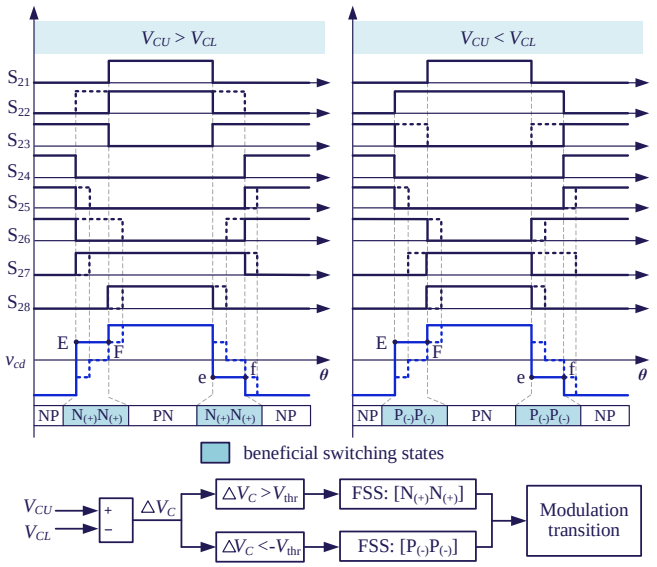


Fig. 13. Implementation of the fixed-switching-state (FSS) voltage balancing method.

capacitor voltages. Furthermore, an additional PI controller is used to regulate the time intervals of certain beneficial/adverse switching states in the MDC and MPSDC methods, while it is not required for the CSS and FSS methods as the regulated time intervals are determined by the phase-shift angles and duty cycles.

IV. EVALUATION OF CAPACITOR VOLTAGE BALANCING CONTROL STRATEGIES

The four voltage balancing control strategies apply different approaches to achieve the required neutral-point charges and realize capacitor voltage balance. Thus, they have different characteristics in terms of dynamics, robustness, implementation complexity, and so on. To benchmark these voltage balancing strategies, experimental tests are carried out based on a 2/3-level DAB setup, as shown in Fig. 15, and the main parameters are given in Table IV. It should be noted that the capacitor voltage imbalance in all the following experiments is generated by the asymmetrical gate pulses (see Fig. 4).

A. Dynamics

Fig. 16 shows the experimental results with various voltage balancing control strategies under the same operating parameters. In order to compare the voltage and current waveforms between steady state and balancing state, and verify the that the fluctuations on inductor current and output voltage are caused by the variations of terminal voltage v_{cd} as theoretical

TABLE IV
MAIN PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameters	Values
Rated power P	2.5 kW
Series inductor L_s	100 μH
DC-link capacitors C_{in}, C_U, and C_L	680 μF
Transformer turns ratio n	2
Switching frequency f_s	10 kHz
Power switches (IGBT)	Semikron SK35GB12T4

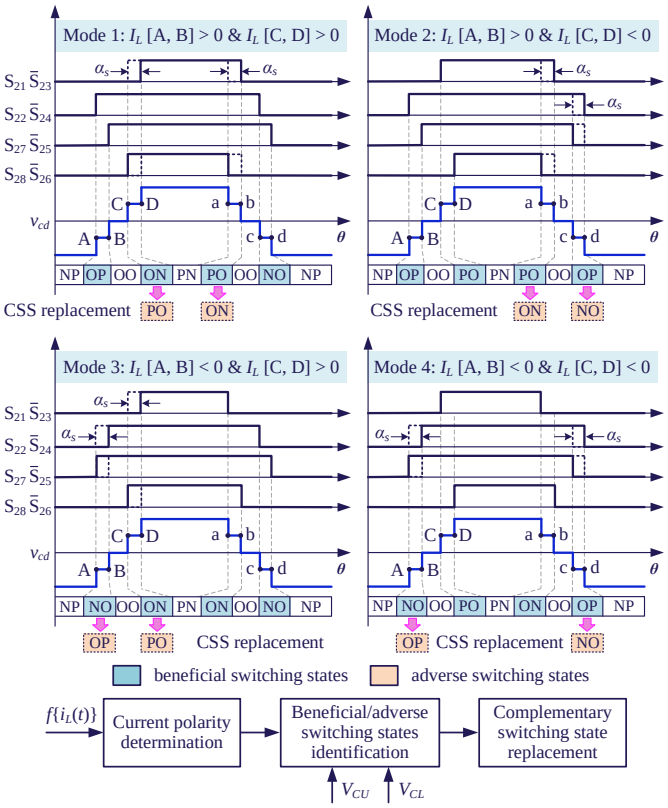


Fig. 14. Implementation of the complementary-switching-state (CSS) voltage balancing method for the condition of $V_{CU} > V_{CL}$.

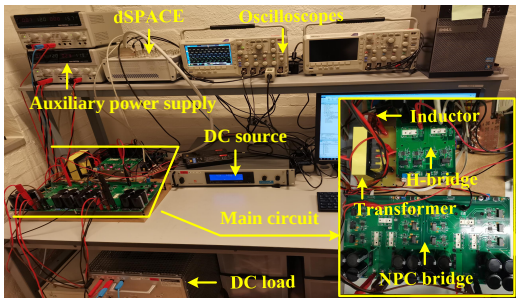
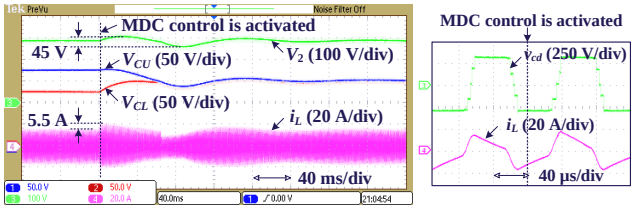
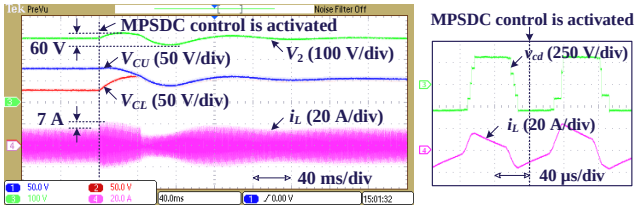


Fig. 15. A two-three (2/3)-level NPC-based DAB prototype.

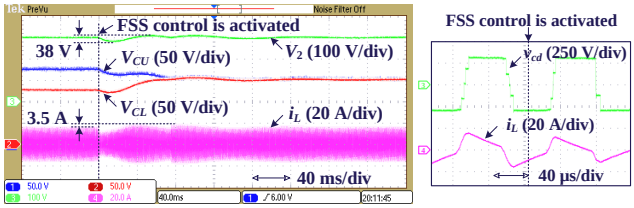
analysis, a large voltage imbalance value (i.e., $\triangle V_C = 50$ V) is applied in Fig. 16 to clearly show the balancing-state performances with various voltage balancing methods. It can be seen from Fig. 16 that the inductor current i_L and output voltage V_2 (i.e., the transferred power) will fluctuate in the MDC, MPSDC, and FSS methods, due to the changed voltage v_{cd} during the transition, which can be seen from the zoom-



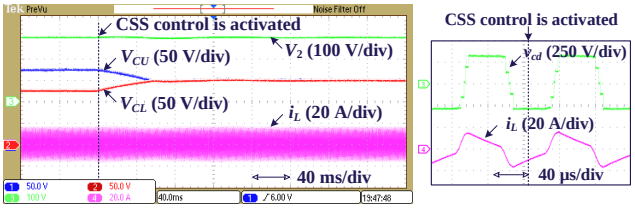
(a)



(b)



(c)

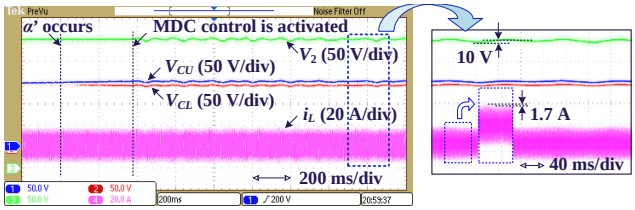


(d)

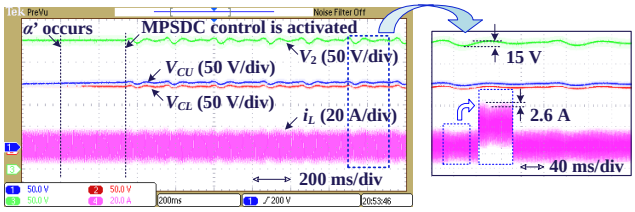
Fig. 16. Experimental results during the voltage balancing under the condition: $V_1 = 120$ V, $V_2 = 300$ V, $P = 950$ W, $\triangle V_C = 50$ V, $\varphi_1 = 0.9\pi$, $\alpha_p = 0.05\pi$, $\alpha_s = 0.06\pi$, and α_{ps} is regulated by PI controller to achieve reference output voltage with: (a) MDC method ($M = 0.05\pi$), (b) MPSDC method ($M = 0.05\pi$), (c) FSS method, and (d) CSS method.

in waveforms in Fig. 16(a)-(c). Furthermore, when the upper boundary (i.e., M) of the modified duty cycle/phase-shift angle and the parameters of PI controller in the MDC and MPSDC methods are the same, the inductor current and output voltage oscillation is larger with the MPSDC method (60-V $\triangle V_2$ and 7-A $\triangle I_L$) compared to the MDC method (45-V $\triangle V_2$ and 5.5-A $\triangle I_L$). This is because all the four intervals [A, B], [C, D], [a, b], and [c, d] are regulated in the MPSDC method, which causes more severe voltage distortion. However, the balancing period will also be shorten with the MPSDC method due to the same reason. On the other hand, the transition dynamics can be maintained smooth without inductor current and output voltage fluctuations with the CSS method, since the voltage v_{cd} can be kept unchanged, as shown in Fig. 16(d).

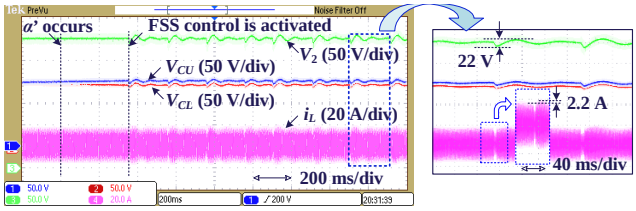
When there is a continuous imbalance source in the modulation or hardware circuits, the DAB converter will be switched between the steady state and the balancing state frequently. Fig. 17 shows the experimental results of the four voltage balancing methods with a continuous disturbance phase-shift angle α', which is constant in each switching cycle. Since



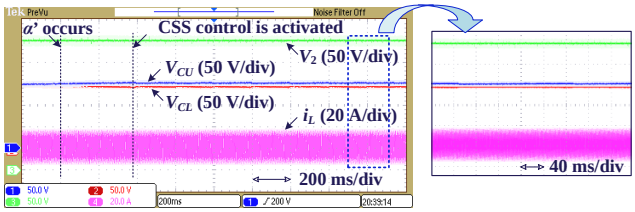
(a)



(b)



(c)



(d)

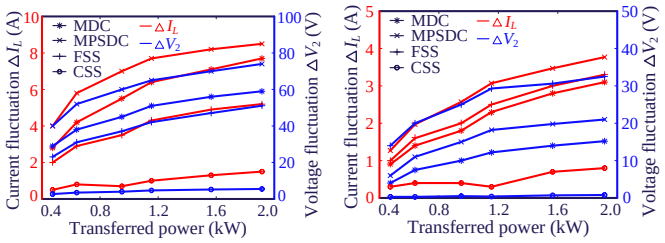
Fig. 17. Experimental results under a continuous α' ($\alpha' = 0.005\pi$) and the same parameters as Fig. 16 with: (a) MDC method, (b) MPSDC method, (c) FSS method, and (d) CSS method.

the threshold voltage V_{thr} for activating the voltage balancing control should not be too large to avoid significant voltage imbalance (e.g., $V_{\text{thr}} = 5$ V is applied in Fig. 17), the additional control variables φ_M and α_M in the MPSDC method will be limited. Thus, the inductor current and output voltage fluctuations caused by the frequent transitions will be low, as shown in Fig. 17(a) and (b). As for the FSS method, due to more significant change on the voltage v_{cd} (see Fig. 13), the fluctuations will be more severe, which can be seen from Fig. 17(c). On the other hand, as shown in Fig. 17(d), the dynamics can be improved with the CSS method, because the voltage v_{cd}, as well as the inductor current and the transferred power, will be the same between the steady and balancing states, even if the converter is switched between the two states frequently.

The inductor current and output voltage oscillation (i.e., $\triangle I_L$ and $\triangle V_2$) with various voltage balancing approaches under different power levels is shown in Fig. 18, which is expressed as

$$\begin{aligned} \triangle I_L &= I_{pb} - I_{ps} \\ \triangle V_2 &= V_{2max} - V_{2min} \end{aligned} \tag{7}$$

where I_{pb} and I_{ps} are peak values of inductor current in the balancing state and steady state, respectively, and V_{2max}



Transferred power (W)	Control variables
475	$\{\alpha_p, \alpha_s, \varphi_1\}$={0.1$\pi$, 0.06$\pi$, 0.95$\pi$,}
640	$\{\alpha_p, \alpha_s, \varphi_1\}$={0.05$\pi$, 0.06$\pi$, 0.95$\pi$,}
950	$\{\alpha_p, \alpha_s, \varphi_1\}$={0.05$\pi$, 0.06$\pi$, 0.9$\pi$,}
1155	$\{\alpha_p, \alpha_s, \varphi_1\}$={0.05$\pi$, 0.06$\pi$, 0.9$\pi$,}
1565	$\{\alpha_p, \alpha_s, \varphi_1\}$={0.05$\pi$, 0.06$\pi$, 0.9$\pi$,}
1915	$\{\alpha_p, \alpha_s, \varphi_1\}$={0.05$\pi$, 0.06$\pi$, 0.9$\pi$,}

(c)

Fig. 18. Fluctuations of inductor current and output voltage with various voltage balancing control strategies under different power levels when $V_1 = 120$ V and $V_2 = 300$ V: (a) for the condition when $\triangle V_C = 50$ V, (b) for the condition with a continuous imbalance factor ($\alpha' = 0.005\pi$ and $V_{\text{thr}} = 5$ V), and (c) the control variables under various power levels (Note: the outer phase-shift angle α_{ps} is regulated by a PI controller).

and V_{2min} are the highest and lowest values of the output voltage during the voltage balancing. Fig. 18(a) illustrates the fluctuations when the capacitor voltage error is 50 V (similar to Fig. 16), and Fig. 18(b) shows the condition with a continuous imbalance factor (similar to Fig. 17). As shown in Fig. 18(a), MPSDC method will cause the highest inductor current and output voltage fluctuations under various power levels with a large voltage imbalance ($\triangle V_C = 50$ V). In addition, it can be seen from Fig. 18(b) that the output voltage will oscillate the most with the FSS method with a continuous imbalance factor and limited threshold V_{thr} ($\alpha' = 0.005\pi$ and $V_{\text{thr}} = 5$ V) due to more severe waveform distortion on v_{cd}. On the other hand, the CSS method can achieve lowest transient fluctuations under various power levels.

Fig. 19 shows the experimental waveforms under various capacitor voltage balancing methods with a step change on the output voltage and transferred power under the condition of $\alpha' = 0.005\pi$ (i.e., continuous imbalance source) and $V_{\text{thr}} = 5$ V. It can be seen from Fig. 19 that these methods can balance the capacitor voltages in these cases. On the other hand, the CSS method can achieve the best dynamic performance, while the other three methods will result in inductor current and output voltage fluctuations.

B. Efficiency

Generally, the efficiency of the DAB converters is determined by the conduction and switching losses of power switches, and magnetic losses. The root-mean-sqaure (RMS) values of the inductor current will strongly affect the conduction losses and magnetic losses [49]. Thus, due to the inductor current fluctuations during the voltage balancing in the MDC, MPSDC, and FSS methods, the conduction losses and magnetic losses will be affected. As for the CSS method, the inductor current can be kept unchanged, and thus, the conduction and magnetic losses will be similar to those of

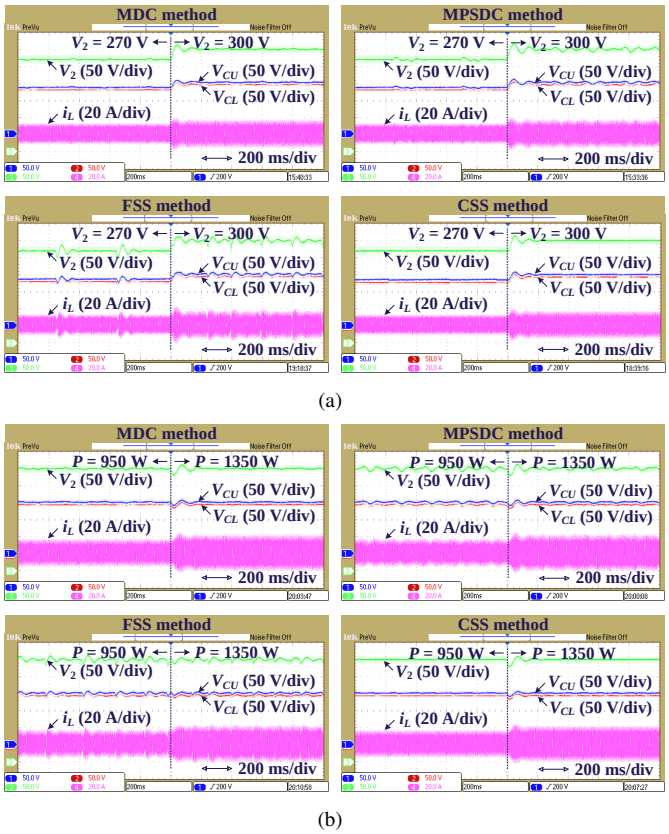


Fig. 19. Experimental results under various capacitor voltage balancing methods with a step change on: (a) output voltage (from 270 V to 300 V), and (b) transferred power (from 950 W to 1350 W).

the steady state. On the other hand, the number of switching for all the voltage balancing control strategies is not increased, i.e., all the switches are turned ON and OFF once during each switching period with the four voltage balancing methods. Therefore, the switching losses will not be increased by the number of switching. However, the hard/soft-switching states for the switches will be affected due to the current zero-crossing point drift. For instance, Fig. 20 illustrates the ZVS conditions during the steady and balancing states using different voltage balancing methods based on the 2/3-level DAB prototype. The operating parameters are identical to those shown in Fig. 16. As shown in Fig. 20, the inductor currents at the turn-ON instants (i.e., points A, B, C, and D) are positive in the steady state. Thus, all the switches are turned ON in ZVS based on the ZVS constraints [50], [51], which can be seen, for instance, from the waveforms of the collector-emitter and gate-emitter voltages (i.e., v_{ce} and v_{ge}) of S_{22}. Nevertheless, after activating the MDC, MPSDC, or FSS balancing control, the waveforms of v_{cd} and i_L will change, as well as the current polarity at the switching instants. As a result, certain switches, e.g., S_{22}, will be turned-ON in non-ZVS, as shown in Fig. 20. On the other hand, although the switching sequence will also change in the CSS method, the current polarity at the turn-ON instants will not change. Thus, the soft-switching operation will not be affected. Fig. 21 shows the corresponding average power loss distribution obtained by simulation in PLECS, where the conduction and switching losses of IGBTs are obtained based on the parameters (e.g., on resistance)

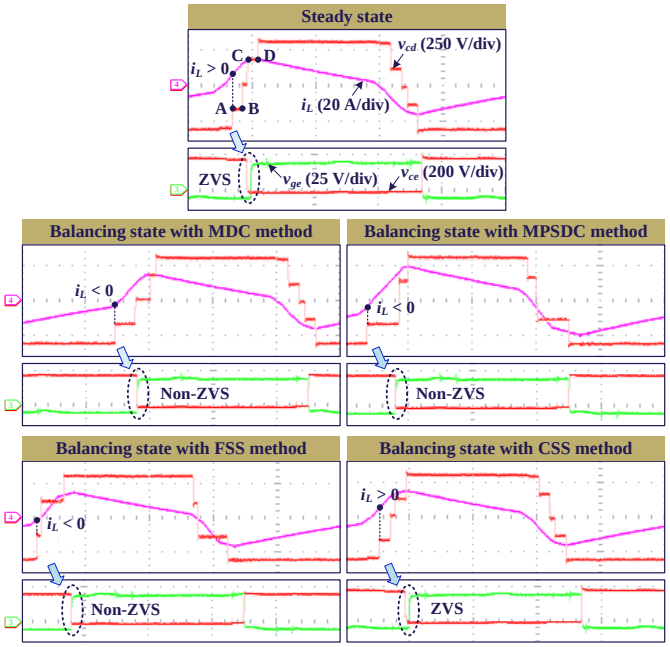


Fig. 20. Experimental results of the ZVS states in steady state and the balancing state with various voltage balancing methods based on the 2/3-level DAB prototype.

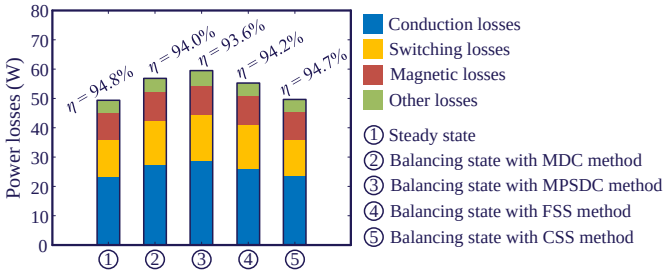


Fig. 21. Power loss distribution and corresponding efficiency (i.e., η) with various voltage balancing methods applied to the 2/3-level DAB prototype.

and electro-thermal model (extracted from datasheet) of the IGBT. On the other hand, the power losses of transformer, inductor and other components are calculated based on the analytical power-loss models discussed in [49], [52]. It can be seen from Fig. 21 that the conduction losses, switching losses, and magnetic losses after applying the CSS control can basically be maintained constant compared to those of the steady state, while the power losses with the the other three methods will be increased. Therefore, the efficiency (i.e., η) of the DAB converter under the CSS control is similar to that of the steady state. However, by applying the MDC, MPSDC, or FSS control, the efficiency will be lowered. This can be further confirmed by the experimental efficiency comparison under different power levels based on the 2/3-level DAB prototype, as shown in Fig. 22, where the operating parameters are the same as Fig. 18(c).

C. Robustness

The beneficial and adverse switching states in the MDC, MPSDC, and CSS methods are identified based on the inductor current polarity at the instant of voltage balancing control activation, and are generally assumed to be unchanged during

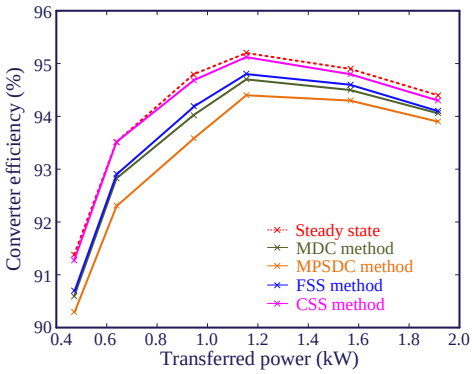


Fig. 22. Converter efficiency with various voltage balancing control methods under different power levels in the 2/3-level DAB prototype.

the voltage balancing process (i.e., before a balancing state finishes). This is because: (1) when the parameters change during balancing state, the dynamic current polarity cannot be estimated by the steady-state current model. In addition, the current model during dynamic process is very difficult to be obtained, making the current polarity during balancing state hard to determine; (2) when the current polarity is re-identified during the balancing process with the CSS method, the control variables (i.e., phase-shift angles and duty cycles) cannot be obtained by (6), because the switching sequence has already been changed after the voltage balancing control is activated. Thus, to determine the switching sequence if the voltage balancing control is updated during the balancing state, the new expressions of the control variables should be explored, which will make the modulation system very complicated due to multiple transition cases. Therefore, the capacitor voltage balancing control keeps unchanged during the balancing state. As a result, when the operating parameters change during the voltage balancing, the performance of these three methods will be deteriorated in certain conditions due to their model-based feature.

Fig. 23 illustrates the simulations when a step change occurs on the transferred power levels during the voltage balancing. As shown in Fig. 23(a), when the voltage balancing control is enabled, the current polarity is positive during interval [A, B]. Thus, the corresponding switching state is identified as a beneficial one when $V_{CU} > V_{CL}$, and increasing its duration is needed for the MDC method. However, following the step change, the current polarity during [A, B] becomes negative, making the switching state adverse for voltage balancing. As a result, the extended interval [A, B] for the MDC control will increase the incorrect-direction charges to the neutral point, which will impede the voltage balancing. The worst condition is when the required neutral-point charge is less than that of the other direction due to the incorrect identification of the beneficial and adverse switching states, the voltage imbalance will become worse, and the two capacitor voltages cannot be balanced, as shown in Fig. 23(a). The MPSDC and CSS methods have similar issue due to the model-based feature, as shown in Fig. 23(b) and (d). On the contrary, the FSS method will not be affected by the changed current polarity, and thus, the two capacitor voltages can still be balanced after the step change, as shown in Fig. 23(c). Therefore,

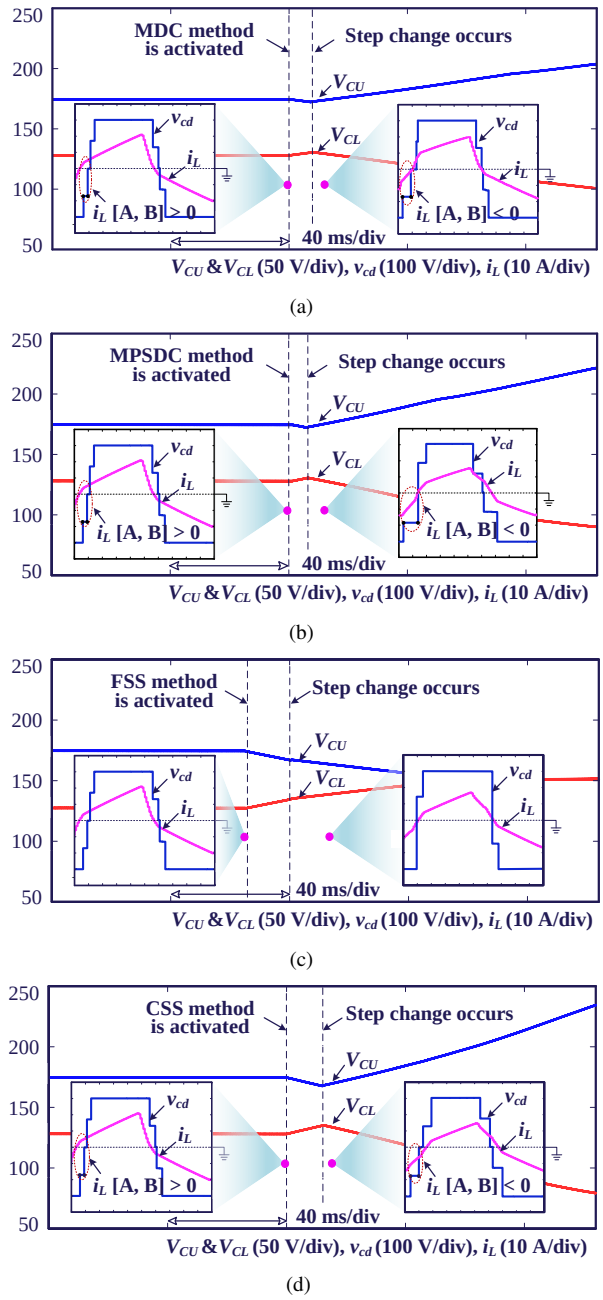


Fig. 23. Simulation results when the transferred power changes from 1580 W to 1200 W under $V_1 = 200$ V and $V_2 = 300$ V with: (a) MDC method, (b) MPSDC method, (c) FSS method, and (d) CSS method.

compared to the other three approaches, the robustness against parameter variations can be enhanced by the FSS method. Furthermore, even though there is no parameter change, the variation of zero-crossing point of the inductor current during voltage balancing with the MDC and MPSDC methods may also cause a wrong inductor current polarity identification and opposite neutral-point current. This issue will not occur on the CSS method, as the inductor current waveform (i.e., current zero-crossing point) maintains unchanged after applying the CSS method. Therefore, the CSS method has better robustness compared to the MDC and MPSDC methods.

It is worth pointing out that when the operating parameters of the DAB converters remain within a limited range, or when

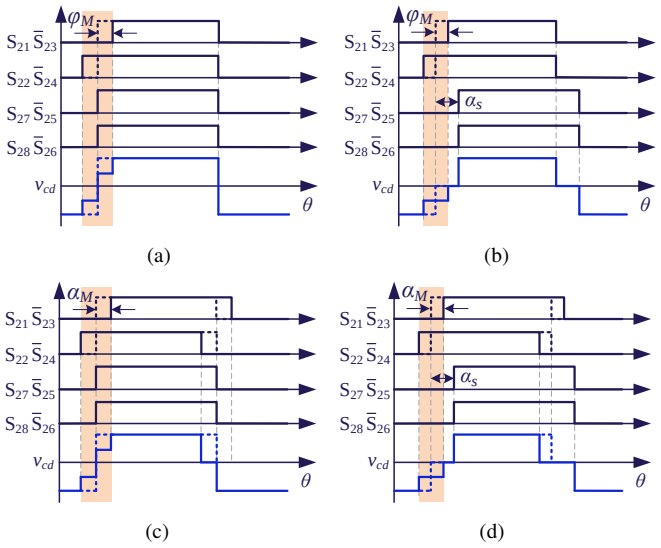


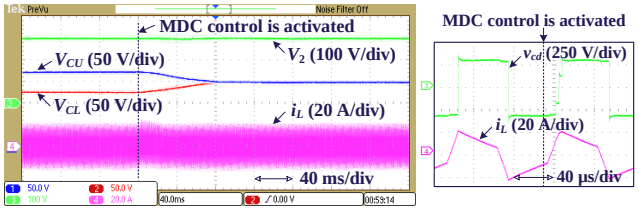
Fig. 24. Balancing-state waveforms with: (a) MDC method in SPS control, (b) MDC method in TPS control, (c) MPSDC method in SPS control, and (d) MPSDC method in TPS control.

it operates in ZVS state across the entire power range, the inductor current polarity will remain constant during specific intervals (e,g., [A, B]). Consequently, parameter variations will not affect the identification of beneficial and adverse switching states, which can improve the robustness of the MDC, MPSDC, and CSS methods under such conditions. In addition, multiple current polarity identification and voltage balancing update during the balancing process can also enhance the robustness, which requires more exploration in the future.

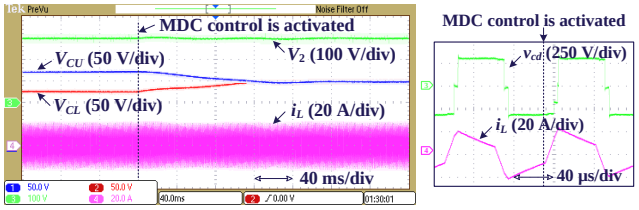
D. Applicability With Modulation Strategy

All the above is analyzed based on the five-level control, and the voltage balancing control strategies should also be applied to other control schemes if different control schemes are used to achieve certain optimization objectives. For the SPS and TPS control, the current will not flow through the neutral point o in ideal operation, i.e., the four switching states [OP], [PO], [ON], and [NO] are not employed, as shown in Fig. 7. Therefore, the CSS method cannot be used to balance the capacitor voltages in the SPS and TPS control, since the interval of the complementary switching states after replacement is 0. As for the MDC and MPSDC methods, by modifying the phase-shift angle or duty cycle, the intervals where the current can flow through the neutral point will appear, as shown in the shaded area of Fig. 24. Fig. 25 shows the experimental results when the MDC and MPSDC voltage balancing methods are applied to the SPS and TPS control, where it can be seen that after activating the voltage balancing method, the capacitor voltages can be balanced with the additional intervals. Furthermore, when the FSS method is applied, two intervals [E, F] and [e, f] (see Fig. 13) are used to balance the capacitor voltages, and the two intervals are expressed as

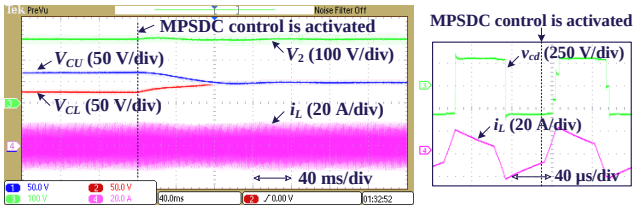
$$t_{[E,F]} = t_{[e,f]} = \alpha_s + \frac{\varphi_2 - \varphi_1}{2} \tag{8}$$



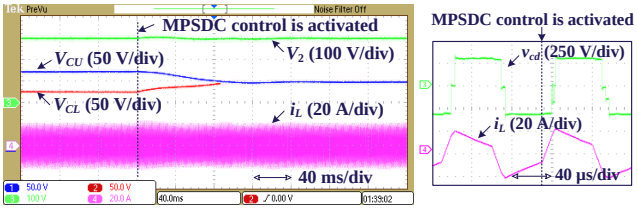
(a)



(b)



(c)



(d)

Fig. 25. Experimental results for the voltage balancing control under the condition of $V_1 = 120$ V, $V_2 = 300$ V, $P = 950$ W, and $M = 0.06\pi$ V with: (a) MDC method in SPS control, (b) MDC method in TPS control ($\alpha_s = 0.08\pi$), (c) MPSDC method in SPS control, and (d) MPSDC method in TPS control.

In the TPS control, the two duty cycles φ_1 and φ_2 are the same (see Fig. 7(b)), and the intervals [E, F] and [e, f] are equal to α_s based on (8). Thus, the FSS method can be used to balance the capacitor voltages with the TPS control. On the other hand, in the SPS control, the two intervals are 0 due to $\alpha_s = 0$ and $\varphi_1 = \varphi_2$. Therefore, if the FSS method is applied to the SPS control, the two switching states [$N_{(+)}N_{(+)}$] and [$P_{(-)}P_{(-)}$] can be added by an additional control variable φ_M, as shown, e.g., in Fig. 26. As is to say, the FSS method is able to be used to SPS control, but requires additional regulation on the gate pulses, since the relationship among the control variables in (5) is no longer applicable.

It should be noted that when the phase-shift angle α_s is close to 0, the five-level control shown as Fig. 2 will be similar to TPS control. Thus, although the NPC-based DAB converter still works in five-level control scheme, the intervals where the charges can flow through the neutral point are close to 0. As a result, the capacitor voltage balancing will be very slow if applying the CSS method. In this scenario, the other three methods, i.e., MDC, MPSDC, and FSS methods can be applied to achieve voltage balancing. Furthermore, if the duty

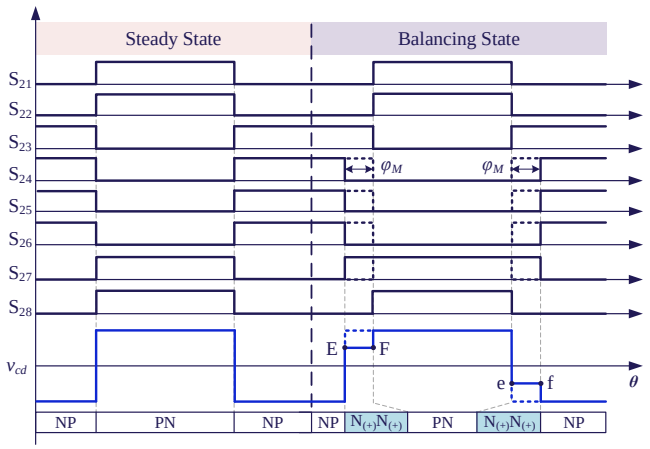


Fig. 26. An example when the FSS method id used to the SPS control.

cycles φ_1 and φ_2 in the five-level control are close to 50%, the five-level control will be similar to SPS control, and thus, MDC or MPSDC method is preferred for voltage balancing.

E. Implementation Complexity

According to the previous analysis, the MDC, MPSDC and CSS methods require identification of the beneficial and adverse switching states based on the inductor current polarity. Thus, in order to increase the duration of the beneficial switching states in the MDC and MPSDC methods, or to replace the adverse switching states in the CSS method, the current polarity models during the four intervals should be pre-calculated, as this current is usually not measured physically with a sensor. Especially, compared to the CSS method where the waveform of the inductor current remains unchanged, the zero-crossing points of the inductor current will dynamically float during the voltage balancing with the MDC and MPSDC methods, resulting in a more complicated pre-calculation and current polarity identification. Moreover, the voltage balancing may be affected if the current model is not accurate due to the non-ideal factors, e.g., power losses and slight DC bias on i_L. On the other hand, the employed switching states in the FSS method enable the neutral-point current to flow independently of the inductor current polarity. Therefore, the pre-calculation for the inductor current polarity is not needed in the FSS method, and thus, its implementation can be simplified compared to the other three approaches. In addition, the performance of the MDC and MPSDC methods is affected by the value of M (see Figs. 9 and 11). Fig. 27 shows the experimental results for the MPSDC method with different M (MDC method has similar performance). It can be seen that with a lower M, the current and power fluctuations can be reduced, while the settling time will be increased. Thus, a trade-off between the current fluctuations and balancing period should be made by suitably selecting the value of M when the MPSDC or MDC method is used. Therefore, the implementation of MPSDC and MDC methods are more complicated than the CSS method.

TABLE V
EVALUATION OF THE CAPACITOR VOLTAGE BALANCING APPROACHES

Method	References	Dynamics	Efficiency	Robustness	Extensibility	Implementation
MDC	[45], [46]	current and output voltage fluctuations are large with a large M and $\triangle V_C$	lower than the steady state in ZVS operation	low, will be affected by load variation and current zero-crossing point drift	high, can be used to various control schemes	difficult, due to current polarity identification and choice for M
MPSDC	[38]–[44]	current fluctuations are larger than the MDC method	lower than MDC method due to larger RMS current	same as the above	same as the above	same as the above
FSS	[27], [47]	output voltage fluctuations are large with a continuous imbalance source	lower than the steady state in ZVS operation	high, will not be affected by current polarity variation	medium, can be used to TPS control, but needs additional regulation in SPS control	simple, due to no need of current polarity identification
CSS	[28], [48]	smooth without significant current fluctuation	high, equal to the steady state	low, will be affected by load variation, but will not be affected by current zero-crossing point drift	low, cannot be used to SPS/TPS control	medium, due to current polarity identification

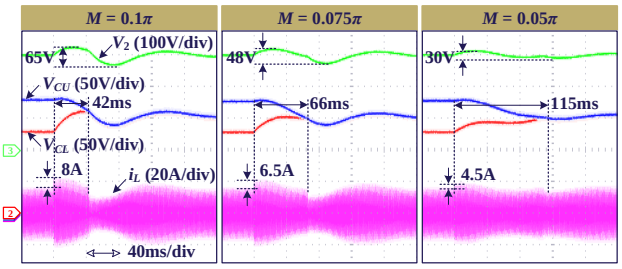


Fig. 27. Dynamics with the MPSDC method under various M (i.e., the upper boundary of α_M in Fig. 11).

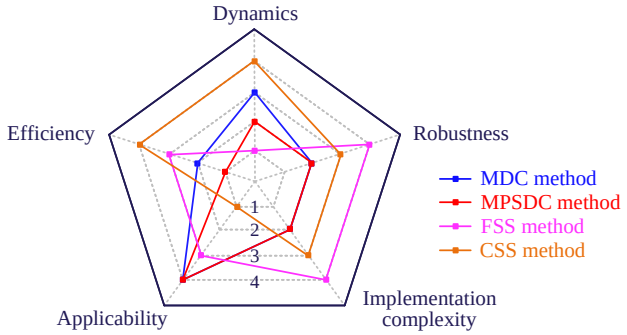


Fig. 28. Comparison chart for various voltage balancing approaches.

F. Discussion and Application

Table V summarizes the characteristics of the four voltage balancing approaches based on the above analysis. Furthermore, a quantitative comparison among these methods is conducted, as shown in Fig. 28, where the four approaches are sorted under each performance issue and assigned scores of 1 to 4. Note that a higher score indicates less pre-calculation burdens and implementation complexity, and better dynamics, efficiency, robustness, and extensibility. In addition, when two voltage balancing methods have similar performance, e.g., pre-calculation burdens for MDC and MPSDC methods, the two methods are assigned the same score. It should be noted that according to the previous analysis, the MPSDC method has worst dynamics with a large capacitor voltage error (see Fig. 16 and Fig. 18(a)), while the FSS method will cause the most significant output voltage oscillation with a continuous imbalance source and limited threshold V_{thr} (see Fig. 17 and Fig. 18(b)). In most cases, when the voltage balancing control is included in the control system, the capacitor voltage error $\triangle V_C$ will not increase to a large value, as the threshold V_{thr} for triggering the voltage balancing will be set as limited. In addition, a continuous imbalance source will cause a more severe negative effect, which requires focused consideration. Thus, the dynamics are evaluated based on the second condition (i.e., Fig. 17 and Fig. 18(b)).

From Table V and Fig. 28, the superiority and suitable applications for each approach can be obtained as:

- CSS control method exhibits superior dynamics, particularly when there is a continuous factor causing voltage imbalance. Additionally, it can improve the efficiency of the DAB converter during the transition compared to the other three methods. However, the model-based feature of this approach restricts its application to the scenarios where operating parameters vary extensively, due to its low robustness against parameter variations and heavy pre-calculation burdens. In addition, the CSS method cannot be extended to SPS and TPS control, which will also hinder its use in certain conditions. Therefore, the typical situations where this method is applicable are: 1) variation range of operating parameters is limited, so that the the inductor current polarity can be easily determined; 2) soft-switching operation under five-level control, as the inductor current polarity is unchanged at the switching instants; 3) applications with a continuous imbalance factor, due to the low current and power oscillation, and high efficiency under the long-term adjustment.
- The two switching states $[\text{N}_{(+)}\text{N}_{(+)}]$ and $[\text{P}_{(-)}\text{P}_{(-)}]$ involved in the FSS method provide the advantages of low pre-calculation burdens, high robustness, and simple implementation due to independence on inductor current polarity. Nevertheless, frequent transitions between steady and balancing states may cause large fluctuations on inductor current and output voltage that can negatively affect its performance. Thus, the FSS method is mainly suitable for the condition with a wide parameter variation (e.g., energy storage systems), while without continuous imbalance factor and frequent transitions.
- MDC and MPSDC methods have similar performances, and they do not have superiority in terms of most performance

indices compared to the other two methods. However, they can be extended to various phase-shift control strategies without additional regulation. Thus, when SPS or TPS control is employed to the steady state to simplify the control algorithm compared to the five-level control [50], [53], MDC and MPSDC methods can be used to balance the capacitor voltages. Notably, it has been confirmed that SPS control will be used for the condition of $k = 1$ (k is the voltage conversion ratio, defined as $k = nV_1/V_2$), and TPS control is suitable under the condition of $k > 1$ [4], [54]. Therefore, MDC or MPSDC method is suitable to such conditions.

V. Conclusion

This paper has presented four capacitor voltage balancing approaches for the NPC-based DAB converters, i.e., MDC, MPSDC, FSS, and CSS methods. Subsequently, an evaluation of these approaches was conducted based on a 2/3-level NPC-based DAB prototype, where the characteristics including dynamics, efficiency, robustness, applicability, and implementation complexity have been compared. Comparative results show that the FSS method can achieve lowest control complexity and highest robustness against operating parameter variations. However, the dynamics and efficiency of the DAB converter are negatively affected, especially with frequent transitions between steady and balancing states caused by a continuous imbalance source. On the contrary, the CSS method can realize the best performance in terms of dynamics and efficiency. If the DAB converter operates under soft-switching conditions or in applications where operating parameters remain within a limited range, it is easy to determine and maintain the inductor current polarity regardless of the operating parameters. Consequently, the performance in terms of robustness and implementation complexity can also be improved. Under such conditions, the CSS method is the most suitable voltage balancing approach. Nevertheless, the CSS method is not suitable in SPS and TPS control schemes, where the MDC or MPSDC method can be applied easily. Certain issues about voltage balancing of the NPC-based DAB converters should be analyzed in the future, e.g., the voltage balancing during the start-up/shut-down process (as the dynamic current polarity is difficult to be determined), and multiple current polarity identification and updates during balancing state to enhance the robustness of the MDC, MPSDC, and CSS methods.

References

[1] S. Zhao, Y. Chen, S. Cui, B. J. Mortimer, and R. W. De Doncker, "Three-Port Bidirectional Operation Scheme of Modular-Multilevel DC-DC Converters Interconnecting MVDC and LVDC Grids," *IEEE Trans. Power Electron*., vol. 36, no. 7, pp. 7342-7348, Jul. 2021.

[2] L. Wang, Q. Zhu, W. Yu, and A. Q. Huang, "A Medium-Voltage Medium-Frequency Isolated DC-DC Converter Based on 15-kV SiC MOSFETs," *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 5, no. 1, pp. 100-109, Mar. 2017.

[3] S. Du, B. Wu, K. Tian, D. Xu, and N. R. Zargari, "A Novel Medium-Voltage Modular Multilevel DC-DC Converter," *IEEE Trans. Ind. Electron*., vol. 63, no. 12, pp. 7939-7949, Dec. 2016.

[4] C. Song, A. Sangwongwanich, Y. Yang, Y. Pan, and F. Blaabjerg, "Analysis and optimal modulation for 2/3-Level DAB converters to minimize current stress with five-level control," *IEEE Trans. Power Electron*., vol. 38, no. 4, pp. 4596-4612, Apr. 2023.

[5] Y. Chen, S. Zhao, Z. Li, X. Wei, and Y. Kang, "Modeling and Control of the Isolated DC-DC Modular Multilevel Converter for Electric Ship Medium Voltage Direct Current Power System," *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 5, no. 1, pp. 124-139, Mar. 2017.

[6] J. Yao, W. Chen, C. Xue, Y. Yuan, and T. Wang, "An ISOP Hybrid DC Transformer Combining Multiple SRCs and DAB Converters to Interconnect MVDC and LVDC Distribution Networks," *IEEE Trans. Power Electron*., vol. 35, no. 11, pp. 11442-11452, Nov. 2020.

[7] S. Du, B. Wu, K. Tian, D. Xu, and N. R. Zargari, "A Novel Medium-Voltage Modular Multilevel DC-DC Converter," *IEEE Trans. Ind. Electron*., vol. 63, no. 12, pp. 7939-7949, Dec. 2016.

[8] I. Alhurayyis, A. Elkhateb, and J. Morrow, "Isolated and Nonisolated DC-to-DC Converters for Medium-Voltage DC Networks: A review," *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 9, no. 6, pp. 7486-7500, Dec. 2021.

[9] Y. Chen, S. Zhao, Z. Li, X. Wei, and Y. Kang, "Modeling and Control of the Isolated DC-DC Modular Multilevel Converter for Electric Ship Medium Voltage Direct Current Power System," *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 5, no. 1, pp. 124-139, Mar. 2017.

[10] L. Zhu, C. Li, H. Yang, S. Ren, S. Zhang, W. Li, and X. He, "Buck-Boost Type High Step-Down Low Power Modular Converter for Medium Voltage DC Systems," *IEEE Trans. Power Electron*., vol. 38, no. 1, pp. 634-646, Jan. 2023.

[11] E. A. Gunther. The State of Medium voltage Architectures for Utility-Scale PV. (2018). [Online]. Available: https://www.pv-tech.org/the-state-of-medium-voltage-dc-architectures-for-utility-scale-pv/

[12] G. Ning, W. Chen, L. Shu, J. Zhao, W. Cao, J. Mei, C. Liu, and G. Qiao, "A Hybrid Resonant ZVZCS Three-Level Converter for MVDC-Connected Offshore Wind Power Collection Systems," *IEEE Trans. Power Electron*., vol. 33, no. 8, pp. 6633-6645, Aug. 2018.

[13] F. Zhang, Y. Ren, X. Yang, W. Chen, and H. Wu, "Capacitor Voltage Balancing Control for a Novel 5-Level Dual Active Bridge Converter," *IEEE Trans. Power Electron*., vol. 37, no. 12, pp. 14738-14754, Dec. 2022.

[14] D. Liu, F. Deng, and Z. Chen, "Five-Level Active-Neutral-Point-Clamped DC/DC Converter for Medium-Voltage DC Grids," *IEEE Trans. Power Electron*., vol. 32, no. 5, pp. 3402-3412, May 2017.

[15] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Open-Circuit Fault Diagnosis and Tolerant Control for 2/3-Level DAB Converters," *IEEE Trans. Power Electron*., vol. 38, no. 4, pp. 5392-5410, Apr. 2023.

[16] Z. Feng, H. Wen, Q. Bu, Y. Zhu, X. Han, J. Zhu, E. Lim, W. Liu, and Y. Hu, "Loss Balance and Transient DC-Bias Suppression Strategies in Three-Level DAB Converters Modulated With Five DoFs," *IEEE Trans. Power Electron*., Early access, doi: 10.1109/TPEL.2023.3262797.

[17] Y. Xuan, X. Yang, W. Chen, T. Liu, and X. Hao, "A Novel NPC Dual-Active-Bridge Converter With Blocking Capacitor for Energy Storage System," *IEEE Trans. Power Electron*., vol. 34, no. 11, pp. 10635-10649, Nov. 2019.

[18] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Optimal Control of Multi-Level DAB Converters for Soft-Switching and Minimum Current Stress," *IEEE Trans. Power Electron*., Early Access, doi: 10.1109/TPEL.2024.3362051.

[19] R. Pradhan, S. B. Shah, M. I. Hassan, Z. Wang, and A. Emadi, "A 15 kW Wide-Input Reconfigurable Three-Level DAB Converter for On-Board Charging of 1.25 kV Electric Vehicle Powertrains," *IEEE Trans. Transport. Electrific*., Early access, doi: 10.1109/TTE.2024.3358110.

[20] C. Li, T. Yang, P. Kulsangcharoen, G. Lo Calzo, S. Bozhko, C. Gerada, and P. Wheeler, "A Modified Neutral Point Balancing Space Vector Modulation for Three-Level Neutral Point Clamped Converters in High-Speed Drives," *IEEE Trans. Ind. Electron*., vol. 66, no. 2, pp. 910-921, Feb. 2019.

[21] A. Agarwal, S. Sharma, and S. Bhattacharya, "Comparison and Performance Evaluation of the Mid-Point Voltage Balance Modulation Schemes for A Three-phase 2L-3L DAB," in *Proc. IEEE ECCE*, Nashville, TN, USA, 2023, pp. 3372-3379.

[22] L. Dai, H. Wen, P. Xu, Z. Feng, G. Wang, X. Wang, and J. Rodriguez, "Boundary Control Based Capacitor Voltage Balancing for Two/three-Level Neutral-Point-Clamped Dual-Active-Bridge Converters,"in *Proc. IEEE IPEMC2024-ECCE Asia*, Chengdu, China, 2024, pp. 3101-3106.

[23] S. Busquets Monge, S. Somavilla, J. Bordonau, and D. Boroyevich, "Capacitor Voltage Balance for the Neutral-Point-Clamped Converter using the Virtual Space Vector Concept With Optimized Spectral Performance," *IEEE Trans. Power Electron*., vol. 22, no. 4, pp. 1128-1135, Jul. 2007.

[24] F. Zhang, Y. Ren, X. Yang, W. Chen, and H. Wu, "Capacitor Voltage Balancing Control for a Novel 5-Level Dual Active Bridge Converter," *IEEE Trans. Power Electron*., vol. 37, no. 12, pp. 14738-14754, Dec. 2022.

[25] A. Zorig, S. Barkat, and A. Sangwongwanich, "Neutral Point Voltage Balancing Control Based on Adjusting Application Times of Redundant Vectors for Three-Level NPC Inverter," *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 10, no. 5, pp. 5604-5613, Oct. 2022.
[26] S. Mukherjee, S. K. Giri, and S. Banerjee, "A Flexible Discontinuous Modulation Scheme With Hybrid Capacitor Voltage Balancing Strategy for Three-Level NPC Traction Inverter," *IEEE Trans. Ind. Electron*., vol. 66, no. 5, pp. 3333-3343, May 2019.
[27] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "A Model-Free Capacitor Voltage Balancing Method for Multilevel DAB Converters," *IEEE Trans. Power Electron*., vol. 38, no. 1, pp. 79-84, Jan. 2023.
[28] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Capacitor Voltage Balancing for Multilevel Dual-Active-Bridge DC-DC Converters," *IEEE Trans. Ind. Electron*., vol. 70, no. 3, pp. 2566-2575, Mar. 2023.
[29] L. A. Budiwicaksana and D. -C. Lee, "Submodule Capacitor Voltage Balancing Through High-Frequency-Side Control for Multiport MMC-Based Solid-State Transformers," *IEEE Open J. Ind. Electron. Soc*., vol. 5, pp. 302-316, Apr. 2024.
[30] Y. Lyu, Y. Zi, and X. Li, "Improved Control of Capacitor Voltage Balancing in Modular Multilevel Converter Submodules," *IEEE Access*, vol. 12, pp. 19510-19519, Jan. 2024.
[31] J. Saha, N. B. Y. Gorla, and S. K. Panda, "Implementation of Power Balance Control Scheme for a Cascaded Matrix-Based Dual-Active-Bridge (CMB-DAB) MVAC-LVDC Converter," *IEEE Trans. Ind. Appl..*, vol. 58, no. 1, pp. 388-399, Jan.-Feb. 2022.
[32] H. Yang, Z. Cheng, X. Zhang, P. Zhou, T. Yang, and S. Jing, "Topology and Hybrid Modulation of Six-Level Switched-Capacitor HC Converter With Improved DC-Link Capacitor Voltage Balancing," *IEEE Trans. Power Electron*., vol. 39, no. 4, pp. 4325-4349, Apr. 2024.
[33] M. R. Chowdhury, S. Chowdhury, M. A. Rahman, and M. R. Islam, "Advanced Switching Sequences Based Model-Predictive Control for Single-Phase NPC Converters," *IEEE Trans. Ind. Electron*., vol. 69, no. 4, pp. 3515-3526, Apr. 2022.
[34] R. Stala, "Application of Balancing Circuit for DC-Link Voltages Balance in a Single-Phase Diode-Clamped Inverter With Two Three-Level Legs," *IEEE Trans. Ind. Electron*., vol. 58, no. 9, pp. 4185-4195, Sept. 2011.
[35] P. Liu and S. Duan, "Analysis of the Neutral-Point Voltage Self-Balance Mechanism in the Three-Level Full-Bridge DC-DC Converter by Introduction of Flying Capacitors," *IEEE Trans. Power Electron*., vol. 34, no. 12, pp. 11736-11747, Dec. 2019.
[36] H. Feng et al., "Passive Capacitor Voltage Balancing of SiC-Based Three-Level Dual-Active-Bridge Converter Using Hybrid NPC-Flying Capacitor Structure," *IEEE Trans. Power Electron*., vol. 37, no. 4, pp. 4183-4194, Apr. 2022.
[37] J. Pang, K. Wang, Z. Zheng, and Y. Li, "Modulation and Capacitor Voltage Balancing Control of a Hybrid Four-Level DAB With Reduced Switches," in *Proc. ICEMS*, Zhuhai, China, 2023, pp. 3698-3703.
[38] G. Niyitegeka, E. M. Harerimana, G. Park, and J. Choi, "Phase Shift Modulation and DC-Link's Voltage Balancing Control for a DAB DC-DC Converter," in *Proc. icSmartGrid*, Nagasaki, Japan, 2018, pp. 70-75.
[39] M. A. Moonem, T. Duman, and H. Krishnaswami, "Capacitor Voltage Balancing in a Neutral-Point Clamped Multilevel DC-DC Dual Active Bridge Converter," in *Proc. IEEE PEDG*, Brazil, 2017, pp. 1-7.
[40] A. F. Martinez, S. B. Monge, and J. Bordonau, "Modulation and Capacitor Voltage Balancing Control of Multilevel NPC Dual Active Bridge DC-DC Converters," *IEEE Trans. Ind. Electron*., vol. 67, no. 4, pp. 2499-2510, Apr. 2020.
[41] X. Yu, K. Jin, and Z. Liu, "Capacitor Voltage Control Strategy for Half-Bridge Three-Level DC/DC Converter," *IEEE Trans. Power Electron*., vol. 29, no. 4, pp. 1557-1561, Apr. 2014.
[42] A. F. Martinez, S. B. Monge, J. N. Apruzzese, and J. Bordonau, "Operating Principle and Performance Optimization of a Three-Level NPC Dual-Active-Bridge DC-DC Converter," *IEEE Trans. Ind. Electron*., vol. 63, no. 2, pp. 678-690, Feb. 2016.
[43] J. Pang, K. Wang, Z. Zheng, T. Zheng, and Y. Li, "Quasi Two-Level Operation and Neutral-Point Voltage Balance Method for a Four-Level ANPC based Dual Active Bridge DC-DC Converter," in *Proc. IEEE ECCE*, Detroit, MI, USA, 2022, pp. 1-7.
[44] P. Joebges, A. Gorodnichev, and R. W. De Doncker, "Modulation and Active Midpoint Control of a Three-Level Three-Phase Dual-Active Bridge DC-DC Converter under Non-Symmetrical Load," in *Proc. IEEE ECCE Asia*, Niigata, Japan, 2018, pp. 375-382.
[45] J. Yang, Z. Shu, T. Wang, S. Xiang, J. Nie, S. Wang, Y. Lei, and L. Ma, "Online Digital Implementation of Wide Voltage Range RMS-Current-Optimized Control With Voltage Balancing Capability for DAB Converter," *IEEE Trans. Power Electron*., vol. 38, no. 4, pp. 4360-4377, Apr. 2023.
[46] X. Wu, Y. Zhang, and J. Yang, "Neutral-Point Voltage Balancing Method for Three-Phase Three-Level Dual-Active-Bridge Converters," *Energies*, 15(17):6463, Sep. 2022.
[47] M. A. Awal, M. R. H. Bipu, O. A. Montes, H. Feng, I. Husain, W. Yu, and S. Lukic, "Capacitor Voltage Balancing for Neutral Point Clamped Dual Active Bridge Converters," *IEEE Trans. Power Electron*., vol. 35, no. 10, pp. 11267-11276, Oct. 2020.
[48] J. Lee, H. Choi, and J. Jung, "Three Level NPC Dual Active Bridge Capacitor Voltage Balancing Switching Modulation," in *Proc. IEEE INTELEC*, Broadbeach, Australia, 2017, pp. 438-443.
[49] B. Liu, P. Davari, and F. Blaabjerg, "An Optimized Hybrid Modulation Scheme for Reducing Conduction Losses in Dual Active Bridge Converters," *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 9, no. 1, pp. 921-936, Feb. 2021.
[50] L. Jin, B. Liu, and S. Duan, "ZVS Soft Switching Operation Range Analysis of Three-Level Dual-Active Bridge DC-DC Converter under Phase Shift Control Strategy," *IEEE Trans. Ind. Appl*., vol. 55, no. 2, pp. 1963-1972, Mar-Apr. 2019.
[51] P. Liu and S. Duan, "A ZVS Range Enhancement Strategy for the DAB Converter by Using Blocking Capacitors," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 9, no. 2, pp. 1389-1398, Apr. 2021.
[52] M. Turzynski, S. Bachman, M. Jasinski, S. Piasecki, M. Rylko, H. Chiu, S. Kuo, and Y. Chang. "Analytical Estimation of Power Losses in a Dual Active Bridge Converter Controlled with a Single-Phase Shift Switching Scheme," *Energies*, 15(21):8262, Nov. 2022.
[53] Y. Wang, H. Wen, Y. Zhu, H. Shi, Q. Bu, Y. Hu, and Y. Yong, "Minimum-Current-Stress Scheme of Three-Level Dual-Active-Bridge DC-DC Converters With the Particle Swarm Optimization," *IEEE Trans. Transport. Electrific*., vol. 7, no. 4, pp. 2067-2084, Dec. 2021.
[54] N. Hou, W. Song, and M. Wu, "Minimum-Current-Stress Scheme of Dual Active Bridge DC-DC Converter With Unified Phase-Shift Control," *IEEE Trans. Power Electron*., vol. 31, no. 12, pp. 8552-8561, Dec. 2016.

Chaochao Song (S'21-M'24) received the B.S. degree in automation and M.S. degree in power electronics from Shandong University, Ji'nan, China, in 2016 and 2019, respectively, and the Ph.D. degree in energy technology from Aalborg University, Denmark, in 2023. He was a Visiting Researcher with Fraunhofer ISE, Freiburg, Germany from June to September, 2022.

He is currently working as a postdoc at Aalborg University, Aalborg, Denmark. His current research interests include control of DAB converters, multi-level converters, and modeling of SiC-based power electronic converters.

Ning Wang (S'22) received the B.Eng. and M.Sc. degrees from Jilin University, Changchun and Xi'an Jiaotong University, Xi'an, China, in 2015 and 2018, respectively. Now he has been working toward a PhD degree in Aalborg University, Aalborg, Denmark. His research interests include DC-DC converter, advance control algorithm and renewable energy system.

Ariya Sangwongwanich (S'15-M'19-SM'24) received the B.Eng. degree in electrical engineering from Chulalongkorn University, Thailand, in 2013, and the M.Sc. and Ph.D. degree in energy engineering from Aalborg University, Denmark, in 2015 and 2018, respectively. He is currently working as an Assistant Professor at the Department of Energy, Aalborg University, where he is a Vice-Leader of Photovoltaic Systems research program. He was a Visiting Researcher with RWTH Aachen, Aachen, Germany in 2017 and University of Cambridge, Cambridge, United Kingdom in 2023.

Dr. Sangwongwanich was the recipient of the Danish Academy of Natural Sciences' Ph.D. Prize and the Spar Nord Foundation Research Award for his Ph.D. thesis in 2019. His research interests include control of grid-connected converters, photovoltaic systems, and reliability and sustainability in power electronics.

Yongheng Yang (SM'17) earned his B.Eng. degree in electrical engineering and automation from Northwestern Polytechnical University, China, in 2009, and his Ph.D. degree in energy technology from Aalborg University, Denmark, in 2014.

He pursued postgraduate studies at Southeast University, China, from 2009 to 2011 and was a Visiting Scholar at Texas A&M University, USA, during March-May 2013. From 2014 to 2020, he was associated with the Department of Energy Technology at Aalborg University, where he achieved the rank of tenured Associate Professor in 2018. In January 2021, he joined Zhejiang University in China as a ZJU100 Professor. He became a Zhejiang Kunpeng Investigator in 2023. His research focuses on grid-friendly integration of photovoltaic systems and control of power converters, specifically grid-forming technologies.

Dr. Yang served as the Chair of the IEEE Denmark Section in 2019-2020 and is an Associate Editor for several IEEE Transactions. He received the 2018 IET Renewable Power Generation Premium Award and was recognized as an Outstanding Reviewer for the IEEE Transactions on Power Electronics in 2018. He was the recipient of the 2021 Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society (PELS) and the 2022 IEEJ Isao Takahashi Power Electronics Award. In addition, he has received three IEEE Best Paper Awards. He was included on the list of the Highly Cited Chinese Researchers by Elsevier in 2022-2023. He is presently a Vice Chair of the IEEE PELS Technical Committee on Sustainable Energy Systems and a Council Member of the China Power Supply Society.

Frede Blaabjerg (S'86-M'88-SM'97-F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998 at AAU Energy. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania in 2017 and Tallinn Technical University (TTU), Estonia in 2018.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, Power-2-X, power quality and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of eight monographs and editor of fourteen books in power electronics and its applications eg. the series (4 volumes) Control of Power Electronic Converters and Systems published by Academic Press/Elsevier.

He has received 38 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves as a President of IEEE Power Electronics Society. He has been Vice-President of the Danish Academy of Technical Sciences. He is nominated in 2014-2020 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.