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Published in:
I E E E Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2012.2204713

Publication date:
2013

Document Version
Early version, also known as pre-print

Small-Signal Modeling of Digitally Controlled Grid-Connected Inverters with LCL Filters

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***Abstract*—When LCL filters are applied to digitally controlled grid-connected inverters, the design of controllers is usually implemented using classic average models. The accuracy of these models in s-domain is only guaranteed in low frequency range. In order to predict the dynamic behaviors, new small-signal z-domain models are deduced for digitally controlled grid-connected inverters with converter current control scheme and converter current plus grid current control scheme. The proposed methods model the inverters including different delay effects under most possible circumstances, which allows direct design for controllers in z-domain. The stability boundaries obtained from the root loci of the classic average models and the proposed z-domain models and the discrete state space models are compared to the simulation results, showing that the proposed z-domain models are more effective in predicting instabilities. Experimental results are presented and compared to the average models predictions and z-domain models predictions, which shows the proposed models are capable of predicting the values of control variables at the true sampling instants.**

***Index Terms*—Average models, digital control, grid-connected inverters, z-domain models.**

I. Introduction

In the last years, the use of LCL output filters to connect PWM inverters to the grid has been studied in detail [1]–[9]. Major part of this work consists of current sources connected to the grid that tries to export the maximum active power given by the prime mover, e.g. photovoltaic systems or wind turbine, by means of a maximum power point tracker (MPPT) algorithm. Compared to L filters, LCL filters employ much smaller size and lower cost inductors, since the capacitor impedance is inversely proportional to frequency of current. There is a trend that the LCL filters will be employed for all the grid-connected inverters in the future [10]. The design for the LCL filter has already been addressed [1]. However, maintaining stability of the control system when using an LCL filter is still an issue in the controller design, since those filters can bring even undesired resonance effects and thus stability problems, caused by zero impedance seen by some higher order harmonics of current.

Conventional proportional plus integral (PI) controllers for the current control loop have been commonly used for grid-connected LCL inverters, however the PI controller presents a steady-state error when tracking a sinusoidal reference and presents poor disturbance rejection capability. In order to overcome these problems, a proportional plus resonant (PR) controller was introduced and applied to three-phase pulse width modulation (PWM) inverter control. The resonant term was based on a general integrator tuned at the fundamental line frequency. Later on, PR scheme has been completed by means of harmonic resonant terms, which were general integrators tuned at the harmonics of interest frequencies. This way the total harmonic distortion (THD) of the current injected to the grid can be further reduced. However, the modeling of those digital controlled inverters where represented by means of analog models, being not precise and impacting over the closed-loop system performances.

Further, nowadays fully digital controllers are more and more used instead of analog controllers in high power switching converters, since the price/performance ratio of digital signal processors (DSPs) is decreasing dramatically. With floating-point DSPs embedding high resolution, high speed analog-to-digital converters (ADCs) and enhanced PWMs, the application of more complicated control algorithms becomes feasible. Moreover, although the signals measured from the power circuits contain considerable disturbance around switching instants, sampling algorithms can be used to obtain the average values with reduced switching ripple and noise [11], [12]. Due to these advantages, digital controllers for switching converters have attracted extensive interests during the last decade. However, the modeling for complicated digitally controlled systems is another issue in the controller design.

Generally, the design of digital controllers and the evaluation of the control performances are usually implemented by using classic average models. For digital control of grid-connected inverters with LCL filters, many control strategies have been proposed [5]–[8], [13]–[15] without including the sample and hold effect. In a more precise model, sample and hold effect has been well modeled [16], but the analog-to-digital conversion delay, the computation delay, the PWM delay and the transport delay are combined as a total delay. Since a practical digital controller using synchronous sampling method has complicated delay effect [17], the delay effects are different when the duty-ratio update mode varies. Therefore, more accurate models including delay effects should be provided in respect to different duty-ratio update modes.

In order to obtain a more accurate model, this paper presents a modeling method including the real sample and hold effect and delay effects. The new small-signal z-domain models are derived for two typical digitally controlled grid-connected in-

Manuscript received February 24, 2012; revised April 23, 2012, and May 28, 2012; accepted June 6, 2012.

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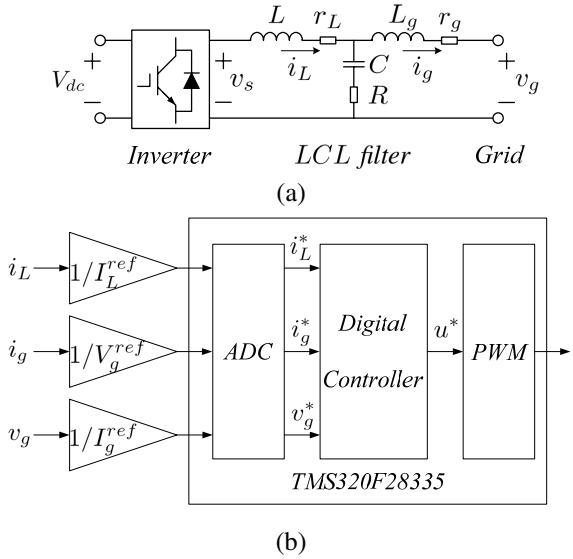


Fig. 1. Single phase inverter. (a) Power circuit. (b) Control circuit.

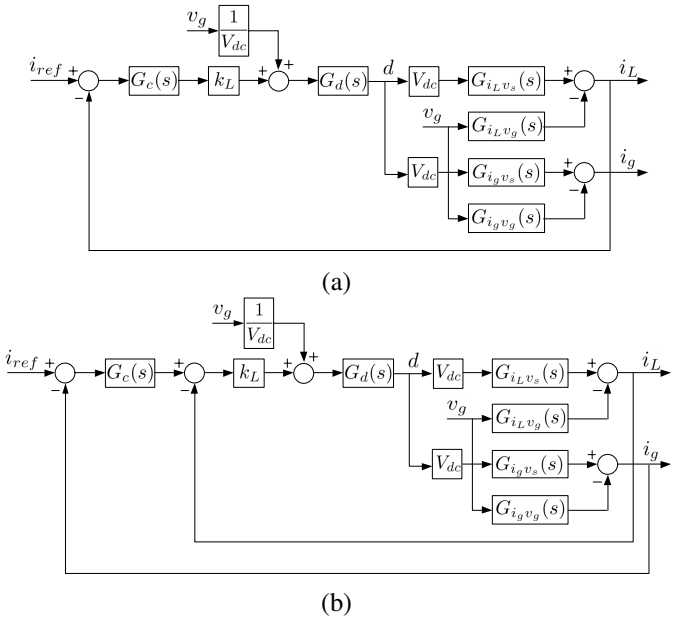


Fig. 2. The s-domain block diagrams of grid-connected inverters. (a) Converter current feedback scheme. (b) Converter current plus grid current feedback scheme.

verters with LCL filters. The z-domain models can be used to predict the stability boundaries, while using s-domain models may lead to erroneous results for stability analysis. Simulation results are provided to verify the capability of the proposed models in predicting gain boundaries. By using the proposed z-domain models, the design of the digital controllers can be directly implemented in z-domain. An experimental setup is implemented to validate the z-domain models in predicting the steady-state and transient responses.

This paper is organized as following. Section II presents the structure of digitally controlled grid-connected LCL inverters. Section III reviews the conventional average modeling for grid-connected inverters by using Laplace transform. Section IV presents the small-signal modeling of grid-connected digitally controlled inverters by using the z-transform. The PWM modeling is discussed and analyzed and, then, z-domain models and stability analysis are presented. Section V provides the discrete state space models to compare with the z-domain models. Section VI shows the validation of the presented models by means of simulations and experimental results. Finally, Section VII gives the conclusion.

II. Digitally Controlled Grid-Connected Inverters

The typical circuit diagram of a digitally controlled grid-connected inverter with an LCL filter is shown in Fig. 1. The analog variables (usually the converter current i_L, the grid current i_g and the grid voltage v_g) are converted into digital quantities via appropriate measurement circuits and ADCs. The process of converting signals into the specified range of ADCs can be ideally represented by scaling factors ($1/I_L^{ref}$, $1/V_g^{ref}$ and $1/I_g^{ref}$) [18]. To avoid the erroneously sampled value in the vicinity of the switching instant, the conversion of ADC is started when the PWM counters reach to zero or period values [11]. The digital quantities (i_L^*, i_g^* and v_g^*) converted from ADCs are scaled to be numerically equivalent to the relevant analog variables. By using a digital control algorithm, the duty-ratio is calculated and updated into the PWM controller as a command signal u^*. To generate the drive signals for the switches, the symmetric-on-time modulator is used in this paper [16].

III. Classic Average Models for Grid-Connected Inverters

Classic average models derive the transfer functions from the duty-ratio to the filter input voltage and current by averaging the filter input voltage in a switching cycle. The control circuit, although implemented digitally, is represented by a group of continuous equivalent transfer functions. In this paper, two typical control schemes are provided for examples, as is shown in Fig. 2. The first control scheme (see Fig. 2(a)) is the converter current feedback control scheme [6]. The second control scheme (see Fig. 2(b)), i.e., the converter current plus grid current feedback control scheme [19], is a typical controller with cascaded control loops. Although many papers use the converter current plus capacitor current feedback control scheme [15], [20], the control strategy is equivalent to the converter current plus grid current feedback control scheme from the dynamic point of view. Both controllers have the same total delay (processing delay and PWM delay) from the command signal to drive signals, which is expressed as $G_d(s) = e^{-s\tau_d}$. The delay effect with three typical values for τ_d can be used, i.e., with $\tau_d = T_s/2$ defined as the minimum delay, with $\tau_d = T_s$ defined as the medium delay and with $\tau_d = 3T_s/2$ defined as the maximum delay. The classic PR compensator (represented by $G_c(s)$) and the proportional compensator (represented by k_L) are used as examples for modeling. However, the modeling method in this paper is also applicable if other types of controllers are used.

Define the following as $f_a = LL_gC$, $f_b = C(L_g(R+r_L)+L(R+r_g))$, $f_c = L+L_g+C(r_Lr_g+Rr_L+Rr_g)$ and $f_d =$

TABLE I
PARAMETERS OF THE INVERTER

Symbol	Quantity	Value
V_{dc}	Input voltage amplitude	200 V
V_g	Grid voltage RMS value	110 V
T_s	Sampling and switching period	50 μs
τ_d	Delay time	150 μs
ω_1	Fundamental angular frequency	2π·50 rad/s
L	Converter side inductor	1642 μH
r_L	Converter side inductor parasite resistance	0.4 Ω
C	Capacitor	10 μF
L_g	Grid side inductor	1642 μH
r_g	Grid side inductor parasite resistance	0.4 Ω
R	Damping resistance	0 Ω
k_L	Proportional gain	0.08
k_p	PR compensator proportional gain	0.5
k_r	PR compensator resonant gain	60
ξ	Damping factor	0.01

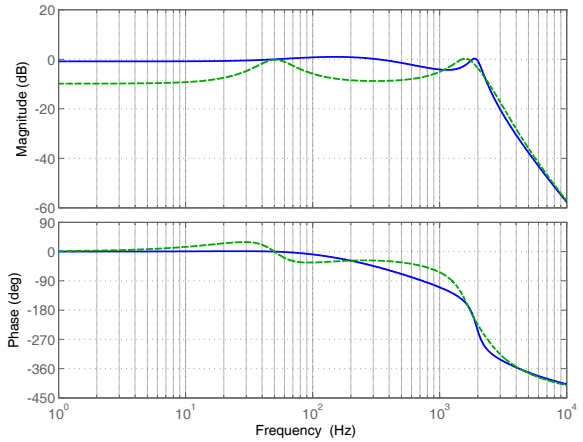


Fig. 3. Bode diagrams of closed-loop transfer functions from i_{ref} to i_g (full line: converter current feedback control scheme; dashed line: converter current plus grid current control scheme).

r_L+r_g. The transfer functions describing the converter current i_L and the grid current i_g as a function of the switch voltage v_s are given by

$$G_{i_L v_s}(s) = \frac{s^2 L_g C + sC(R+r_g)+1}{s^3 f_a + s^2 f_b + s f_c + f_d} \tag{1}$$

and

$$G_{i_g v_s}(s) = \frac{sCR+1}{s^3 f_a + s^2 f_b + s f_c + f_d} \tag{2}$$

respectively.

The closed-loop transfer function $\frac{i_g(s)}{i_{ref}(s)}$ of the converter current feedback scheme and of the converter current plus grid current feedback scheme can be obtained as

$$G_{cl1}(s) = \frac{G_c(s)k_L G_d(s) V_{dc} G_{i_g v_s}(s)}{1 + G_c(s)k_L G_d(s) V_{dc} G_{i_L v_s}(s)} \tag{3}$$

and

$$G_{cl2}(s) = \frac{G_c(s)k_L G_d(s) V_{dc} G_{i_g v_s}(s)}{1 + k_L G_d(s) V_{dc} G_{i_L v_s}(s) + G_c(s)k_L G_d(s) V_{dc} G_{i_g v_s}(s)} \tag{4}$$

respectively.

The compensators are usually represented in s-domain. In this paper, the PR compensator is used as an example, which transfer function is given by

$$G_c(s) = k_p\left(1 + k_r \frac{2\xi\omega_1 s}{s^2 + 2\xi\omega_1 s + \omega_1^2}\right). \tag{5}$$

By using the parameters in Table I and first order Padé approximation [21] for $G_d(s)$ with the maximum delay, the Bode diagrams of the closed-loop transfer functions $G_{cl1}(s)$ and $G_{cl2}(s)$ are shown in Fig. 3.

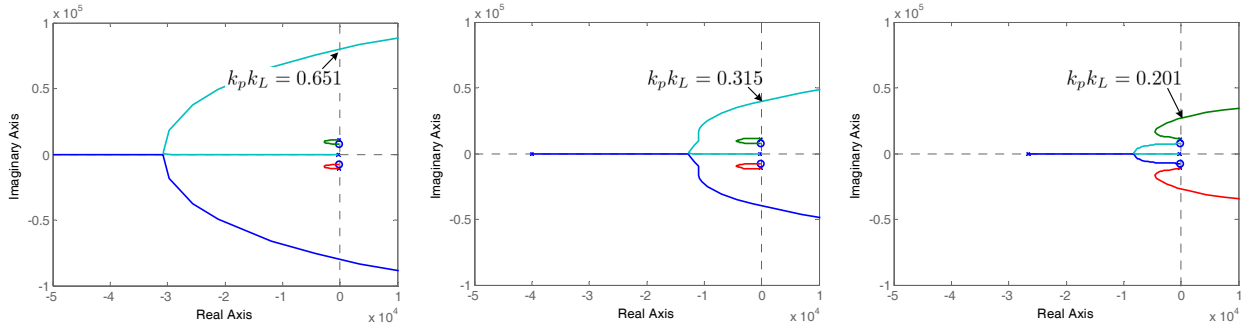
The Bode diagrams of the closed-loop transfer functions show that the converter current control scheme has an unity closed-loop gain at the fundamental frequency. If the grid frequency deviates slightly from the nominal fundamental frequency, the closed-loop gain is almost constant and the phase error is zero. When the converter current plus grid current control scheme is applied, the closed-loop gain at the fundamental frequency approaching unity is achieved by the high gain of the resonant compensator. The phase error in this control scheme is considerable when the grid frequency varies (see Fig. 3), but this error can be limited within a tolerable range [7]. The converter current control scheme achieves a faster dynamic response since it has higher gain over a wide frequency range. Both of the two control schemes are possible solutions for practical implementation. The control performance interested at the fundamental frequency and low order harmonic frequencies can be studied using s-domain models with good accuracy, but the instabilities with high oscillatory frequencies can not be precisely predicted. The root loci of the average models for the two control schemes are shown in Fig. 4 and Fig. 5. These root loci give the stability boundaries under different delay conditions. In the next section, the root loci of z-domain models will also be obtained to predict the stability boundaries. The z-domain models will be derived, which allows a full comparison between the classic models and the proposed models.

IV. SMALL-SIGNAL z-DOMAIN MODELS FOR DIGITALLY CONTROLLED GRID-CONNECTED INVERTERS

In this section, the two typical controllers described in the previous section are modeled in z-domain. For digitally controlled grid-connected inverters, the converter current control scheme is a commonly used control strategy in switching converters. The z-domain model in [16] is extended for this third-order system. The converter current plus grid current control scheme, which is used in the control of grid-connected inverters, is a typical structure with converter current control in cascaded control loops. The z-domain model for the cascaded digital control loops is derived in this paper as the modeling method in [16] is not straightforwardly applicable. Since the analysis is implemented with small-signal models, the transfer functions in this section represent the behavior when signals have small excursions to their steady-state values.

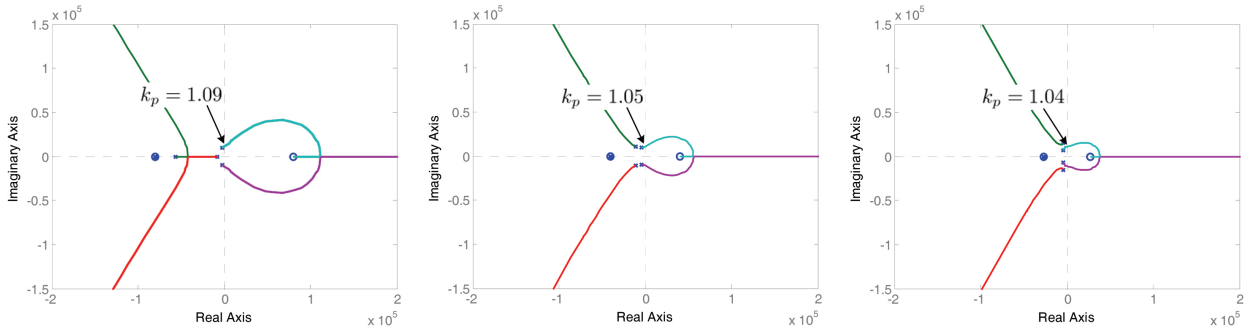
A. PWM Models with Different Delays

The processing delay of a digital controller is usually considered as one sampling cycle [2], [13]. However, in this paper



(a) (b) (c)

Fig. 4. Root loci of the converter current feedback controlled grid-connected inverters in s-plane. (a) Minimum delay. (b) Medium delay. (c) Maximum delay.



(a) (b) (c)

Fig. 5. Root loci of the converter current plus grid current feedback controlled grid-connected inverters in s-plane with $k_L = 0.08$. (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

the total delay from sampling instants to the relevant switching instants is analyzed. Disregarding the quantization effects, the uniformly-sampled bipolar switched symmetric-on-time triangle PWM including different delay effects is modeled. The sampling of signals is synchronized with the triangle carrier. The sampled quantities are converted to a duty-ratio value having the associate analog-to-digital conversion delay and computation delay. Then, the PWM compare register can update the duty-ratio value after it is calculated. There are two duty-ratio update modes in a practical digital signal processor, i.e., shadow mode and immediate load mode. In shadow mode, the duty-ratio is updated when the PWM counter reaches to zero and/or period value. In immediate load mode, the duty-ratio is updated directly once it is calculated. The time-domain diagrams from sampling input to drive output in shadow mode with double update are depicted in Fig. 6, where q^* and d^* represent the sampled quantities and the calculated duty-ratio value, respectively. u^* is the duty-ratio which is loaded into PWM compare register. τ_{d1} and τ_{d2} represent the analog-to-digital conversion delay and the computation delay, respectively. Note that if the total processing delay $\tau_{d1} + \tau_{d2}$ is larger than one sampling period, the digital controller could malfunction. Hence, two possible practical situations are studied. Fig. 6(a) shows the first situation when a fast processor is used ($\tau_{d1}+\tau_{d2} < \frac{T_s}{2}$) and the duty-ratio value is updated twice each switching period. In contrast, Fig. 6(b) shows the second situation when a slow processor is used ($\frac{T_s}{2} < \tau_{d1} + \tau_{d2} < T_s$) and the PWM has to wait until the next sampling time to update the duty-ratio value. The output of PWM is defined as $y = v_s/V_{dc}$.

Assuming x^* is the ideal quantity of u^* which is synchronized to the sample q^* without delay, the input and the output of the PWM model are x^* and y, respectively. Therefore the small-signal PWM model describing $\widehat{y}(s)$ as a function of $\widehat{x}^*(s)$ in shadow mode is derived as

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1+D)T_s}{2}} + e^{-s\frac{(3-D)T_s}{2}}) \qquad (6)$$

when $\tau_{d1} + \tau_{d2} < \frac{T_s}{2}$, and

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}}) \qquad (7)$$

when $T_s > \tau_{d1}+\tau_{d2} > \frac{T_s}{2}$, where D is the normalized average duty-ratio[1].

The delay is strongly dependent on the average duty-ratio value D in immediate load mode. The time-domain diagrams from sampling input to drive output in immediate load mode are shown in Fig. 7, where u_1^* and u_2^* represent the duty-ratio higher (lower) and lower (higher) than the critical value, respectively. The small-signal PWM model with delay in immediate load mode using a fast processor ($\tau_{d1} + \tau_{d2} < \frac{T_s}{2}$)

[1]In average models, the PWM carrier and the instantaneous duty-ratio d are ranging within $(-1, 1)$. For the convenience of the analysis, the PWM carrier and the average duty-ratio D in small-signal models are scaled into the range of $(0, 1)$. This normalization does not alter the pulse-to-continuous transfer functions of $G^*_{PWM}(s)$ in small-signal analysis.

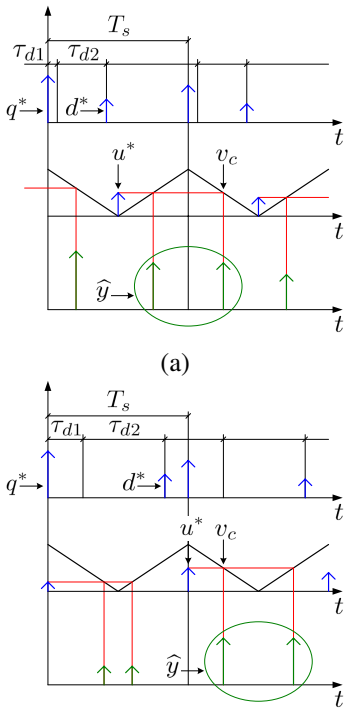


Fig. 6. Time-domain diagrams in shadow mode with double update. (a) Fast processor ($\tau_{d1}+\tau_{d2}<\frac{T_s}{2}$). (b) Slow processor ($\frac{T_s}{2}<\tau_{d1}+\tau_{d2}<T_s$).

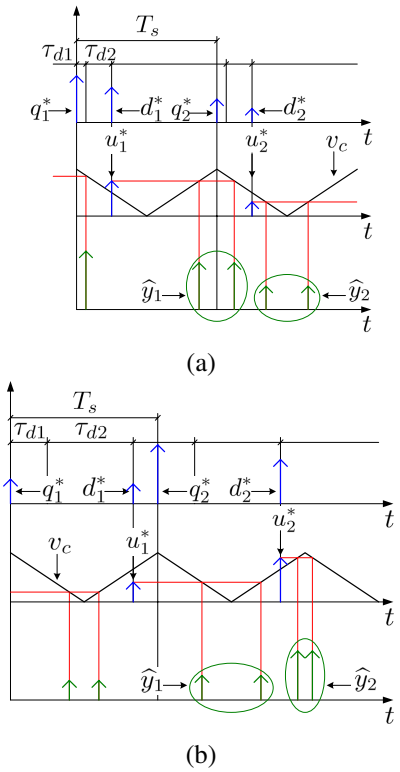


Fig. 7. Time-domain diagrams in immediate load mode. (a) Fast processor ($\tau_{d1}+\tau_{d2}<\frac{T_s}{2}$). (b) Slow processor ($\frac{T_s}{2}<\tau_{d1}+\tau_{d2}<T_s$).

is given by

$$G^*_{PWM}(s)=\frac{T_s}{2}(e^{-s\frac{(1+D)T_s}{2}}+e^{-s\frac{(3-D)T_s}{2}}) \tag{8}$$

when $\frac{T_s}{2}>\tau_{d1}+\tau_{d2}>\frac{(1-D)T_s}{2}$, and

$$G^*_{PWM}(s)=\frac{T_s}{2}(e^{-s\frac{(1-D)T_s}{2}}+e^{-s\frac{(1+D)T_s}{2}}) \tag{9}$$

when $\tau_{d1}+\tau_{d2}<\frac{(1-D)T_s}{2}$. On the other hand, the small-signal PWM model with delay in immediate load mode using a slow processor ($\frac{T_s}{2}<\tau_{d1}+\tau_{d2}<T_s$) is expressed as

$$G^*_{PWM}(s)=\frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}}+e^{-s\frac{(3+D)T_s}{2}}) \tag{10}$$

when $T_s>\tau_{d1}+\tau_{d2}>\frac{(1+D)T_s}{2}$, and

$$G^*_{PWM}(s)=\frac{T_s}{2}(e^{-s\frac{(1+D)T_s}{2}}+e^{-s\frac{(3-D)T_s}{2}}) \tag{11}$$

when $\frac{T_s}{2}<\tau_{d1}+\tau_{d2}<\frac{(1+D)T_s}{2}$.

B. z-Domain Models for Grid-Connected Inverters

As the gain of the delay e^{-sT_s} is almost unity at the fundamental frequency ($e^{-j\omega_1 T_s}\approx 1$), the continuous-time models can be used to investigate the control performance in low frequency range. However, in order to design digital controllers, discrete models are required. To simplify the analysis, the disturbances of grid voltage are removed from the models without affecting the closed-loop transfer functions. Hence, by modeling the digital processing delay τ_{d1} and τ_{d2} into the PWM, the block diagrams of the digitally controlled grid-connected inverters can be precisely represented in Fig. 8, where $\tau_\triangle$ is the total time delay of the switches drive, signals transport and measurements. Compared to the digital PWM delay, this delay is negligible.

If a classic PR compensator is used for control, the digitalized compensator is represented as $G_c(z)$ in z-domain [6]. Usually, $G_c(z)$ is derived as the discrete equivalent of $G_c(s)$ in Fig. 2 by using bilinear transform. For the PR compensator $G_c(s)$ in s-domain, its discrete equivalent $G_c(z)$ is written as

$$G_c(z)=k_p(1+k_r\frac{a_{z1}z^2+b_{z1}z+c_{z1}}{A_{z1}z^2+B_{z1}z+C_{z1}}), \tag{12}$$

with $A_{z1}=\frac{4}{T_s^2}+\frac{4\xi\omega_1}{T_s}+\omega_1^2$, $B_{z1}=-\frac{8}{T_s^2}+2\omega_1^2, C_{z1}=\frac{4}{T_s^2}-\frac{4\xi\omega_1}{T_s}+\omega_1^2$, $a_{z1}=\frac{4\xi\omega_1}{T_s}$, $b_{z1}=0$ and $c_{z1}=-\frac{4\xi\omega_1}{T_s}$.

To obtain the closed-loop discrete transfer functions of the two control structures, the feedback paths in Fig. 8 should be represented in z-domain. Hence, z-transform is used to obtain discrete transfer functions of the feedback paths which contain continuous plants followed by ideal samplers. The discrete transfer functions describing $\widehat{i}_L^*$ and $\widehat{i}_g^*$ as a function of $\widehat{x}^*$ in small signal are derived as

$$G_{i_Lx}(z)=\mathcal{Z}\{G^*_{PWM}(s)V_{dc}G_{i_Lv_s}(s)e^{-s\tau_\triangle}\} \tag{13}$$

and

$$G_{i_gx}(z)=\mathcal{Z}\{G^*_{PWM}(s)V_{dc}G_{i_gv_s}(s)e^{-s\tau_\triangle}\}, \tag{14}$$

respectively. The exact expressions of transfer functions $G_{i_Lx}(z)$ and $G_{i_gx}(z)$ can be obtained using the method extended from [16]. A detailed derivation of the z-transforms is provided in the Appendix for reference.

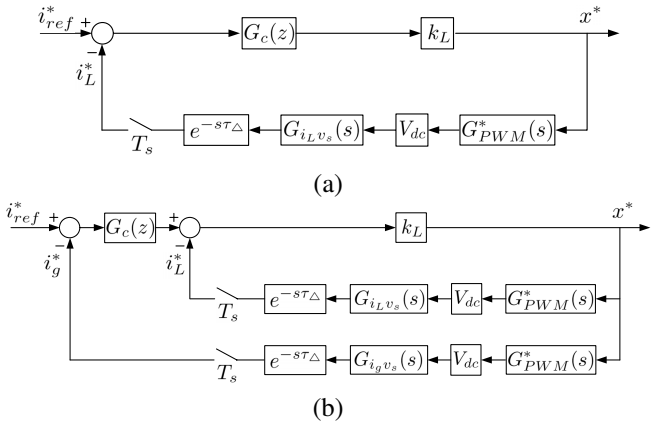


Fig. 8. Block diagrams of grid-connected inverters. (a) Converter current feedback scheme. (b) Converter current plus grid current feedback scheme.

With the discrete transfer functions of the feedback paths, the z-domain closed-loop transfer function $\frac{\widehat{i}^*_g(z)}{\widehat{i}^*_{ref}(z)}$ of the converter current feedback scheme can be obtained according to Fig. 8(a) as

$$G_{cl1}(z) = \frac{G_c(z)k_L G_{i_g x}(z)}{1 + G_c(z)k_L G_{i_L x}(z)}. \tag{15}$$

The closed-loop transfer function $\frac{\widehat{i}^*_g(z)}{\widehat{i}^*_{ref}(z)}$ in respect to Fig. 8(b) is written as

$$G_{cl2}(z) = \frac{G_c(z)k_L G_{i_g x}(z)}{1 + k_L G_{i_L x}(z) + G_c(z)k_L G_{i_g x}(z)}. \tag{16}$$

Using the same parameters listed in Table I and $D = 0.5$, the Bode diagrams of $G_{cl1}(z)$ and $G_{cl2}(z)$ are shown in Fig. 9. Comparing the results to the average models derived Bode diagrams in s-domain (see Fig. 3), it can be seen that in the low frequency range, s-domain models results and z-domain models results are almost identical. When the control performance is investigated in the low frequency range, s-domain models can be used with good accuracy. However, s-domain models fail to describe the dynamic behaviors of the digitally controlled systems apart from low frequency range. z-domain models are necessary for dynamic performance analysis. When frequency response specifications are given, controllers design can be performed according to the Bode plots of the z-domain models.

C. Stability Analysis for Internal Current Loop

As most digital control strategies involve an internal converter current control loop, the stability of the internal loop is studied first. A pure proportional feedback control in the internal loop is usually used to imitate the peak current control in naturally-sampled power converters. Even if a PR controller or a PI controller may be used in the converter current control loop, the proportional gains are of most importance for the stability issue [5]. Assuming that the voltage on the filter capacitor has a much slower dynamic behavior compared to the PWM output, the small-signal transfer function from PWM

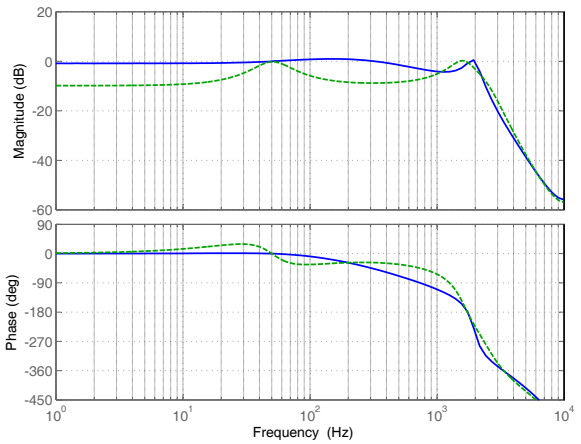


Fig. 9. Bode diagrams of closed-loop transfer functions from i^*_{ref} to i^*_g with maximum delay (full line: converter current feedback control scheme; dashed line: converter current plus grid current control scheme).

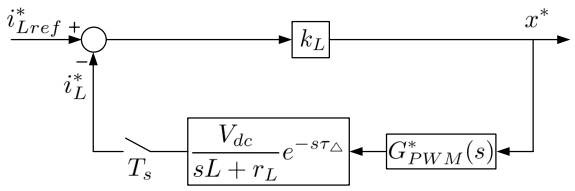


Fig. 10. Block diagram for the simplified converter current control loop of a grid-connected inverter.

output to converter current can be approximated by

$$P(s) = \frac{V_{dc}}{sL + r_L} e^{-s\tau_\triangle}. \tag{17}$$

The simplified control loop for the converter current regulator of a buck inverter is schematically represented in Fig. 10. The PWM model has three possible expressions, i.e., $G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1-D)T_s}{2}} + e^{-s\frac{(1+D)T_s}{2}})$, $G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1+D)T_s}{2}} + e^{-s\frac{(3-D)T_s}{2}})$ and $G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}})$, corresponding to the cases of minimum delay (average delay time $T_s/2$), medium delay (average delay time T_s) and maximum delay (average delay time $3T_s/2$), respectively. In the case of the minimum delay, the discrete transfer function from $\widehat{x}^*$ to $\widehat{i}^*_L$ is derived as

$$G_{i_L x}(z) = \frac{V_{dc}T_s}{2L} \frac{e^{\frac{r_L}{L}(\tau_\triangle + \frac{-1-D}{2}T_s)} + e^{\frac{r_L}{L}(\tau_\triangle + \frac{-1+D}{2}T_s)}}{z - e^{-\frac{r_L}{L}T_s}}. \tag{18}$$

Similarly, in the cases of the medium delay and the maximum delay, $G_{i_L x}(z)$ can be expressed as

$$G_{i_L x}(z) = \frac{V_{dc}T_s}{2L} \frac{e^{\frac{r_L}{L}(\tau_\triangle + \frac{-1+D}{2}T_s)}z + e^{\frac{r_L}{L}(\tau_\triangle + \frac{-1-D}{2}T_s)}}{z^2 - e^{-\frac{r_L}{L}T_s}z} \tag{19}$$

and

$$G_{i_L x}(z) = \frac{V_{dc}T_s}{2L} \frac{e^{\frac{r_L}{L}(\tau_\triangle + \frac{-1-D}{2}T_s)} + e^{\frac{r_L}{L}(\tau_\triangle + \frac{-1+D}{2}T_s)}}{z^2 - e^{-\frac{r_L}{L}T_s}z}, \tag{20}$$

respectively. As $\frac{r_L T_s}{L} \ll 1$, the exponent terms in (18)–(20) approximately equal to 1. Hence, the pole of the converter

current control loop with the minimum PWM delay can be obtained by solving the equation

$$z - 1 + \frac{k_L V_{dc} T_s}{L} = 0, \tag{21}$$

which gives the stable operating condition of

$$0 < k_L < \frac{2L}{V_{dc} T_s}. \tag{22}$$

Similarly, in the cases of medium delay and maximum delay, the characteristic equations are given by

$$z^2 + (\frac{k_L V_{dc} T_s}{2L} - 1)z + \frac{k_L V_{dc} T_s}{2L} = 0, \tag{23}$$

and

$$z^2 - z + \frac{k_L V_{dc} T_s}{L} = 0, \tag{24}$$

respectively, yielding the relevant stable operating conditions of

$$0 < k_L < \frac{2L}{V_{dc} T_s}, \tag{25}$$

and

$$0 < k_L < \frac{L}{V_{dc} T_s}, \tag{26}$$

respectively. Note that in the case of maximum delay, the stable operating range of the proportional gain is dramatically reduced, resulting in a more limited achievable bandwidth. While designing controllers, the proportional gain for the converter current loop is usually chosen to be smaller than $\frac{L}{V_{dc} T_s}$. The similar result related to the gain setting in a digital proportional current regulator can also be found in [22].

D. Discrete Root Loci Design

While designing a controller, a typical specification evaluating the robustness of a system is the gain margin in root locus. For digitally controlled grid-connected inverters, more precise stability boundaries can be obtained from discrete root loci. Based on root loci, the dynamic performances in time-domain (rise time, settling time and percent overshoot, etc.) can be evaluated according to the conjugate pole pairs in z-plane.

Using the same parameters listed in Table I and $D = 0.5$ (or any other values for D between 0 and 1), the root loci[2] of the converter current feedback controlled inverter are shown in Fig. 11. The real poles of the converter current feedback scheme with minimum and medium delay will move across the unit circle when the total proportional gain equals to 0.324 and 0.306 (see Fig. 11(a) and (b)), respectively. When the maximum delay is employed, the two conjugate poles will move across the unit circle when the proportional gain equals to 0.139 (see Fig. 11(c)). Even when the minimum delay is involved, a gain higher than 0.167 may result in a ringing dynamic response. Note that $\frac{2L}{V_{dc} T_s} = 0.328$. As is illustrated in the previous subsection, the internal current loop proportional gain is usually chosen to be much smaller than $\frac{L}{V_{dc} T_s}$. When $k_L = 0.08$ and $k_p = 0.5$ with the maximum delay, it can be seen from Fig. 11(c) that the closed-loop system still has a gain margin of 3.46. The longest settling time and the highest overshoot in percentage of the conjugate pole pairs are 3.1 ms and 68%, respectively.

The root loci of converter current plus grid current feedback controlled inverter are shown in Fig. 12. The conjugate poles in the cases of minimum delay, medium delay and maximum delay will move across the unit circle when the proportional gain k_p equals to 1.04, 1.04 and 1.02, respectively. These results are strongly related to the damping of the LCL resonance, for which an analytical expression is difficult to obtain. However, the PWM delay can reduce the stable operating range dramatically when the damping resistance increases. In this paper where the maximum PWM delay is achieved in experiment, the proportional gain is chosen as $k_p = 0.5$. Hence, a stable gain margin of 2 is guaranteed[3].

V. Discrete State-Space Models for Grid-Connected Inverters

To compare with the proposed z-domain models, the discrete state-space models are also provided. These models can precisely represent the dynamic behaviors of the systems, but they are not commonly used for the following reasons [23]. The first reason is that a discrete state-space model depends on the type of modulator. If the modulator is changed, remodeling procedure is required. The second reason is that the state transition matrix computation brings relative complex work, and linearization of exponential matrices sometimes is necessary and inaccurate. The last reason is that the size of the state-space matrices will significantly increase if the controller is complicated or the delay is long. Hence, this section provides an example of using discrete state-space models to predict the maximum proportional gains of the controllers.

A. Switching States with Delays

The switching states are dependent of duty-ratios. For example, in the nth sampling period, the proportional controllers give the discrete duty-ratios d_n as

$$d_n = k_p k_L (i_{ref}(n) - i_L(n)) \tag{27}$$

for converter current control scheme and

$$d_n = k_L (k_p (i_{ref}(n) - i_g(n)) - i_L(n)) \tag{28}$$

for converter current plus grid current control scheme. Note that $-1 < d_n < 1$. As we prefer to use the normalized duty-ratio $0 < D_n < 1$, the normalized discrete duty-ratios can be represented by

$$D_n = \frac{k_p k_L + 1}{2} (i_{ref}(n) - i_L(n)) \tag{29}$$

[2]The root loci are derived when using pure proportional compensators. However, under the condition of $k_r \ll \frac{1}{\xi \omega_1 T_s}$, the root loci in z-plane do not differ even if additional resonant compensators are used. The only difference introduced by the resonant compensators is that a pair of conjugate poles moving within the unit circle appears in the root loci.

[3]Though the discrete closed-loop transfer functions are average duty-ratio D dependent, the root loci are derived with duty-ratio fixed as $D = 0.5$. These results have very little difference when D is changing within $(0, 1)$. This conclusion is only valid when the symmetric triangle carriers are used for PWM generation.

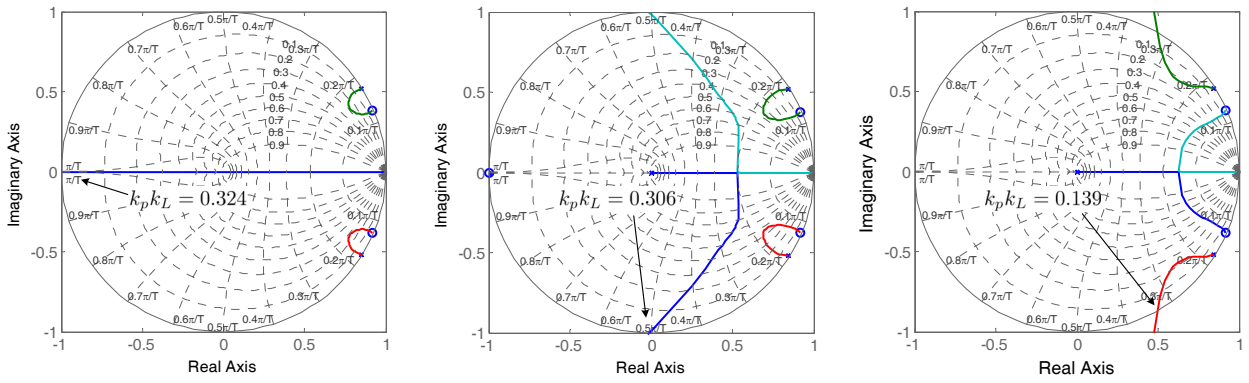


Fig. 11. Root loci of the converter current feedback controlled grid-connected inverters in z-plane. (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

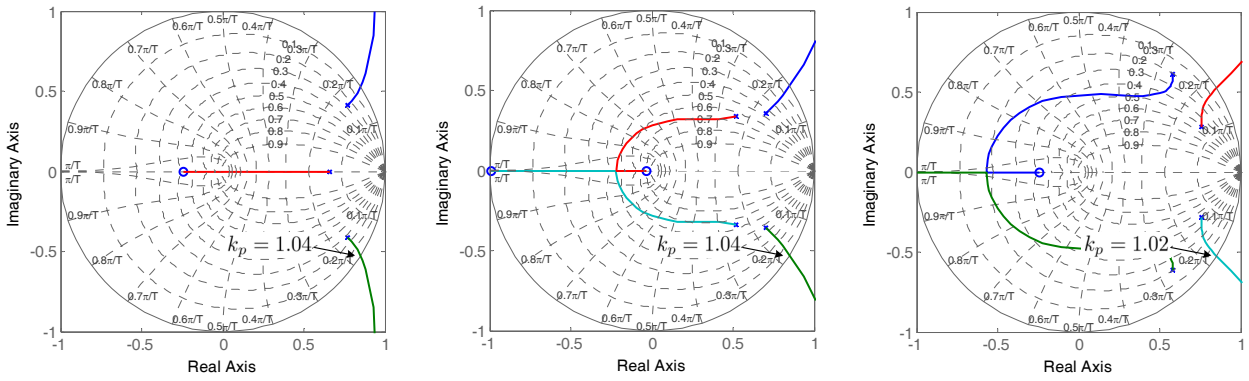


Fig. 12. Root loci of the converter current plus grid current feedback controlled grid-connected inverters in z-plane with $k_L = 0.08$. (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

for converter current control scheme and

$$D_n = \frac{k_L + 1}{2}(k_p(i_{ref}(n) - i_g(n)) - i_L(n)) \qquad (30)$$

for converter current plus grid current control scheme.

There are three switching states in each sampling period for bipolar PWM. Fig. 13 shows the time-domain waveforms of the switching states with medium delay. In the first and last states, the switch voltage is given by $v_s = -V_{dc}$. In the second state, the switch voltage is represented as $v_s = V_{dc}$. To simplify the expression, the time intervals of the three states are represented by t_{1n}, t_{2n} and t_{3n} instead of $t_1(n)$, $t_2(n)$ and $t_3(n)$, respectively. According to Fig. 13, one can obtain that $t_{1n} = (1 - D_{n-1})T_s/2$, $t_{2n} = (D_{n-1} + D_n)T_s/2$ and $t_{3n} = (1-D_n)T_s/2$ with medium delay applied. Moreover, for minimum delay and maximum delay, the expressions of t_{1n}, t_{2n} and t_{3n} can be directly derived. For minimum delay, one can obtain that $t_{1n} = (1 - D_n)T_s/2$, $t_{2n} = D_nT_s$ and $t_{3n} = (1 - D_n)T_s/2$; For maximum delay, $t_{1n} = (1 - D_{n-1})T_s/2$, $t_{2n} = D_{n-1}T_s$ and $t_{3n} = (1 - D_{n-1})T_s/2$.

B. Discrete Maps for Grid-Connected Inverters

To obtain the discrete maps of the grid-connected inverter, the state vector x is defined as $x = [i_L \ i_g \ v_C]^{\mathrm{T}}$ [24]. No matter what switching state the converter is in, the state-space model can be described as

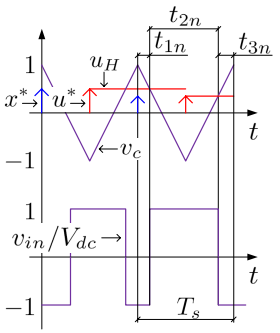


Fig. 13. Switching states of the bipolar PWM with medium delay.

$$\dot{x} = Ax + e \qquad (31)$$

with $A = \begin{bmatrix} -\frac{r_L+R}{L} & \frac{R}{L} & -\frac{1}{L} \\ \frac{R}{L_g} & -\frac{r_g+R}{L_g} & \frac{1}{L_g} \\ \frac{1}{C} & -\frac{1}{C} & 0 \end{bmatrix}$ and $e = \begin{bmatrix} \frac{v_s}{L} \\ -\frac{v_g}{L_g} \\ 0 \end{bmatrix}$.

If $nT_s < t < nT_s + t_{1n}$ and $(n+1)T_s - t_{3n} < t < (n+1)T_s$, $e = e_1 = [-V_{dc}/L \ \ -v_g/L_g \ 0]^{\mathrm{T}}$. If $nT_s + t_{1n} < t < (n + 1)T_s - t_{3n}$, $e = e_2 = [V_{dc}/L \ \ -v_g/L_g \ 0]^{\mathrm{T}}$. The state-space vector can be solved using the linearization method in [25],

[26], which is written as

$$x_{n+1} = e^{AT_s}x_n + (e^{AT_s} - e^{A(t_{2n}+t_{3n})} + e^{At_{3n}} - I)A^{-1}e_1 + (e^{A(t_{2n}+t_{3n})} - e^{At_{3n}})A^{-1}e_2 \quad (32)$$

with x_n and x_{n+1} representing $x(nT_s)$ and $x((n+1)T_s)$, respectively. Using first order linearization, (32) can be finally approximated by

$$x_{n+1} = \Phi x_n + \Gamma_1 e_1 + \Gamma_2 e_2. \quad (33)$$

with $\Phi = e^{AT_s}$, $\Gamma_1 = T_s - t_{2n}$ and $\Gamma_2 = t_{2n}$.

C. Jacobian Matrix with Delays

The small-signal stability of a discrete model can be predicted by the eigenvalues of the Jacobian matrix. The Jacobian matrix of (33) with minimum delay can be derived without augmentation of the matrices. However, in the cases of medium delay and maximum delay, augmentation of the matrices are required as t_{2n} is a function of D_{n-1}. Therefore, the derivation of the Jacobian matrix becomes quite complex. So far, discrete state-space modeling of power converters with more than one cycle delay can hardly be found in the existing literature. Here we provide an example of derivation when medium delay is involved, where t_{2n} is a function of both D_{n-1} and D_n.

Define $y_n = x_{n+1}$, (33) can be re-written as

$$\begin{bmatrix} y_n \\ x_n \end{bmatrix} = \begin{bmatrix} \Phi & \mathbf{0} \\ \mathbf{I} & \mathbf{0} \end{bmatrix} \begin{bmatrix} y_{n-1} \\ x_{n-1} \end{bmatrix} + \Gamma_1 \begin{bmatrix} e_1 \\ \mathbf{0}_v \end{bmatrix} + \Gamma_2 \begin{bmatrix} e_2 \\ \mathbf{0}_v \end{bmatrix} \quad (34)$$

with $\mathbf{I} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$, $\mathbf{0} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$ and $\mathbf{0}_v = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$. The Jacobian matrix for the inverter with medium delay can be derived by

$$\begin{aligned} J &= \begin{bmatrix} \Phi & \mathbf{0} \\ \mathbf{I} & \mathbf{0} \end{bmatrix} + \begin{bmatrix} e_1 \\ \mathbf{0}_v \end{bmatrix} \frac{\partial \Gamma_1}{\partial \begin{bmatrix} y_{n-1} \\ x_{n-1} \end{bmatrix}} + \begin{bmatrix} e_2 \\ \mathbf{0}_v \end{bmatrix} \frac{\partial \Gamma_2}{\partial \begin{bmatrix} y_{n-1} \\ x_{n-1} \end{bmatrix}} \\ &= \begin{bmatrix} \Phi & \mathbf{0} \\ \mathbf{I} & \mathbf{0} \end{bmatrix} + \begin{bmatrix} e_1 \\ \mathbf{0}_v \end{bmatrix} \left(\frac{\partial \Gamma_1}{\partial D_n} \frac{\partial D_n}{\partial \begin{bmatrix} y_{n-1} \\ x_{n-1} \end{bmatrix}} + \frac{\partial \Gamma_1}{\partial D_{n-1}} \frac{\partial D_{n-1}}{\partial \begin{bmatrix} y_{n-1} \\ x_{n-1} \end{bmatrix}} \right) \\ &+ \begin{bmatrix} e_2 \\ \mathbf{0}_v \end{bmatrix} \left(\frac{\partial \Gamma_2}{\partial D_n} \frac{\partial D_n}{\partial \begin{bmatrix} y_{n-1} \\ x_{n-1} \end{bmatrix}} + \frac{\partial \Gamma_2}{\partial D_{n-1}} \frac{\partial D_{n-1}}{\partial \begin{bmatrix} y_{n-1} \\ x_{n-1} \end{bmatrix}} \right). \end{aligned} \quad (35)$$

For the converter current control scheme, one can obtain that $\partial D_n / \partial [y_{n-1}^{\mathrm{T}}, x_{n-1}^{\mathrm{T}}]^{\mathrm{T}} = [-k_p k_L/2,\ 0,\ 0,\ 0,\ 0,\ 0]$ and $\partial D_{n-1} / \partial [y_{n-1}^{\mathrm{T}}, x_{n-1}^{\mathrm{T}}]^{\mathrm{T}} = [0,\ 0,\ 0, -k_p k_L/2,\ 0,\ 0]$; For the converter current plus grid current control scheme, $\partial D_n / \partial [y_{n-1}^{\mathrm{T}}, x_{n-1}^{\mathrm{T}}]^{\mathrm{T}} = [-k_L/2, -k_p k_L/2,\ 0,\ 0,\ 0,\ 0]$ and $\partial D_{n-1} / \partial [y_{n-1}^{\mathrm{T}}, x_{n-1}^{\mathrm{T}}]^{\mathrm{T}} = [0,\ 0,\ 0, -k_L/2, -k_p k_L/2,\ 0]$.

With the parameters in Table I, for the converter current control scheme, it can be calculated that the eigenvalues of J will move across the unit circle when $k_p k_L = 0.300$ (eigenvalues of $[0,\ 0,\ 0.8467 + 0.3455i,\ 0.8467 - 0.3455i,\ 0.0361 + 0.9996i,\ 0.0361 - 0.9996i]^{\mathrm{T}}$). On the other hand, for the converter current plus grid current control scheme with $k_L = 0.08$, it can be calculated that the eigenvalues will move across the unit circle when $k_p = 1.05$ (eigenvalues of $[0,\ 0.8511 + 0.5252i,\ 0.8511 - 0.5252i,\ 0,\ 0.3671 + 0.3271i,\ 0.3671 - 0.3271i]^{\mathrm{T}}$). Comparing the eigenvalues on the gain boundaries to the roots on the gain boundaries of Fig. 11(b) and Fig. 12(b), it can be conclude that the results of z-domain models are almost the same as the results of discrete state-space models. This is because of the natural that the two modeling methods are the same in theory.

Moreover, using the similar method, the gain boundaries of the discrete space state models with minimum delay and with maximum delay can be obtained. Due to space limitations, the derivation is not shown here. However, with minimum delay, the calculated gain boundaries for the converter current control scheme and the converter current plus grid current control scheme are $k_p k_L = 0.326$ and $k_p = 1.07$, respectively. With maximum delay, the calculated gain boundaries for the converter current control scheme and the converter current plus grid current control scheme are $k_p k_L = 0.131$ and $k_p = 1.04$, respectively.

VI. Models Validation

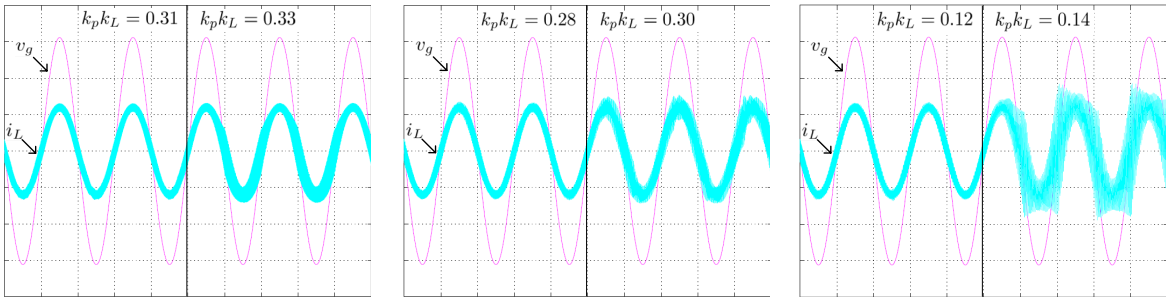
A. Simulation Results

For safety issue reasons, computer simulations were used to verify the capability of the small-signal z-domain models in predicting stability boundaries. The s-domain models predictions are also used for comparison to show the advantage of proposed models. The predicted maximum proportional gains of the two control schemes with different delay effects are summarized from Fig. 4, Fig. 5, Fig. 11 and Fig. 12. The maximum proportional gains predicted by discrete state-space models are also compared. These predicted results are shown in Table II. For the converter current feedback control scheme, the actual proportional gain is equal to $k_p k_L$. For the converter current plus grid current feedback control scheme, the proportional gain k_p in the grid current control loop is investigated with $k_L = 0.08$.

Using the parameters in Table I, Fig. 14 shows the simulation results of the converter current controlled grid-connected inverter when the actual proportional gain steps over the stability boundaries. Under the condition of the minimum delay, the root locus in Fig. 11(a) shows that a real pole will move out of the unit circle when the proportional gain increases. As $\frac{\pi}{T_s}$ represents half of the sampling frequency, the oscillation frequency is $\frac{1}{2T_s}$ and period-2 bifurcation may appear. This phenomenon is named as fast-scale instability [27]. After the bifurcated converter current passes through the CL filter, the bifurcation on the grid current becomes not obvious. To give a clear view of the bifurcation, the simulated converter current i_L is shown in Fig. 14(a), where period-2 bifurcation can be seen after $k_p k_L$ steps higher than 0.32. In contrast, with the medium delay and the maximum delay (see Fig. 11(b) and (c)), conjugate pole pairs will move out of the unit circle when $k_p k_L$ is higher than 0.29 and 0.13, respectively. Hence, oscillations with lower frequencies may occur. The root loci move across the unit circle by angular frequencies of $\frac{\pi}{2T_s}$ and $\frac{\pi}{3T_s}$ for medium delay and

TABLE II
PREDICTED MAXIMUM PROPORTIONAL GAINS

	Control loop	Minimum delay	Medium delay	Maximum delay
Average models predictions	Converter current loop	0.651	0.315	0.201
	Grid current loop	1.09	1.05	1.04
Proposed models predictions	Converter current loop	0.324	0.306	0.139
	Grid current loop	1.04	1.04	1.02
Discrete models predictions	Converter current loop	0.326	0.300	0.131
	Grid current loop	1.07	1.05	1.04
Simulation results	Converter current loop	0.32	0.29	0.13
	Grid current loop	1.0	1.0	1.0



(a) (b) (c)

Fig. 14. Simulated waveforms of the converter current controlled grid-connected inverter (X–axis: Time, 5 ms/div; Y–axis: Magnitude of converter current: 5 A/div; and grid voltage: 50 V/div). (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

the maximum delay, respectively. Hence, period-4 and period-6 bifurcations may occur, respectively. The relevant simulation results obviously show that the converter current becomes unstable with lower oscillatory frequencies after the steps (see Fig. 14(b) and (c)). Comparing the simulated stability boundaries to the predicted boundaries of the average model, the proposed model and the discrete state-space model, it can be seen in Table II that the accuracy of the proposed model is much better than that of the average model. Both the proposed model and the discrete state-space model for the converter current control loop are capable of predicting the fast-scale instabilities while the classic average model is not. The z-domain model and the discrete state-space model are naturally equivalent. However, the z-domain modeling is more convenient and practical for frequency domain design than the discrete state-space modeling.

Fig. 15 shows the simulation results of the converter current plus grid current controlled grid-connected inverter when the proportional gain of the external control loop steps over the stability boundaries. It can be clearly observed that the grid current i_g becomes unstable after each step. Slow-scale instabilities appear on the grid current. The oscillation frequencies observed in the simulation are around 1.7 kHz, which are very low compared to the sampling frequency of 20 kHz. All the conjugated pole pairs in the s-plane root loci (see Fig. 5) and z-plane root loci (see Fig. 12) move across the stability boundary with oscillation frequencies around 1.77 kHz. It can be seen from Table II that the simulation results are in good agreement with all the stability predictions for the grid current control loop. The reason is that the slow-scale instabilities in the external control loop are mainly caused by the LCL resonance. When the damping resistance increases, the difference between s-domain results and z-domain results becomes bigger, since the sample and hold effect will play a more important role. However, the high accuracy of z-plane root loci predictions for the two control schemes verified in Table II shows that the proposed models are capable of evaluating robustness of controllers.

B. Experimental Results

To show the capability of predicting time-domain waveforms, both the classic s-domain models and small-signal z-domain models predicted steady-state responses and transient responses were compared to the relevant experimental results. The s-domain models and the z-domain models with the maximum PWM delay and the parameters listed in Table I are used for predictions. Although the z-domain models are dependent of the average duty-ratio D, the predictions are retrieved with a time-variant D.

According to the proposed modeling methods, the single loop controller and the cascaded loops controller were experimentally implemented on an 110 V grid connected inverter, as is shown in Fig. 16. A phase-locked loop (PLL) is used for the grid synchronization. The current reference is generated from the PLL. The experimental grid current and grid voltage are retrieved from the shunt and the left side of the transformer in Fig. 16, respectively. To compare the experimental results with the models predicted results, the same compensators and the same parameters listed in Table I are used in the tests. The digital controller is performed in TMS320F28335, a floating-point DSP. The ADCs are with a resolution of 12 bits. The H bridge of the inverter is implemented by Mitsubishi Intelligent Power Modules (IPM). The inverter is bipolar switched with the deadband time of 2.67 μs. The uniformly-sampled symmetric-on-time triangle PWM is applied. The

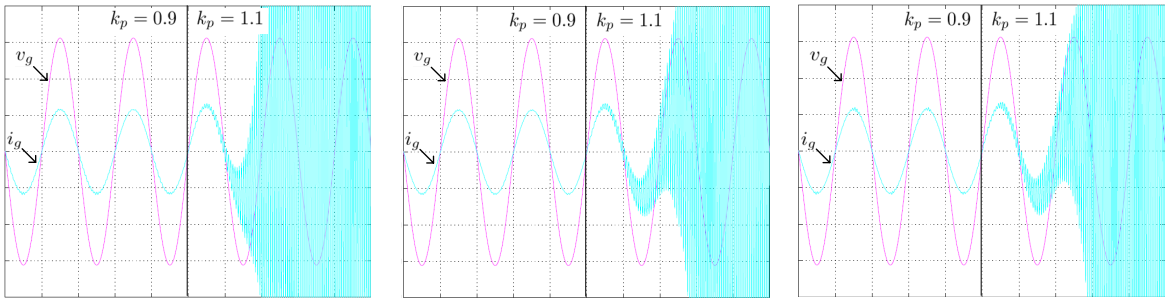


Fig. 15. Simulated waveforms of the converter current plus grid current controlled grid-connected inverter (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current: 5 A/div; and grid voltage: 50 V/div). (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

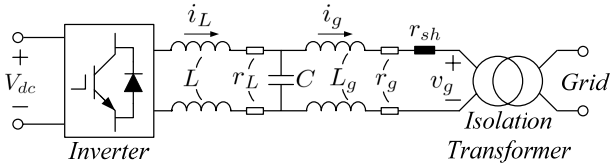


Fig. 16. Experimental grid connected inverter.

duty-ratio value is loaded to the PWM compare register at each sampling instant, therefore the processing delay is one switching period and the maximum delay is achieved.

The steady-state responses were performed using a sinusoidal current reference with an RMS value of 4.6 A. The classic average models, z-domain models and experimental tests retrieved waveforms of the converter current controlled and converter current plus grid current controlled grid-connected inverters are shown in Fig. 17 and Fig. 18, respectively. The classic average model and the z-domain model retrieved steady-state responses of the converter current controlled grid-connected inverter are almost identical (see Fig. 17(a) and Fig. 17(b)). The predicted current amplitudes (I_g) and phase angles ($\Delta\phi$) are 4.6 A and 1.1°, respectively. However, it is shown in Fig. 17(c) that under the practical condition of a weak grid, a larger phase lag exists in the current with a phase angle of $\Delta\phi = 8.1^\circ$. When the grid voltage contains considerable harmonic components (THD $\approx 2.0\%$), the grid current THD is about 2.6%. The performance of this control scheme is severely affected by the quality of the grid voltage.

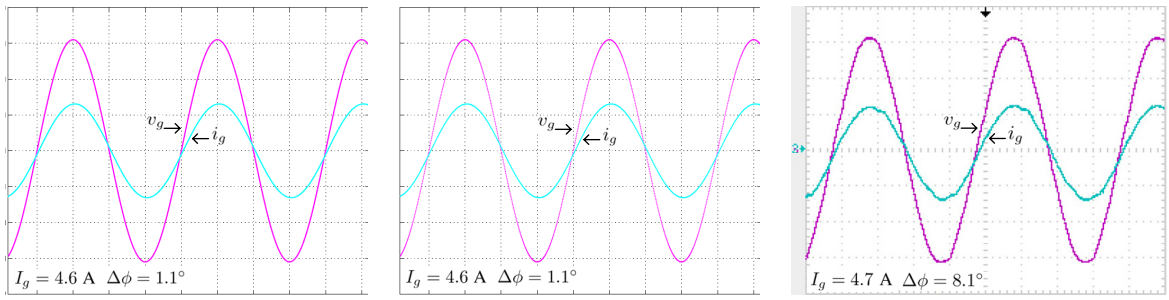
The steady-state responses of the converter current plus grid current controlled grid-connected inverter show that the predictions of the classic average model and the z-domain model are almost the same (see Fig. 18(a) and Fig. 18(b)). The current amplitudes and phase angles in models predictions are 4.5 A and 0.23°, respectively. However, in the experimental results (see Fig. 18(c)), the current amplitude is 4.6 A and the phase angle is 5.4°. The current distortion remains low (THD $\approx 2.1\%$) in this control scheme.

Since the converter current control scheme achieves a higher closed-loop gain, the amplitude of grid current in Fig. 17 is higher than that in Fig. 18. It can be seen from Fig. 17 that when the converter current feedback scheme is used, the grid current has a larger lagging phase error. In contrast, when the converter current plus grid current feedback scheme is used, a smaller grid current phase error is achieved (see Fig. 18). In the environment when a distorted grid voltage appears, exact predictions for experimental waveforms are not guaranteed. However, it is concluded that both the classic average models and z-domain models can be used with good accuracy.

Fig. 19 shows the transient response of the converter current controlled grid-connected inverter when the reference current steps at its peak. The grid current achieves steady-state operation within two line cycles after the step. The dynamic response time of this control scheme is short. The average model and z-domain model predicted waveforms after the step are slightly different. The predicted results are similar to the experimental results. However, in this control scheme, the grid voltage adds significant harmonic components to the experimental data. When the amplitude of the grid current is small, this disturbance from the grid is more obvious. To a first approximation, the agreement between predicted results and experimental result is good.

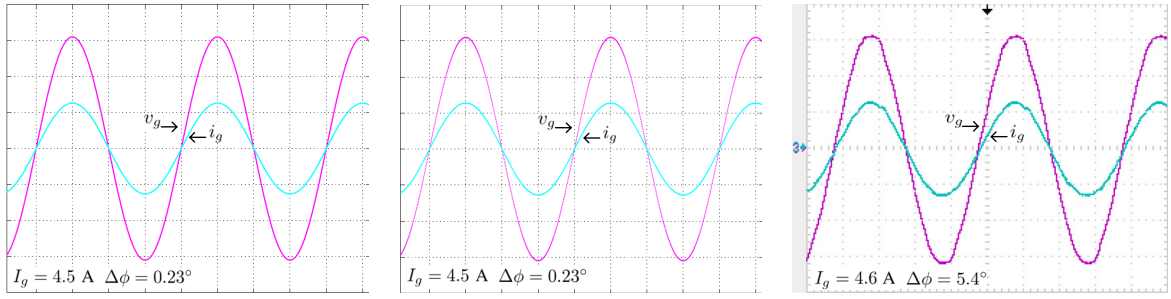
The transient response of the converter current plus grid current controlled grid-connected inverter is shown in Fig. 20, where the disturbance from the grid in this control scheme is quite small. Hence, the z-domain model predicted transition (see Fig. 20(b)) is more similar to the experimentally retrieved result (see Fig. 20(c)). After the step, the grid current achieves steady-state in more line cycles. During this time, both of the average model and the z-domain model predicted results are very close to the experimental result. A longer transition exists in the converter current plus grid current control scheme since the closed-loop gain on the Bode plot is always lower than that of the converter current control scheme. For the cascaded control scheme, it is verified that the z-domain model is capable of predicting the transient response with good accuracy. The difference between the predicted waveforms of the s-domain model and that of the z-domain model is not significant. This is because the difference of the two models is mainly focused on the high frequency range. When the high frequency signals pass through an LCL filter and appear on the grid side, it may be even smaller than the high frequency signals from the disturbance of the grid. Therefore, it is reasonable that the z-domain models do not show significant advantage in predicting the experimental waveforms.

An obvious disadvantage existing in the z-domain models



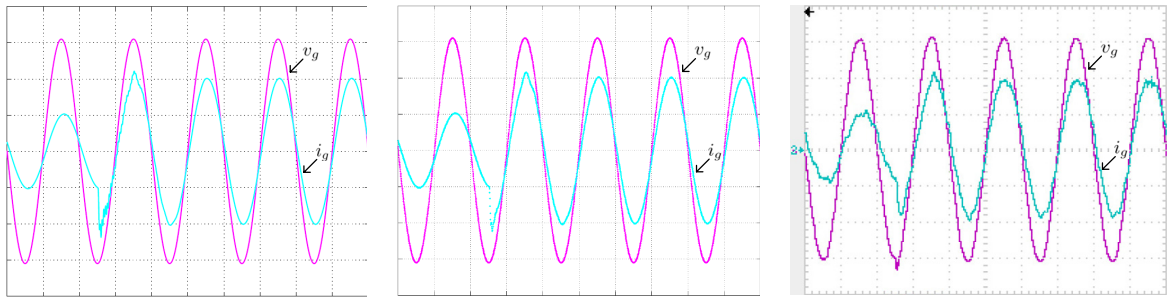
(a) (b) (c)

Fig. 17. Steady-state response of the converter current controlled grid-connected inverter (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current: 5 A/div; and grid voltage: 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Experimental result.



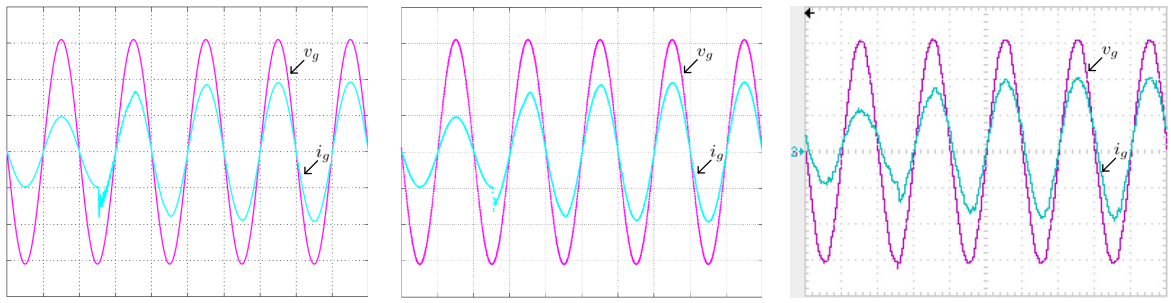
(a) (b) (c)

Fig. 18. Steady-state response of the converter current plus grid current controlled grid-connected inverter (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current: 5 A/div; and grid voltage: 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Experimental result.



(a) (b) (c)

Fig. 19. Transient response of the converter current controlled grid-connected inverter with a step in the commanded current peak value from 2 A to 4 A (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current: 2 A/div; and grid voltage: 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Experimental result.



(a) (b) (c)

Fig. 20. Transient response of the converter current plus grid current controlled grid-connected inverter with a step in the commanded current peak value from 2 A to 4 A (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current: 2 A/div; and grid voltage: 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Experimental result.

is the duty-ratio dependent instinct. When triangle carriers are used, the PWM delay is approximately equivalent to an averaged delay with half switching period [28]. The error of this approximation is negligible when the duty-ratio varies. This error is only unacceptable if sawtooth carriers are used. However, in sampled-data systems with ac references, sawtooth PWMs which cannot guarantee an average current sampling are rarely used.

VII. Conclusion

In this paper, digitally controlled grid-connected inverters with converter current control scheme and converter current plus grid current control scheme have been studied. The classic average models for the two control schemes have been described in s-domain. In contrast, new small-signal z-domain models have been derived with precisely modeled delay effects. This permits a direct design of the digital compensators in z-domain. The discrete state-space models are also provided. The gain boundaries obtained from root loci of both average models and proposed models and the gain boundary obtained from discrete state-space models have been compared with the simulation results, which demonstrates that the proposed models are more accurate than the average models in predicting fast- and slow-scale instabilities. Furthermore, the proposed models are capable of predicting the steady-state and dynamic responses of the control variables at the true sampling instants. The experimental prototype has been implemented according to the proposed models. The comparison between the predictions of the models and the experimental results with the two control schemes confirms the validity of the proposed models.

Appendix
Derivations of the z-Domain Transfer Functions

Let $f_Q = \sqrt{(2f_b^3 - 9f_af_bf_c + 27f_a^2f_d)^2 - 4(f_b^2 - 3f_af_c)^3}$, $f_C = \sqrt[3]{\frac{1}{2}(f_Q + 2f_b^3 - 9f_af_bf_c + 27f_a^2f_d)}$, $a = \frac{f_b}{3f_a} + \frac{f_C}{3f_a} + \frac{(f_b^2 - 3f_af_c)}{3f_af_C}$, $b = \frac{f_b}{3f_a} - \frac{(1+j\sqrt{3})f_C}{6f_a} - \frac{(1-j\sqrt{3})(f_b^2-3f_af_c)}{6f_af_C}$ and $c = \frac{f_b}{3f_a} - \frac{(1-j\sqrt{3})f_C}{6f_a} - \frac{(1+j\sqrt{3})(f_b^2-3f_af_c)}{6f_af_C}$. The transfer function $G_{i_Lv_s}(s)$ can be split to

$$G_{i_Lv_s}(s) = \frac{A_L}{s+a} + \frac{B_L}{s+b} + \frac{C_L}{s+c} \tag{36}$$

with $A_L = \frac{a^2L_gC - aC(R+r_g)+1}{(a-b)(a-c)LL_gC}$, $B_L = \frac{b^2L_gC - bC(R+r_g)+1}{(b-a)(b-c)LL_gC}$ and $C_L = \frac{c^2L_gC - cC(R+r_g)+1}{(c-b)(c-a)LL_gC}$. For the PWM model with maximum delay, i.e., $G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}})$, the z-transform of $G_{i_Lx}(z)$ can be deduced using the method as

$$\begin{aligned} &Z\{G^*_{PWM}(s)V_{dc}\frac{A_L}{s+a}e^{-s\tau_\triangle}\} \\ &= \frac{V_{dc}T_sA_L}{2}\frac{e^{a(\tau_\triangle - \frac{1+D}{2}T_s)} + e^{a(\tau_\triangle - \frac{1-D}{2}T_s)}}{z^2 - e^{-aT_s}z}. \end{aligned} \tag{37}$$

Defining $e_a = \frac{1}{2}(e^{a(\tau_\triangle - \frac{1+D}{2}T_s)} + e^{a(\tau_\triangle - \frac{1-D}{2}T_s)})$, $e_b = \frac{1}{2}(e^{b(\tau_\triangle - \frac{1+D}{2}T_s)} + e^{b(\tau_\triangle - \frac{1-D}{2}T_s)})$, $e_c = \frac{1}{2}(e^{c(\tau_\triangle - \frac{1+D}{2}T_s)} + e^{c(\tau_\triangle - \frac{1-D}{2}T_s)})$, $D_2 = -e^{-aT_s} - e^{-bT_s} - e^{-cT_s}$, $D_1 = e^{-(a+b)T_s} + e^{-(b+c)T_s} + e^{-(a+c)T_s}$ and $D_0 = -e^{-(a+b+c)T_s}$, the discrete transfer function $G_{i_Lx}(z)$ can be written as

$$G_{i_Lx}(z) = \frac{N_{L2}z^2 + N_{L1}z + N_{L0}}{z^4 + D_2z^3 + D_1z^2 + D_0z} \tag{38}$$

with $N_{L2} = V_{dc}T_s(A_Le_a + B_Le_b + C_Le_c)$, $N_{L1} = -V_{dc}T_s(A_Le_a(e^{-bT_s} + e^{-cT_s}) + B_Le_b(e^{-aT_s} + e^{-cT_s}) + C_Le_c(e^{-aT_s} + e^{-bT_s}))$ and $N_{L0} = V_{dc}T_s(A_Le_ae^{-(b+c)T_s} + B_Le_be^{-(a+c)T_s} + C_Le_ce^{-(a+b)T_s})$.

Similarly, the transfer function $G_{i_gv_s}(s)$ can be split to

$$G_{i_gv_s}(s) = \frac{A_g}{s+a} + \frac{B_g}{s+b} + \frac{C_g}{s+c} \tag{39}$$

with $A_g = \frac{1-aCR}{(a-b)(a-c)LL_gC}$, $B_g = \frac{1-bCR}{(b-a)(b-c)LL_gC}$ and $C_g = \frac{1-cCR}{(c-b)(c-a)LL_gC}$. Then the discrete transfer function $G_{i_gx}(z)$ can be written as

$$G_{i_gx}(z) = \frac{N_{g2}z^2 + N_{g1}z + N_{g0}}{z^4 + D_2z^3 + D_1z^2 + D_0z} \tag{40}$$

with $N_{g2} = V_{dc}T_s(A_ge_a + B_ge_b + C_ge_c)$, $N_{g1} = -V_{dc}T_s(A_ge_a(e^{-bT_s} + e^{-cT_s}) + B_ge_b(e^{-aT_s} + e^{-cT_s}) + C_ge_c(e^{-aT_s} + e^{-bT_s}))$ and $N_{g0} = V_{dc}T_s(A_ge_ae^{-(b+c)T_s} + B_ge_be^{-(a+c)T_s} + C_ge_ce^{-(a+b)T_s})$.

References

[1] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1281–1291, Sept./Oct. 2005.

[2] J. Dannehl, C. Wessels, and F. W. Fuchs, "Limitations of voltage-oriented PI current control of grid-connected PWM rectifiers with LCL filters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 380–388, Feb. 2009.

[3] A. A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1205–1217, Apr. 2011.

[4] L. Asiminoaei, R. Teodorescu, F. Blaabjerg, and U. Borup, "Implementation and test of an online embedded grid impedance estimation technique for PV inverters," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 4, pp. 1136–1144, Aug. 2005.

[5] E. Twining and D. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Transactions on Power Electronics,*, vol. 18, no. 3, pp. 888–895, May 2003.

[6] M. Castilla, J. Miret, J. Matas, L. G. de Vicuna, and J. M. Guerrero, "Linear current control scheme with series resonant harmonic compensator for single-phase grid-connected photovoltaic inverters," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp. 2724–2733, Jul. 2008.

[7] ——, "Control design guidelines for single-phase grid-connected photovoltaic inverters with damped resonant harmonic compensators," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 11, pp. 4492–4501, Nov. 2009.

[8] M. Castilla, J. Miret, A. Camacho, J. Matas, and L. de Vicuna, "Reduction of current harmonic distortion in three-phase grid-connected photovoltaic inverters via resonant current control," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, p. 1, 2011.

[9] I. Balaguer, Q. Lei, S. Yang, U. Supatti, and F. Z. Peng, "Control for grid-connected and intentional islanding operations of distributed power generation," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 147–157, Jan. 2011.

[10] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[11] D. M. Van de Sype, K. De Gusseme, A. P. Van den Bossche, and J. A. Melkebeek, "A sampling algorithm for digitally controlled boost PFC converters," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 649–657, May 2004.

[12] P. Mattavelli, G. Spiazzi, and P. Tenti, "Predictive digital control of power factor preregulators with input voltage estimation using disturbance observers," *IEEE Transactions on Power Electronics*, vol. 20, no. 1, pp. 140–147, Jan. 2005.
[13] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Transactions on Power Electronics,*, vol. 21, no. 1, pp. 263–272, Jan. 2006.
[14] F. Liu, Y. Zhou, S. Duan, J. Yin, B. Liu, and F. Liu, "Parameter design of a two-current-loop controller used in a grid-connected inverter system with LCL filter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 11, pp. 4483–4491, Nov. 2009.
[15] G. Shen, X. Zhu, J. Zhang, and D. Xu, "A new feedback method for PR current control of LCL-filter-based grid-connected inverter," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 6, pp. 2033–2041, Jun. 2010.
[16] D. M. Van de Sype, K. De Gusseme, F. M. L. L. De Belie, A. P. Vanden Bossche, and J. A. Melkebeek, "Small-signal z-domain analysis of digitally controlled converters," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 470–478, Mar. 2006.
[17] P. Mattavelli, F. Polo, F. Dal Lago, and S. Saggini, "Analysis of control-delay reduction for the improvement of UPS voltage-loop bandwidth," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 2903–2911, Aug. 2008.
[18] D. M. Van de Sype, K. D. Gusseme, A. P. M. Van den Bossche, and J. A. Melkebeek, "Duty-ratio feedforward for digitally controlled boost PFC converters," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 108–115, Feb. 2005.
[19] P. C. Loh and D. G. Holmes, "Analysis of multiloop control strategies for $LC/CL/LCL$-filtered voltage-source and current-source inverters," *IEEE Transactions on Industry Applications*, vol. 41, no. 2, pp. 644–654, Mar./Apr. 2005.
[20] X. Wang, X. Ruan, S. Liu, and C. K. Tse, "Full feedforward of grid voltage for grid-connected inverter with lcl filter to suppress current distortion due to grid voltage harmonics," *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3119–3127, Dec. 2010.
[21] J. C. Vasquez, J. M. Guerrero, A. Luna, P. Rodriguez, and R. Teodorescu, "Adaptive droop control applied to voltage-source inverters operating in grid-connected and islanded modes," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 10, pp. 4088–4096, Oct. 2009.
[22] H. Fujita, "A single-phase active filter using an H-bridge PWM converter with a sampling frequency quadruple of the switching frequency," *IEEE Transactions on Power Electronics*, vol. 24, no. 4, pp. 934–941, Apr. 2009.
[23] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*. Morgan and Claypool Publishers, 2007.
[24] J. Massing, M. Stefanello, H. Grundling, and H. Pinheiro, "Adaptive current control for grid-connected converters with LCL-filter," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1–14, 2011.
[25] V. Rajasekaran, J. Sun, and B. S. Heck, "Bilinear discrete-time modeling for enhanced stability prediction and digital control design," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 381–389, Jan. 2003.
[26] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled PWM converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2552–2556, nov. 2007.
[27] S. K. Mazumder, A. H. Nayfeh, and D. Boroyevich, "Theoretical and experimental investigation of the fast- and slow-scale instabilities of a DC-DC converter," *IEEE Transactions on Power Electronics*, vol. 16, no. 2, pp. 201–216, Mar. 2001.
[28] L. Corradini, P. Mattavelli, M. Corradin, and F. Polo, "Analysis of parallel operation of uninterruptible power supplies loaded through long wiring cables," *IEEE Transactions on Power Electronics*, vol. 25, no. 4, pp. 1046–1054, Apr. 2010.

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