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Suppressing Inter-module Oscillations for Paralleled 10 kV SiC MOSFET Modules

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***Abstract*-- This paper demonstrates the parallel connection of two 10 kV SiC MOSFET modules with a focus on eliminating inter-module oscillations during the turn-on switching event. A dual-gate driver structure is proposed to drive paralleled 10 kV SiC MOSFETs. Based on the platform, the mechanism of inter-module oscillation is observed and analyzed, revealing the cause as the circulating current flowing in the loop with the lowest impedance between paralleled modules. To dampen inter-module oscillations, ferrite beads are added to the gate loop. The effectiveness of the ferrite beads in the paralleling of medium voltage modules case is analyzed and experimentally verified by a double pulse test (DPT) with two paralleled 10 kV SiC MOSFET power modules at 6000 V/ 50 A.**

Index Terms—inter-module oscillation, 10 kV SiC MOSFET, ferrite bead, capacitive coupling, gate stability.

I. Introduction

The emerging 10 kV Silicon-Carbide (SiC) MOSFET features multiple device superiorities: higher breakdown voltage, higher switching speed, and lower on-state resistance, compared with silicon-based power devices [1]. These advantages allow power electronic converters (PEC) to operate with low losses, high switching frequencies, and simple topologies [2].

However, the maximum rated current of 10 kV SiC MOSFET die is limited by material properties and manufacturing immaturity [3]. Until now, the available engineering samples of 10 kV SiC MOSFET bare dies have a rated current of 20 A [4]. To further increase the power of converters, paralleled power devices are fundamental and widely used [5].

Extensive research has been presented related to the paralleled SiC MOSFETs from dies [6], discrete devices [7], to power modules [8], working on the practical issues of switching oscillation [9], and current imbalance [10]. This paper mainly focuses on the inter-module oscillations of paralleled MOSFETs.

The oscillations in the PEC system have negative effects on the power converters, including electromagnetic interference (EMI), additional power loss, and power shoot-through [11]. In terms of the oscillation type, the switching oscillations can be divided into common-mode and differential-mode oscillations.

Common-mode oscillations have been reviewed in [11], which can be explained by the resonance between parasitic inductances and device capacitances in the power loop. In contrast, differential-mode oscillations are observed between the paralleled devices [12]. The significant feature of differential-mode oscillations is the 180-degree phase difference between voltage and current across paralleled devices [13]. The oscillation frequency of differential-mode oscillations can be much higher, ranging from tens to hundreds of MHz [13].

In [14], inter-chip oscillations between two paralleled 1.2 kV SiC MOSFETs are considered as the typical differential-mode oscillation, which is reasoned by the mismatch from an asymmetric layout and the variable chip parameters. The influence of specific parasitic parameters on the inter-chip oscillations is summarized based on the proposed stability model. Severe oscillations happening in the gate-source voltage are also discovered when paralleling two 1.2 kV SiC MOSFET multichip modules with unbalanced drain inductance [9]. However, these differential-mode oscillations are all presented in low-voltage (LV) devices.

In the case of paralleled medium-voltage (MV) SiC MOSFETs, the increased amount of capacitive energy stored in the paralleling loop can have a stronger impact on the paralleling system stability [1]. In the meantime, the gate capability of MV SiC MOSFET keeps +25 V / -10 V, which is the same as LV SiC MOSFET [16]. Therefore, the risk of gate instability causing fault turn-on or turn-off in the MV SiC MOSFET application case is higher. Therefore, it is necessary to explore if the existing mitigation methods are still feasible for MV SiC MOSFET. Ferrite beads are recommended to be employed in the gate loop or the power loop to dissipate the high-frequency losses [17]. Therefore, the high-frequency oscillations cannot be sustained. None of the known papers have utilized ferrite beads to suppress inter-module oscillations happening in paralleled 10 kV SiC MOSFET modules.

To fill this gap, the inter-module oscillation will be demonstrated based on the paralleled 10 kV SiC MOSFET modules platform. Then, the generation mechanism and hypothesized loop of inter-module oscillations are analyzed. The gate-side ferrite bead method is adopted to dampen the inter-module oscillations, which will be validated through circuit simulations and DPT experiments. Finally, the experimental demonstration of paralleled 10 kV SiC MOSFET modules is performed at a DC-link voltage of 6 kV and a total load current of 50 A by introducing gate-side ferrite beads to reduce the inter-module oscillations.

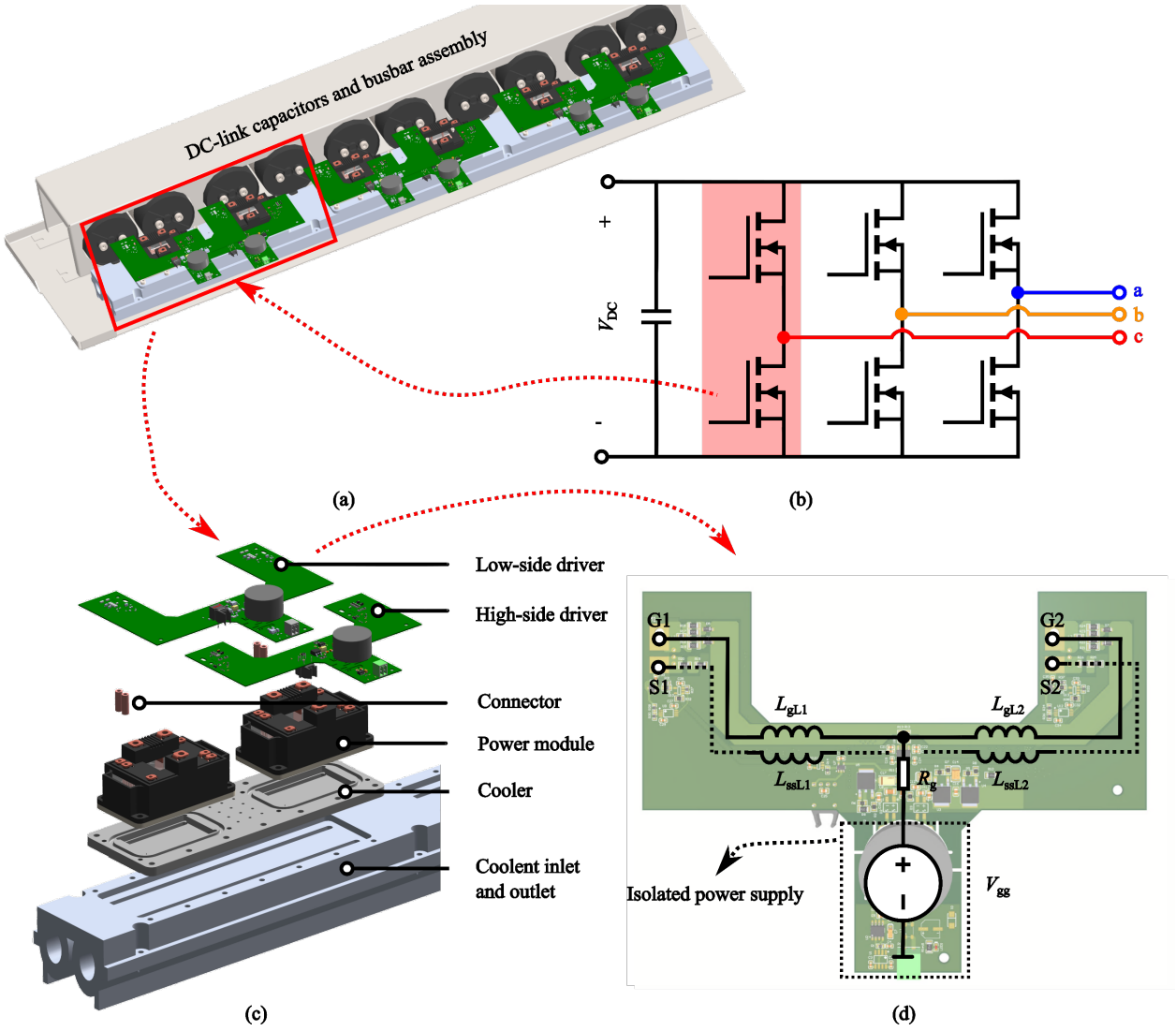

Fig. 1. (a) Three-phase power stack with two paralleled half-bridge 10 kV SiC MOSFET power modules per phase. (b) Schematic of a two-level topology for three phase MV power stack. (c) Exploded view of each phase. (d) PCB layout and equivalent circuit of dual-gate driver board.

II. Problem Formulation

In this section, the paralleling system is presented, with the highlight of the inter-module oscillations during the turn-on switching event.

A. Paralleling system

To increase the nominal power of a three-phase MV power stack, employing several power modules in parallel connection is common. Fig. 1(a) shows the CAD model of the liquid-cooled medium voltage three-phase power stack, with two paralleled 10 kV SiC MOSFET power modules in each phase. Exploded view of each phase is shown in Fig. 1(b). The half-bridge 10 kV SiC MOSFET modules populated with the 3rd generation Wolfspeed 10 kV/20 A dies are utilized for paralleling. To fit the two power modules into the existing industrial cooling system, the two power modules are placed beside each other to make a parallel connection.

From the mechanical point of view, it is challenging to arrange the gate driver board to drive two adjacent modules simultaneously. To address this issue, as shown in Fig. 1(c), two printed circuit boards (PCBs) are used to drive high-side and low-side switches individually. The copper connectors link the gate drivers and power modules, compensating for the height difference to maintain the required 6 kV insulation distance. The detailed assemblies of the power stack have been introduced in [18] .

Dual-gate driver is specially designed as shown in Fig. 1(d). To avoid the gate signal delay, two paralleled devices in the same switch position shared a gate drive IC in the middle of the driver board [19]. Therefore, the gate loop denoted in the black wire is a 'tree-like' loop. L_g and L_s with variable footnotes H1, H2, L1, and L2 stand for the parasitic inductance from the copper trace on the gate loop. R_g is a common gate resistor with a value of 23.5 Ω.

B. Inter-module oscillation

DPT is a typical test setup for predicting the realistic switching performance in the real case. The schematics for the low-side DPT setup are shown in Fig. 2.

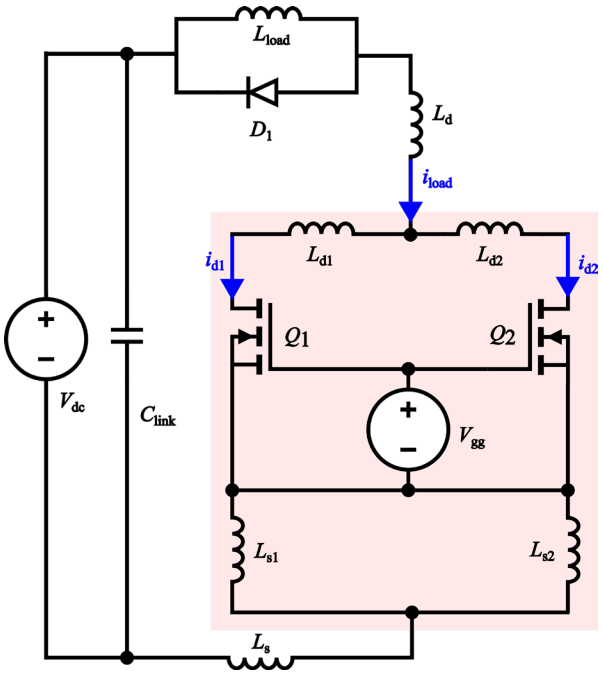

Fig. 2. Circuit diagram of low-side DPT setup with two paralleled MOSFETs.

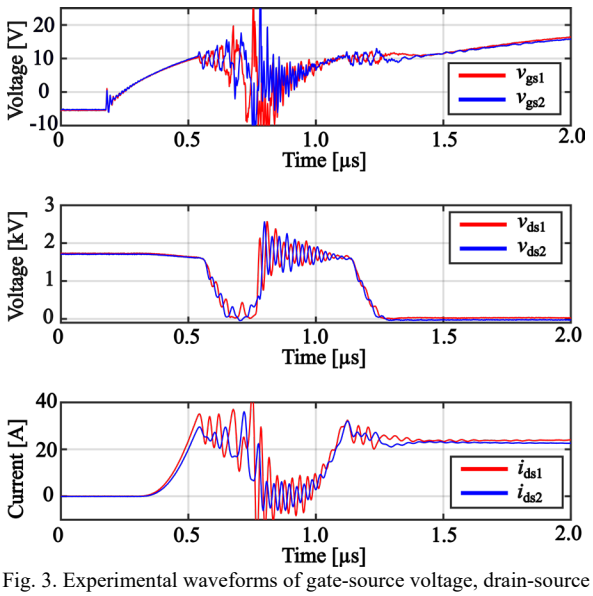

Fig. 3. Experimental waveforms of gate-source voltage, drain-source voltage, and drain current, showing the fault turn-off caused by severe oscillations during the Miller plateau.

The experimental switching waveforms of paralleled 10 kV SiC MOSFET modules under 2000 V DC bus voltage and 40A load current are shown in Fig. 3. Inter-module oscillations with increasing magnitude are observed in gate-source voltage (v_{gs}), drain current (i_d), and drain-source voltage (v_{ds}) in the Miller plateau. The oscillation frequency is in a range from 25 Mhz to 35 Mhz. Especially, a phase shift of 180° can be discovered between the oscillations in paralleled SiC MOSFETs (like v_{gs1} and v_{gs2}). In the worst case, the gate oscillation keeps going with a fast divergence speed and the maximum gate voltage can exceed the allowable value of gate-source voltage with the potential damage of gate oxide. In the meantime, the minimum gate-source voltage reaches -10 V, which causes a short-time fault turn-off.

The inter-module oscillations also exist in the drain currents (i_{d1} and i_{d2}) and drain-source voltage (v_{ds1} and v_{ds2}), which get worse with higher DC link voltage and higher load current. Therefore, it is necessary to eliminate inter-module oscillations to operate two 10 kV SiC MOSFET modules in parallel connection. To understand the cause of inter-module oscillations, the oscillation loop will be derived in the following section.

III. Inter-module Oscillation Analysis

The equivalent circuit of low-side DPT with two SiC MOSFETs (Q_1 and Q_2) in parallel connection is shown in Fig. 2. Based on this configuration, the turn-on switching event of Q_1 and Q_2 can be divided into 4 stages: 1) turn-on delay stage; 2) Miller plateau stage; 3) voltage fall stage; 4) on-state stage.

During the current rise stage, the load current (i_{load}) which formerly flowed through the reverse diode of the high-side switch (D_1) has transferred to the paralleled branches of Q_2 and Q_2 (i_{d1} and i_{d2}). It is observed in Fig. 3 that, after the current commutation period, the inter-module oscillations are building up when the drain-source voltage dramatically goes down. Therefore, a major insight into Miller plateau stage is provided.

During the Miller plateau stage, the MOSFET operates in the saturation region, where the current flowing the channel is controlled by the gate-source voltage via the transfer curve. The channel current can be expressed as (1) with g_d being the transconductance of the MOSFET. Considering the parasitic capacitance drain-source capacitance (C_{gd}), gate-drain capacitance (C_{gd}), and gate-source capacitance (C_{gs}), the parallel connection of two SiC MOSFETs can be depicted in Fig. 4. The current path is highlighted inside the SiC MOSFET. According to Kirchhoff's Current Law, the channel current (i_{ch}) can be expressed as (1) in this stage, whereas the displacement current induced by the dv/dt flowing through the parasitic capacitance can be shown as (3) and (4).

$$i_{ch} = i_d + i_{gd} + i_{ds} \tag{1}$$

$$i_{ch} = g_d \cdot \left(v_{gs} - v_{th}\right) \tag{2}$$

$$i_{gd} = C_{gd} \cdot \frac{\mathrm{d}v_{gd}}{\mathrm{d}t} \tag{3}$$

$$i_{ds} = C_{ds} \cdot \frac{\mathrm{d}v_{ds}}{\mathrm{d}t} \tag{4}$$

$$\begin{aligned} \Delta i_d &= i_{d1} - i_{d2} \\ &= g_d\left(v_{gs1} - v_{gs2}\right) + C_{oss} \cdot \frac{\mathrm{d}(v_{ds1} - v_{ds2})}{\mathrm{d}t} \end{aligned} \tag{5}$$

Therefore, the difference of drain current in two paralleled branches can be concluded as (5). From (5), it can be inferred that Δi_d equals zero when the following three conditions are satisfied: 1) v_{gs1}=v_{gs2}, 2) v_{ds1}=v_{ds2}, 3) The device parameters include g_d, V_{th}, and C_{oss} are the same.

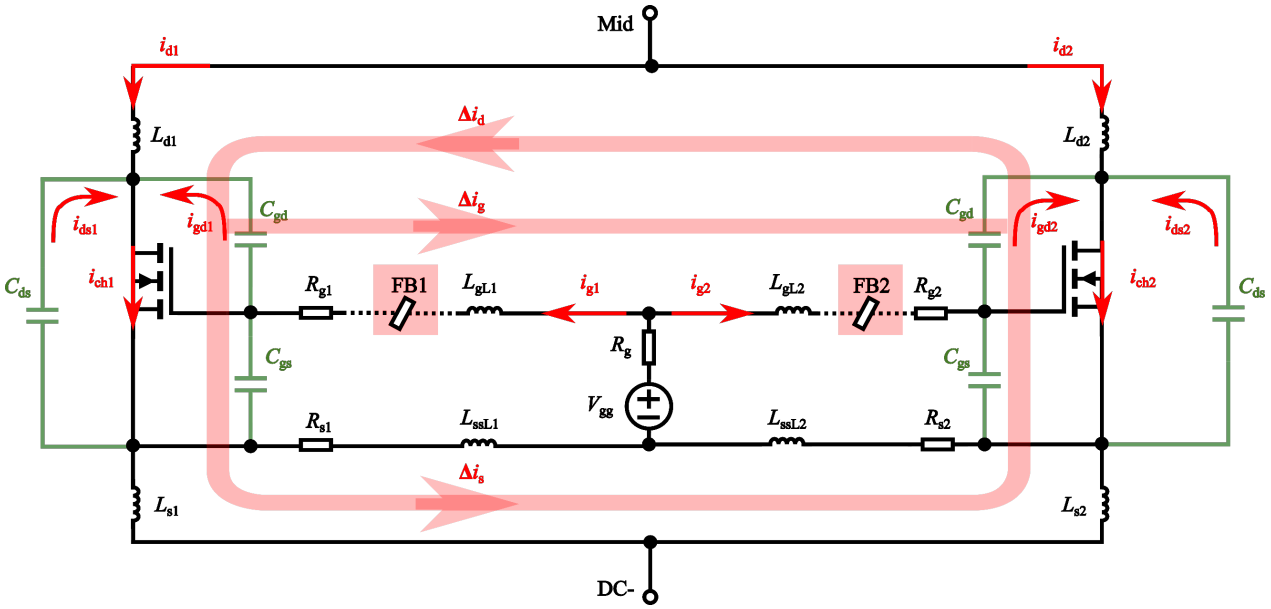

Fig. 4. Resonate tanks between two paralleled 10 kV SiC MOSFETs, showing the differential current loop.

However, the current imbalance can happen due to the realistic limitation during this transient, which can be the results of device variation (Δg_d, ΔV_{th}, ΔC_{oss}), gate signal mismatch (Δv_{gs}), and different rates of change in v_{ds} (dv_{ds}/dt). The formed differential current would flow within the resonant tank. If the MOSFET is regarded as a node, the differential current (Δi_d) has two loops to flow: the gate loop and the source loop. The gate loop includes the C_{gd}, L_d, R_g, and L_g, while the source loop consists of C_{ds}, L_{ss}, L_s, and R_s. The nonlinear parasitic capacitors C_{gd} and C_{ds} are strongly dependent on the v_{ds}, which means the stability of the resonance loop is modified during the voltage fall period. Differential current can excite the inter-module oscillations when the paralleling system comes to an unstable point.

Therefore, the mechanism of inter-module oscillation is that the differential current is first generated by the mismatch, which would exaggerate the inter-module oscillations when the resonance tank is unstable. There are two kinds of mitigation strategies. The first strategy is conducting the transfer function of paralleled circuits and changing the circuit parameters to minimize the instability. Another strategy is to decrease the differential current by increasing the loop impedance, which is adopted in this paper and will be analyzed in the next section.

IV. Damping Method with Gate Ferrite Bead

The ferrite bead method is regarded as an effective method to dampen the switching oscillations [11]. In this section, the influence of gate-side ferrite beads on the inter-module oscillations between two 10 kV SiC MOSFET modules is discussed, which is validated by the circuit simulations in LTspice.

A. Gate-side ferrite bead

The equivalent model of a ferrite bead is the parallel connection of frequency-dependent inductor, resistor, and capacitor. The typical impedance frequency of a ferrite bead can be shown in Fig. 5.

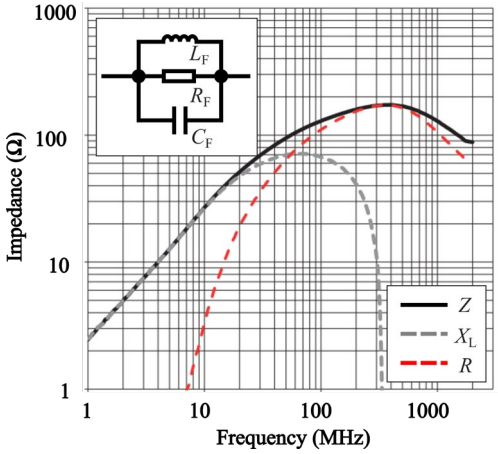

Fig. 5. Impedance frequency plot of ferrite bead (Würth Electronic: 74279202). [20]

At working frequency (5 – 10 kHz), a ferrite bead is regarded as an inductor, while at high oscillation frequency (20 – 100 MHz), it works as a resistor. Thanks to its special characteristics, it can be placed on the gate loop to dissipate high-frequency differential current flowing through the gate loop and attenuate the inter-module oscillations.

Two conditions should be satisfied when selecting the ferrite bead [17]. Firstly, the ferrite bead impendency at oscillation frequency should be mainly resistive. Secondly, at the normal working frequency, the resistance value of the ferrite bead should be low to keep the overall loss at a low level.

B. Simulations

The impact of gate-side ferrite beads is validated by simulations. A low-side double pulse test is simulated in LTspice, using the validated SPICE model in [21]. The DC-link voltage is 6 kV, and the total load current is 10 A.

The voltage fall time is 175 ns, which means that the turn-on dv/dt equals 34 V/ns. The source inductance difference (ΔL_s) is set to 10 nH to mimic the unbalanced power loop,

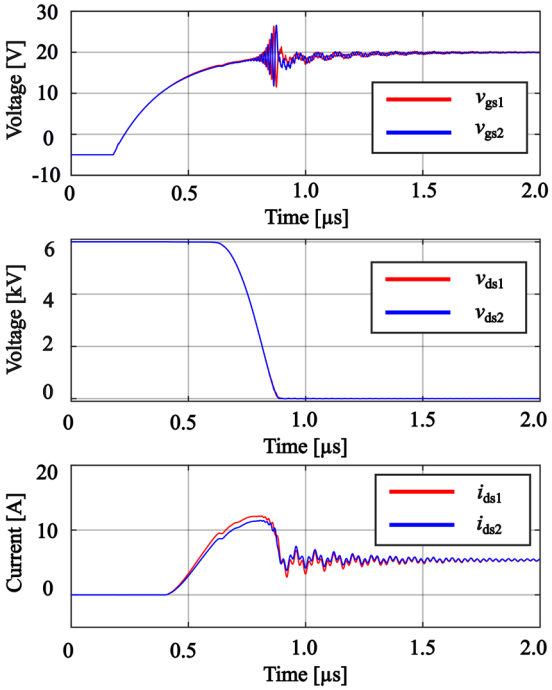

Fig. 6. Turn-on switching waveforms.

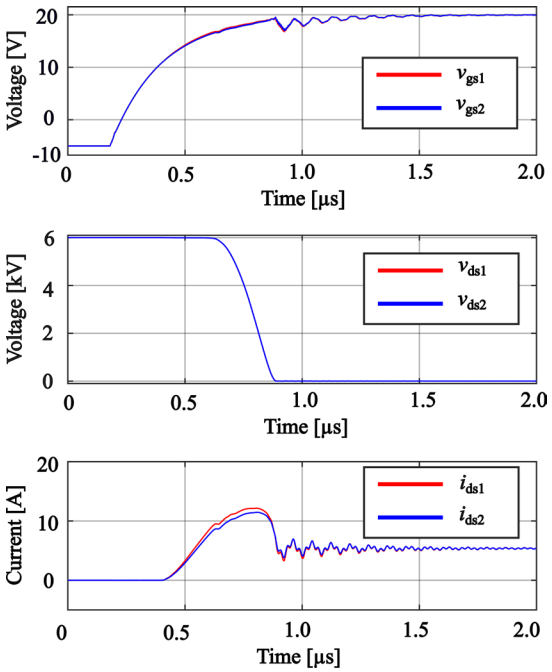

Fig. 7. Turn-on switching waveforms (with ferrite beads).

which excites the inter-module oscillations based on the hypothesis. The waveforms of turn-on switching events are shown in Fig. 6. Inter-module oscillations are obviously observed on the gate-source voltage. The maximum v_{gs} amplitude approach to 27V.

Fig. 7 shows the achieved turn-on switching event with the inter-module oscillations damped by applying a ferrite bead (The impedance frequency characteristic is given in Fig. 5) in the gate loop. The voltage fall time remains 176 ns, which is almost the same as before. The magnitude of inter-module oscillations is reduced to 3 V, which shows the gate-side ferrite beads can dampen the oscillations without sacrificing the switching speed.

V. Experimental Validation

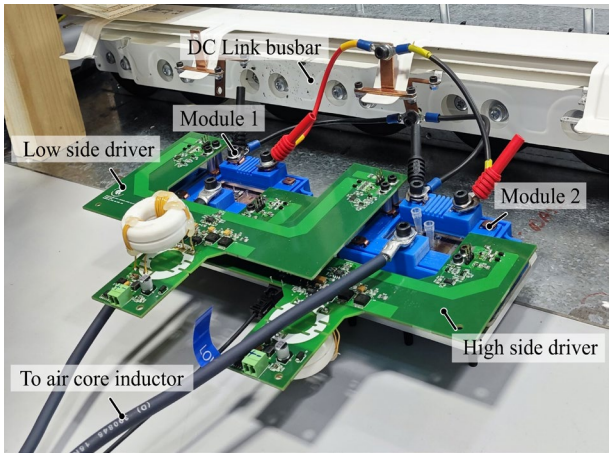

Fig. 8. Double pulse test platform.

TABLE II
EQUIPMENT AND KEY COMPONENTS.

Component	Specification
Air core inductor	47 mH / ≤12 pF
Gate resistance	23.5 Ω
v_{gs} measurement	LeCroy HVFO10360
v_{ds} measurement	LeCroy HVD3605A
i_d measurement	LeCroy CP030
Oscilloscope	LeCroy 8208HD

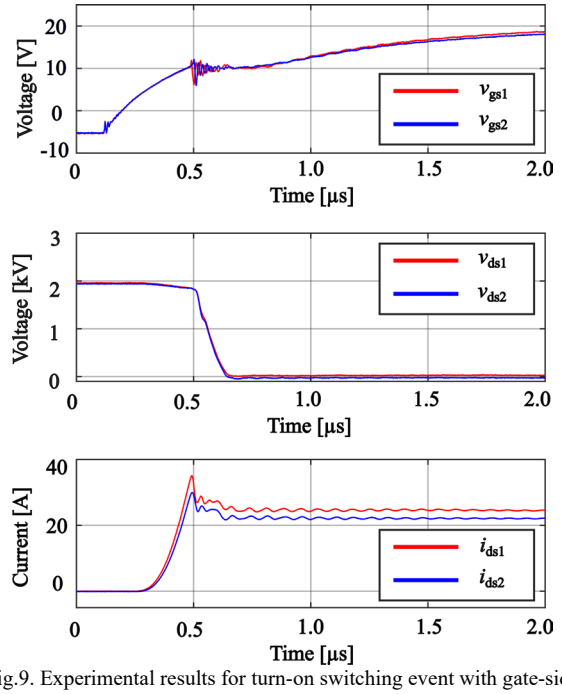

Fig.9. Experimental results for turn-on switching event with gate-side ferrite beads.

To validate the effectiveness of the mitigation approach of adding the gate-side ferrite bead, the double pulse test platform is built as shown in Fig. 8.

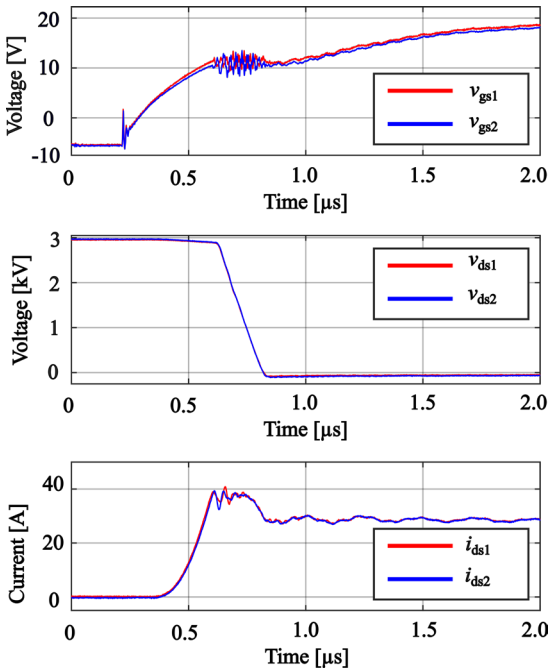

Fig. 10. Experimental results for turn-on switching event at 6 kV DC link voltage and 50 A total load current.

The key components and measurement are summarized in Table II. Fig. 9 illustrates the waveforms of gate-source voltage (v_{gs}), drain-source voltage (v_{ds}), and drain current (i_d) with ferrite bead (Würth Electronic: 74279202) to suppress inter-module oscillations. Compared to the experimental results shown in Fig. 3, at the same DC link voltage and load current, the peak-to-peak gate-source voltage of the inter-module oscillations has been damped to 4 V.

With the DC link voltage increase to 6 kV, the v_{gs} oscillations still maintain 5 V peak-to-peak voltage, which demonstrates the parallel operation of two 10 kV SiC MOSFET modules successfully shown in Fig. 10. Therefore, adding a ferrite bead in the gate loop can suppress the inter-module oscillations.

VI. Conclusion

This paper presents a study for paralleling two 10 kV SiC MOSFET modules by suppressing the inter-module oscillations. A dual-gate driver for driving two 10 kV power modules has been introduced. The oscillation loops of inter-module oscillations are investigated at the circuit level. To mitigate oscillations, gate-side ferrite beads are added to increase high-frequency impedance of oscillation loop and decrease differential current. Simulations and experiments show that ferrite beads can be used to reduce inter-module oscillations.

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