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Moving Average Filter Based Phase-Locked Loops: Performance Analysis and Design Guidelines

Saeed Golestan, *Member, IEEE*, Malek Ramezani, Josep M. Guerrero, *Senior Member, IEEE*, Francisco D. Freijedo, and Mohammad Monfared *Member, IEEE*

Abstract—The phase locked-loops (PLLs) are probably the most widely used synchronization technique in grid-connected applications. The main challenge associated with the PLLs is how to precisely and fast estimate the phase and frequency when the grid voltage is unbalanced and/or distorted. To overcome this challenge, incorporating moving average filter(s) (MAF) into the PLL structure has been proposed in some recent literature. A MAF is a linear-phase finite impulse response filter which can act as an ideal low-pass filter, if certain conditions hold. The main aim of this paper is to present the control design guidelines for a typical MAF-based PLL. The paper starts with the general description of MAFs. The main challenge associated with using the MAFs is then explained, and its possible solutions are discussed. The paper then proceeds with a brief overview of the different MAF-based PLLs. In each case, the PLL block diagram description is shown, the advantages and limitations are briefly discussed, and the tuning approach (if available) is evaluated. The paper then presents two systematic methods to design the control parameters of a typical MAF-based PLL: one for the case of using a proportional-integral (PI) type loop-filter (LF) in the PLL, and the other for the case of using a proportional-integral-derivative (PID) type LF. Finally, the paper compares the performance of a well-tuned MAF-based PLL when using the PI-type LF with the results of using the PID-type LF, which provides useful insights into their capabilities and limitations.

Index Terms—Moving average filter (MAF), phase-locked loop (PLL), grid synchronization.

I. INTRODUCTION

PROPER synchronization with the utility grid, particularly when the grid voltage is unbalanced and harmonically distorted, is an issue of high importance for almost all grid-connected power electronic equipment. In recent years, many synchronization techniques have been proposed in literature. They can be broadly classified into the *open-loop* and *closed-loop* methods [1], [2].

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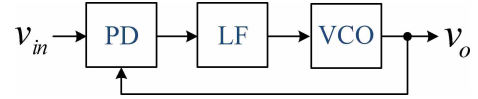


Fig. 1. Block diagram description of a typical single-phase PLL.

A variety of open-loop synchronization techniques can be found in literature. The methods based on using the extended Kalman filters (EKFs) [3], [4], the space vector filters (SVFs) [3], the weighted least-square estimation (WLSE) algorithms [5], [6], the cascaded delayed signal cancellation (CDSC) [7], and the moving average filters (MAFs) [8] are among the existing open-loop synchronization techniques.

The key feature of open-loop synchronization techniques is that they are unconditionally stable. They typically yield a satisfactory performance in terms of the phase/frequency detection accuracy when the grid frequency is at, or close to, its nominal value; however, their performance tends to worsen when the input frequency deviates from its nominal value. To overcome this problem, incorporating frequency estimation/control algorithms into the open-loop schemes have been proposed in [3]-[5], and [8]. However, this measure is usually at the cost of increasing the implementation complexity. An overview of different open-loop synchronization techniques can be found in [9].

The closed-loop synchronization techniques are closed-loop feedback control systems that regulate an error signal to zero. They can be classified into two major categories: 1) the phase-locked loops (PLLs) in which the error signal is made by the difference between the estimated and reference phases; and 2) the frequency-locked loops (FLLs) in which the error signal is made by the difference between the estimated and reference frequencies.

The PLLs are probably the most popular and widely used synchronization technique within the areas of power electronic and power system [10]-[11]. They typically consist of three basic parts: a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO) [12]. Fig. 1 shows the block diagram description of a typical single-phase PLL.

Focusing on grid-connected applications, a major challenge associated with the PLLs is how to precisely and fast estimate the phase and frequency when the grid voltage is unbalanced and/or distorted. To overcome this challenge, incorporating different filtering techniques into the PLL structure have been proposed in literature [13]-[39]. Among these filtering techniques, the MAF is one of the most popular and widely

used techniques owing to its simple digital realization, low computational burden, and effectiveness.

The main objective of this paper is to present control design guidelines for a typical MAF-based PLL. The paper starts with a general description of the MAFs. The major problem associated with the MAFs, that is their frequency-dependent attenuation characteristics, is then addressed, and the possible solutions are discussed. A comparison among these solutions is also carried out, which provides a guideline for selecting the proper method for a given application. The paper proceeds with a brief overview of the different MAF-based PLLs. In each case, the PLL block diagram description is shown, the advantages and limitations are briefly discussed, and the tuning approach (if available) is evaluated. Two systematic methods to design the control parameters of a typical MAF-based PLL are then presented: one for the case of using a proportional-integral (PI) type LF in the PLL, and the other for the case of using a proportional-integral-derivative (PID) type LF. Finally, the paper compares the performance of a well-tuned MAF-based PLL when using the PI-type LF with the results of using the PID-type LF, which provides useful insights into their capabilities and limitations.

II. DESCRIPTION AND IMPLEMENTATION ISSUES OF MAFs

MAFs are linear-phase finite impulse response (FIR) filters that can act as ideal low-pass filters (LPFs) if certain conditions hold [24], [40]. They are easy to realize in practice, and are cost effective in terms of the computational burden. In this section, the continuous-time description and the discrete-time realization of MAFs are presented. The major problem associated with using the MAFs is then addressed, and the possible solutions are discussed.

A. Continuous-Time Description

A MAF with the input signal $x(t)$ and the output signal $\bar{x}(t)$ can be described in continuous-time domain by

$$\bar{x}(t) = \frac{1}{T_w} \int_{t-T_w}^t x(\tau) d\tau \quad (1)$$

where T_w is referred to as the window length. From (1), the MAF transfer function can be simply obtained as

$$G_{MAF}(s) = \frac{\bar{x}(s)}{x(s)} = \frac{1 - e^{-T_w s}}{T_w s}. \quad (2)$$

The transfer function (2) shows that the MAF requires a time equal to its window length to reach steady-state condition. Therefore, the wider the window length, the slower the MAF transient response will be.

By substituting $s = j\omega$ into (2), and performing some simple mathematical manipulations, the magnitude and phase expressions of the MAF can be obtained as

$$G_{MAF}(j\omega) = \left| \frac{\sin(\omega T_w/2)}{\omega T_w/2} \right| \angle -\omega T_w/2. \quad (3)$$

From (3), it can be noticed that, the MAF provides unity gain at zero frequency, and zero gain at frequencies $f = n/T_w$

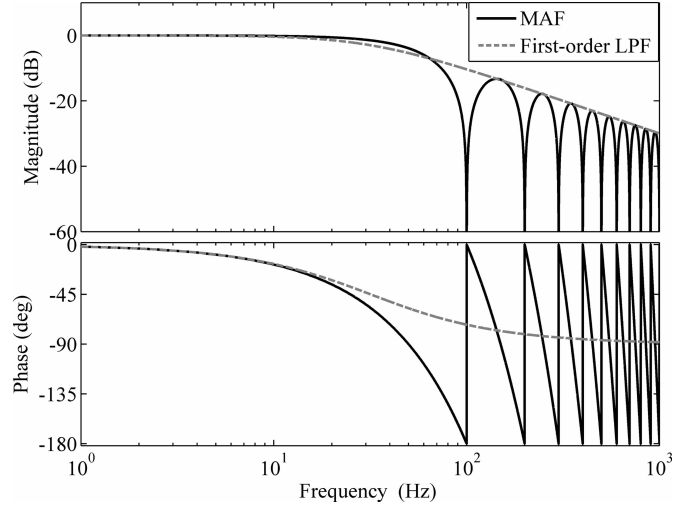


Fig. 2. Bode plots of MAF and its first-order counterpart for $T_w = 0.01$ s.

($n = 1, 2, 3, \dots$) in hertz. It means that the MAF passes the dc component, and completely blocks the frequency components of integer multiples of $1/T_w$ in hertz. This can be better visualized through the MAF Bode plot shown in Fig. 2. The window length T_w is considered to be 0.01 s. To provide a means of comparison, the Bode plot of the first-order counterpart of the MAF, i.e.,

$$G_{MAF}(s) \big|_{e^{-T_w s} \approx \frac{1 - T_w s/2}{1 + T_w s/2}} \approx \frac{1}{\frac{T_w}{2}s + 1} \quad (4)$$

is also shown in Fig. 2. Notice that (4) is obtained by approximating the delay term in (2) by the first-order Padé approximation. As shown, the MAF frequency response includes an infinite set of notches centered at $1/T_w = 100$ Hz and its integer multiples. Therefore, as mentioned before, the MAF completely blocks these frequency components. It is an interesting feature which enables the MAF to act as an ideal LPF.

B. Discrete-Time Realization

Equation (1) defines the MAF in the continuous-time domain. However, to realize it in practice, a discrete-time definition is required. Assuming that the window length of the MAF contains N samples (N is an integer which, as we will see later, determines the MAF order) of its input signal, i.e., $T_w = NT_s$ where T_s is the sampling time, the discrete-time description of MAF can be obtained, based on (1), as

$$\bar{x}(k) = \frac{1}{N} \sum_{i=0}^{N-1} x(k-i) \quad (5)$$

where $x(k)$ is the current sample.

The difference equation (5) can be expressed in Z-domain as

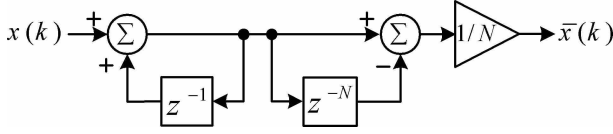


Fig. 3. Discrete-time realization of MAF.

$$\begin{aligned}
 \bar{X}(z) &= G_{MAF}(z)X(z) \\
 &= \frac{1}{N} \left(X(z) + z^{-1}X(z) + \dots + z^{-(N-1)}X(z) \right) \\
 &= \left(\frac{1}{N} \sum_{i=0}^{N-1} z^{-i} \right) X(z) \\
 &= \frac{1}{N} \frac{1 - z^{-N}}{1 - z^{-1}} X(z). \tag{6}
 \end{aligned}$$

The implementation of the discrete transfer function $G_{MAF}(z)$ is shown in Fig. 3. As shown, the MAF is computationally efficient; For a fixed window length, it requires only one multiplication, one addition, and one subtraction.

C. Frequency-Adaptive MAF Implementation

Assume that the MAF has been designed to block the sinusoidal disturbances of integer multiples of the frequency f_d in hertz, i.e., $T_w = NT_s = 1/f_d$ (it will be shown later that, for a typical MAF-based PLL, the disturbance frequency f_d is equal to twice the fundamental grid frequency (i.e., $f_d = 100$ Hz in a 50 Hz system) in most practical cases). The problem arises when the grid frequency, and as a result, the disturbance frequency f_d changes. In such a case, the MAF cannot completely block the disturbance components. It is the main challenge associated with using the MAFs.

To achieve a frequency-adaptive MAF, several approaches have been proposed in literature. What all these approaches have in common is the online adjustment of the MAF window length according to the grid frequency variations. A brief overview of these approaches is presented in the following.

In [25]–[28], the MAF window length is adapted to the grid frequency variations by adaptively adjustment of the PLL sampling frequency. It should be noticed that the PLL is a small part of the control strategy in most cases. Therefore, due to the restrictions and requirements of the control strategy, implementation of a variable sampling rate PLL may not be always possible.

Adjustment of the MAF order, N , according to the grid frequency variations is another approach to make the MAF frequency adaptive. To do this, different approaches can be found in literature. In its simplest form, the MAF order can be adjusted by rounding-down or rounding-up T_w/T_s to the nearest integer, i.e.,

$$N = N_f = \text{floor}(T_w/T_s) \tag{7}$$

$$N = N_c = \text{ceil}(T_w/T_s) \tag{8}$$

where $T_w = 1/\hat{f}_d$ (\hat{f}_d is an estimation of f_d , and is calculated using an estimation of grid frequency). Another approach,

suggested by Freijedo *et al.* [40], uses a look-up table to adaptively adjust N . The look-up receives an estimation of the grid frequency as input, and calculates the MAF order as the nearest integer to T_w/T_s , i.e.,

$$N = N_r = \text{round}(T_w/T_s) \tag{9}$$

where, again, $T_w = 1/\hat{f}_d$.

Originally developed for reducing the detection error in the delayed signal cancellation (DSC) methods, the “mean value” approach [41] can also be used to make the MAF frequency adaptive. By using this approach, the MAF can be defined as

$$\bar{x}(k) = \frac{1}{2} \left(\frac{1}{N_f} \sum_{i=0}^{N_f-1} x(k-i) + \frac{1}{N_c} \sum_{i=0}^{N_c-1} x(k-i) \right) \tag{10}$$

where N_f and N_c are given in (7) and (8), respectively.

Notice that (10) has time-varying parameters. Therefore, it cannot be represented in the transfer-function form in the general case. However, for a given window length, it can be represented by

$$\begin{aligned}
 \bar{X}(z) &= G_{MAF}^{MV}(z)X(z) \\
 &= \frac{1}{2} \left(\frac{\frac{1}{N_f} + \frac{1}{N_f+1}}{1 - z^{-1}} - \frac{1}{N_f} z^{-N_f} - \frac{1}{N_f+1} z^{-(N_f+1)} \right) X(z) \tag{11}
 \end{aligned}$$

where the superscript “MV” denotes the mean value approach.

Another solution, again developed for reducing the detection error in the DSC methods, is the “weighted mean value” approach [41]. By using this approach, the MAF can be defined as

$$\bar{x}(k) = \frac{1-\alpha}{N_f} \sum_{i=0}^{N_f-1} x(k-i) + \frac{\alpha}{N_c} \sum_{i=0}^{N_c-1} x(k-i) \tag{12}$$

where α is called the weighting factor. Obviously, when $T_w = N_f T_s$, the weighting factor α should be equal to zero, and when $T_w = N_c T_s = (N_f+1)T_s$, the weighting factor α should be equal to one. Therefore, it can be defined in a simple form as

$$\alpha = \frac{T_w - N_f T_s}{T_s}. \tag{13}$$

For a given window length, (12) can be represented in transfer-function form by

$$\begin{aligned}
 \bar{X}(z) &= G_{MAF}^{WMV}(z)X(z) \\
 &= \frac{\left(\frac{1-\alpha}{N_f} + \frac{\alpha}{N_f+1} \right) - \frac{1-\alpha}{N_f} z^{-N_f} - \frac{\alpha}{N_f+1} z^{-(N_f+1)}}{1 - z^{-1}} X(z) \tag{14}
 \end{aligned}$$

where the superscript “WMV” denotes the weighted mean value approach.

Another approach is to incorporate the linear interpolation method into the MAF, as shown in Fig. 4 [30]. By using this approach, the MAF is defined as

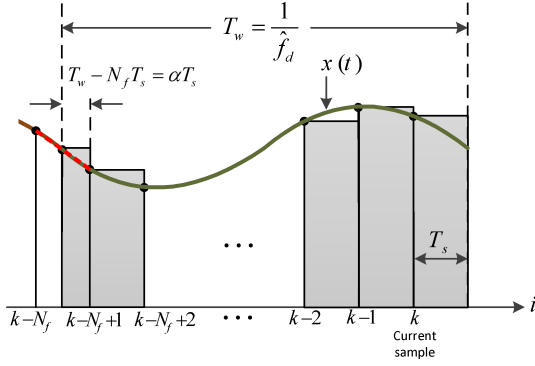


Fig. 4. Incorporating the linear interpolation method into MAF. The dashed red line shows the linear interpolation to estimate the inter-sample value.

$$\bar{x}(k) = \frac{T_s}{T_w} \left(\sum_{i=0}^{N_f-1} x(k-i) + \alpha [(1-\alpha)x(k-N_f+1) + \alpha x(k-N_f)] \right) \quad (15)$$

where α is the same as that given in (13).

For a given window length, (15) can be represented in transfer-function form by (16), where the superscript “LIP” denotes the linear interpolation.

A natural thought to further improve the MAF performance under frequency varying environments is to use a high-order polynomial interpolation instead of the linear interpolation. Considering the fact that the sampling time is very small, the performance improvement by using the high order polynomial interpolation will be very limited, and cannot counterbalance the extra complexity.

To provide a comparison among these adaptive methods, we perform the following procedure for each method: the disturbance frequency f_d is changed from 96 Hz to 104 Hz, and the magnitudes of MAF at different values of f_d are obtained and shown in Fig. 5. To provide a base for comparison, the obtained result for a nonadaptive MAF ($N = 100$) is also shown in this figure. The sampling time T_s is set to 0.0001 s in this study. As shown, the weighted mean value method [Fig. 5(f)] and the linear interpolation method [Fig. 5(g)] give the best results. Round-to-nearest-integer method [Fig. 5(d)] and mean value method [Fig. 5(e)] can be considered as the next best options.

III. MAF-BASED PLLS

This section provides an overview of different MAF-based PLLs. In each case, the PLL general structure is shown, the advantages and limitations are discussed, and the tuning approach (if available) is evaluated.

A. PLLs With Nonadaptive MAF(s)

All PLLs reviewed in this section use nonadaptive MAF(s) within their control loop(s). In some literature, this is justified by the reason that the grid voltage frequency changes within a limited range in most practical cases.

In [31] and [32], incorporating the MAF into the phase-control loop of a conventional synchronous reference frame PLL (SRF-PLL) are suggested. Fig. 6 shows the block diagram description of this PLL, which is referred to as the MA-PLL. The experimental results reported in [31] and [32] show that including MAF within the phase control loop of a SRF-PLL improves its filtering capability at the cost of slows down its transient response. A design method for selecting the control parameters of the MA-PLL is also suggested in [31]. In this method, the dynamic of the MAF is approximated by a first-order LPF with a time-constant of T_w , i.e., $G_{MAF}(s) \approx 1/(T_w s + 1)$, which is inaccurate [see (4)]. Besides, the design method is based on a trial-and-error procedure, and, therefore, is time-consuming.

In [34], a modified power-based PLL (pPLL), referred to as the discrete Fourier transform (DFT) PLL is proposed. Fig. 7 shows a block diagram description of this PLL. The DFT-PLL offers a high degree of immunity to the input signal harmonics when the grid frequency is at, or close to, its nominal value. However, it may suffer from a high double frequency error when the grid frequency deviation from its rated value is high.

For accurate phase, frequency and amplitude detection capability under adverse grid conditions, a three-phase PLL, here called the modified multiple reference frame (MRF) PLL, is proposed in [35]. Fig. 8 shows the block diagram description of this PLL. When compared to the original MRF-PLL [22], the modification of this PLL is to replace the first-order LPFs in the MRF network with nonadaptive MAFs, which improve its filtering capability, particularly when the grid frequency is at, or close to, its nominal value.

In [36], incorporating the MAFs (where they are called the rectangular windows in [36]) into the control loops of the enhanced PLL (EPLL) is suggested. A method to design the LF gains for a windowed PLL is also suggested in [36]. In this method, the characteristic equation of the PLL phase-control loop is considered as

$$s^2 + V k_p G_{MAF}(s)s + V k_i G_{MAF}(s) = 0 \quad (17)$$

where V is the input signal amplitude, and it is assumed to be equal to 1 pu for the sake of simplicity, and k_p and k_i are the proportional and integral gains of the PI-type LF, respectively. The proportional and integral gains are then defined as $k_p = 2\zeta\omega_n$ and $k_i = \omega_n^2$, where ζ is the damping factor and ω_n is the natural frequency. The design method suggests to 1) select $\zeta = 1$; 2) draw the root locus of the closed-loop poles versus the natural frequency ω_n ; 3) obtain ω_n by selecting the location of the dominant poles; and 4)

$$\bar{X}(z) = G_{MAF}^{LIP}(z)X(z) = \frac{T_s}{T_w} \frac{1 - (\alpha^2 - \alpha)z^{-(N_f-1)} - (1 + \alpha - 2\alpha^2)z^{-N_f} - \alpha^2 z^{-(N_f+1)}}{1 - z^{-1}} X(z) \quad (16)$$

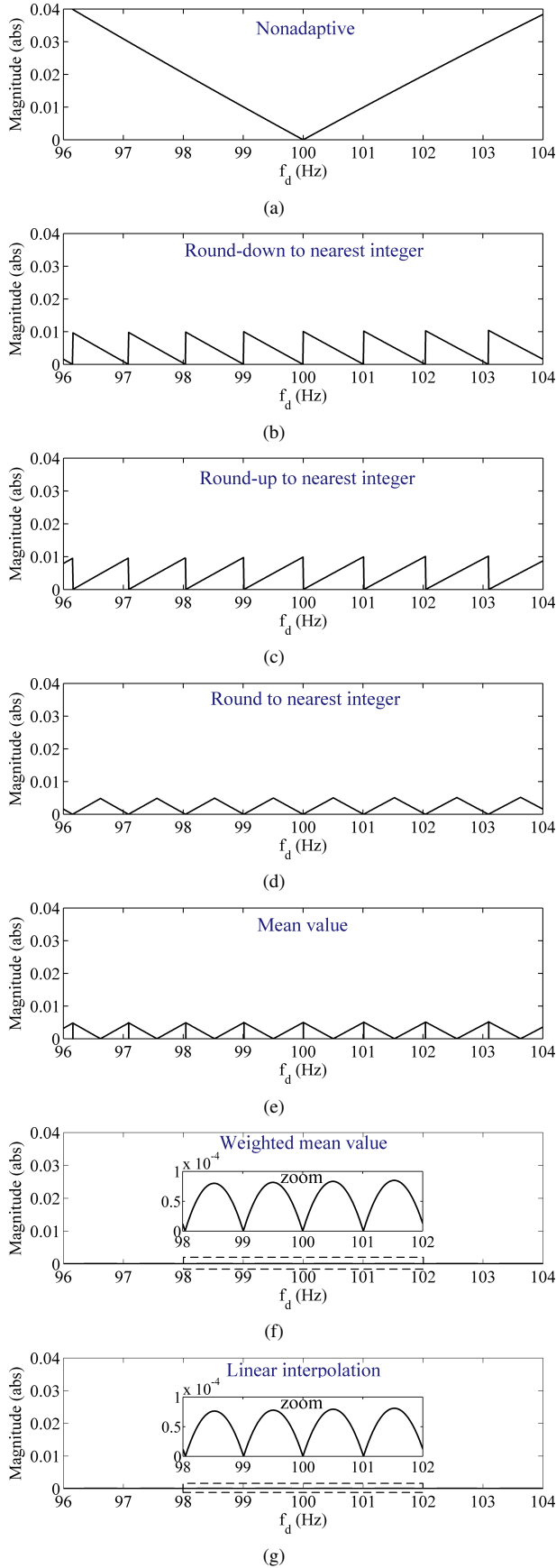


Fig. 5. Magnitude of MAF at the disturbance frequency f_d when f_d is changed from 96 Hz to 104 Hz ($T_w = 1/f_d$, and $T_s = 0.0001$ s). (a) Nonadaptive MAF, (b) Round-down to nearest integer method, (c) Round-up to nearest integer method, (d) round to nearest integer method, (e) mean value method, (f) weighted mean value method, and (g) linear interpolation method.

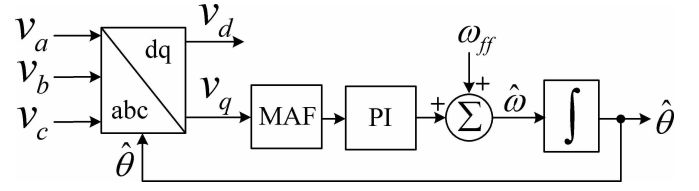


Fig. 6. Block diagram description of the MA-PLL.

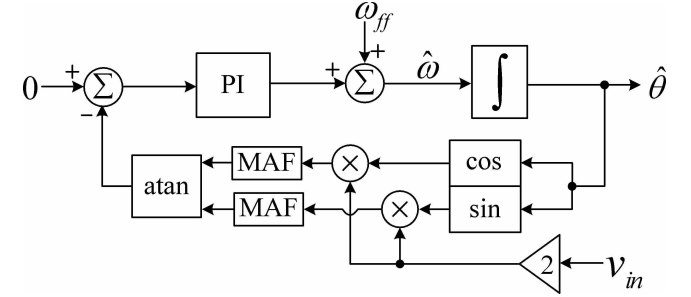


Fig. 7. Block diagram description of the DFT-PLL.

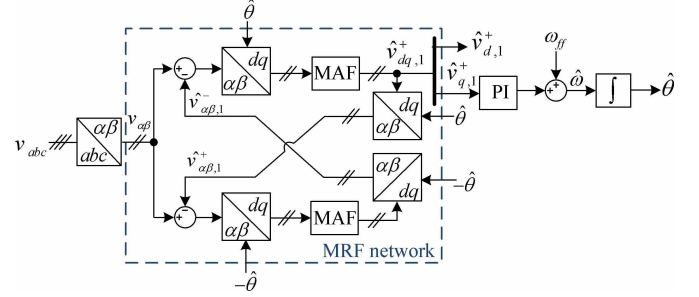


Fig. 8. Block diagram description of the modified MRF-PLL.

calculate the proportional and integral gains using the selected values for ζ and ω_n . A drawback associated with this approach is that it is a relatively time-consuming procedure, and it may take some trial and error, depending on the designer's experience.

B. PLLs With Frequency-Adaptive MAF(s)

All PLLs reviewed in this section use frequency adaptive MAF(s) in their control loop(s).

Fig. 9 shows the block diagram description of the MAF-based PLL proposed in [37] and [38], which consists of a conventional SRF-PLL and two frequency adaptive MAFs. As shown, the estimated frequency by the PLL is used to make the MAFs frequency adaptive, however, the adaptive mechanism is not explained. The parameters design method suggested in [37] and [38] is based on neglecting the dynamic of the MAF and modeling the PLL as a second order system. This design method, although simple, is not optimum at all.

To estimate the amplitude and angle of the fundamental frequency positive and negative sequence components, a PLL referred to as the double Matlab-PLL (mPLL) is proposed in [9]. The block diagram description of this PLL is shown in Fig. 10. As shown, the double mPLL employs two SRF-PLLs with in-loop MAFs: one for the positive sequence and the

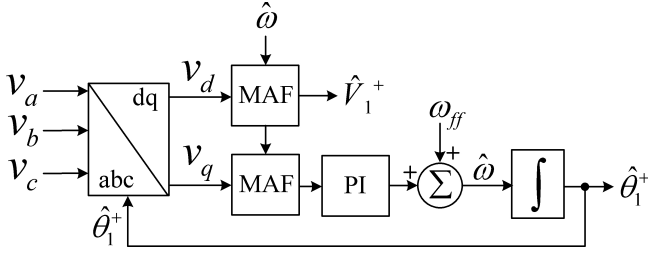


Fig. 9. A conventional SRF-PLL with frequency adaptive MAFs.

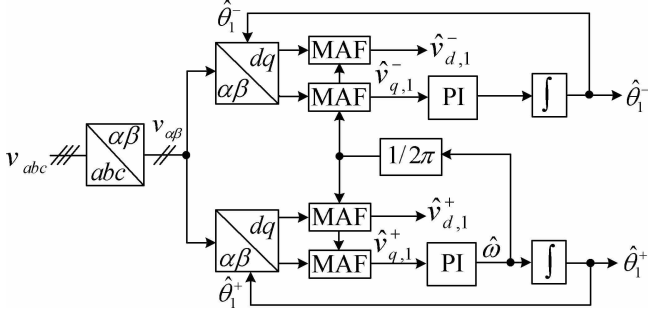


Fig. 10. Block diagram description of the double mPLL.

other for the negative sequence. The estimated frequency by the positive sequence SRF-PLL is used to make the MAFs frequency adaptive.

In [26], a single-phase PLL for synchronization purposes under adverse grid conditions is proposed. A simple block diagram of this PLL, here called the variable sampling frequency PLL (VSF-PLL), is shown in Fig. 11. As shown, this PLL is basically a pPLL; however its sampling period is adjusted to adapt the MAF window length to the grid frequency variations. The limitation of variable sampling rate PLLs was already discussed in section II-C. To tune the control parameters of this PLL, some z-domain design guidelines, mainly based on a trial and error method, are also suggested in [26].

In [27], a three-phase PLL, referred to as the variable sampling period filter PLL (VSPF-PLL) is proposed. The VSPF-PLL uses the same idea of the VSF-PLL (Fig. 11). Therefore, it has the same characteristics as the VSF-PLL. A modification of this PLL is to use a PID controller (instead of the PI controller) as the LF, which improves its dynamic response during grid disturbances. Some design guidelines to adjust the parameters of the PID-type LF are also suggested in [27]. It is worth mentioning that the single-phase version of VSPF-PLL can be found in [28].

Fig. 12 shows the block diagram of the proposed PLL in [30], which can be considered as the modified version of the PLL shown in Fig. 9. The main modifications are incorporating two units, referred to as the initial phase angle detector and the reconstructor, into the PLL structure which improve its performance during grid disturbances. The linear interpolation method is used in this PLL to make the MAFs frequency adaptive.

Several other MAF-based PLLs can be found in [24], [42], and [43].

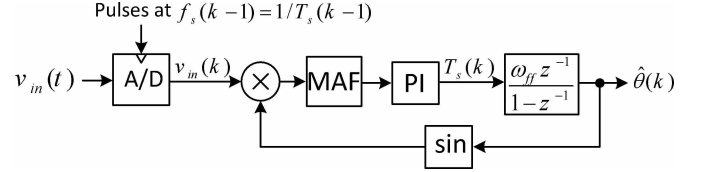


Fig. 11. Block diagram description of the VSF-PLL.

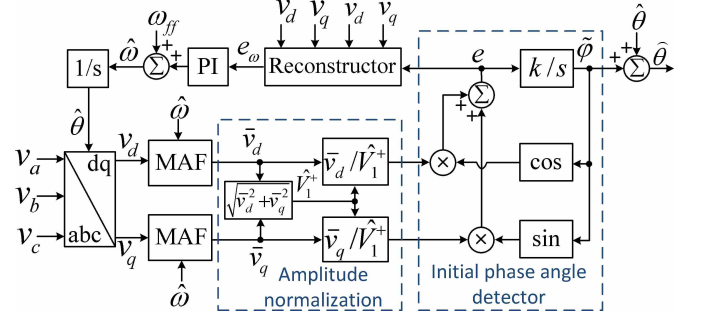


Fig. 12. Block diagram description of the proposed PLL in [30].

IV. DESIGN GUIDELINES

In this section, some control design guidelines for MAF-based PLLs are presented. A pPLL with in-loop MAF, shown in Fig. 13, and a conventional SRF-PLL with in-loop MAF (MA-PLL), shown in Fig. 14, are considered for this study. In both of these PLLs, $LF(s)$ is the transfer function of the LF which can be a PI controller or a PID controller. The nonadaptive MAF is considered in this study. The design guidelines are based on the small-signal model of these PLLs, which are derived in the following.

A. Small-Signal Modeling

First, the small-signal model of the pPLL is derived. Let the single-phase input voltage of the pPLL be represented by

$$v_{in} = V_1 \cos(\omega t + \phi_1) + V_3 \cos(3\omega t + \phi_3) + \dots \quad (18)$$

where V_h , θ_h , and ϕ_h ($h = 1, 3, 5, \dots$) are the amplitude, phase-angle, and initial phase-angle of the h th harmonic component of the input voltage, respectively, and ω is the input voltage angular frequency. Notice that the even harmonic components and the dc offset are not considered, since they have much smaller magnitudes than the odd harmonic components in practice.

From Fig. 13, the MAF input signal p' can be expressed as

$$p' = 2v_{in}i_s = V_1 \sin(\hat{\theta}_1 - \theta_1) + V_1 \sin(\hat{\theta}_1 + \theta_1) + V_3 \sin(\hat{\theta}_1 - \theta_3) + V_3 \sin(\hat{\theta}_1 + \theta_3) + \dots \quad (19)$$

Notice that each component of order h in the pPLL input leads to two different components of orders $h \pm 1$ after multiplier if $\omega = \hat{\omega}$.

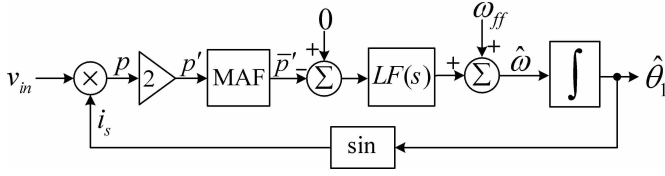


Fig. 13. pPLL with in-loop MAF.

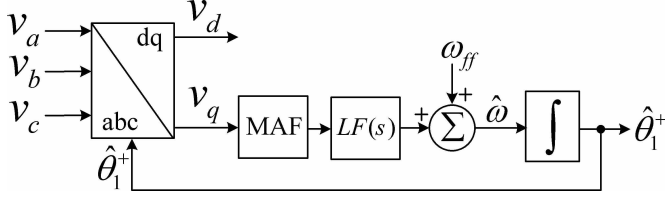


Fig. 14. MA-PLL.

Under a quasi-locked state (i.e., when $\theta_1 \approx \hat{\theta}_1$ and $\omega = \hat{\omega}$), (19) can be approximated by

$$p' \approx V_1(\hat{\theta}_1 - \theta_1) + f(2\omega, 4\omega, 6\omega, \dots). \quad (20)$$

Using (20) and Fig. 13, the pPLL small-signal model can be obtained as shown in Fig. 15, where $D(s) = -L[f(2\omega, 4\omega, 6\omega, \dots)]$ (L denotes the Laplace operator).

Now, the small-signal model of the MA-PLL is derived. Let the three-phase input voltages of the MA-PLL be represented by

$$\begin{aligned} v_a &= \sum_{h=1,5,7,\dots} [V_h^+ \cos(\theta_h^+) + V_h^- \cos(\theta_h^-)] \\ v_b &= \sum_{h=1,5,7,\dots} [V_h^+ \cos(\theta_h^+ - \frac{2\pi}{3}) + V_h^- \cos(\theta_h^- + \frac{2\pi}{3})] \\ v_c &= \sum_{h=1,5,7,\dots} [V_h^+ \cos(\theta_h^+ + \frac{2\pi}{3}) + V_h^- \cos(\theta_h^- - \frac{2\pi}{3})] \end{aligned} \quad (21)$$

where V_h^+ (V_h^-) and θ_h^+ (θ_h^-) ($h = 1, 5, 7, 11, 13, \dots$) are the amplitude and phase angle of the h th harmonic component of the positive- (negative-) sequence of the input voltages, respectively. The zero-sequence components are not considered, as the Clarke (abc -to- $\alpha\beta$) transformation blocks them [13]. The even harmonic components and dc offset are also neglected as they have negligible magnitudes in most practical cases.

Applying the Clarke transformation to the three-phase input voltages, yields

$$\begin{aligned} v_\alpha &= \sum_{h=1,5,7,\dots} [V_h^+ \cos(\theta_h^+) + V_h^- \cos(\theta_h^-)] \\ v_\beta &= \sum_{h=1,5,7,\dots} [V_h^+ \sin(\theta_h^+) - V_h^- \sin(\theta_h^-)]. \end{aligned} \quad (22)$$

Applying the Park ($\alpha\beta$ -to- dq) transformation to the $\alpha\beta$ coordinate voltage, yields the q -axis component v_q as

$$v_q(t) = \sum_{h=1,5,7,\dots} [V_h^+ \sin(\theta_h^+ - \hat{\theta}_1^+) - V_h^- \sin(\theta_h^- + \hat{\theta}_1^+)]. \quad (23)$$

Under a quasi-locked state (i.e., $\omega = \hat{\omega}$ and $\theta_1^+ \approx \hat{\theta}_1^+$), (23) can be approximated by

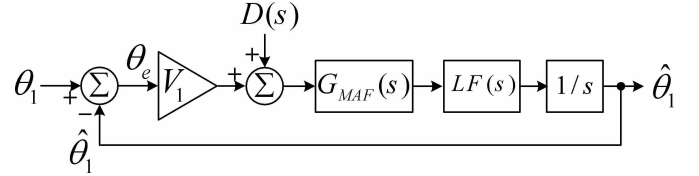


Fig. 15. Small-signal model of the pPLL.

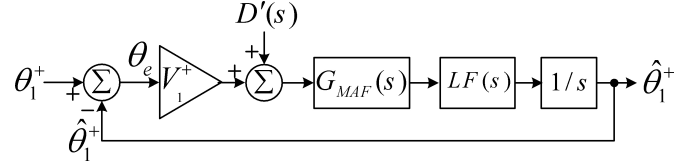


Fig. 16. Small-signal model of the MA-PLL.

$$v_q(t) \approx V_1^+ (\theta_1^+ - \hat{\theta}_1^+) + f'(2\omega, 4\omega, 6\omega, \dots). \quad (24)$$

Using (24) and Fig. 14, the small-signal model of the MA-PLL can be obtained as shown in Fig. 16, where $D'(s) = L[f'(2\omega, 4\omega, 6\omega, \dots)]$.

Notice that the pPLL and MA-PLL have the same small-signal model. Therefore, a same design approach can be applied to both PLLs. The accuracy of the small-signal models will be confirmed later.

B. Selection of the MAF window length

The selection of the window length of the MAF is an issue of high importance, and it should be done according to the possible disturbance components in the PLL input voltage(s). In the previous section, the odd harmonics and the non-triplen odd harmonics were considered as the dominant harmonic components in the input voltage(s) of the pPLL and the MA-PLL, respectively. It was shown that, in the presence of such harmonic components, the control loop of both PLLs suffer from even harmonic ripples. Therefore, to cancel out these ripples, the MAF window length should be set equal to the half of the fundamental period of grid voltage, i.e., $T_w = \pi/\omega = 0.01$ s in a 50 Hz system (remember that the MAF blocks the sinusoidal components of integer multiples of $1/T_w$ in hertz).

In this paper, the presence of dc offset and the even harmonic components in the input voltage(s) of the PLLs under study were neglected due to their much smaller magnitude than the odd harmonic components in most practical cases. Anyway, for those applications where they may have considerable magnitudes, the MAF window length should be set equal to the fundamental period of grid voltage, i.e., $T_w = 2\pi/\omega = 0.02$ s in a 50 Hz system.

C. PI-Type LF Parameters Design

In this section, a systematic method to design the control parameters of a PI-type LF for the PLLs under study is proposed. The suggested design approach is performed on the MA-PLL, which is valid for the pPLL as well. The LF

transfer function is $LF(s) = k_p + k_i/s$, where k_p and k_i are the proportional and integral gains, respectively. The proposed method is based on the symmetrical optimum method, which is a standard design procedure in various applications, such as electric motor drives [44], the frequency synthesizers [45], and the grid synchronization PLLs [46]-[47].

According to the symmetrical optimum method, for a PLL with an open-loop transfer function of the form

$$G_{ol} = V \frac{\omega_p(k_p s + k_i)}{s^2(s + \omega_p)} \quad (25)$$

the control parameters k_p , k_i , and ω_p can be selected as

$$\omega_p = b\omega_c \quad (26a)$$

$$k_p = \omega_c/V \quad (26b)$$

$$k_i = \omega_c^2/(bV) \quad (26c)$$

where ω_c is the gain crossover frequency, and b is a design constant which should be selected according to the required transient response and stability margin. It is shown in the following that this design procedure is applicable to the MA-PLL.

From Fig. 16, the open-loop transfer function of MA-PLL can be obtained as

$$G_{ol}(s) = \frac{\hat{\theta}_1^+}{\theta_e} \bigg|_{D'(s)=0} = V_1^+ G_{MAF}(s) LF(s) \frac{1}{s}. \quad (27)$$

By substituting $LF(s) = k_p + k_i/s$, and approximating the MAF with its first-order counterpart [see (4)], (27) can be approximated by

$$G_{ol}^{PI}(s) \approx V_1^+ \frac{k_p s + k_i}{s^2 \left(\frac{T_w}{2} s + 1 \right)} = V_1^+ \frac{\frac{2}{T_w} (k_p s + k_i)}{s^2 \left(s + \frac{2}{T_w} \right)}. \quad (28)$$

Comparing (25) and (28), it can be noticed that they are the same transfer functions for $\omega_p = 2/T_w$ and $V = V_1^+$. Therefore, the same design procedure as that summarized in (26) can be used to design the LF parameters (i.e., k_p and k_i) of MA-PLL.

Substituting $\omega_p = 2/T_w$ into (26a), yields the gain crossover frequency ω_c as

$$\omega_c = \frac{2}{bT_w}. \quad (29)$$

By substituting (29) into (26b) and (26c), we can obtain the proportional and integral gains as

$$\begin{aligned} k_p &= \frac{2}{V_1^+ b T_w} \\ k_i &= \frac{4}{V_1^+ b^3 T_w^2}. \end{aligned} \quad (30)$$

The design constant b is selected to be 2.4, as this value makes the PLL transient response fast and well-damped, and provides a phase margin (PM) of about 45° for the PLL which guarantees its stability [47]. With this selection, and following the suggested guidelines in previous section about selecting the MAF window length, the control parameters of MA-PLL

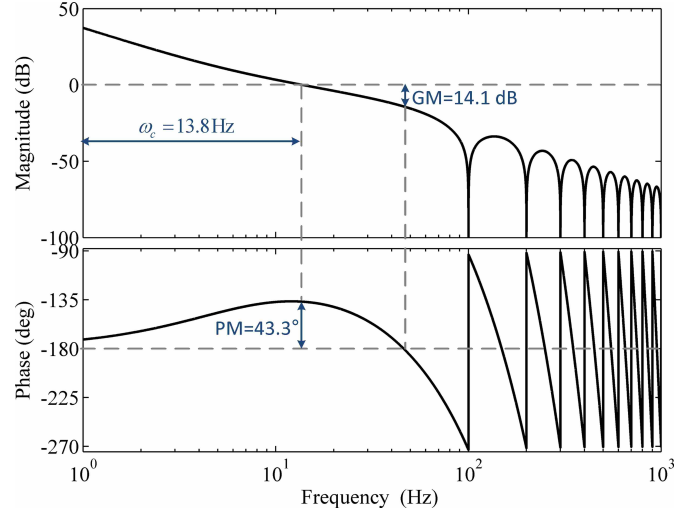


Fig. 17. Bode plot of open-loop transfer function (27) when using the PI-type LF. Parameters: $T_w = 0.01$, $V_1^+ = 1$ pu, $k_p = 83.33$, and $k_i = 2893.5$.

can be calculated as

$$\begin{aligned} T_w &= \pi/\omega = 0.01 \\ k_p &= 2/(V_1^+ b T_w) = 83.33 \\ k_i &= 4/(V_1^+ b^3 T_w^2) = 2893.5 \end{aligned} \quad (31)$$

Notice that to calculate the parameters, $V_1^+ = 1$ pu, and $\omega = 2\pi 50$ rad/s were considered.

Fig. 17 shows the Bode plot of the open-loop transfer function (27) using the designed control parameters. As shown, the designed parameters result in a PM of 43.3° and a gain margin (GM) of 14.1 dB, which guarantees the PLL stability. Notice that the crossover frequency corresponds to the peak of phase plot.

To evaluate the accuracy of the small-signal modeling, and to confirm the validity of the approximation made during the design procedure (i.e., approximating MAF with its first-order counterpart), the transient response of the MA-PLL (Fig. 14) is compared to the transient response of its small-signal model (Fig. 16) when the MAF in the model is replaced by its first order counterpart. The obtained results are shown in Fig. 18, which confirms the accuracy of the small-signal model, as well as the validity of the approximation.

In practice, the PLL is implemented in a discrete device. Therefore, it seems to be more accurate to perform the LF parameters tuning in the z-domain instead of the s-domain. It should be noticed that the PLL bandwidth is much lower than its sampling frequency. Therefore, the s-domain analysis/tuning can provide an accuracy as good as that achievable in z-domain. In addition, the analysis/tuning in the Laplace domain is more convenient and straightforward than that in the z-domain. For these reasons, the s-domain analysis/tuning was considered here. Anyway, the designers who are interested in a z-domain analysis/tuning, will find some z-domain control design guidelines for a MAF-based PLL in [26].

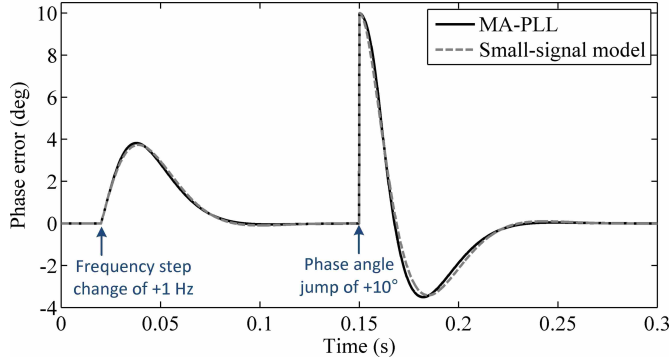


Fig. 18. Performance comparison between the MA-PLL and its small-signal model (MAF in the model is replaced by its first-order counterpart) under grid voltage disturbances. Parameters: $T_w = 0.01$, $V_1^+ = 1$ pu, $k_p = 83.33$, and $k_i = 2893.5$

D. PID-Type LF Parameters Design

In this section, a systematic method to design the control parameters of a PID-type LF for the MA-PLL is proposed. This method is valid for the case of pPLL as well.

Let the transfer function of the PID-type LF be of the form

$$LF(s) = k'_p \frac{1 + \tau_i s}{\tau_i s} \frac{1 + \tau_d s}{1 + \beta \tau_d s} \quad (32)$$

where k'_p is the proportional gain, and τ_i and τ_d are the integral and derivative time constants, respectively. The term $1 + \beta \tau_d s$ in the denominator produces a high frequency pole in order to filter the derivative action of the PID controller. For this reason, it is referred to as the derivative filter, and β is referred to as the derivative filter factor. A typical value for β is 0.1.

By substituting (32) into (27), and approximating the MAF with its first order counterpart, the open-loop transfer function of MA-PLL becomes

$$G_{ol}^{PID}(s) \approx V_1^+ k'_p \frac{1}{\frac{T_w}{2}s + 1} \frac{1 + \tau_i s}{\tau_i s} \frac{1 + \tau_d s}{1 + \beta \tau_d s} \frac{1}{s}. \quad (33)$$

According to (33), it can be noticed that the phase delay caused by the MAF can be compensated by selecting the derivative time constant equal to half the window length, i.e., $\tau_d = T_w/2$. With this selection, and considering that the derivative filter (which corresponds to a high frequency pole) has a small effect on the PLL dynamics, (33) can be simplified to

$$G_{ol}^{PID}(s) \approx V_1^+ k'_p \frac{1 + \tau_i s}{\tau_i s^2}. \quad (34)$$

Using (34) and Fig. 16, the closed-loop transfer function of the MA-PLL can be obtained as

$$G_{cl}^{PID}(s) = \frac{G_{ol}^{PID}(s)}{1 + G_{ol}^{PID}(s)} \approx \frac{V_1^+ k'_p s + V_1^+ k'_p / \tau_i}{s^2 + \underbrace{V_1^+ k'_p}_{2\zeta\omega_n} s + \underbrace{V_1^+ k'_p / \tau_i}_{\omega_n^2}}. \quad (35)$$

The closed-loop transfer function (35) is a standard second-order transfer function with a zero, and is characterized by two parameters: 1) the damping factor ζ ; and 2) the natural

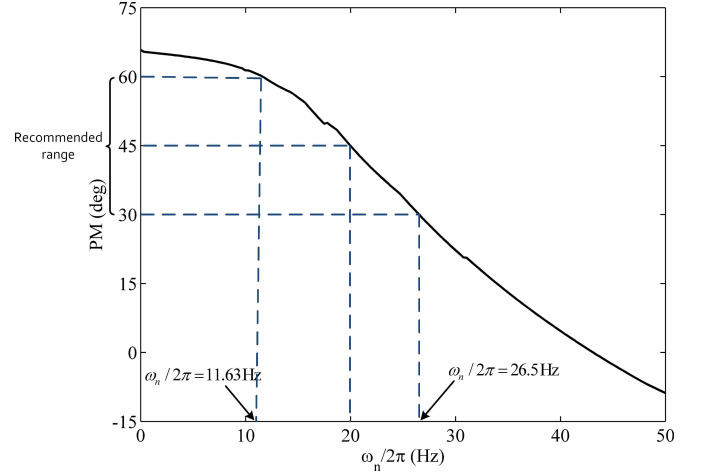


Fig. 19. PM versus the natural frequency ω_n . Parameters: $T_w = 0.01$, $V_1^+ = 1$ pu, $\zeta = 0.707$, $\tau_d = T_w/2$, $\beta = 0.1$, $\tau_i = 2\zeta/\omega_n$, $k'_p = 2\zeta\omega_n/V_1^+$.

frequency ω_n . Typically, a value of 0.707 is recommended as the optimum value for the damping factor ζ . However, selection of the natural frequency ω_n depends on the application requirements. In most applications, a fast dynamic response for the PLL is desirable, which requires a high value for the natural frequency ω_n . However, it should be noticed that a very high value for ω_n may jeopardize the MA-PLL stability because of presence of the MAF within its control loop. This fact can be better visualized through the curve plotted in Fig. 19, which shows the PM variations of MA-PLL as a function of ω_n . Notice that the exact open-loop transfer function (27) is used to obtain this plot. As shown, the PM decreases as ω_n increases. Therefore, as mentioned before, the value of ω_n cannot be arbitrary increased, and it should be chosen carefully.

In most control texts, a PM within the range of $30^\circ - 60^\circ$ is recommended. In this paper, a PM in the middle of this range, i.e., $PM = 45^\circ$, is selected, which corresponds to $\omega_n \approx 2\pi 20$ rad/s as shown in Fig. 19.

With these selections for ζ and ω_n , and following the suggested guidelines in section IV-B about selecting the MAF window length, the control parameters can be calculated as

$$\begin{aligned} T_w &= \pi/\omega = 0.01 \\ k'_p &= 2\zeta\omega_n/V_1^+ = 177.69 \\ \tau_i &= 2\zeta/\omega_n = 0.01125 \\ \tau_d &= T_w/2 = 0.005 \end{aligned} \quad (36)$$

Again, to calculate the parameters, $V_1^+ = 1$ pu, and $\omega = 2\pi 50$ rad/s were considered.

Fig. 20 shows the Bode plot of the open-loop transfer function (27) using the designed control parameters. As shown, the PID-type LF can provide a higher bandwidth (a faster dynamic response) than that obtained by the PI-type LF without jeopardizing the PLL stability.

V. NUMERICAL RESULTS

In this section, the MA-PLL (Fig. 14) is numerically simulated in the MATLAB/Simulink environment for two different

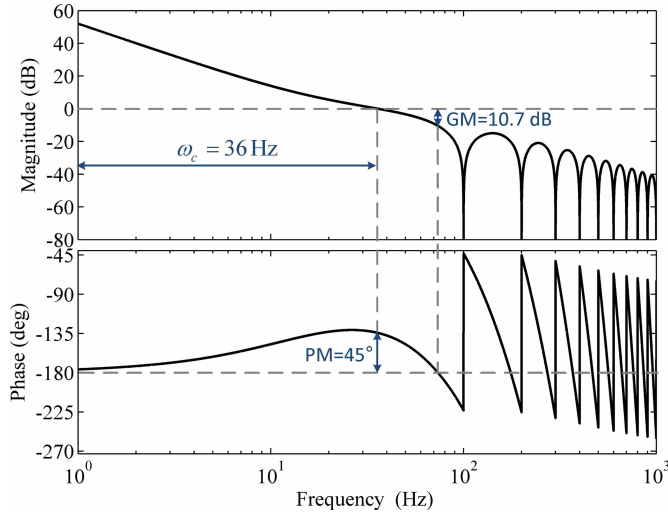


Fig. 20. Bode plot of the open-loop transfer function of (27) when using the PID-type LF. Parameters: $T_w = 0.01$, $V_1^+ = 1$ pu, $k_p' = 177.69$, $\tau_i = 0.01125$, $\tau_d = 0.005$, and $\beta = 0.1$.

cases: one for the case of using the PI-type LF [control parameters values are given in (31)], and the other for the case of using the PID-type LF [the control parameter values are given in (36)]. In both cases, the MAF is considered to be nonadaptive. Throughout the simulation studies, the sampling frequency of the MA-PLL is fixed to 10 kHz, and the nominal angular frequency is set to $2\pi 50$ rad/s.

A. Frequency step change

Fig. 21 shows the simulations results for the MA-PLL when the grid voltage undergoes a frequency step change of +5 Hz. As shown, the PID-type LF results in much better transient response than the PI-type LF. The 2% settling time, i.e., the time after which the estimated frequency by the MA-PLL reaches and remains within 0.1 Hz of its final value, is about 37 ms for the case of using the PID-type LF, while it is about 74 ms for the case of using the PI-type LF. The phase-error overshoot is about 19.2° for the case of using the PI-type LF, while it is about 7.8° for the case of using the PID-type LF.

B. Phase-angle jump

Fig. 22 shows the simulations results when the grid voltage undergoes a phase-angle jump of $+40^\circ$. Again, the PID-type LF results in a shorter transient time. The 2% settling time, i.e., the time after which the phase error reaches and remains within 0.8° neighborhood of zero, is about 37 ms for the case of using the PID-type LF, while it is about 75 ms for the case of using the PI-type LF. However, the PID-type LF results in a frequency overshoot of about 16.7 Hz, which is almost twice of that for the case of using the PI-type LF.

C. Unbalanced and harmonically distorted grid conditions

Fig. 23 shows the steady-state peak-to-peak phase error of the MA-PLL under off-nominal grid frequency conditions

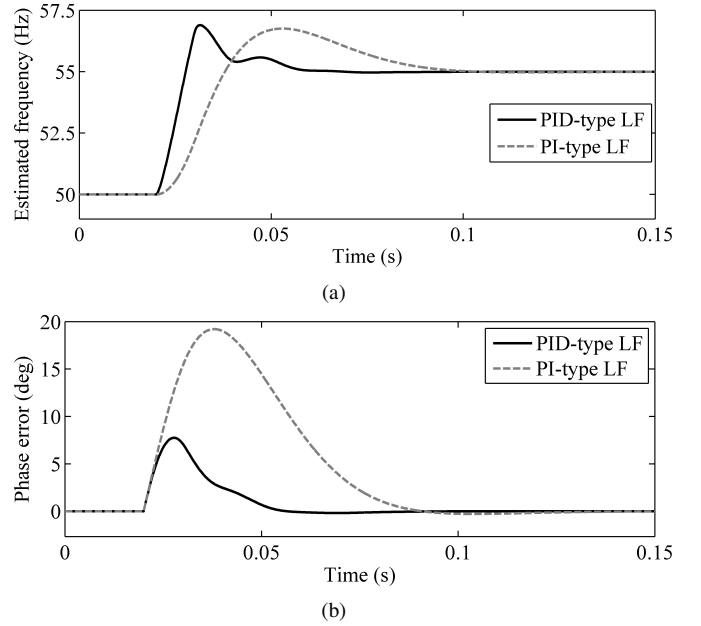


Fig. 21. Simulations results when the grid voltage undergoes a frequency step change of +5 Hz.

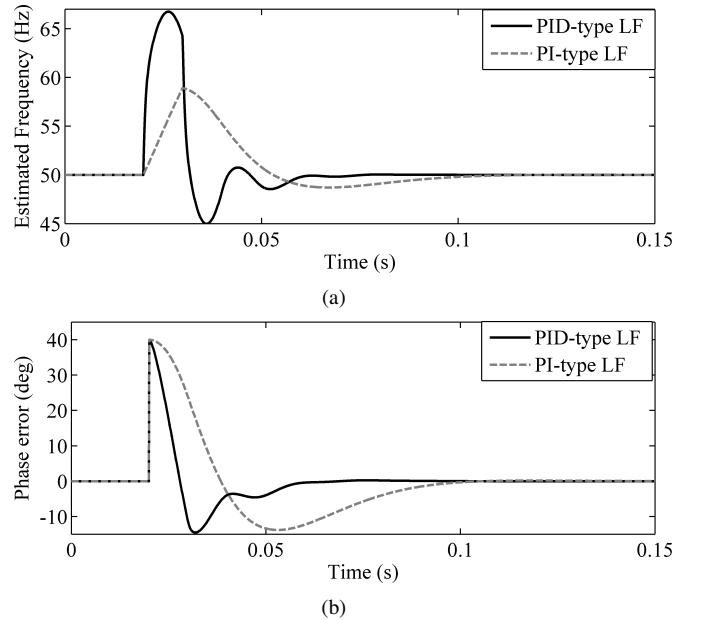


Fig. 22. Simulations results when the grid voltage undergoes a phase angle jump of $+40^\circ$.

($2\pi 51$ rad/s and $2\pi 55$ rad/s) and in the presence of fundamental negative sequence component and the low-order harmonic components in its input signals. This figure shows that

- For both PI-type and PID-type LFs, the phase error of the MA-PLL increases with increasing its input harmonic content (or its unbalance level) or increasing the deviation of the grid frequency from its nominal value.
- The PI-type LF results in a much better disturbance rejection capability than the PID-type LF. This conclusion can also be confirmed through the closed-loop Bode plots shown in Fig. 24.

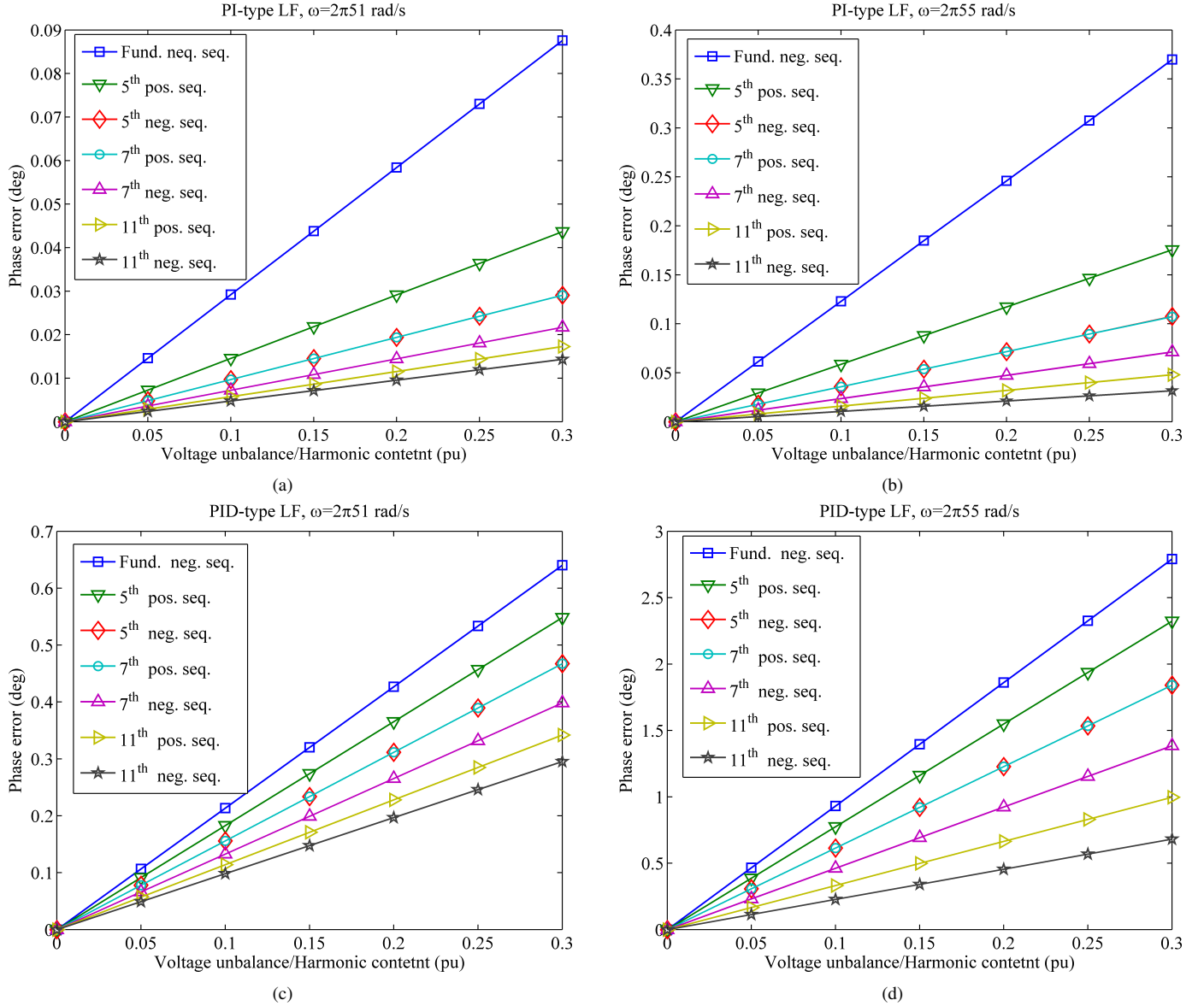


Fig. 23. Steady-state peak-to-peak phase error of the MA-PLL under off-nominal grid frequency condition and in the presence of fundamental negative sequence component and the low-order harmonic components in its input signals. (a) PI-type LF and $\omega = 2\pi 51$ rad/s, (b) PI-type LF and $\omega = 2\pi 55$ rad/s, (c) PID-type LF and $\omega = 2\pi 51$ rad/s, and (d) PID-type LF and $\omega = 2\pi 55$ rad/s.

- Contrary to the case of using the PI-type LF, which yields acceptable results even under large frequency deviations, the obtained results for the case of using the PID type LF are acceptable just when the grid voltage frequency is close to its nominal value.

According to these results, we recommend to use the frequency-adaptive MAF in the MA-PLL when the PID-type LF is employed. For the case of using the PI-type LF in the MA-PLL, the frequency adaptation of the MAF may not be required for most practical purposes.

It should be noted that, for the case of pPLL, the control loop suffers from a double frequency sinusoidal ripple with the same amplitude as the fundamental voltage component [see (19) and (20)]. Notice that this ripple is a by-product of the PD's multiplication function which continues to be present even if the pPLL input signal is a clean sine wave. This high

amplitude ripple makes the frequency adaptation of the MAF necessary for the pPLL, particularly when the PID-type LF is used.

D. Noise Contamination

In practical applications, the noise contamination is inevitable. Therefore, the noise immunity is a feature of high importance for the PLLs. This section evaluates the level of MA-PLL noise immunity. To perform a thorough simulation, the dynamics of the anti-aliasing filter is also considered in this study. The anti-aliasing filter is an analog filter in practice which is used before analog to digital conversion to limit the noise bandwidth [48].

The input signal in this study is a balanced three-phase set of signals with the amplitude of 1 pu which are contaminated with a zero-mean white Gaussian noise of variance

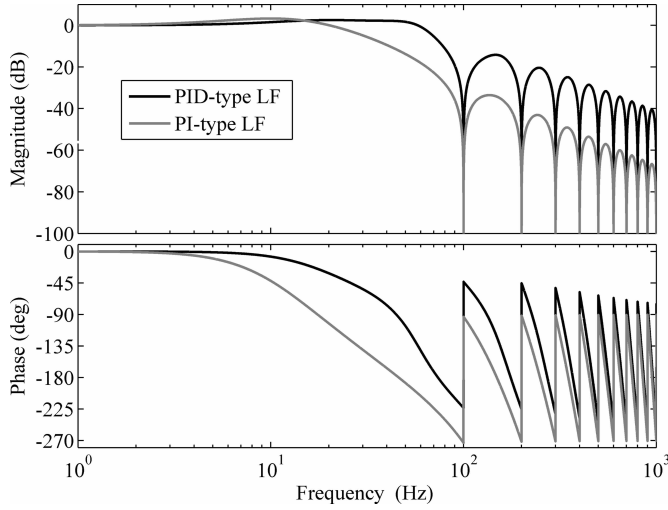


Fig. 24. Closed-loop Bode plots of the MA-PLL.

$\sigma^2 = 0.05$. This corresponds to a signal-to-noise-ratio (SNR) of $SNR = 10 \log\left(\frac{1}{2\sigma^2}\right) = 10 \text{ dB}$. The noisy waveform is sampled as a rate of 100 kHz, and is then fed to a digital anti-aliasing filter. This high sampling rate is to avoid the aliasing effects [49]. Here, the anti-aliasing filter is made by three digital first-order LPFs with the cutoff frequency of $2\pi 4000 \text{ rad/s}$. The outputs of anti-aliasing filter are then downsampled to 10 kHz to perform the PLL algorithm. Throughout this study, the grid voltage frequency is fixed at its nominal value.

Fig. 25 shows the simulation results in this condition. The description of plots are as follows. Fig. 25(a) shows the noise-contaminated three-phase input signals (SNR=10 dB). Fig. 25(b) shows the output signals of the anti-aliasing filter. The SNR at the output of anti-aliasing filter is numerically calculated, which is about 19 dB. Figs. 25(c) and (d) show the three-phase output signals of the MA-PLL when using the PI-type and PID-type LFs, respectively. The SNR is about 44 dB when using the PI-type LF, while it is about 40 dB for the case of using the PID-type LF. Thus, as expected, the PI-type LF results in a higher degree of noise immunity. The estimated frequencies by the MA-PLL using the PI-type LF (gray line) and PID-type LF (black line) are shown in Fig. 25(e). These plots more clearly show the higher noise immunity of MA-PLL when using the PI-type LF.

VI. CONCLUSION

The main objective of this paper was to present control design guidelines for a typical MAF-based PLL. We started the study with a general description of the MAFs, followed by their discrete-time realization. The practical challenge associated with the MAFs, which is their frequency-dependent attenuation characteristics, was then briefly discussed. Online adjustment of the sampling frequency, online adjustment of the MAF's order, using the mean value method, using the weighted mean value method, and using the interpolation techniques were mentioned as the possible solutions to overcome this challenge. To provide a guideline for selecting the appropriate method for a given application, a comparison

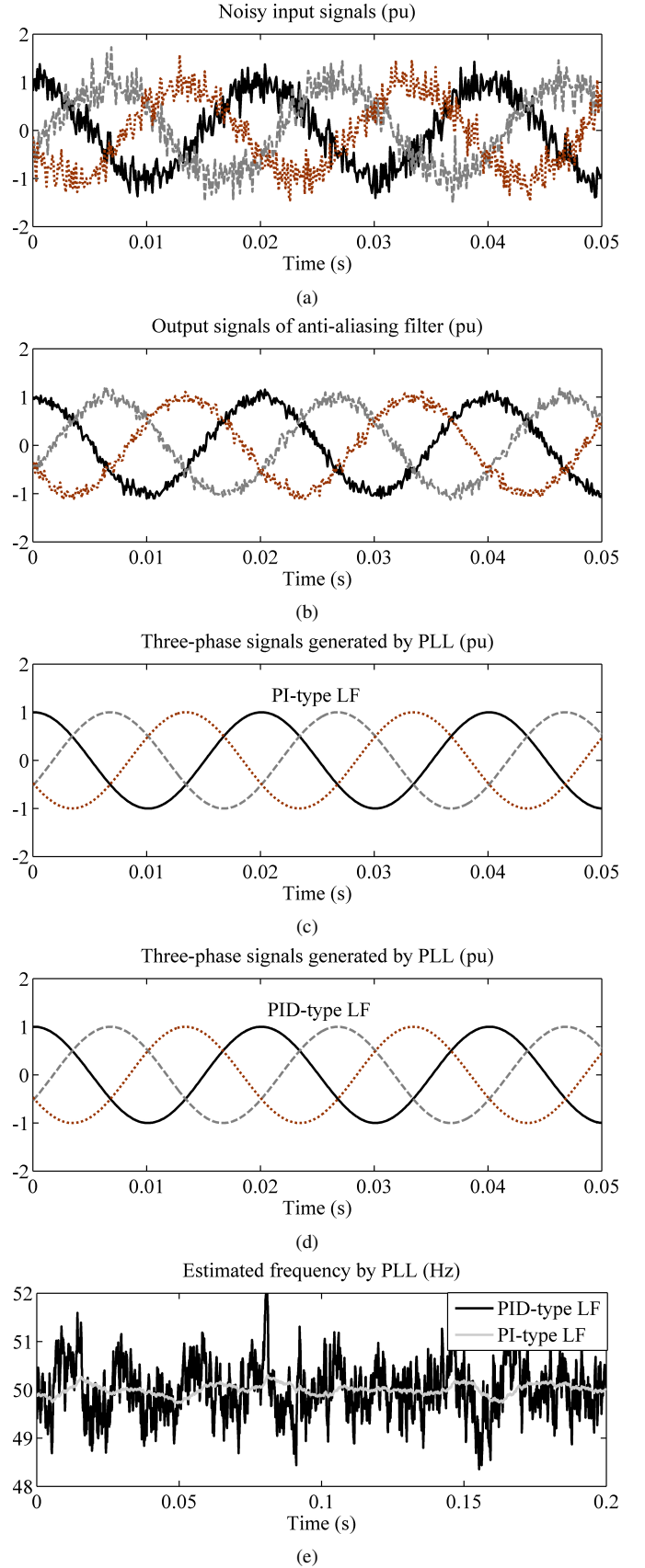


Fig. 25. Simulations results when the input signal is contaminated with a zero mean white Gaussian noise of variance 0.05.

among these solutions was also carried out. An overview of the different MAF-based PLL was then given in the paper. Two systematic methods to design the control parameters of a typical MAF-based PLL were then presented: one for the case of using a PI-type LF in the PLL, and the other for the case of using a PID-type LF. Finally, the paper compared the performance of a well-tuned MAF-based PLL when using the PI-type LF with the result of using the PID-type LF. It was shown that the PID-type LF can provide a higher bandwidth (a faster dynamic response) than that achievable by the PI-type LF, but at the cost of reduced noise immunity and disturbance-rejection capability.

REFERENCES

- [1] M. Karimi-Ghartemani, and M. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," *IEEE Trans. Power Syst.*, vol. 19, no. 3, pp. 1263-1270, Aug. 2004.
- [2] M. Boyra, and J. L. Thomas, "A review on synchronization methods for grid-connected three-phase VSC under unbalanced and distorted conditions," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Birmingham, U.K., Aug. 2011, pp. 1-10.
- [3] J. Svensson, "Synchronisation methods for grid-connected voltage source converters," *Proc. Inst. Electr. Eng. Gener. Transm. Distrib.*, vol. 148, no. 3, pp. 229-235, May 2001.
- [4] V. M. Moreno, M. Liserre, A. Pigazo, and A. Dell'Aquila, "A comparative analysis of real-time algorithms for power signal decomposition in multiple synchronous reference frames," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1280-1289, Jul. 2007.
- [5] H. S. Song, and K. Nam, "Instantaneous phase-angle estimation algorithm under unbalanced voltage-sag conditions," *Proc. Inst. Electr. Eng. Gener. Transm. Distrib.*, vol. 147, no. 6, pp. 409-415, Nov. 2000.
- [6] H. S. Song, K. Nam, and P. Mutschler, "Very fast phase angle estimation algorithm for single-phase system having sudden phase angle jumps," in *Proc. IEEE Ind. Applicat. Soc. 37th Annu. Meeting*, Oct. 2002, pp. 925-931.
- [7] Y. F. Wang, and Y. W. Li, "A grid fundamental and harmonic component detection method for single-phase systems," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2204-2213, Jul. 2013.
- [8] E. Robles, J. Pou, S. Ceballos, J. Zaragoza, J. L. Martin, and P. Ibanez, "Frequency-adaptive stationary-reference-frame grid voltage sequence detector for distributed generation systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4275-4286, Sep. 2011.
- [9] M. Boyra, "Power-flow control and power-quality enhancement in interconnected distribution networks," Ph.D. dissertation, Supélec, France, Oct. 2012.
- [10] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2167-2177, Jun. 2013.
- [11] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Advantages and challenges of a type-3 PLL," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4985-4997, Nov. 2013.
- [12] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923-2932, Aug. 2008.
- [13] Y. F. Wang, and Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1987-1997, Jul. 2011.
- [14] F. Cupertino, E. Lavopa, P. Zanchetta, M. Sumner, and L. Salvatore, "Running DFT-based PLL algorithm for frequency, phase and amplitude tracking in aircraft electrical systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 3, pp. 1027-1035, Mar. 2011.
- [15] M. Karimi-Ghartemani, M. Mojiri, A. Safaei, J. A. Walth, S. A. Khajehoddin, P. Jain, and A. Bakhshai, "A new phase-locked loop system for three-phase applications," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1208-1218, Mar. 2013.
- [16] A. V. Timbus, R. Teodorescu, F. Blaabjerg, M. Liserre, and P. Rodriguez, "PLL algorithm for power generation systems robust to grid voltage faults," in *Proc. 37th IEEE PESC*, Jeju, Korea, Jun. 2006, pp. 1-7.
- [17] M. Rashed, C. Klumpner, and G. Asher, "Repetitive and resonant control for a single-phase grid-connected hybrid cascaded multilevel converter," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2224-2234, May 2013.
- [18] F. A. S. Neves, H. E. P. de Souza, M. C. Cavalcanti, F. Bradaschia, and E. Bueno, "Digital filters for fast harmonic sequence components separation of unbalanced and distorted three-phase signals," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3847-3859, Oct. 2012.
- [19] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1194-1204, Apr. 2011.
- [20] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 765-778, Feb. 2013.
- [21] F. Gonzalez-Espin, E. Figueres, and G. Garcera, "An adaptive synchronous-reference-frame phase-locked loop for power quality improvement in a polluted utility grid," *IEEE Trans. Ind. Electron.*, vol. 59, no. 6, pp. 2718-2731, Jun. 2012.
- [22] P. Xiao, K. A. Corzine, and G. K. Venayagamoorthy, "Multiple reference frame-based control of three-phase PWM boost rectifiers under unbalanced and distorted input conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2006-2017, Jul. 2008.
- [23] F. D. Freijedo, A. G. Yepes, O. Lopez, A. Vidal, and J. Doval-Gandoy, "Three-phase PLLs with fast postfault tracking and steady-state rejection of voltage unbalance and harmonics by means of lead compensation," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 85-97, Jan. 2011.
- [24] E. Robles, S. Ceballos, J. Pou, J. L. Martin, J. Zaragoza, and P. Ibanez, "Variable-frequency grid-sequence detector based on a quasi-ideal low-pass filter stage and a phase-locked loop," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2552-2563, Oct. 2010.
- [25] P. Sumathi, and P. A. Janakiraman, "Integrated phase-locking scheme for SDF-based harmonic analysis of periodic signals," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 1, pp. 51-55, Jan. 2008.
- [26] M. A. Perez, J. R. Espinoza, L. A. Moran, M. A. Torres, and E. A. Araya, "A robust phase-locked loop algorithm to synchronize static-power converters with polluted AC systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2185-2192, May 2008.
- [27] I. Carugati, S. Maestri, P. G. Donato, D. Carrica, and M. Benedetti, "Variable sampling period filter PLL for distorted three-phase systems," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 321-330, Jan. 2012.
- [28] I. Carugati, P. Donato, S. Maestri, D. Carrica, and M. Benedetti, "Frequency adaptive PLL for polluted single-phase grids," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2396-2404, May 2012.
- [29] J. Rothen, J. Espinoza, F. Villarroel, M. Perez, J. Munoz, P. Melin, and E. Espinosa, "Static power converter synchronization and control under varying frequency conditions," in *39th IEEE Annual Conference of Industrial Electronics, IECON, 2012*, pp. 786-791.
- [30] L. Wang, Q. Jiang, L. Hong, C. Zhang, and Y. Wei, "A novel phase-locked loop based on frequency detector and initial phase angle detector," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4538-4549, Oct. 2013.
- [31] A. Ghoshal, and V. John, "A method to improve PLL performance under abnormal grid conditions," in *Proc. NPEC, Bangalore, India*, Dec. 2007.
- [32] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of phase-locked loops for power converters under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2039-2047, Dec. 2009.
- [33] N. Ama, F. Martinez, L. Matakas, Jr, and F. Junior, "Phase locked loop based on selective harmonics elimination for utility applications," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 144-153, Jan. 2013.
- [34] L. Liu, H. Li, Z. Wu, and Y. Zhou, "A cascaded photovoltaic system integrating segmented energy storages with self-regulating power allocation control and wide range reactive power compensation," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3545-3559, Dec. 2011.
- [35] L. Shi, and M. L. Crow, "A novel phase-locked-loop and its application in STATCOM system," in *Proc. North American Power Symposium, 2010 (NAPS '10)*, pp. 1-5.
- [36] M. Karimi-Ghartemani, S. A. Khajehoddin, P. K. Jain, and A. Bakhshai, "Derivation and design of in-loop filters in phase-locked loop systems," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 4, pp. 930-940, Apr. 2012.
- [37] F. P. Marafao, S. M. Deckmann, and E. K. Luna, "A novel frequency and positive sequence detector for utility applications and power quality analysis," in *proc. ICREPQ'04 conf.*, Barcelona, Spain, Apr. 2004.
- [38] M. S. Padua, S. M. Deckmann, and F. P. Marafao, "Frequency-adjustable positive sequence detector for power conditioning applications," in *Proc. IEEE Power Electron. Spec. Conf.*, 2005, pp. 1928-1934.

- [39] A. Nicastrì, and A. Nagliero, "Comparison and evaluation of the PLL techniques for the design of the grid-connected inverter systems," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 2010, pp. 3865-3870.
- [40] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "A generic open-loop algorithm for three-phase grid voltage/current synchronization with particular reference to phase, frequency, and amplitude estimation," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 94-107, Jan. 2009.
- [41] J. Svensson, M. Bongiorno, and A. Sannino, "Practical implementation of delayed signal cancellation method for phase-sequence separation," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 18-26, Jan. 2007.
- [42] D. Jovcic, "Phase locked loop system for FACTS," *IEEE Trans. Power Syst.*, vol. 18, no. 3, pp. 1116-1124, Aug. 2003.
- [43] A. M. Salamah, S. J. Finney, and B. W. Williams, "Three-phase phase-locked loop for distorted utilities," *IET Electr. Power Appl.*, vol. 1, no. 6, pp. 937-945, Nov. 2007.
- [44] W. Leonard, *Control of Electrical Drives*. Berlin, Germany: Springer-Verlag, 1990.
- [45] K. Shu and E. Sanchez-Sinencio, *CMOS PLL Synthesizers-Analysis and Design*. New York: Springer-Verlag, 2005.
- [46] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 58-63, Jan. 1997.
- [47] S. Golestan, M. Monfared, F. D. Freijedo, J. M. Guerrero, "Design and tuning of a modified power-based PLL for single-phase grid connected power conditioning systems," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3639-3650, Aug. 2012.
- [48] M. Karimi-Ghartemani, and H. Karimi, "Processing of symmetrical components in time-domain," *IEEE Trans. Power Syst.*, vol. 22, no. 2, pp. 572-579, 2007.
- [49] M. Karimi-Ghartemani, "A novel three-phase magnitude-phase-locked loop system," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 53, no. 8, pp. 1792-1802, Aug. 2006.



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