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Valve-side Single-phase-to-ground Fault Analysis in Bipolar MMC-HVDC Systems with Hybrid SMs

Pingyang Sun, *Student Member, IEEE*, Gen Li*, *Senior Member, IEEE*, Hongyi Wang, *Student Member, IEEE*, Jun Liang, *Fellow, IEEE*, Georgios Konstantinou, *Senior Member, IEEE*

Abstract—This letter presents a comprehensive fault analysis for a modular multilevel converter high-voltage direct current (MMC-HVDC) system with hybrid half-bridge submodules (HBSMs) and full-bridge SMs (FBSMs) under valve-side single-phase-to-ground (SPG) faults. The analysis shows protection for upper arms is necessary due to the inevitable upper arm overvoltage. It further specifies that the proportion of FBSMs utilized in each arm should be at least 86.6% of the available voltage to safely clear valve-side SPG faults without overvoltage in the lower arms. The accuracy of the theoretical analysis is validated in the positive pole of a bipolar MMC-HVDC system with different ratios of FBSMs modelled in PSCAD/EMTDC.

Index Terms—Valve-side ac fault, single-phase fault, hybrid SMs, HVDC, MMC.

I. INTRODUCTION

MODULAR multilevel converter-based high-voltage direct current (MMC-HVDC) systems are now commonplace in modern power systems, such as the renewable energy integration and offshore power transmission [1]. The valve-side single-phase-to-ground (SPG) faults are frequently occurred in bipolar MMC-HVDC systems, raising two possible problems: 1) the grid-side non-zero-crossing currents, and 2) the continuous charging of submodule (SM) capacitors [2]. In this case, the grid-side ac circuit-breakers (ACCBs) may encounter challenges in interrupting non-zero-crossing currents, while continuous SM charging can result in severe arm overvoltage, threatening SM capacitors and MMC insulations [3].

The issue of non-zero-crossing grid currents presents in the MMC with half-bridge SMs (HBSMs). The reason of this phenomenon is that lower-arm currents unidirectionally flow from the converter dc-side grounding point, through lower-arm diodes, to the ac-side. This issue can be addressed by using an LR dc grounding circuit to dampen the dc offset currents and therefore, create grid-side current zero-crossings [3]. However, a large reactance is required to ensure uninterrupted zero-crossings.

Adopting bipolar SMs such as full-bridge SMs (FBSMs) is another solution by utilizing their capacitor voltage to suppress the fault currents at the cost of using more devices [4]. Thyristor-pairs and damping SMs embedded in lower arms can block fault currents, while additional conduction losses are induced during normal operation [5]. Moreover, grid-side zero-crossing currents can also be created by triggering the antiparallel thyristors in parallel with the lower arms [6]. However, the upper arm overvoltage is not solved.

The upper arm overvoltage can be addressed through arm current transfer [7], [8] or blocking [5]. A thyristor branch at the dc-side [8] or antiparallel thyristors in parallel with the upper arms [7] are two available methods to avoid SM

overvoltage by transferring the fault currents into thyristors. The current flows can be interrupted by switching off the thyristor-pairs in series with the upper arms following valve-side SPG faults [5].

The hybrid MMC with FBSMs in lower arms and HBSMs in upper arms has been discussed in [9] to address the grid-side non-zero-crossing problem. The upper-arm overvoltage problem remains challenging. The valve-side SPG fault behavior of the MMC with hybrid HBSMs and FBSMs in each arm has not been unveiled in the existing literature, yet. Compared to FB-MMC, such hybrid MMC can reduce the capital cost without compromising the dc fault self-clearing capability [10]. Although the required number of FBSMs for handling dc faults has been investigated [11], *valve-side SPG faults result in distinct fault behavior which necessitates a reassessment of the necessary number of FBSMs in each arm.*

In this letter, the fault characteristics of bipolar MMC-HVDC systems with hybrid SMs are analyzed under valve-side SPG faults. Moreover, the minimum ratio of FBSMs in each arm is calculated to prevent lower-arm overvoltage following the valve-side SPG faults. The theoretical analysis demonstrates that 1) the upper arm overvoltage is serious and ever-present for any ratios of FBSMs in each arm; 2) the FBSM overvoltage in the lower arms is extremely severe for a low ratio of FBSMs; and 3) the current FBSM ratio determination method regarding dc fault clearing is inadequate for addressing valve-side SPG faults. Therefore, it is required to implement protection for the upper arms, which has been extensively explored in the current literature [5], [7], [8]. In addition, the ratio of FBSMs in each arm should be at least 86.6% of the available voltage for safely clearing the valve-side SPG faults with no lower-arm overvoltage.

II. FAULT CHARACTERISTIC ANALYSIS

A. Upper Arms

Fig. 1 shows the positive pole circuit of a bipolar hybrid MMC with HBSMs and FBSMs in each arm. The widely used star/delta transformer connection is considered in this work to block zero-sequence currents on the valve side, thereby eliminating third harmonics [12]. As the SPG fault occurs at the terminal of the MMC, large fault currents will flow through the IGBTs, hence all SMs will be immediately blocked to protect the devices, as shown in Fig. 2(a). The following analysis is based on that the lower arms will not conduct after the fault, which will be analyzed in the next section. Then, the voltages of all SMs in the upper arms (u_{upx}) can be expressed as:

$$u_{upx} = V_{dc} - L \cdot \frac{di_{upx}}{dt} - R \cdot i_{upx} - u'_x \quad (x = a, b, c), \quad (1)$$

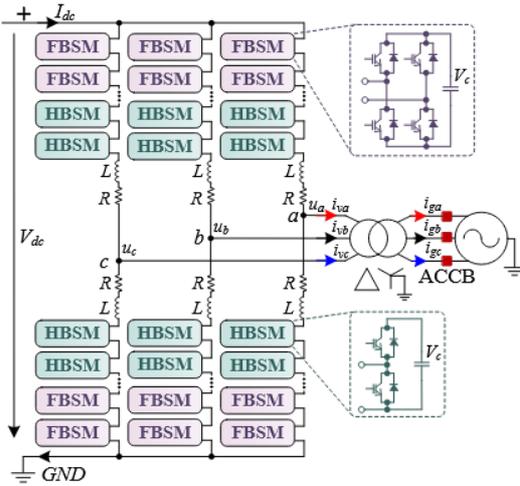


Fig. 1. Circuit diagram of a three-phase MMC with hybrid SMs in each arm.

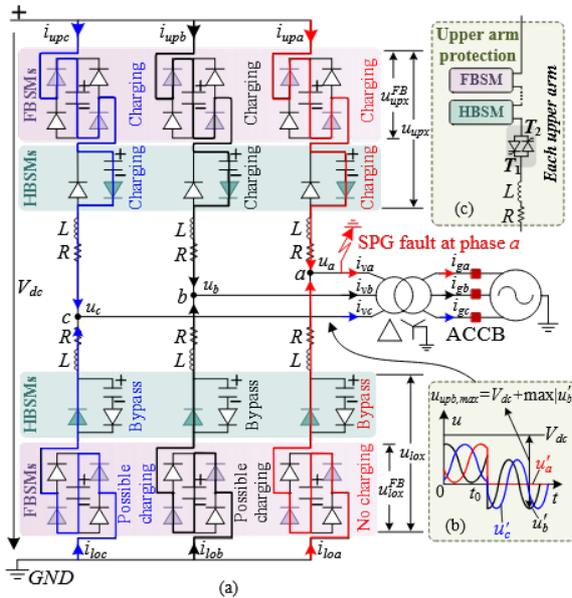


Fig. 2. Post-fault circuit of a blocked MMC with hybrid SMs: (a) equivalent circuit, (b) post-fault valve-side ac phase voltage, and (c) antiparallel thyristor-based upper-arm protection scheme.

where V_{dc} is the dc-link voltage, L is the arm inductor, R is the arm resistor, i_{upx} is the upper arm currents, and u'_x refers to the post-fault valve-side ac phase voltages. For the faulted phase (e.g. phase a , $u'_a = 0$), the maximum upper arm voltage after blocking is:

$$u_{upa,max} = V_{dc} + \Delta V_{dc}, \quad \text{when } i_{upa} = 0, \quad (2)$$

where ΔV_{dc} indicates the transient dc voltage deviation after blocking. In the non-faulted phases (e.g. phase b), both HBSMs and FBSMs in the upper arms will be charged during the negative half-cycles of the post-fault ac voltages [3], hence the maximum upper-arm voltage can reach [7]:

$$u_{upb,max} = V_{dc} + \max |u'_b| + \Delta V_{dc} = V_{dc} + \sqrt{3} \times \sqrt{2} U_b + \Delta V_{dc}, \quad (3)$$

where $U_b = mV_{dc}/(2\sqrt{2})$ refers to the pre-fault ac phase voltage at the valve side [Fig. 2(b)], and m is the modulation

index. If $m = 0.85$, $u_{upb,max}$ will be increased to $1.74V_{dc}$ assuming $\Delta V_{dc} = 0$. This result demonstrates that the SM capacitors in the upper arms of the two healthy phases will experience significant overvoltage.

It should be noted that the dc voltage will gradually increase if the SPG fault occurs at the dc voltage-controlled MMC, functioning as inverter station [7]. The increase is attributed to the consistent power delivery from the power controlled-MMC, resulting in a rapid increase of dc voltage. Therefore, eq. (3) can be finally rewritten as:

$$u_{upb,max} = (1 + 0.866m)V_{dc} + \Delta V_{dc}, \quad (4)$$

Eq. (4) shows $u_{upb,max} > 1.74V_{dc}$ when $m = 0.85$. It can be concluded that protection of the upper arms is essential for the MMC with hybrid SMs, and the use of antiparallel thyristors in series with upper arms is an effective scheme to address the issue as shown in Fig. 2(c) [5].

B. Lower Arms

Using a certain number of FBSMs can address the non-zero-crossing grid-side currents by utilizing capacitor voltages to prevent currents from flowing through the lower arms [8]. The ratio of FBSMs within the arms significantly affects the overvoltage level in the lower arms, although the number of FBSMs in upper arms has no impact on the SM capacitor charging loop.

The current method for determining the required number of FBSMs in each arm only relies on dc fault analysis, ensuring that the used number of FBSMs is sufficient to completely extinguish the dc fault current. As the dc fault current flows into both lower and upper arms, the required minimum number of FBSMs for dc fault protection is (taking the loop from phase a to phase b as an example) [11]:

$$\mathcal{N}_{FB,critical}^{DCF} = \frac{U_{ab}}{2V_c} = \frac{\sqrt{3} \times \sqrt{2} U_b}{2V_c} = 0.433mN_T, \quad (5)$$

where U_{ab} refers to the line voltage between phases a and b , V_c is the average value of capacitor voltage, and N_T is the total number of SMs in each arm.

Nevertheless, the required number of FBSMs should be re-evaluated to avoid possible lower-arm overvoltage subject to a valve-side SPG fault. According to the fault current paths in the lower arms after SM blocking [Fig. 2(a)], there is a potential capacitor charging path within FBSMs for each nonfaulted phase if the number of FBSMs is lower than a critical value. This value is determined by:

$$\mathcal{N}_{FB,critical}^{SPG} = \frac{\max |u'_b|}{V_c} = \frac{\sqrt{3} \times \sqrt{2} U_b}{V_c} = 0.866mN_T, \quad (6)$$

so that the total capacitor voltage of all FBSMs is equal to the post-fault valve-side ac phase voltage. Therefore, the maximum voltages across all the FBSMs in the lower arms ($u_{lox,max}^{FB}$) after blocking are:

$$u_{loa,max}^{FB} = \mathcal{N}_{FB} V_c \quad \text{for faulted phase } a, \quad \text{and} \quad (7)$$

$$\begin{cases} u_{lob,max}^{FB} = \mathcal{N}_{FB} V_c, & \mathcal{N}_{FB} \geq \mathcal{N}_{FB,critical}^{SPG} \\ u_{lob,max}^{FB} = \max |u'_b| = \mathcal{N}_{FB}(V_c + \Delta V_c), & \mathcal{N}_{FB} < \mathcal{N}_{FB,critical}^{SPG} \end{cases} \quad (8)$$

for non-faulted phase b , where ΔV_c is the capacitor voltage increment in each FBSM. If $\mathcal{N}_{FB} = \mathcal{N}_{FB,critical}^{DCF}$, the capacitor

TABLE I
RATIO OF FBSMS IN EACH ARM.

Ratios	DC fault ¹	valve-side SPG fault ²
$\mathcal{N}_{FB} < 43.3\%m$	✗	✗
$43.3\%m \leq \mathcal{N}_{FB} < 86.6\%m$	✓	✗
$\mathcal{N}_{FB} \geq 86.6\%m$	✓	✓

¹: dc fault current interruption under dc faults.
²: no lower arm overvoltage under valve-side SPG faults.

voltage in each FBSM will increase to $2V_c$ due to $\Delta V_c = V_c$ exhibiting substantial lower-arm overvoltage. Thus, the number of FBSMs in each arm should be at least $0.866mN_T$ ($\mathcal{N}_{FB}/N_T = 73.6\%$ for $m = 0.85$), considering the impact of valve-side SPG faults. Table I summarizes the required FBSM ratio under dc and valve-side SPG faults.

III. CASE STUDIES

The positive pole of a bipolar hybrid MMC-HVDC link is implemented in PSCAD/EMTDC, as shown in Fig. 3. The MMC parameters are listed in Table II. A valve-side SPG fault (phase a) occurs at 1 s with a 0.001Ω grounding resistance in V_{dc}/Q controlled MMC2 at the inverter side, to mimic the most serious overvoltage in the upper arms. Three cases are studied to show the fault behavior under different ratios of FBSMs, including: 1) 15 FBSMs ($43.3\%mN_T$), which is a critical value to extinguish dc fault current; 2) 24 FBSMs ($70\%mN_T$), which is between $\mathcal{N}_{FB,critical}^{DCF}$ and $\mathcal{N}_{FB,critical}^{SPG}$; 3) 30 FBSMs ($86.6\%mN_T$), which is a critical value to avoid lower-arm overvoltage.

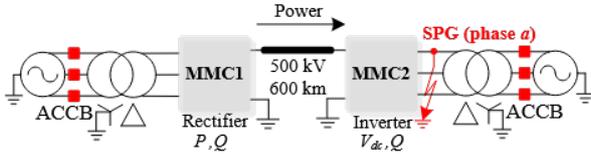


Fig. 3. MMC-based monopole HVDC system with hybrid SMs.

TABLE II
PARAMETERS OF THE MMC-HVDC SYSTEM WITH HYBRID SMs.

Parameters	Values	Parameters	Values
MMC capacity (MW)	1500	Modulation index m	0.85
Rated dc voltage (kV)	500	Arm inductance (H)	0.04
Transf. ratio (kV/kV)	230/260	Arm resistance (Ω)	0.1
Transf. leakage reactance (p.u.)	0.15	AC system resistance (Ω)	0.35092
Number of SMs in each arm N_T	40	AC system reactor (H)	0.01117
SM capacitance (mF)	2.5	Length of OHL (km)	600

All SMs in MMC2 are blocked if any arm current exceeds 4.5 kA. However, power can still be transmitted from the unblocked MMC1 (assuming a 5 ms communication delay), resulting in the rapid dc voltage increase under all cases. This, in turn, contributes to the increase of the upper arm voltage for all the three cases as shown in Fig. 4. The lower arm voltage also increases if the number of FBSMs is less than 30 ($86.6\%mN_T$), based on (6). Although the lower-arm overvoltage can be partially alleviated by increasing the dc grounding impedance (Fig. 5), it induces additional power losses in steady-state operation, which is not desirable in MMC-HVDC systems.

In all three cases, it is necessary to adopt an appropriate protection scheme, and antiparallel thyristors with suitable I^2t

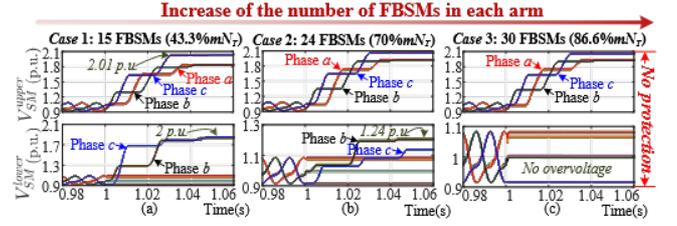


Fig. 4. MMCs without protection under a valve-side SPG fault: (a) case 1, (b) case 2 and (c) case 3.

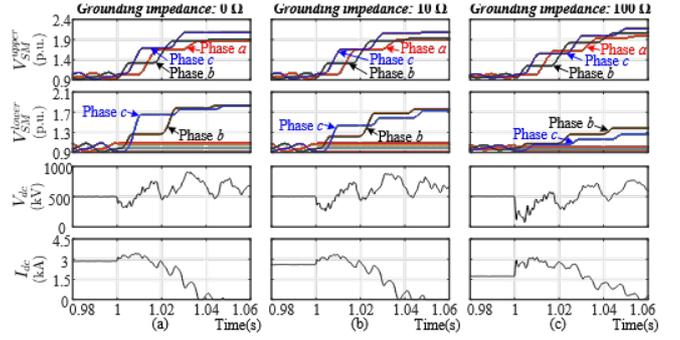


Fig. 5. Fault responses under a valve-side SPG fault for case 1 with different dc grounding impedance: (a) 0Ω , (b) 10Ω and (c) 100Ω .

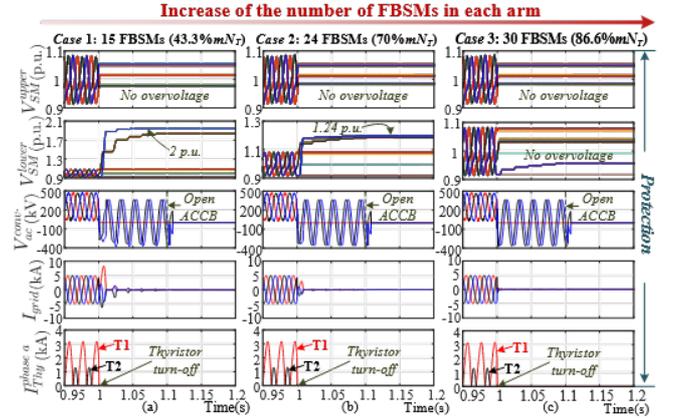


Fig. 6. MMCs with protection under a valve-side SPG fault: (a) case 1, (b) case 2 and (c) case 3.

capacity are used in the upper arms [Fig. 2(c)], to address the issue of upper arm overvoltage. All thyristors are turned off during the discontinuous conduction period of upper arm currents after SM blocking [5]. Moreover, an additional 0.1 s delay is used to emulate the operating time of the grid-side ACCB. Fig. 6 shows the upper arm overvoltage is solved after the adoption of the protection, and the lower-arm overvoltage is not presented when the FBSM ratio is increased to 73.6% ($86.6\%m$).

IV. CONCLUSION

This letter evidences 1) the upper-arm voltage can only be addressed by external protection schemes in a bipolar MMC-HVDC system with hybrid HBSMs & FBSMs following valve-side SPG faults; 2) $86.6\%m$ (m refers to the modulation

index) of the FBSMs in each arm can mitigate the lower-arm overvoltage issue. Moreover, the MMC with HBSMs and FBSM represents two special cases that the ratio of FBSMs is 0 and 1 in each arm, respectively. Simulations conducted in PSCAD/EMTDC through three cases with different FBSM ratios effectively showcase the accuracy of the theory analyses. It should be mentioned that the ratio higher than 86.6% can not only address the lower arm overvoltage issue under valve-side SPG faults, it can also achieve the dc side fault blocking.

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