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Published in:
Proceedings of the 12th Wind Integration Workshop

Publication date:
2013

Document Version
Accepted author manuscript, peer reviewed version

An Assessment of Converter Modelling Needs for Offshore Wind Power Plants Connected via VSC-HVDC Networks

Jakob Glasdam, Lorenzo Zeni, Jesper Hjerrild,
Łukasz Kocewiak, Bo Hesselbaek
Wind Power, Electrical Systems
DONG Energy
Fredericia, Denmark
jakgl@dongenergy.dk

Poul E. Sørensen, Anca D. Hansen
Dept. of Wind Energy
Technical University of Denmark
Lyngby, Denmark

Claus L. Bak, Philip C. Kjær
Dept. Energy Technology
Aalborg University
Aalborg, Denmark

***Abstract*—Modular multilevel cascaded converter (MMCC) based high voltage direct current (HVDC) transmission is technically superior to other technologies, especially in case of connection of offshore wind power plants (OWPPs). Modelling challenges are faced by OWPP developers, who are not acquainted with detailed information regarding the internal behaviour of such complex devices.**

This paper presents an investigation of the modelling requirements of the MMCC HVDC system, based on comparison between simulation results using a detailed HVDC representation in PSCAD/EMTDC and two less detailed models realised in EMT and RMS environments in DIgSILENT PowerFactory, respectively.

The results show that the simplified EMT/RMS models can be trusted for slow dynamic studies like those related to power control considered in this work. The results obtained from the detailed EMT model highlights the necessity for voltage balancing of the distributed capacitor voltages in the MMCC for both steady state operating conditions and during dynamic events such as step changes in the reference signals.

Keywords: HVDC, wind power integration and control, PSCAD/EMTDC, DigSILENT PowerFactory

I. INTRODUCTION

The uprising deployment of voltage sourced converter (VSC) based HVDC technology for bulk power exchange and, especially, for the connection of large OWPPs pushes the market players, namely wind turbine manufacturers, HVDC suppliers, OWPP developers and operators and transmission system operators (TSOs), towards an evaluation of the modelling needs for the complex HVDC converters and their utilisation in simulation studies of diverse nature. Moreover, the current outlook is that a massive utilisation of HVDC will possibly lead to the birth of a very large DC grid, provided that a number of challenges are overcome [1-2].

Hence, studies involving all relevant power electronic devices (PEDs) and their controllers will be needed and the modelling approach must look for a right compromise between accuracy and computational speed. Furthermore, from an OWPP developer and TSO perspective, details regarding the internal behaviour of HVDC converters are often unknown or only partially known, and it is therefore crucial to get confidence on the validity of less detailed models that may offer satisfying accuracy in certain investigations.

When considering grid connection studies, detailed EMT based models are surely those offering the most accurate representation of the physical system, but might indeed become excessively heavy for simulations of large systems, especially when the converter is an MMCC. Novel solutions have been devised for a more efficient modelling of the HVDC MMCC without loss of accuracy [3]. Others have proposed the use of averaged (switched [4] or non-switched [5-6]) models and demonstrated their usability for certain kinds of studies, such as slow dynamics during normal operation and faults on the AC side. On the other hand, their limitations have been shown, for example for faults on the DC side or for studies regarding the internal dynamics (e.g. variation in the distributed DC link voltages - see Section II for MMCC HVDC description -, etc…). As can be seen, a common effort is being made in the research world in order to create awareness upon the level of accuracy and efficiency of the various models [7-8].

From an OWPP developer and TSO perspective, it is however important to assess the validity of models that are readily available in commercial simulation tools, in particular those that are based on root-mean-square (RMS), approach, suitable for stability and several grid compliance studies.

This paper finds room in the above pictured scenario and aims at providing a comparison between detailed EMT-

type models in PSCAD/EMTDC and corresponding EMT-type and RMS built-in models in DIgSILENT PowerFactory, focusing on suitable events that are usually considered in OWPP integration studies.

The remainder of this paper is organised as follows: Section II briefly introduces the MMCC technology, while Section III provides a description of the system under focus and illustrates detailed and simplified converter models and their controls. Section IV proceeds by showing simulation results, leading to the concluding remarks reported in Section V.

II. MMCC TECHNOLOGY

The MMCC technology was introduced for motor applications in [9],[10] and for reactive power compensation (as a static compensator (STATCOM)) [11]. [12] extended the MMCC technology to the HVDC, and is now considered state-of-the-art within the industry [13]. [13] presents a qualitative description of the commercially available MMCC based VSC-HVDC schemes. This paper will focus on the double star configuration with series connection of N number of half bridge sub-modules (SMs) in each phase arm as shown in Figure 1. By appropriate switching of the SMs, their respective capacitances are either connected in series or bypassed in order to achieve the desired waveform of the output voltage. The phase legs are connected in parallel on the DC side; hence the DC current (I_{DC}) will (under balanced conditions) be split equally between the three phase legs. The phase reactor is located in the phase arm due to multiple purposes; the reactor is placed in series in case of a DC fault, limiting the current rate of rise, protecting the insulated gate bipolar transistor (IGBT) in the SM. The phase current (I_{Acj}, $j=a,b,c$) splits evenly between the two phase arms, which halves the voltage drop across the reactor, compared to the case when the reactor is placed on the AC line side of the converter. Furthermore, the reactors will limit the balancing current that will flow between the phase legs, as the generated voltages of the three phase legs cannot be exactly equal [14],[15].

III. SYSTEM DESCRIPTION

A. Studied system

The VSC-HVDC system considered in this work is inspired by ABB's 4th generation HVDC Light, described in [16]. Only one converter terminal will be considered and the AC and DC sides are each represented by a Thevenin equivalent network, as shown in Figure 2. Stiff AC and DC voltage sources are used to represent the AC and DC networks, respectively.

A capacitor (C_p) is inserted in the mid-point of the arm reactor in Figure 2, which together with the reactor forms a filter with the purpose of reducing the alternating part of the circulating current [16], which mainly consist of a 2nd harmonic component.

Table I shows the electrical parameters of the studied system. The parameters will be described in the following.

The reactor resistance (R_r) and filter capacitance (C_p) have been adapted and calculated according to [17], respectively. C_p is calculated as (1), where ω_0 is the fundamental frequency in rad/s:

$$C_p = \frac{1}{8\varpi_o^2 L_r} \ [\mathrm{F}] \tag{1}$$

The energy stored in the SM capacitances (E_{tot}) is selected based on trade-off between arm voltage ripple requirement and capacitor size. The value of E_{tot} = 40 kJ/MVA is selected according to [16], giving a ripple in U_{sm} in the range of 10 %. The SM capacitance is calculated as (2):

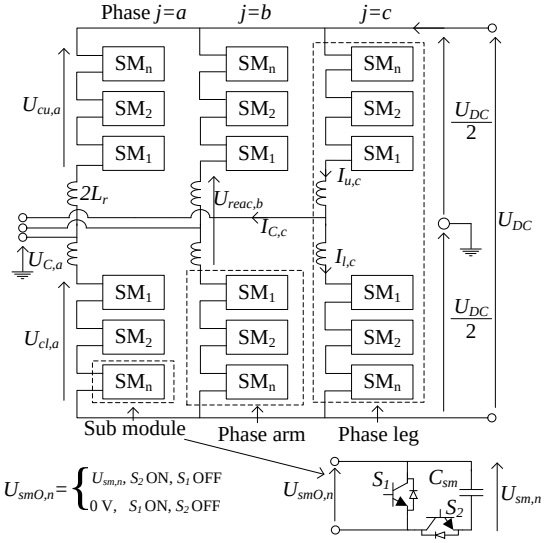


Figure 1 Simplified schematic of the three phase double star MMCC converter with *N* SMs per phase arm. The indicated current flow is for idealised conditions.

$$E_{tot} \cdot S_{VSC} = 6 \cdot N \cdot \tfrac{1}{2} \cdot C_{sm} \cdot U_{sm}^2 \ \rightarrow$$
$$C_{sm} = \frac{E_{tot} \cdot S_{VSC}}{3 \cdot N \cdot U_{sm}^2} = \frac{N \cdot E_{tot} \cdot S_{VSC}}{3 \cdot U_{DC}^2} \tag{2}$$

Where $U_{DC} = N \cdot U_{sm}$. Inserting the values from Table I into (2) yields C_{sm} = 1.5 mF.

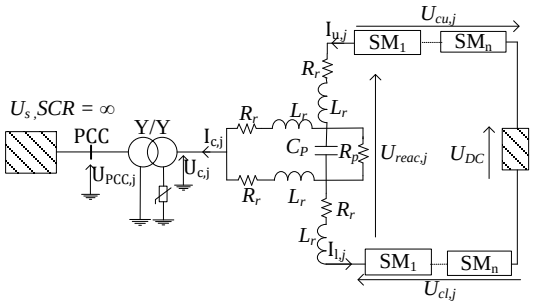


Figure 2 Single line diagram of one phase of the studied converter system.

B. Detailed MMCC model

In this work, "detailed MMCC model" refers to a representation of the double star MMCC in the simulation tool, where all the internal dynamics usually relevant for EMT studies (i.e. generated harmonic due to switching, individual SM capacitor charging etc.) are taken into account. Losses due to commutation process are not included.

The relatively high number of switching elements (IGBTs and diodes) in the MMCC VSC-HVDC poses some challenges in EMT programs (EMTPs) as a high

computational effort is required for re-triangularisation of the electrical network subsystem admittance. Based on the "Nested Fast and Simultaneous Solution" [18], an efficient and accurate representation of each of the phase arms of the MMCC VSC-HVDC was proposed in [3]. The large number of IGBT/diode pairs and distributed capacitances in the phase arm are collapsed into a single Norton equivalent. The number of frequently switched branches in the resulting network admittance matrix is thereby significantly reduced, while all branch currents and node voltages information is retained within the Norton equivalent and accessible to the main EMTP solver. The detailed model implemented in PSCAD/EMTDC in this work is based on a similar modelling approach and is therefore not described in further details.

Table 1 System electrical parameters.

	Parameter	Symbol	Value	Unit
AC Grid	Nominal voltage L-L	U_{PCC}	400	kV
	Short circuit ratio	SCR	∞	-
	Fundamental frequency	f_0	50	Hz
DC grid	Nominal voltage	$U_{dc}/2$	±320	kV
VSC Converter	Rated power	S_{VSC}	1216	MVA
	SM cascade number	N	38	-
	SM rated voltage	$U_{sm,r}$	16.84	kV
	Energy stored in SM capacitors per MVA	E_{tot}	40	kJ/MVA
	SM switching frequency	f_{sw}	3.37*f_0	Hz
	Total reactor inductance	L_r	75 (0.16 PU)	mH
	Reactor resistance	R_r	50	mΩ
	Reactor filter capacitance	C_p	17	μF
	Reactor filter resistance	R_p	50	MΩ
VSC Transformer	Rated power	S_{trf}	1290	MVA
	Short circuit voltage	U_k	12	%

C. Simplified EMT and RMS converter model

The simplified model considered in this paper is based, at the AC side, on an equivalent controlled voltage source behind a phase reactor L_{ph}, the value of which is given by:

$$L_{ph} = L_r \tag{3}$$

On the DC side, an equivalent capacitance must be defined which, following what stated in [19], can be computed as (4):

$$C_{eq} = 6 \cdot C_{sm} / N \tag{4}$$

Inserting the values from Table I and (2) into (4) yields C_{eq} = 238 μF. When employing a stiff voltage source on the DC side as done in this work, the value of C_{eq} is however irrelevant.

A circuital representation of the simplified model is shown in Figure 3, which is valid for both EMT and RMS environments. L_k represents the transformer short circuit inductance derived from U_k (see Table 1). The equivalent inductance between the converter and the point of common coupling (PCC) is therefore (5):

$$L_{eq} = L_{ph} + L_k \tag{5}$$

The modelling approach is identical to the standard representation of two-level converters in DIgSILENT PowerFactory, neglecting their switching nature and representing them as controlled voltage sources [20]. The validity of such approach should be even greater in MMCC applications, from an external grid perspective. On the other hand, all the very complex internal dynamics, and related control loops, of MMCCs are neglected.

The RMS model, as well-known, differs from the EMT in that the electrical quantities are represented in the phasor domain (thus averaged over a fundamental frequency period) and the impedances are characterised by constant reactance instead of constant inductance/capacitance. The AC network equations therefore become algebraic and some of the dynamic characteristics are lost.

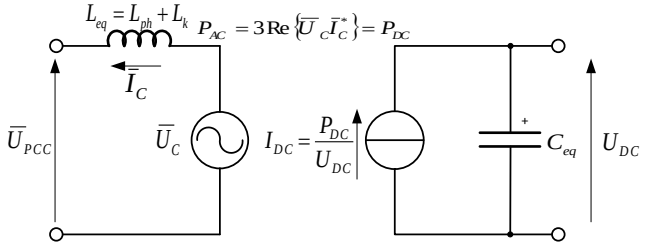


Figure 3 **Simplified EMT and RMS model of HVDC converter.**

D. Implemented control system

The control system in this work is divided into two levels:

- **Upper level**, which regulates the power transfer between the AC and DC sides. See following Subsection III.C.a)
- **Lower level**, responsible for controlling the internal dynamics of the converter, such as ensuring voltage balancing between the SMs. See subsection III.C.b)

The upper level control is identical in all three models considered in this work, whereas the lower level control is only implemented in the detailed EMT model.

a) Upper level control

Conventional cascaded control is employed in ABB's HVDC Light 4th Generation [16], with slower outer loop control responsible for determining the references for the fast inner current control (ICC) loop. The ICC operates in the synchronous reference frame (SRF), where a phase-locked loop (PLL) is used for synchronization between the natural reference frame and SRF.

As described in Section I, the paper compares the accuracy and modelling complexity of detailed EMT-type models in PSCAD/EMTDC and corresponding EMT-type and RMS built-in models in DIgSILENT PowerFactory, described in Section III-B and III-C, respectively. Therefore, only the ICC is considered, as it is expected that the slower outer loops will perform in a similar way, as long as there is an agreement between the performance of the ICCs from the two simulation tools.

The ICC makes use of conventional PIs working in the SRF, where the measured PCC voltage (U_{PCC}) is fed-forward together with cross-decoupling terms determined by the reactor voltage drop as in (6), which can be built

with measured or reference currents, depending on the application.

$$\begin{bmatrix} U_d^* \\ U_q^* \end{bmatrix} = \begin{bmatrix} U_{d,PCC} + i_q \varpi L_{eq} + K_1\left(\left[i_d^* - i_d\right] + 1/T_1 \int \left[i_d^* - i_d\right] dt\right) \\ U_{q,PCC} - i_d \varpi L_{eq} + K_1\left(\left[i_q^* - i_q\right] + 1/T_1 \int \left[i_q^* - i_q\right] dt\right) \end{bmatrix} \quad (6)$$

K_1 and T_1 in (6) are the proportional gain and integral time constant, respectively. $U_{d,PCC}$ and $U_{q,PCC}$ are the measured U_{PCC} transformed into the SRF using the angle θ_{PLL}, calculated by the PLL. Similarly, i_d and i_q are the measured converter output current i_c (see Figure 2) transformed into SRF. U_d* and U_q* are transformed back to phase components (i.e. U_j*, where j=a,b,c) and fed as reference to the converter bridge PWM modulator. Built-in PLLs have been used in the two tools.

Third harmonic injection is used, so the reference to the modulator is U_j*'= U_j*+ $U_{j,3\omega}$*/6. Figure 4 shows the implemented ICC, which is identical for the three models considered.

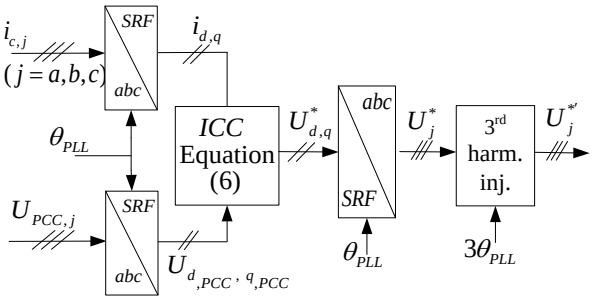


Figure 4 Implemented ICC.

b) Lower level control

Balancing of the SM voltages is needed in the detailed MMCC model, so as to ensure e.g. that the voltage of the n^{th} SM converges to $U_{sm,r}$. Phase shifted pulse width modulation (PWM) with a pulse number of 3.37 for each SM has been adapted from [16]. This is used as it has been shown that a non-integer value has a balancing effect on the SM capacitors [21]. Furthermore, active control is used for the balancing, which, with reference to [22], can be divided into two parts: Leg averaging and individual SM balancing.

- **Leg averaging,** ensures that the phase leg voltage coverges to U_{dc}.

The average SM voltage of the j^{th} phase leg (j=a,b,c) is (7):

$$U_{AV,j} = \tfrac{1}{2N} \sum_{n=1}^{2N} U_{sm,j,n} \quad (7)$$

where $U_{sm,j,n}$ is the voltage across the capacitor in the n^{th} SM in the j^{th} phase leg. The following DC loop equation exists in Figure 2 for the j^{th} phase leg (neglecting R_r, R_c and C_P for simplicity) (8):

$$\begin{aligned} U_{dc} &= U_{cu,j} + U_{cl,j} + U_{reac,j} \\ &= \sum_{n=1}^{2N} U_{sm0,j,n} + U_{reac,j} \\ &= \sum_{n=1}^{2N} U_{sm0,j,n} + 2L_r \tfrac{d}{dt}\left(i_{u,j} + i_{l,j}\right) \\ &= \sum_{n=1}^{2N} U_{sm0,j,n} + 4L_r \tfrac{d}{dt}\left(\tfrac{i_{u,j}+i_{l,j}}{2}\right) \end{aligned} \quad (8)$$

Where $U_{sm0,j,n}$ is the output voltage of the n^{th} SM in the j^{th} phase leg (see Figure 1). i_z = ($i_{u,j}$+$i_{l,j}$)/2 is the circulating current flowing along the DC loop for the j^{th} phase. As evident from (8), i_z can be used to control $U_{AV,j}$ Figure 5 shows the implemented average controller, which is divided into an outer voltage and inner current loop.

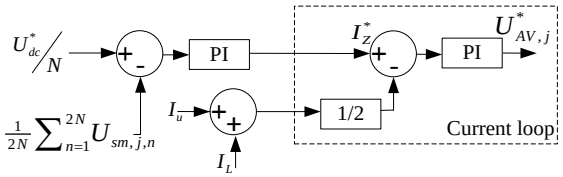


Figure 5 Average SM voltage controller for the j^{th} (j=a,b,c) phase.

The voltage loop controls the $U_{AV,j}$ by determing the reference, I*$_z$, for the current loop compensator. I*$_z$ increases if U*$_{sm}$ > $U_{AV,j}$. I*$_z$ is then substracted from the measured i_z in the current loop, reducing the voltage command U*$_{AV,j}$. U*$_{AV,j}$ is then added to $U^*_{cu,j}$ and $U^*_{cl,j}$, causing an increase in i_z, responsible for increasing $U_{AV,j}$.

- **Individual SM balancing,** ensures that the voltage in the n^{th} SM converges to $U_{sm,r}$.

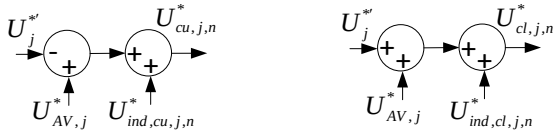
The individual balancing control forms an active power component ($P_{ind,u/l,j,n}$) between the fundamental component (i.e. 50 Hz) of the output voltage ($U_{smO,u/l,j,n}$) of the n^{th} SM in the upper or lower arm (u/l, respectively) and the corresponding frequency component in the arm current (i_u and i_l for the upper and lower phase arm, respectively). Therefore the reference for the n^{th} SM is as in (9) and (10) for the upper (u) and lower arm (l), respectively.

$$U^*_{ind,cu,j,n} = \begin{cases} K_{ind}\left(U_{AV,j} - U_{sm,u,j,n}\right) & (i_u > 0) \\ -K_{ind}\left(U_{AV,j} - U_{sm,u,j,n}\right) & (i_u < 0) \end{cases} \quad (9)$$

$$U^*_{ind,cl,j,n} = \begin{cases} K_{ind}\left(U_{AV,j} - U_{sm,l,j,n}\right) & (i_l > 0) \\ -K_{ind}\left(U_{AV,j} - U_{sm,l,j,n}\right) & (i_l < 0) \end{cases} \quad (10)$$

The polarity for the individual balancing reference (U*$_{ind,cu/l,j,n}$) has been aligned with the polarity of the arm current in (9) and (10), so $P_{ind,u/l,j,n}$ > 0 for $U_{AV,j}$ > $U_{SM,j,n}$ charging the n^{th} SM in the upper/lower arm capacitor (u/l, respectively) from the DC side of the converter regardless of the polarity of the arm current.

Figure 6 shows the derivation of upper -a)- and lower -b)- arm voltage commands for the n^{th} SM in the j_{th} phase. U_j*' is given by the ICC in Figure 4, U*$_{AV,j}$ is obtained from the average leg voltage controller and U*$_{ind,cu/l,j,n}$ is calculated from (9) and (10) for SMs in the upper and lower arms, respectively.



a) b)

Figure 6 Reference signals for the n^{th} SM in the j^{th} phase in the a) upper arm and b) lower arm.

Note that U_j*' is subtracted in the upper arm in Figure 6a). The reason for this is evident by applying KVL in the j^{th} phase in Figure 1 as in (11) and (12) for the upper and lower arms, respectively. The voltage across the inductor $2L_r$ has been neglected in (11) and (12), for simplicity.

$$U_{cu,j} = U_{DC}/2 - U_{C,j} \quad (11)$$

$$U_{cl,j} = U_{DC}/2 + U_{C,j} \quad (12)$$

The parameter design of the control parameters of the ICC in (6), follows standard control design for VSC converters, see e.g. [23]. The parameter design of the

average control in Figure 5 and individual balancing in (9) and (10) is less straightforward and is beyond the scope of the paper. The authors intend to prepare a more detailed analysis and description of the design procedure in future work.

IV. Simulation Results and Discussion

The comparison between the three models described in Section III is only focussing on converter response to step changes in the command orders of I_d* and I_q*.

Table 2 summarises the step changes imposed on the system during the simulation. Figure 7 shows the simulated i_d and i_q during the step change sequence indicated in Table 2. Figure 8 shows a zoom-in on the i_d and i_q during step sequences at t = 200 ms and t = 1200 ms.

Table 2 Step changes in I_d* and I_q*.

t [ms]	I_d* [PU]	I_q* [PU]
0	0.0	0.0
200	0.5	0.0
700	0.5	0.5
1200	-0.5	0.0
1700	-0.5	-0.5

As can be appreciated from the figures, the models offer similar dynamic performance. Rise times for detailed and simplified EMT models are relatively close to each other and the RMS model represents a good approximation of the behavior, neglecting dynamic differences due to the phasor averaging. However, low frequency oscillations of relevant magnitude, with cross-coupling between *d*- and *q*- axes are present in simulation results using the detailed EMT model. These oscillations are most likely due to the slow action of the leg averaging control described in Section III.C.b). Figure 9a shows the average phase leg voltages during the step sequence at t = 1200 ms, where $U_{AV,tot}$ is the average voltage of the 6N SM capacitors in the studied MMCC and calculated from (7) as $U_{AV,tot} = \frac{1}{3}\sum_{j=1}^{3} U_{AV,j}$ (j=a,b,c).

The 1 PU and 0.5 PU change in i_d and i_q, respectively, at t = 1200 s causes a 0.1 PU change in $U_{AV,tot}$ as well as inbalance between the three $U_{AV,j}$ in Figure 9a. $U_{AV,tot}$ roughly returns to 1 PU 200 miliseconds later. The excursion in $U_{AV,tot}$ may therefore be the source of the oscillations in i_d and i_q and compensation means should be provided to counteract them.

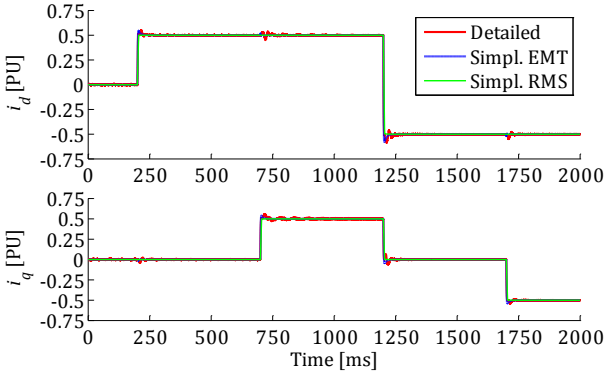
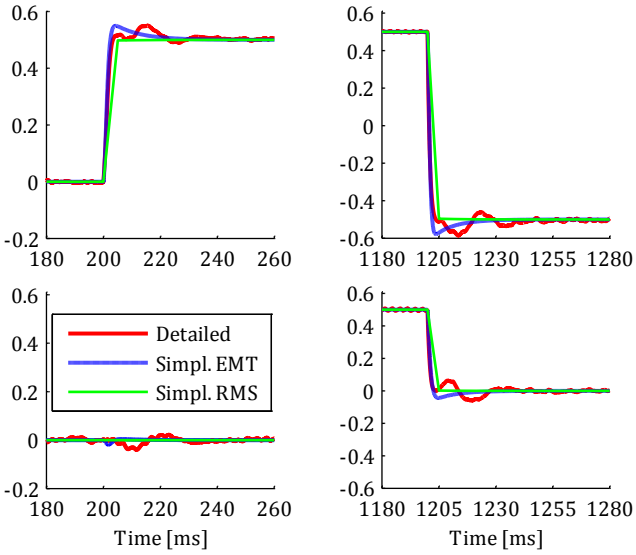


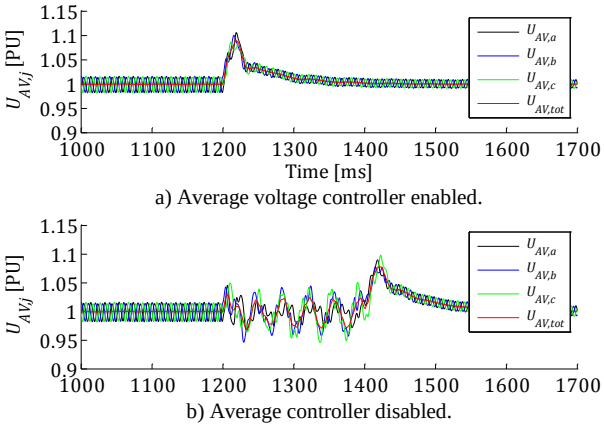
Figure 7 Simulated i_d and i_q during the step change sequence indicated in Table 2.

A parameter optimisation search on the PI and P controllers in the average controller in Figure 5 has been undertaken in the work based on trial-and-error, which is very tedious, due to the small simulation time steps required in all EMT related simulations. As mentioned in Section III.C.b) authors intend to prepare a more detailed analysis on the design of the parameters in future work.



a) Step change in i_d at t = 200 ms. b) Step change in i_d and i_q at t = 1200 ms.

Figure 8 Simulated i_d and i_q (top and bottom plot, respectively) for step changes at t = 200 ms and t = 1200 ms.



a) Average voltage controller enabled.

b) Average controller disabled.

Figure 9 Average phase leg voltages voltages. $U_{AV,tot}$ is the average of the 6N SMs in the converter. Average voltage controller is disabled for 1100 ms ≤ t ≥ 1400 ms.

In order to demonstrate the performance and necessity for SM voltage balancing means, the simulation has been repeated with the average controller disabled for 1100 ms ≤ t ≥ 1400 ms (see Figure 9b). By comparing Figure 9a and b it is evident that the waveforms become distorted and drifts away from the design point, leading to instability if the controller is not being re-enabled at t = 1400 ms. Figure 10 shows simulated phase A capacitor voltages for the upper arm N = 38 SMs, with (top) and without (bottom plot) the controller enabled for 1100 ms ≤ t ≥ 1400 ms. The figure also shows the importance of balancing means.

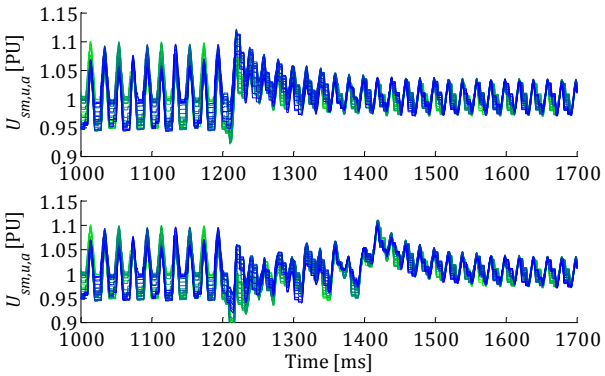


Figure 10 Upper arm capacitor voltages of N = 38 SMs in phase A. The top plot shows the results under normal operating conditions, whereas the average voltage controller is disabled for 1100 ms ≤ t ≥ 1400 ms in the lower plot.

V. CONCLUSION AND OUTLOOK

This paper highlighted the challenges in the design of the controllers of the MMCC internal dynamics, such as voltage balancing of the SMs. The knowledge required for detailed representation of the commercial HVDC converter is often not known to the end-user such as the OWPP developer. The paper has therefore adressed the applicability of more simplified RMS and EMT models readily available in the commercial tool DigSILENT PowerFactory with a more detailed user defined EMT model in PSCAD/EMTDC for step changes in the active and reactive power commands.

The comparison shows that the simplified EMT/RMS models can be trusted for slow dynamic studies like those related to power control considered in this work.

However, further work is needed to clarify whether the relevant dynamic differences are due to imperfections in the detailed model, insufficient control actions, or intrinsic inapplicability of simplified models. Also, further work is required in order to refine the controller tuning and/or provide further compensation means for the dynamic arm leg voltage excursions.

The authors will in future work address more complex behavior of the MMCC HVDC during e.g. unbalanced faults as well as the design procedure of the voltage balancing controllers required in the detailed MMCC model.

VI. ACKNOWLEDGMENT

This work was mainly financed by DONG Energy Wind Power with support from Danish Ministry of Science, Innovation and Higher Education.

Further support to the elaboration of this article came from OffshoreDC project (www.offshoredc.dk) which belongs to the Top-level Research Initiative funded by Nordic Energy Research under project no. TFI PK-int 02.

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