A Crossed Pack-to-Cell Equalizer Based on Quasi-Resonant LC Converter with Adaptive Fuzzy Logic Equalization Control for Series-connected Lithium-Ion Battery Strings

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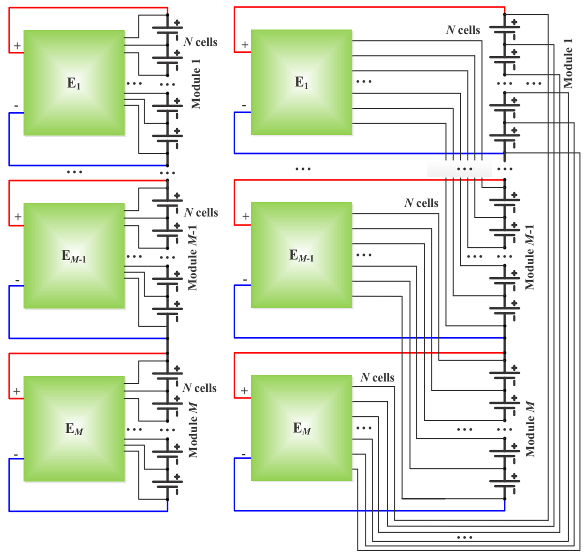
***Abstract*—The equalization speed, efficiency, and control are the key issues of battery equalization. This paper proposes a crossed pack-to-cell equalizer based on quasi-resonant LC converter (QRLCC). The battery string is divided into M modules, and each module consists of N series-connected cells. The energy can be transferred directly from a battery module to the lowest voltage cell (LVC) in the next adjacent module, which results in an enhancement of equalization efficiency and current. The QRLCC is employed to gain zero-current switching (ZCS), leading to a reduction of power losses and electromagnetic interference (EMI). Furthermore, an adaptive fuzzy logic control (AFLC) algorithm is employed to online regulate the equalization period according to the voltage difference between cells and the cell voltage, not only greatly abbreviating the balancing time but also effectively preventing over-equalization. A prototype with eight lithium-ion battery cells is implemented. Experimental results show the proposed scheme exhibits outstanding balancing performance, and the equalization efficiency is higher than 98%. The proposed AFLC algorithm abridges the total equalization time about 47%, and reduces the switching cycle about 62% compared with the traditional fuzzy logic control (FLC) algorithm.**

Keywords—Equalizers, adaptive fuzzy logic control (AFLC), zero-current switching (ZCS), lithium-ion batteries, plug in hybrid electric vehicles (PHEVs), electric vehicles (EVs).

I. Introduction

It is well-known that the world is being faced with the unprecedented energy and environmental crisis, which is becoming of paramount concern. To address these crisis, plug in hybrid electric vehicles (PHEVs) and electric vehicles (EVs) are applied and considered to be the most viable and commercially available alternatives to the internal combustion engine vehicles for the future as PHEVs and EVs have the advantages of energy conservation and environmental protection [1]. In addition, as mobile storage equipments, large-scale PHEVs and EVs will be the important pillar of the third industrial revolution. Vehicle power batteries are the power sources of PHEVs and EVs. Their performances have significant impacts on the power performance, fuel economy, and safety for vehicles, and have became the bottleneck in the scale development of PHEVs and EVs. Lithium-ion battery is currently considered to be one of the most popular rechargeable battery due to its high energy density, low self-discharge rate, and no memory effect. It has been dominating the high power products, such as PHEVs and EVs [2]-[3]. However, due to the limited voltage and capacity of one single lithium-ion cell, a battery pack must incorporate thousands of individual cells connected in series and/or in parallel to meet the power and energy requirements of PHEVs and EVs [4]. However, the series-connected lithium-ion pack brings a serious challenge: the variations in manufacturing, environment, and usage will cause the cell voltages to drift apart as the battery pack is charged or discharged, and this imbalance tends to increase as the pack ages [5]. This fact may lead to low efficiency, short lifetime, and high risk of catching fire and explosion. Therefore, equalization is essentially required for the series-connected lithium-ion battery strings.

Numerous equalization schemes have already been developed and well summarized in [6]. According to the energy flow, they can be classified into five groups: adjacent cell-to-cell methods (ACTCMs) [5], [7]-[9], direct cell-to-cell methods (DCTCMs) [4], [10], cell-to-pack methods (CTPMs) [11]-[12], pack-to-cell methods (PTCMs) [13]-[14], and any cell(s) to any cell(s) methods (ACTACMs) [15]. For the ACTCMs and DCTCMs, due to the small voltage difference between cells and the voltage drop across the power devices, the balancing current is very small (only about C/100-C/50) [5], resulting in a long equalization time. For the CTPMs, the energy is transferred from a cell (low voltage) to the pack (high voltage), leading to a very low balancing power. For the ACTACMs, the energy can be transferred from any cell(s) to any cell(s), which



(a) (b)

Fig. 1. System configuration of a battery string with pack-to-cell equalizers.

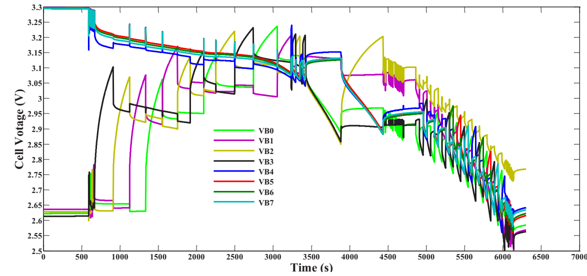


Fig. 2. Over-equalization for an eight-cell battery pack.

need many switches. Thus, the outstanding disadvantages of this system are the bulky size and the complexity control. The PTCMs can obtain large balancing current because of the large voltage difference between the pack and a cell. Fig. 1 (a) shows the conventional architecture of the pack-to-cell equalization for a long series connected lithium-ion battery string. The battery string is divided into M modules, and each module consists of N series-connected cells. In each module, the charge is transferred from the whole module to the least charged cell. When one cell is less charged than the other cells in a module, and the others are balanced in a same voltage level, this method has the best equalization performance [4]. When one cell is more charged than the others while the others are balanced, this is the worst case for this method [4]. Moreover, when the target cell is balanced by the mean of charge with this method, the cell also will be simultaneously discharged through the whole module. Therefore, due to the unnecessary energy waste, the average conversion efficiency with this method is lower than the one conversion efficiency. In addition, there is no any equalization between module and module. Therefore, this architecture can not obtain zero-voltage gap (ZVG) between cells.

To reduce energy losses and the number of equalizers, a novel architecture for the pack-to-cell equalization is proposed in Fig. 1 (b) to achieve high equalization efficiency and large equalization current. In this structure, equalizers are set up for each module. Specifically, the positive and negative terminals of the jth (j=1,2,...,$M-1$.) module is connected to the input of the jth equalizer, and the output of this equalizer is connected to the cells of the $(j+1)th$ module. So, the jth module can equalize the cells of the $(j+1)th$ module. By that analogy, the last module equalizes the cells of the first one. Thus, the energy can be exchanged between modules. This crossed pack-to-cell equalization structure not only reduces energy waste but also achieves ZVG between cells due to the crossed equalization topology.

Equalization control is one key issue of battery equalization. The balancing strategies can be classified into three groups, which include the voltage-based, SOC-based, and pack capacity-based methods [4], [16]. SOC-based and pack capacity-based equalization methods require accurate cell SOC estimation, which are difficult to implement in reality. Voltage-based equalization methods, which target the consistent cell voltages, are the most feasible to realize due to the direct measured cell voltages. However, voltage-based equalization is also challenging due to the transient response and the ohmic resistance of cells. When a cell is charged, the cell voltage will increase instantaneously. On the contrary, when the cell is discharged, the cell voltage will decline instantaneously. After charge or discharge stops, the cell will take a long time to return to the open circuit voltage. Therefore, it is difficult to determine when the battery pack can achieve an optimum balance. Voltage-based equalization algorithm cannot directly represent the ultimate purpose of the equalization, hence it often suffers from over-equalization [16]. As shown in Fig. 2, without an appropriate equalization control algorithm, the equalizer depletes the battery instead of equalizing the cell voltages. Over-equalization can be prevented by directly lowering the equalization time and current. But this also increases the total equalization time and switching cycle. In order to overcome these drawbacks, equalization algorithms based on fuzzy logic control (FLC) have been studied in literature [4], [5], [16]-[23]. These algorithms are all employed to regulate the equalization current according to the voltage difference, effectively preventing over-equalization. However, the equalization current is limited by the maximum value, which results in a small improvement in the equalization speed. Therefore, an adaptive fuzzy logic control (AFLC) algorithm is proposed in this paper to online regulate the equalization period according to the voltage difference between cells and the cell voltage, not only greatly abbreviating the balancing time but also effectively preventing over-equalization.

The remainder of this paper is organized as follows. The design concept and operation principle of the proposed system are analyzed in Section II. The design of the adaptive fuzzy logic controller is presented in Section III. The experimental results are presented in Sections IV. The conclusion is presented in Section V.

II. Proposed Equalizer

We have previously proposed a cell-to-cell battery equalizer with ZCS and ZVG based on QRLCC that offers several major advantages over conventional equalizers [4]. Based on

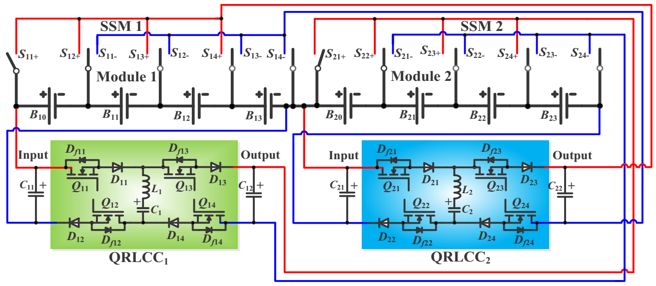


Fig. 3. The structure of the proposed two-module pack-to-cell equalizer based on QRLCC.

the precedent work, this paper proposes a crossed pack-to-cell equalizer based on QRLCC, which has the similar operational principle and circuit analysis as presented in [4].

A. Configuration of the Proposed Equalizer

Fig. 3 presents the proposed two-module pack-to-cell e-qualizer based on QRLCC, where each module consists of 4 series-connected battery cells. Each equalizer consists of two parts, the QRLCC and the selection switch modules (SSMs). The QRLCC, as the core of the proposed equalizer, is made up of a LC converter, four MOSFET switches, and four diodes. The MOSFET switches are divided into two pairs (i.e., Q_{i1}, Q_{i2} and Q_{i3}, Q_{i4}, i=1, 2.), which are controlled by a pair of complementary pulse width modulation (PWM) pulses, enabling the QRLCC to alternatively operate between the state of charging and the state of discharging. Particularly, zero-current switching (ZCS) is achieved when the switching frequency is equal to the inherent resonant frequency of the QRLCC. The diodes are used to isolate the balanced cell from the battery pack. The major role of the QRLCC is to achieve the energy transfer with zero switching loss. The SSMs consist of N pairs of relays, through which the energy can be transferred from a module to the LVC at any position in the next adjacent module without unnecessary energy waste.

B. Operational Principle

In order to simplify the analysis for the operation modes, the following assumptions are made: the energy is transferred from Module 1 (M_1) to the LVC, e.g., B_{21} in Module 2 (M_2). Thus, the SSM 2 S_{22+}, S_{22-} are first turned ON. As shown in Figs. 4 (a) and (b), the proposed topology has two consecutive working states.

Working state I: Q_{11}, Q_{12} are turned ON, and Q_{13}, Q_{14} are turned OFF. QRLCC$_1$ is connected in parallel with M_1 through Q_{11}, D_{11} and Q_{12}, D_{12}, as shown in Fig. 4 (a). M_1, L_1, and C_1 form a resonant loop, and the current path from M_1 is constructed. C_1 is charged by M_1. Then, the capacitor voltage V_{C_1} begins to increase. In an ideal world, the current flowing into QRLCC$_1$ is equal to that flowing out of M_1. Meanwhile, because Q_{13} and Q_{14} maintain OFF, and B_{21} acts as an open path, the charge current into B_{21} is zero (see the state I in Fig. 5).

Working state II: Q_{11}, Q_{12} are turned OFF, and Q_{13}, Q_{14} are turned ON. QRLCC$_1$ is connected in parallel with B_{21} through Q_{13}, D_{13} and Q_{14}, D_{14}, as shown in Fig. 4 (b). L_1,

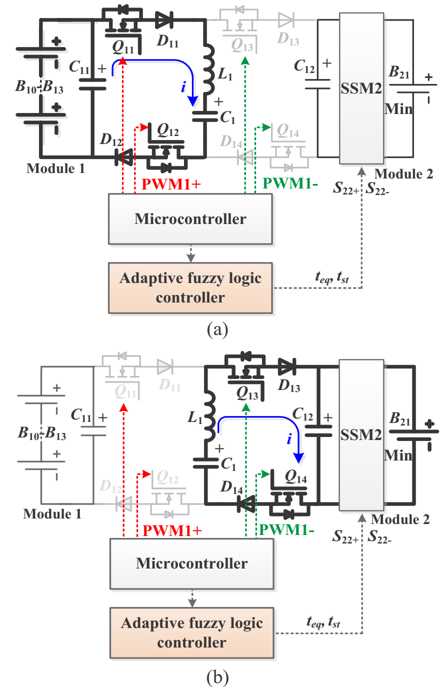


Fig. 4. Two consecutive working states of the proposed equalizer.

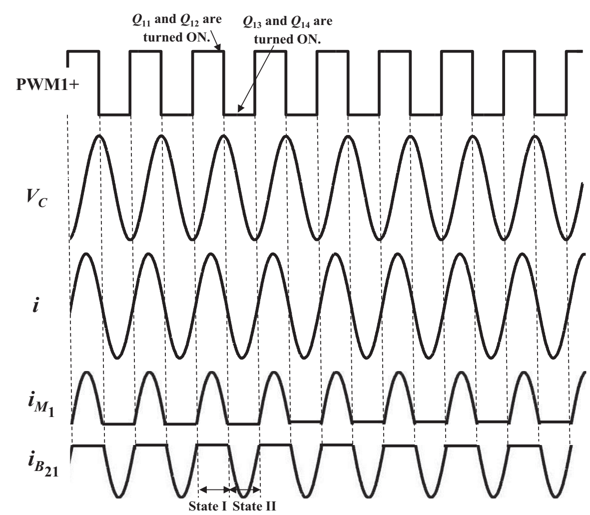


Fig. 5. Timing diagram representing energy transfer from M_1 to B_{21} in M_2 during idle scenario. It is specified that the current flowing out of a battery pack/cell is positive, and vice is negative.

C_1, and B_{21} form a resonant loop. The current path from QRLCC$_1$ into B_{21} is constructed. B_{21} is charged by C_1. Then, V_{C_1} begins to decrease. Simultaneously, M_1 acts as an open path, so the discharge current out of M_1 is zero (see the state II in Fig. 5).

C. Circuit Analysis

The proposed equalization circuit can be simplified as shown in Fig. 6, and the following notations are to be used.

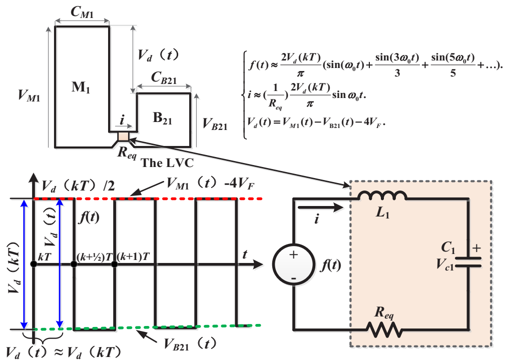


Fig. 6. Series resonant circuit with the AC square wave power source.

1) R_{eq}: the equivalent resistance of QRLCC$_1$, which can be expressed as

$$R_{eq} = R_{LC} + 2R_{DS(on)} \tag{1}$$

where R_{LC} is the internal resistance of the LC converter. $R_{DS(on)}$ is the static drain-source on resistance of the MOSFET switch.

2) T: the switching period of the MOSFET switches, satisfying:

$$T = 2\pi\sqrt{L_1C_1}. \tag{2}$$

3) ω_0: the characteristic angular frequency, satisfying:

$$\omega_0 = \frac{2\pi}{T} = \frac{1}{\sqrt{L_1C_1}}. \tag{3}$$

4) $V_{B21}(t)$: the voltage of the LVC B_{21} in M_2.

5) $V_{M1}(t)$: the battery pack voltage of M_1.

6) $V_d(t)$: the voltage difference between the battery pack and the LVC, which can be represented by

$$V_d(t) = V_{M1}(t) - V_{B21}(t) - 4V_F \tag{4}$$

where V_F is the diode's forward voltage drop.

7) $f(t)$: the AC square wave input of QRLCC$_1$, which can be expressed as

$$f(t) = \begin{cases} V_d(t)/2, & t \in (kT, (k+\frac{1}{2})T) \\ -V_d(t)/2, & t \in ((k+\frac{1}{2})T, (k+1)T) \end{cases} \tag{5}$$

where k=$[\frac{t}{T}]$, and $[\cdot]$ is Gaussian function. The Fourier transform of $f(t)$ can be expressed as

$$f(t) \approx \frac{2V_d(t)}{\pi}(\sin(\omega_0 t) + \frac{\sin(3\omega_0 t)}{3} + \frac{\sin(5\omega_0 t)}{5} + \ldots). \tag{6}$$

Then, the current i in QRLCC$_1$ can be approximatively represented by

$$i \approx \frac{2V_d(t)}{\pi R_{eq}} \sin\omega_0 t. \tag{7}$$

Thanks to (7), the transferred charge Δq_T from M_1 to V_{B21} in one switching cycle can be simplified as

$$\Delta q_T \approx \int_0^{\frac{T}{2}} \frac{2V_d(t)}{\pi R_{eq}} \sin\omega_0 t dt \approx \frac{4V_d(t)\sqrt{L_1C_1}}{\pi R_{eq}}. \tag{8}$$

By dividing (8) by *T*, the transferred charge in unit time can be derived from

$$\frac{\Delta q}{\Delta t} = \frac{\Delta q_T}{T} = \frac{2V_d(t)}{\pi^2 R_{eq}} = \frac{I_1}{\pi} \tag{9}$$

where Δq is the transferred charge in the time period Δt. I_1 is the fundamental wave amplitude of the resonance current i. (9) shows that the amplitude of the resonance current decides the balancing speed, which is not affected by L_1 or C_1 values.

The relationship between the cell voltage and SOC is piecewise linear [4], which can be represented by

$$\Delta V = \lambda\Delta SOC = \lambda\frac{\Delta q}{C_C} = \frac{2\lambda V_d(t)}{\pi^2 R_{eq}\cdot C_C}\Delta t \tag{10}$$

where ΔV is the variation of the cell voltage according to the SOC variation ΔSOC within the time period Δt. λ is the proportionality coefficient between the voltage and SOC in one approximate linear segment, and λ can be viewed as a constant in the balancing process for relatively small SOC variation. C_C represents the whole charge stored in the battery in Coulomb.

By (10), the equalization time *t* can be calculated as follows:

$$\begin{aligned} t &= \frac{\pi^2 R_{eq}\cdot C_C}{2\lambda}\ln\frac{V_d(0)}{V_d(targ)} \\ &= \frac{\pi^2 R_{eq}\cdot C_C}{2\lambda}\ln\frac{V_{M1}(0) - V_{B21}(0) - 4V_F}{V_d(targ)} \end{aligned} \tag{11}$$

where $V_{M1}(0)$ and $V_{B21}(0)$ are the initial voltages of M_1 and B_{21}, respectively. $V_d(targ)$ is the target voltage difference of the equalization.

According to (11), the equalization time t is proportional to R_{eq} and C_C, is inversely proportional to λ, and has no relationship with L_1 or C_1. The larger the equivalent resistance R_{eq}, the longer the equalization time t and the larger the loss. Therefore, the components, such as MOSFET switches, diodes, inductances, and capacitances with low equivalent resistances, should be selected accordingly to satisfy the equalizer fine requirements.

III. Design of Adaptive Fuzzy Logic Controller

As shown in Fig. 3, with the proposed topology, the energy can be transferred directly from M_1 (M_2) to the LVC at any position in M_2 (M_1). Due to lithium-ion battery nonlinear behavior, one single equalization cycle cannot guarantee all cells will be fully balanced, it is necessary to take numerous equalization cycles to complete the energy exchange. Obviously, an appropriate equalization switching period is very important for the consistency of the battery pack. A long equalization time t_{eq} and a short standing time t_{st} are ample in the equalization capability but might lead to over-equalization, while a short equalization time t_{eq} and a long standing time t_{st} can efficiently prevent over-equalization but leads to a long equalization stage and a high switching frequency. To solve these problems, an AFLC algorithm is employed to online regulate the equalization period according to the voltage difference and the cell voltage. The equalization switching period is composed of the equalization time t_{eq} and the standing time t_{st}, which can be regulated through controlling the cell SSMs.

A. Design of Fuzzy Logic Controller

There are two cell states affecting the equalization period as follows.

(1) The cell voltage difference

Actually, the aim of the battery equalization is to make all cell voltage equal. The cell voltage imbalance is essentially the SOC imbalance. A large ΔV indicates a serious situation, which requires a comparative long equalizing time and a comparative short standing time to accelerate the equalizing speed. On the contrary, a small voltage difference stands for a slight imbalance, which is not in hurry to be equalized and requires a comparative short equalizing time and a comparative long standing time to prevent over-equalization of the battery pack. In this situation, the equalizing process can focus more on the improvement of the battery pack consistency.

(2) The cell voltage

As shown in Fig. 7, the uniform charging cell voltage curve of $LiFePO_4$ battery can be divided into about five linear segments (LSs), i.e. [2.5V, 3.16V), [3.16V, 3.32V), [3.32V, 3.4V), [3.4V, 3.48V), and [3.48V, 3.65V) according to the cell voltage. In each LS, the proportionality coefficient between the cell voltage and SOC can be viewed as a constant, but is unequal in different LSs. In other words, the same cell voltage difference in different LSs represents different SOC difference, which need different equalization period. Fig. 8 shows the voltage response curves under pulse charge current in different LSs. The recovery time varies with the cell voltage. Therefore, the equalization standing time also should be adjusted according to the LSs.

Therefore, the inputs of the fuzzy logic controller are the maximum voltage difference between cells ΔV and the balanced cell voltage V. The outputs are the desired battery equalizing time t_{eq} and the standing time t_{st}. As shown in Fig. 9, the FLC system consists of four parts, namely fuzzifier, rule base, inference engine, and defuzzifier [5]. The numerical input of the voltage difference ΔV is converted into two sets of fuzzy variables, i.e., $\mu_{eq,\Delta V}$ and $\mu_{st,\Delta V}$ by the fuzzifiers.

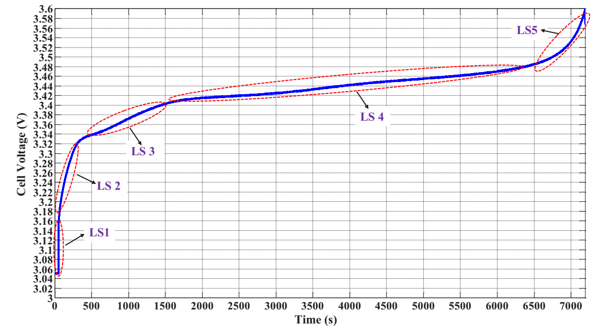


Fig. 7. The uniform charging cell voltage curve of lithium battery.

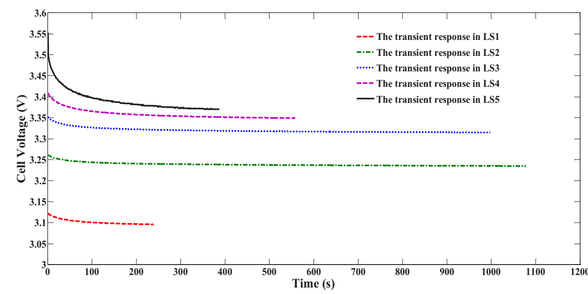


Fig. 8. The transient response of lithium battery after pulse charge.

The numerical input of the cell voltage V is also converted into two sets of fuzzy variables, i.e., $\mu_{eq,V}$ and $\mu_{st,V}$. For example, $\mu_{eq,\Delta V}$ $=Fuz_{eq}(\Delta V)$ =1 and $\mu_{st,\Delta V}$ $=Fuz_{st}(\Delta V)$ =0.5 are the fuzzy results from ΔV when 0.1 $V<\Delta V<0.3$ V. The linguistic control values are achieved based on the input fuzzy variables and the pre-constructed rule bases in the inference engine [5]. A multiplying inference engine is adopted, i.e.,

$$\begin{cases} \omega_{eq} = \mu_{eq,\Delta V} \times \mu_{eq,V} \\ \omega_{st} = \mu_{st,\Delta V} \times \mu_{st,V} \end{cases} \tag{12}$$

where ω_{eq} and ω_{st} are the fuzzy outputs of the equalization time t_{eq} and the standing time t_{st}, respectively. A graphical representation of the fuzzy logic controller outputs corresponding to the cell voltage difference ΔV and the cell voltage V is depicted in Fig. 10.

The linguistic inference results are converted into the numerical outputs by the defuzzifiers, which can be expressed as follows:

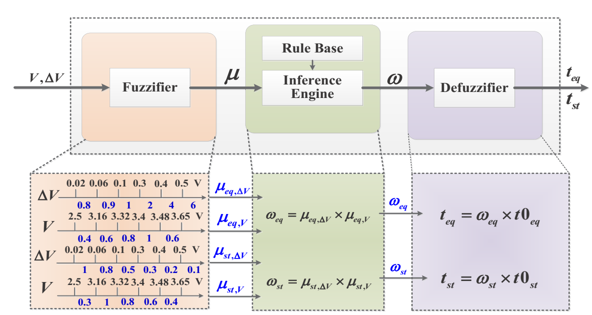
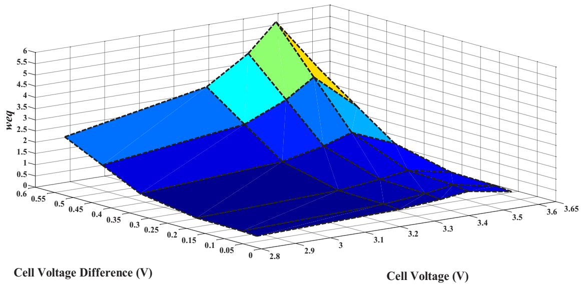
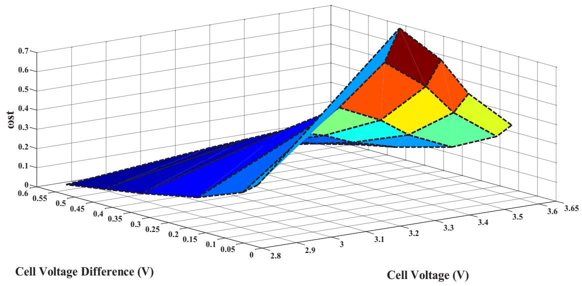


Fig. 9. Block diagram of the fuzzy logic controller.



(a)



(b)

Fig. 10. Surfaces of the fuzzy logic controller outputs corresponding to the cell voltage difference ΔV and the cell voltage V. (a) ω_{eq} with respect to ΔV and V. (b) ω_{st} with respect to ΔV and V.

$$\begin{cases} t_{eq} = \omega_{eq} \times t0_{eq} \\ t_{st} = \omega_{st} \times t0_{st} \end{cases} \tag{13}$$

where $t0_{eq}$ and $t0_{st}$ are the nominal equalization time and the nominal standing time, respectively.

B. Design of Adaptive Controller

Since the consistency of the battery pack will change with time, an appropriate nominal equalization period cannot be preset according to the consistency of the battery pack. Hence, we propose an AFLC algorithm to ongoing revise the nominal equalization time $t0_{eq}$ according to the present voltage difference $\Delta V(k)$, the previous voltage difference $\Delta V(k\text{-}1)$, and the previous nominal equalization time $t0_{eq}(k\text{-}1)$. The kth nominal equalization time is given by

$$t0_{eq}(k) = \frac{\Delta V(k)}{\Delta V(k-1) - \Delta V(k)} \times t0_{eq}(k-1). \tag{14}$$

It can be seen from (14) that the larger present cell voltage difference $\Delta V(k)$ or the smaller previous equalization voltage difference $\Delta V(k-1){-}\Delta V(k)$ will enable the algorithm to generate a longer nominal equalizing time in order to accelerate the equalization process. On the contrary, the algorithm will generate a shorter nominal equalizing time in order to prevent over-equalization. The control system of the proposed AFLC is further displayed in Fig. 11.

IV. Experimental Results

In order to evaluate the performance of the proposed equalizer and verify the validity of the AFLC algorithm, a prototype of eight lithium-ion cells, as shown in Fig. 12, is

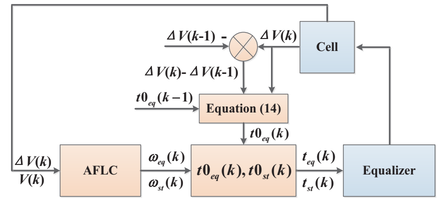


Fig. 11. Schematic diagram of the AFLC algorithm.

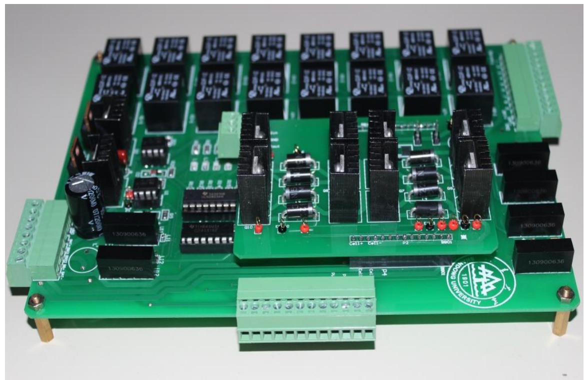


Fig. 12. Photograph of the proposed eight-cell balancing system.

implemented and tested. Table I summarizes the parameters of the QRLCCs and the selection switch modules in Fig. 3. The inductances, capacitances, and resistances in Table I are measured by an Agilent 4263B LCR Meter. The cell voltages are monitored by LTC6802-1 (made by Linear Technology), and are recorded every second.

Fig. 13 shows the experimental waveforms of the resonant current i and the capacitor voltage V_c with L_1=0.87 μH and C_1=0.49 μF. It can be observed that the resonant current i is sinusoidal, whose root meam square is up to 5.8 A. The corresponding capacitor voltage V_c is also a sinusoidal waveform lagging 90^o phase from the resonant current i, and the peak value of the capacitor voltage will occur at zero-crossing point of the current i. The MOSFETs are switched at the near-zero-current state with the frequency of 129.2 kHz, reducing the switching losses.

Fig. 14 shows the experimental results for eight cells with

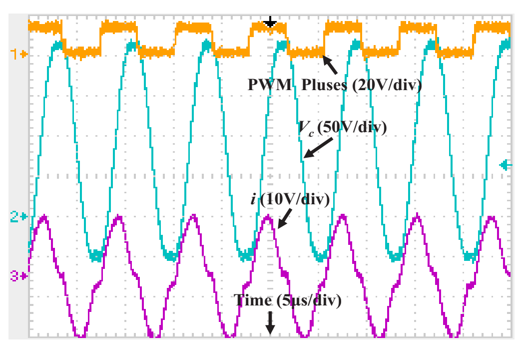


Fig. 13. Experimental waveforms for the resonant current and the capacitor voltage with L_1=0.87μH and C_1= 0.49μF.

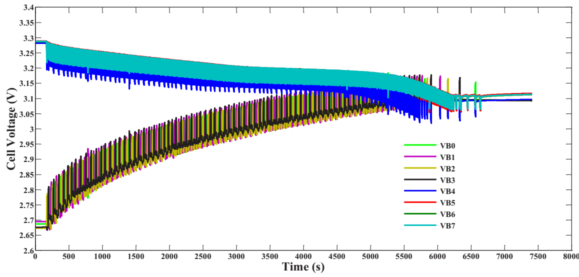


Fig. 14. Experimental results for the eight-cell voltage trajectories with the constant equalization switching period (t_{eq}= 10 s and t_{st}= 10 s).

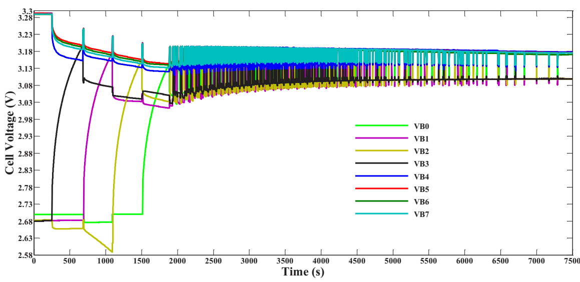


Fig. 15. Experimental results for the eight-cell voltage trajectories with the maximum voltage control strategy.

the constant equalization switching period, i.e., t_{eq}= 10 s and t_{st}= 10 s. The initial cell voltages are 2.687V, 2.695V, 2.673V, 2.676V, 3.282V, 3.289V, 3.287V, and 3.288V, respectively. After about 6800 s, zero-voltage gap (ZVG) between cells is achieved with about 340 switching cycles.

Fig. 15 shows the experimental results for eight cells with the maximum voltage control strategy, i.e., within each equalization cycle, the equalizer charges the LVC until its voltage catches up the maximum cell voltage of the battery pack, then the equalizer stops for 10 s. It can be observed that after about 7000 s and 180 switching cycles, the maximum voltage difference between cells is reduced from 0.62 V to 0.08 V, but ZVG between cells cannot be obtained due to the ohmic internal resistances of cells.

Fig. 16 presents the equalization results with the traditional FLC algorithm. After about 6000 s, ZVG between cells is achieved with about 112 switching cycles. Fig. 17 presents the equalization results with the proposed AFLC algorithm, whose initial voltages are the same as that in Figs. 14, 15, and 16. It can be observed from Fig. 17 (a) that the equalizing time t_{eq} and the standing time t_{st} are adjusted according to the cell voltage difference and the cell voltage. The larger cell voltage

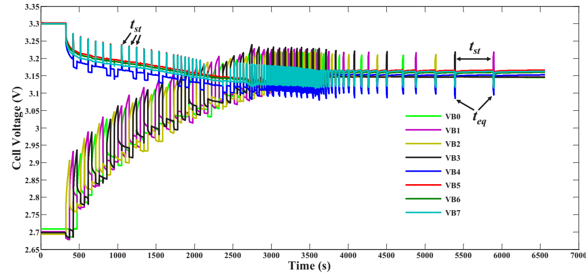


Fig. 16. Experimental results for the eight-cell battery pack with the traditional FLC algorithm.

difference will enable the adaptive fuzzy logic controller to generate a longer equalizing time and a shorter standing time in order to accelerate the equalization process. On the contrary, the smaller cell voltage difference will enable the adaptive fuzzy logic controller to generate a longer standing time and a shorter equalizing time in order to prevent over-equalization of the battery pack. Moreover, through ongoing regulating the nominal equalization time according to the history equalization information, the total equalization time and the switching cycle are reduced to 3200 s and 43 cycles, respectively. A 47% reduction of the total equalization time and a 62% reduction of the switching cycle are achieved compared with the traditional FLC algorithm in Fig. 16. The proposed equalization scheme with the designed AFLC algorithm not only reduces the total equalization time and the switching cycle but also effectively prevents over-equalization. As shown in Fig. 17 (b), during the balancing process, the energy conversion efficiency varies from 99% to 98%, showing high balancing efficiency.

V. Conclusion

In this paper, a crossed pack-to-cell equalizer based on QRLCC is proposed to gain large balancing current, high equalization efficiency, and effectively prevent over-equalization. The proposed scheme configuration, the operation principle, and the design of the adaptive fuzzy logic controller are presented, and a prototype with eight lithium-ion cells is optimally implemented. Experimental results show the proposed scheme exhibits outstanding balancing performance with ZCS and ZVG, and the balancing efficiency is higher than 98%. The AFLC algorithm abridges the total equalization time about 47%, and reduces the switching cycle about 62% compared with the traditional FLC algorithm.

Acknowledgment

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TABLE I. Component Values Used for the Prototype

Parameters			Value
Equalizers	QRLCCs	MOSFETs, Q_{11}-Q_{14}, Q_{21}-Q_{24}	80NF70, $R_{DS(on)}$[1]≤0.0098 Ω
		Diodes, D_{11}-D_{14}, D_{21}-D_{24}	IN5822, V_F[2]=0.55 V
		Inductances, L_1, L_2	0.87 μH, 17.3 $m\Omega$
		Capacitances, C_1, C_2	0.49 μF, 36 $m\Omega$
	Switch Modules	(S_{11+}, S_{11-})-(S_{14+}, S_{14-}), (S_{21+}, S_{21-})-(S_{24+}, S_{24-})	ZHNQI Q3F-1Z
Battery Pack		B_{10}-B_{13}, B_{20}-B_{23}	$LiFePO_4$, IFR26650, 6.2 Ah

[1] $R_{DS(on)}$. Static drain-source on resistance.
[2] V_F. Forward voltage.

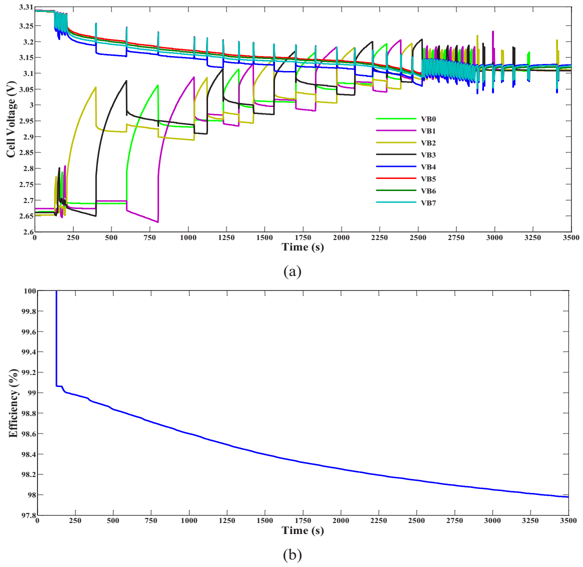

Fig. 17. Experimental results for the eight-cell battery pack with the proposed AFLC algorithm. (a) The 8-cell voltage trajectories. (b) Energy conversion efficiency.

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