Project description

On-chip noise coupling issues for high sensitivity, short range ultra-wide band communication system implementations in standard CMOS technology

Background

Looking at trends and developments within the area of wireless communication, it is clear that the systems applied are getting more and more advanced and therefore also much more complicated. At the same time, there is an increasing focus on, and request for, cheap and compact implementations of such wireless systems. In the context of a “Wireless Future”, the concept of a Personal Area Network (PAN) is widely accepted as a potential scenario for a future wireless world [1]. Based on user-centricity such PANs are to support user activities by enabling seamless and possible ad-hoc based communication to (and between) all of a user's devices capable of network connection whether at home, at the office, or in the wireless vicinity of the user. In such a scenario a vast number of wireless communication devices is to co-exist. This covers both ends of the bandwidth-scale including very low data-rate (LDR) sensory nodes to very high data-rate (HDR) 4G systems.

Ultra-Wide Band (UWB) communication is one of the technology platforms currently being investigated in support of both LDR and HDR applications. For short-range systems, UWB is expected to become one of the main-stream wireless technologies for the next couple of decades [2]. Considering the amount of wireless communication devices pictured in the “wireless world” scenario and the diversity of these devices, the need for cheap and compact implementations is only emphasized. Due to its cost advantage over competing Integrated Circuit (IC) technologies and its leading position in terms of device density, Complementary Metal-Oxide Semiconductor (CMOS) technologies hold a great potential for complying with implementation needs for UWB devices. When UWB short range communication systems are implemented on a single-chip, sensitive RF circuits have to be integrated together with large scale digital circuits and/or analog circuits operating with large signals. Those circuits will result in the generation of significant noise in a wide frequency band. The generated noise will coupled via the power supply system and will also be injected into the substrate. Owing to the low resistivity of Silicon substrates such coupled noise signals propagate effectively to RF areas where it may couple into for instance inductors and transistors in sensitive RF circuits. As simple energy detection receivers are widely used in LDR UWB systems the total noise power may be comparable to the signal power. Under such worst-case conditions the receiver may trigger on the noise and cause the generation of wrong output information which will result in a significant increase in BER. Compared to more expensive technologies CMOS has some performance short-comings that lead to design problems when UWB applications are the focus.

Noise considerations for UWB Implementations in CMOS

In order to avoid interference with current narrow-band communication systems the Power Spectral Density (PSD) for UWB systems is much lower than for narrow-band systems. In a narrow-band system, most of the wide-band noise can be removed through filtering. Filtering of noise is of course also possible in an UWB-system, however, due to the very large bandwidth (more than 500MHz) occupied by the wanted signal, limited - if any - performance gain results. Characteristics like this make UWB receivers much more sensitive to low-level noise than narrow band receivers and noise issues become the main bottleneck in CMOS single-chip implementation of short range UWB wireless communication systems.

The noise in UWB systems originates from one of three sources: (i) noise from the antenna, (ii) noise generated in the receivers RF circuits, and (iii) on-chip noise coupling from other parts of the system. While the noise from the antenna is the same as for any wireless system, the noise generated in the RF part of the receiver presents a much more serious issue for UWB systems. When the bandwidth is increased it becomes more difficult to obtain sufficiently good noise matching which degrades the noise performance of the receiver. The problem of obtaining wideband noise matching is magnified when a CMOS implementation is targeted. Due to the large processing tolerances it is even difficult to obtain accurate narrow-band matching in CMOS implementations. The fact that short-channel CMOS transistors display a high noise level only emphasizes the issue. Despite the challenges involved in low-noise UWB CMOS design the resulting performance is relatively easy to predict. This makes it possible to compensate for the limited performance by good system and circuit design. The last noise source, on-chip noise coupling, is much more difficult to predict and therefore deserves more attention.

State-of-the-Art

While noise coupling issues have been considered in the public literature, the reported works have mainly been done with narrow-band systems in mind [3]. In order to minimize the problem of coupled noise a current strategy for narrow-band systems is to introduce a wide gap in the layout (at least 100µm-200µm) between noisy and sensitive circuit blocks. While this approach does lead to an attenuation of the coupled noise it also implies a large waste of IC area. The cost per area for CMOS technologies increases drastically each time a new technology node is adopted, and for state-of-the-art processes the additional cost presented by the gap is unacceptable. Furthermore, the width of the gap is typically an empirical value without any theoretical or experimental knowledge for support.

Some of the more generally applicable works reported focus on very specific physical details of the coupling mechanisms [4 - 9], while other works focus on coupling between passive components and how to reduce the coupling [10 – 13]. When on-chip noise coupling and the effect it has on circuit performance is considered only very limited information is available. When the focus further is on UWB circuits and systems no, work has been presented in the public literature.

Application Potential

If short-range UWB communication is to become the major player in wireless communication it is foreseen to be, compact and low cost implementation is mandatory. Based on its leading position in terms of both device density and low cost, CMOS IC implementation is considered to be the most promising enabling technology. It is therefore very important that the on-chip noise issues raised by CMOS are carefully considered.

To evaluate the effect of on-chip noise coupling and to derive a strategy for on-chip noise suppression in UWB system implementations, knowledge concerning noise power level, bandwidth and on-chip noise propagation characteristics is necessary. At current, only very limited knowledge is presented in the public literature in general and no reported works have been found with relation to UWB systems. With characteristics such as low signal PSD level, ultra-wide band width and very compact implementation, the UWB systems are going to be very sensitive towards on-wafer noise issues. As the frequency range is increased from the current 3.1 GHz - 10.6 GHz to higher frequencies such as 24 GHz, 60 GHz and 100 GHz the sensitivity problem only increases [8]. Considering the developments on both current and future communication systems, it is clear that UWB short-range low/high data-rate systems will play a very important role in the future. It is therefore important from both a research and strategic point-of-view to conduct research within this area to characterize and solve on-chip noise coupling issues for short range UWB systems.

The project will help to provide valuable insight into the characteristics of on-chip noise issues for UWB systems and it will provide an understanding of the tools needed to solve this problem. The project will produce knowledge that will enable the design of short-range UWB systems for the current 3.1 GHz - 10.6 GHz band as well as the future 24 GHz, 60 GHz, 80 GHz and 100 GHz bands in a compact and low-cost single-chip style.

Research Content

In order to enable the successful implementation of low-cost and compact UWB systems in a single-chip style the noise issues inherent to CMOS technologies have to be solved. To accomplish this, the proposed project focuses on the study and characterization of on-chip noise issues as well as enabling techniques to solve the on-chip noise issue raised by single-chip CMOS implementation of short-range UWB communication systems.

On-chip noise issues for single-chip implementation of UWB short range communication systems fall in one of two categories; (i) substrate background noise and (ii) power supply integrity. The project is divided into two sub tasks to deal with both of these issues.

Task 1: Characterization and modeling of substrate background noise
When a large-scale communication system is operating, a large number of gates will constantly be switching on and off resulting in the generation of a noise signal with significant high frequency content. The frequency of the system clock, the operating speed of the system, and the scale of the digital circuitry are all parameters that determine how strong the noise effect is. If such a system is fully implemented on a single-chip this noise signal will inject a noise current into the substrate from where it may propagated to the rest of the chip resulting in a very broadband substrate background noise. This background noise is going to affect all parts of the implemented system. For digital blocks the noise may manifest it self as clock jitter or bit errors but in most practical implementations digital circuits are reasonably robust towards such disturbances. For analog and RF circuits the background noise may prove to be fatal, especially for UWB implementations where the signal power per unit bandwidth is very low. The semiconducting nature of the Silicon substrate implies that CMOS provides for low-ohmic and high bandwidth propagation paths. Even though it is possible to reduce

part of the noise through the use of PN-well isolation, the substrate background noise represents a serious impairment for compact single-chip implementations of UWB systems.

The different mechanisms of substrate background noise are highly dependent on specific implementation parameters such as the type of substrate and the sheet resistance of the substrate. Base on this, this task focuses on the following problems:

- To enable repeatable results a controllable simulation environment entailing information carrying signals, circuit scale effects, transistor density, and on-chip operating mode must be set-up to evaluate the behavior of complex on-chip systems.
- A statistical description of key characteristics of the frequency spectrum for the CMOS device substrate current injection must be provided. The behavior when operated at high clock speeds is most important but it should also be possible to evaluate the effect of changing clock frequencies.
- Based on the statistical description the relationship between noise intensity and the scale as well as density of CMOS transistors must be quantified.
- An understanding of specific noise propagation and attenuation characteristics is needed. Relationships between noise intensity and variables such as substrate sheet resistance, PN isolator implementations, and propagation distance must be established.
- Relations between the intensity of substrate background noise and the performance of active devices, passive devices, and total systems must be clarified.
- A strategy for dealing with substrate background noise must be devised.

Task goal

The goal of this task is to characterize and model the effect of substrate background noise in complex systems implemented on a single-chip. Another important goal is to present a strategy for dealing with substrate background noise in UWB systems implemented in CMOS.

Time plan: Task 1. Characterization and modeling of substrate background noise			
Task milestones resulting in a deliverable are on a grey background			
Year	month	Sub-task	Description
2006	1-2	Literature study	Literature study on substrate coupling noise issues and mechanisms.
	3-5	Simulation	It is determine how to simulate the on-chip substrate coupling effects.
2006	6-7	Simulation	A simulation system capable of evaluating on-chip noise based on variable parameters such as signal, scale, transistor density and operating mode is devised. Simulation structures, circuits and modules are implemented
	8	Vacation	
	9-12	Prototype design	The first prototypes of various devices and circuits suitable for characterizing the noise coupling mechanisms are designed and submitted for fabrication
2007	1	Measurements	A test plan and other possible requirements for measuring the fabricated structures are prepared.
	2-5	Measurements	The implemented structures are characterized by measurements. The results are analyzed and a prototype model is set up.
	6	Documentation	A test report on the wafer testing and data analysis is prepared.
	7	Documentation	A publication based on the key findings is prepared.
	8	Vacation	
	9-10	Simulation	A modified structure will be setup and simulated to verify the conclusions and models achieved on basis of the first prototypes.
	11	Documentation	A publication based on the results from the first prototype models is prepared
	12	Test structures	The second round prototype structures and circuits are designed. Refinements and/or new circuits and structures aim at improving the models. Structures must support an evaluation of a strategy for dealing with substrate background noise.
2008	1	Measurements	A test plan and other possible requirements for measuring the fabricated structures are prepared.
	2-4	Measurements	The second round prototypes are characterized by measurements.
	5	Documentation	A test report on the wafer testing and data analysis is prepared.
	6	Documentation	The results are analyzed and the model is refined. Theoretical explanations for the propagation of substrate background noise are

			provided. A strategy for dealing with substrate background noise is formalized.
	7	Documentation	A publication based on the results is prepared
	8	Vacation	
	9-12	Documentation	Preparation of Ph.D.-thesis.

Research environment

The project will be carried out at RF Integrated Systems and Circuit (RISC) Division, Center for TeleInFrastructure (CTIF) at Aalborg University. The group counts 14 researchers, including 1 professor, 3 assistant/associate professors and 10 Ph.D.-students. The group has several years of experience in research topics relevant for the attached project including experience in running Ph.D.-projects. The group also has published numerous international scientific papers relevant to the project.

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