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A Multi-Pulse Pattern Modulation Scheme for Harmonic Mitigation in Three-Phase Multi-Motor Drives

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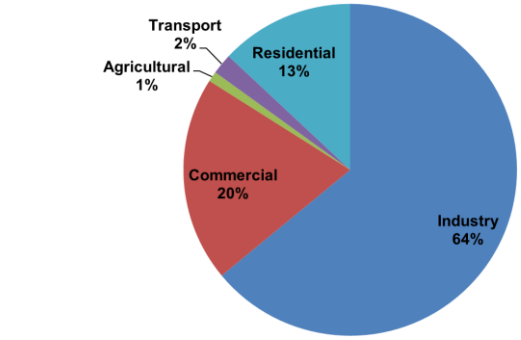
***Abstract*— Continuous improvement of power electronics technology has widely increased the applications of adjustable speed motor drives in many areas. Beyond the control flexibility, the power electronics devices (e.g., diode rectifiers) are also the main harmonic source to the grid due to their nonlinearity, which thus deteriorates the power grid quality and also lowers the conversion efficiency. Both degradations are apt to occur in motor drive applications. At present, many industrial drives are equipped with three-phase diode rectifiers and employ passive filtering techniques on the AC or DC side of the rectifier. In such topologies, it is difficult to implement the prior-art harmonic control strategies. Moreover, the total cost and complexity has become the main obstacle for these harmonic elimination approaches in multiple drive systems. Therefore, in this paper, a new cost-effective harmonic mitigation approach has been proposed for multiple drives. The proposed approach can control the generated current harmonics by benefiting of the nonlinearity of the drive units and through a novel current modulation scheme. The obtained results at the simulation and experimental level validate the effectiveness of the proposed approach.**

***Index Terms*— Adjustable speed drives, active filters, current modulation, harmonic mitigation, multiple drives, three-phase rectifiers.**

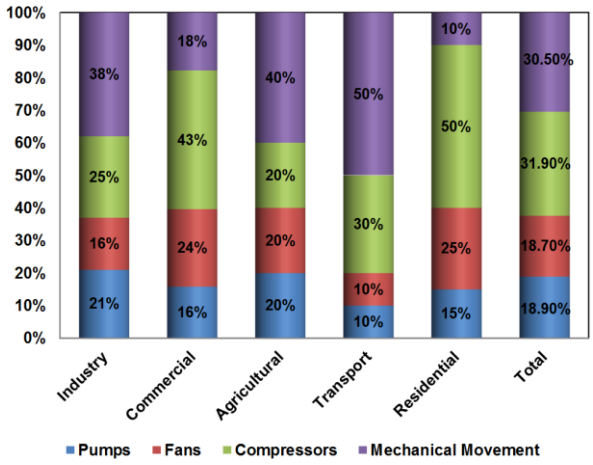
I. Introduction

ELECTRIC motor-driven systems consume more than 40% of the global electricity. In fact, the high demand for electric motors as shown in Fig. 1(a) has made them to be the major source of electricity use [1]. As the global electricity demand is continuously growing at a rapid rate, industry as a key player according to Fig. 1(b) has been pushed towards an era of developing more energy-efficient drives. With the advancement of power electronic devices and their decreasing price due to the market demand, Adjustable Speed Drive (ASD) systems are becoming increasingly common in many applications. Although the benefit of adjustable speed control on energy saving is clear, the penetration of ASD systems is still relatively low, due to the dependency of ASD market trend on the cost and efficiency.

Employing the adjustable speed technology for power electronics based drive systems can improve the efficiency to some extent [2]. However, the generated harmonics as a consequence of employing power electronics devices will



(a)



(b)

Fig. 1. Estimated share of electricity consumption for all electric motors from International Energy Agency (IEA) by: (a) sector and (b) sector and application [1].

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inevitably deteriorate the power grid quality [3]-[5]. These highly-distorted currents appearing in the power grid, cause unnecessary losses and thus may lead to heat in power system transformers, nuisance tripping of circuit breakers, and over-stressing of power factor correction capacitors. This highlights the necessity for the drive systems to comply with international standards like IEC61000 standard [6]. Therefore, it calls for more intelligent and advanced harmonic elimination strategies for the drive systems.

Typically, a standard drive system comprises of three main sections: the front-end power converter that converts AC power from the main grid to DC power, an energy storage unit called the DC-link, and finally an inverter as the rear-end power converter, which converts the DC back to AC at the voltage and frequency demanded by the motor. A three-phase diode bridge rectifier is usually employed, which is an almost-industry-standard choice at the front-end stage, being witnessed as the main harmonic source. As a consequence, a vast of harmonic mitigation methods have been introduced to such drive systems in order to improve the input current quality by shaping it as close as possible to a sinusoidal waveform [4], [5], [7]-[9] as well as using active damping methods [10]-[15]. However, a significant increase of complexity and cost has been observed in the harmonic elimination strategies. As a result, diode rectifiers (uncontrolled) or thyristor-based rectifiers (phase-controlled) of less complexity and cost are still widely used in the modern drive systems like in the ASD systems.

In addition, the undesirable nonlinearity of the conventional AC-DC conversion stage becomes significant, when a large number of industrial converters and ASD systems are connected to the Point of Common Coupling (PCC). It has been found that a proper arrangement of these nonlinear loads either single-phase or three-phase units can contribute to an effective harmonic mitigation, where some of the harmonics from one unit (e.g., diode rectifier) can be cancelled out by the other/s units [16]. The feasibility of this solution is attained only when suitable and accessible communication among the nonlinear units can be performed. It can be observed in many practical applications, where multitudes of ASD based industrial pumps, fans or compressors are operated all together.

In fact, improving the input current quality by combining the nonlinear loads was first introduced in multi-pulse rectifiers [17]. In this method, by employing phase-shifting transformers, the harmonics of each unit can be phase-displaced with respect to each other, and thus they can cancel out certain harmonics. Depending on the number of connected units, a range of harmonics can be eliminated. Taking a 24-pulse rectifier [17] as an example, the current Total Harmonic Distortion (THD_i) can significantly be improved (lower than 5%) using this method. Despite the effectiveness in harmonic mitigation, the volume, associated losses, and the cost of the phase-shifted transformer are the main concerns and these drawbacks become more evident at medium and high power applications.

Therefore, in this paper, a novel harmonic elimination approach is proposed to tackle the aforementioned challenges.

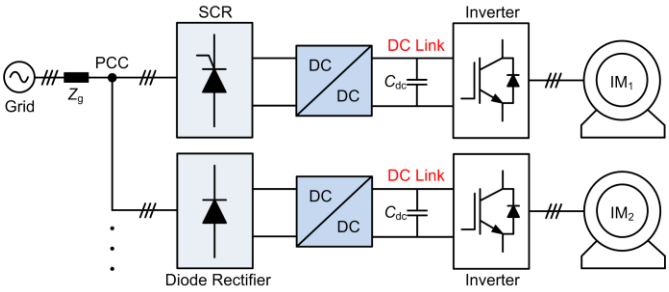


Fig. 2. Typical configuration for a multi-drive application with the proposed harmonic mitigation method: IM – Induction Motor.

The proposed method does not require any phase-shifting transformers like what have been used in multi-pulse rectifiers. Instead, as depicted in Fig. 2, it is based on a combination of the three-phase diode rectifier and three-phase Silicon Controlled Rectifier (SCR) units to cancel out the harmonics of interest. Additionally, in Section II, in order to improve the performance and flexibility of the system, each unit is equipped with a new current modulation technique is applied to the employed DC-DC converter (e.g., boost converter) at the DC-link, which can individually mitigate a certain number of current harmonics. Considering the employed DC-DC converter, the intended power ratings of each drive unit can be in the range of low power (<1 kW) up to medium power (<100 kW). However, depending on the application requirement, the power rating can be extended to a high power range by applying the multi-drive configuration. Optimization of the current modulation technique has also been conducted in Section II to further reduce the harmonic emissions from drive systems. Experimental tests and simulations have been carried out on a 5.5 kW system. Results presented in Section IV have verified the effectiveness of the proposed harmonic elimination method.

II. Proposed Harmonic Elimination Method

A. Nonlinear Loads Combination for Harmonic Cancellation

In order to demonstrate and evaluate the proposed harmonic mitigation method, the front-end stage of a multi-drive system consisting of two three-phase rectifier units is built up as it is shown in Fig. 2. The system operation details are illustrated in Fig. 3, which shows that the current source at the DC-link side of the rectifier draws a constant current (i.e., I_{dc}). In practice, the current source can be implemented in a DC-DC converter (e.g., boost converter) which emulates an ideal inductor behavior [18]-[21]. Therefore, for both rectifiers as shown in Fig. 3, the input currents (i.e., i_s and i_d) of the rectifiers will be square-wave currents with a conduction angle of 120^o, since at each instant of time interval only two phases conduct and circulate the DC-link current through the grid.

For the rectifier system shown in Fig. 3, Fourier series analysis has been adopted to identify the harmonic content of the input currents drawn from the power grid. According to Fig. 3(a), in a controlled rectifier (i.e., an SCR), the harmonics (i.e., $i_s(n)$) of the square-wave input current with a conduction angle of 120^o and an adjustable phase angle of α_0 can be

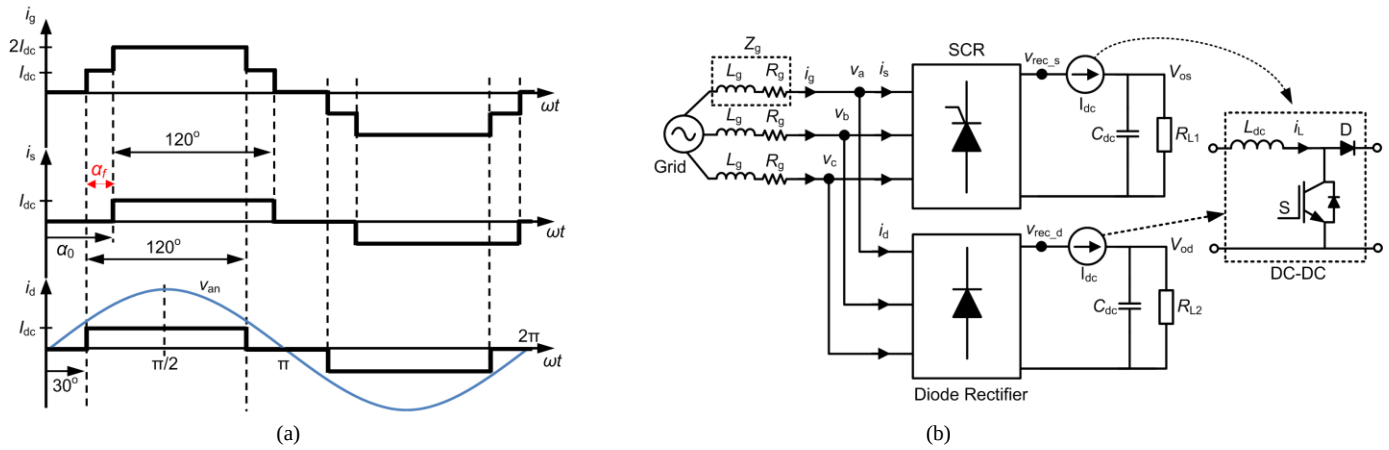


Fig. 3. Current distribution at the PCC of a multi-drive system with one diode rectifier and one SCR unit: (a) ideal currents and (b) system schematic.

identified as:

$$i_s(n) = \sqrt{(a_n)^2 + (b_n)^2} \tag{1}$$

with

$$\begin{cases} a_n = \dfrac{2I_{dc}}{n\pi}\left[-\sin(n\alpha_0) + \sin\left(n\alpha_0 + \dfrac{2\pi n}{3}\right)\right] \\ b_n = \dfrac{2I_{dc}}{n\pi}\left[\cos(n\alpha_0) - \cos\left(n\alpha_0 + \dfrac{2\pi n}{3}\right)\right] \end{cases}$$

in which n = 1, 5, 7, …, is the harmonic order. As for the three-phase diode rectifier, it can be taken as a special case of the SCR with a firing angle of $\alpha_f = 0°$ or a fixed phase angle of $\alpha_0 = 30°$ ($\alpha_0 = 30° + \alpha_f$). In that case, $a_n = 0$ according to (1), and thus the harmonics of the input current induced by the diode rectifier can be given by,

$$i_d(n) = \frac{4I_{dc}}{n\pi}\cos\left(\frac{n\pi}{6}\right) \tag{2}$$

According to Fig. 3, the total current drawn from grid can be expressed as $i_g = i_s + i_d$. Thus, the harmonics appearing in the grid current (i.e., i_g) can be calculated as,

$$i_g(n) = \sqrt{(a_n)^2 + \left(i_d(n) + b_n\right)^2} \tag{3}$$

As a consequence, based on (3), if the transcendental equations given in (4) are solved, any n-th harmonic appearing in the grid current can be cancelled out, and at the same time, the desired fundamental content of the grid current as the modulation index (M_a) can be achieved.

$$\begin{cases} i_g(1) = M_a \\ a_n = 0 \\ b_n + i_d(n) = 0 \end{cases} \tag{4}$$

B. Novel Current Modulation Technique

Although an appropriate adjustment of the phase angle of the SCR unit can contribute to an improvement of the current quality, a new current modulation technique is applied to each DC-DC converter in order to further improve the current quality. In the new current modulation approach, certain low order harmonics in the three-phase input line currents (i.e., the grid currents) can be eliminated by adding (or subtracting) phase-displaced current levels, thus leading to a better overall grid power quality, which will be detailed in the following.

The novel current modulation technique is based on the calculation of a pre-programmed switching pattern (current reference) for the DC-link current to achieve elimination of those specific harmonics in the grid currents. Fig. 4(a) demonstrates the basic idea of the proposed current modulation method for one rectifier unit (i.e., SCR). The illustrated currents in Fig. 4(a), show the new added current levels at the DC-link (i_L) in relation to the three-phase input currents.

For ease to analyze the harmonic characteristics, the switching patterns have been centralized and synchronized in respect to the grid phase voltage. In this approach, the new added current level should be repeated every 1/6 of the fundamental period in order to mitigate the triple harmonics. For instance, in the two sectors of 1 and 2 as shown in Fig. 4(b), where in each sector i_a is circulated through one of the other phase currents, if the new current level is added into sector 1, it should be exactly repeated in sector 2. This means that the frequency of the added pulses at the DC-link should be six times of the fundamental frequency (i.e., i_L in Fig. 4(a)).

It can be seen in Fig. 4(b) that the proposed current modulation pattern consists of three square-wave signals with different magnitudes and angles. The first current waveform has the magnitude of I_{dc1} with the conduction at a phase angle of α_0. Notably, for a three-phase diode rectifier, this phase angle is constant, $\alpha_0 = 30^o$ ($\alpha_f = 0$). The second current waveform has the magnitude of I_{dc2} with the conduction at a phase angle of α_1. The third current waveform has the magnitude of I_{dc2} but with the conduction at a phase angle of α_2. According to (1), the input current harmonics can then be

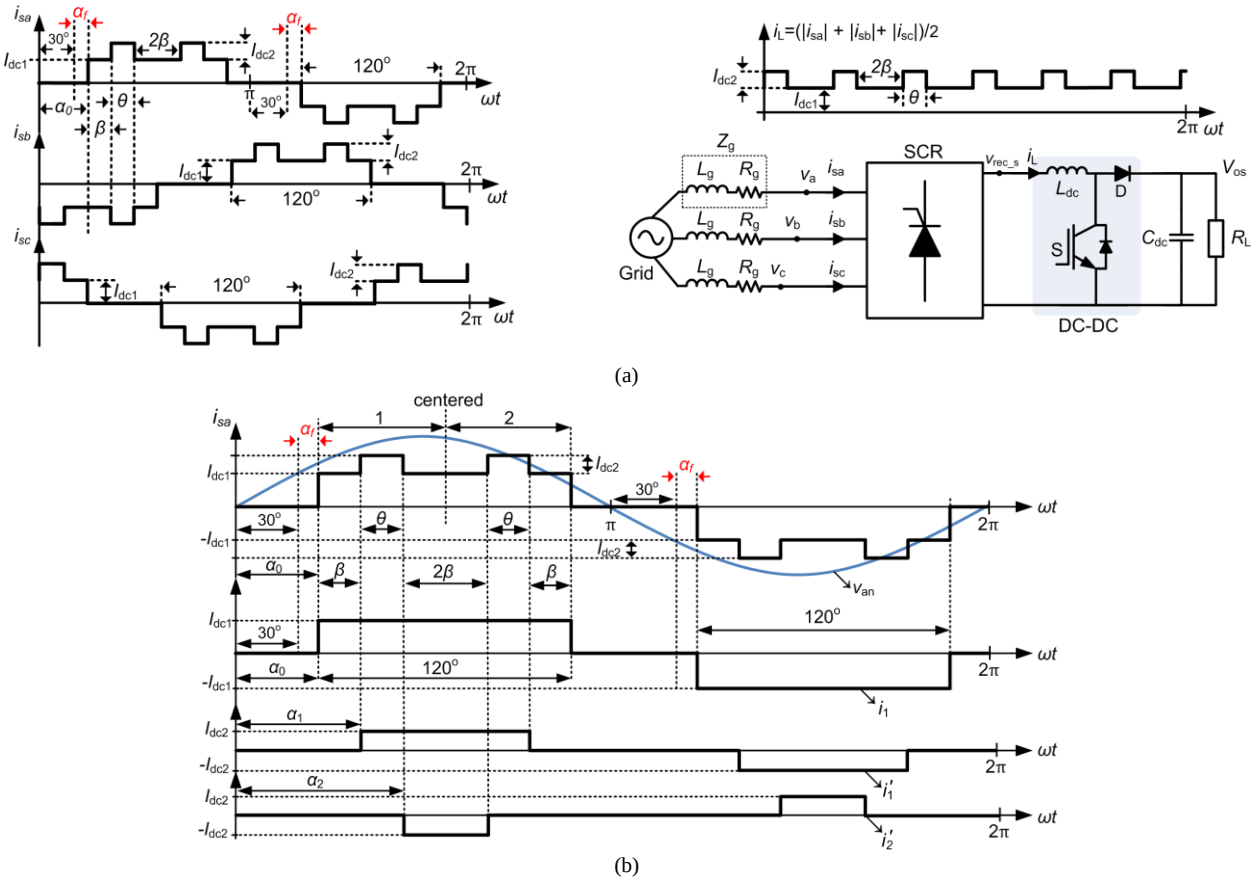


Fig. 4. Illustration of the proposed current modulation with selected harmonic cancellation: (a) typical waveforms in a SCR unit (α_f = 0° in the case of diode rectifiers) and (b) conceptual illustration of the proposed modulation scheme.

calculated as:

$$i_a(n)=\sqrt{\left(a_n+a'_n\right)^2+\left(b_n+b'_n\right)^2} \tag{5}$$

with

$$\begin{cases} a'_n=\sum_{j=1}^{2}\dfrac{2I_{dc2}(-1)^{j+1}}{n\pi}\left[-\sin\left(n\alpha_j\right)+\sin\left(2n\alpha_0-n\alpha_j+\dfrac{2\pi n}{3}\right)\right] \\ b'_n=\sum_{j=1}^{2}\dfrac{2I_{dc2}(-1)^{j+1}}{n\pi}\left[\cos\left(n\alpha_j\right)-\cos\left(2n\alpha_0-n\alpha_j+\dfrac{2\pi n}{3}\right)\right] \end{cases}$$

where i_a is the phase A current of the grid, a'_n and b'_n are the Fourier coefficients of the new added current levels that conduct at α_1 and α_2, and $\alpha_0<\alpha_1<\alpha_2<\alpha_0+60°$. Hence, in order to individually cancel out up to two low order harmonics, e.g., $i_a(m)$ and $i_a(k)$, the following condition holds,

$$2\beta+\theta=60 \quad \text{or} \quad 2\left(\alpha_1-\alpha_0\right)+\left(\alpha_2-\alpha_1\right)=60 \tag{6}$$

In respect to the three-phase diode rectifier, the conduction starts at a fix phase angle α_0 = 30° (α_f = 0°). Thus, according to (5) and (6), in the case of a three-phase diode rectifier, $a_n = a'_n = 0$. Therefore, the harmonics of the diode rectifier input current represented in (5) can be simplified as,

$$i_d(n)=\frac{4}{n\pi}\left[I_{dc1}\cos\left(\frac{n\pi}{6}\right)+I_{dc2}\cos\left(n\alpha_1\right)-I_{dc2}\cos\left(\frac{2\pi n}{3}-n\alpha_1\right)\right] \tag{7}$$

Hence, applying the proposed current modulation technique to both of the rectifier units can significantly improve the input current quality. Notably, the harmonics appearing in the supply line (i.e., grid currents i_g) can be calculated as,

$$i_g(n)=\sqrt{\left(a_n+a'_n\right)^2+\left(i_d(n)+b_n+b'_n\right)^2} \tag{8}$$

which results in a flexible harmonic elimination in the grid currents by solving,

$$\begin{cases} i_g(1)=M_a \\ a_n+a'_n=0 \\ i_d(n)+b_n+b'_n=0 \end{cases} \tag{9}$$

where M_a is the desired fundamental value and a_n, a'_n, b_n, b'_n are the Fourier series coefficients mentioned in (1) and (5).

C. Optimum Harmonic Solution

The above illustrates the impact on the harmonics by selecting proper modulation parameters (amplitudes and switching angles) for the proposed current modulation scheme. However, an optimization for these parameters may result in a more suitable solution and also higher flexibility to eliminate the harmonics of interest. The following demonstrates the harmonic optimization solution considering the maximum allowable harmonic level defined by the application or the grid code. In other words, instead of fully nullifying the distortions, the harmonics could be reduced to acceptable levels by adding suitable constraints (L_n). Then, an optimization problem (Obj_n) that searches a set of α_n and I_{dc} values over the allowable intervals can be defined as,

$$\begin{cases} Obj_1 = M_a - \left|i_g(1)\right| \le L_1 \\ Obj_n = \dfrac{\left|i_g(\mathrm{n})\right|}{\left|i_g(1)\right|} \le L_n \end{cases} \tag{10}$$

where $n = 6k\pm1$ with k being 1, 2, 3, ….

Based on (9), an objective function F_{obj} has to be formed to minimize the error [22]. The objective function plays an important role in leading the optimization algorithm to a suitable solution set. Here, F_{obj} is formed based on a squared error with more flexibility by adding constant weight values (w_n) to each squared error function as,

$$F_{obj} = \sum w_n \cdot \left(Obj_n - L_n\right)^2 \tag{11}$$

in which n =1, $6k\pm1$ with k being 1, 2, 3, ….

In addition to the maximum allowable harmonic level, the THD_i restriction could also be the objective function or included in (10) and prioritized with a suitable weight value. Notably, apart from the optimization constraint L_n, the following condition on the angles has to be included as well in order to ensure a proper rectification operation,

$$\alpha_0 < \alpha_1 < \alpha_2 < \cdots < \alpha_m < \alpha_0 + \frac{\pi}{3} \tag{12}$$

III. Single Switch Three-Phase Boost Rectifier System

In order to control DC-link current shape and magnitude following the waveforms shown in Fig. 2, a boost converter topology based on the electronic inductor [8], [18]-[21] concept is employed. Using the conventional boost topology has the advantage of boosting the output DC voltage to a suitable level when it is fed to an inverter. Moreover, as the DC-link current is controlled based on the load power, it has the advantage of keeping the THD_i independent of load profile. To better understand this, the inductor current in a steady-state Continuous Conduction Mode (CCM) is illustrated in Fig. 5. Here the switching frequency is considered to be high enough so that the rectified voltage and output voltage are constant during one switching cycle. Therefore, the inductor value can be calculated as,

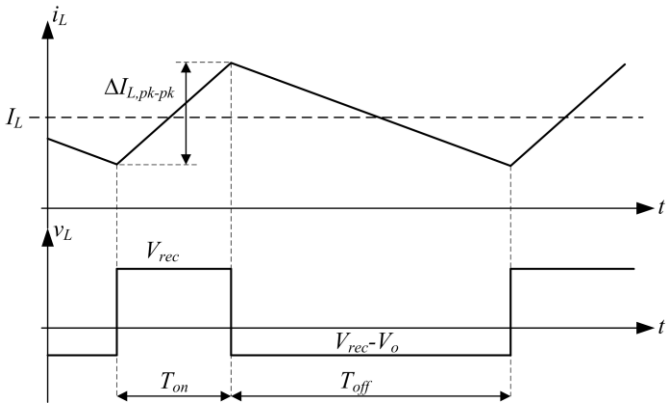


Fig. 5. Inductor current and voltage waveforms in one switching cycle.

$$L = \frac{V_o D(1-D)}{f_{sw}\Delta I_{L,pk-pk}} \quad \text{with} \quad f_{sw} = \frac{1}{T_{sw}} = \frac{1}{T_{on}+T_{off}} \tag{13}$$

where V_o is the output voltage, f_{sw} is the switching frequency, $\Delta I_{L,pk\text{-}pk}$ is the peak to peak inductor current ripple and D is the steady-state duty cycle of the boost converter. Using (13) the minimum required switching frequency (f_{sw}) can be selected by considering the maximum peak to peak inductor current ripple (D = 0.5) as,

$$f_{sw} \ge \frac{V_o}{4L\Delta I_{L,pk-pk,\max}} \tag{14}$$

Following (13) and (14) optimum switching frequency can be selected by making a tradeoff among the system efficiency, size and cost [23]. For example the system efficiency can be optimized by minimizing the switching frequency by allowing more ripple current for high power applications, therefore resulting in lower switching losses.

As mentioned before the THD_i can be independent of the load profile. The equation (13) can be rewritten based on output average current as,

$$L = \frac{V_o D(1-D)^2}{f_{sw} k_{ripple} I_o} \quad \text{with} \quad k_{ripple} = \frac{\Delta I_{L,pk-pk}}{I_L} = \frac{\Delta I_{L,pk-pk}(1-D)}{I_o} \tag{15}$$

in which k_{ripple} is the ripple factor, I_L is the average inductor current, and I_o is the average output current. Hence, keeping the ripple factor as a constant value will make the input current quality independent of the load profile. However, careful selection of the ripple factor is needed, as it has a direct relation with the ripple current, which as stated in (14) can affect the inductor size, system efficiency and cost [23].

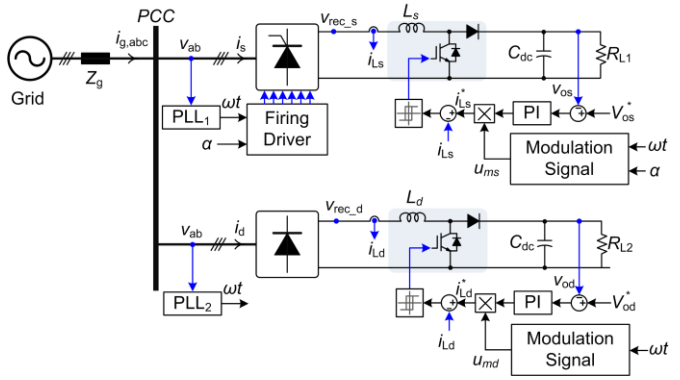


Fig. 6. Block diagram of the overall control structure implemented for the multi-rectifier system.

Fig. 6 depicts the block diagram of the overall control structure for the multi-rectifier units, where a hysteresis controller is adopted as the current controllers for the boost converters. The reference tracking performance of the current controller has an important role in the harmonic mitigation, thus fast current control methods such as hysteresis or dead-beat control should be employed. In order to synchronize the current controllers with the grid, for each rectifier unit a Second-Order Generalized Integrator (SOGI) based Phase Locked Loop (PLL) system is adopted [24]. For simplicity, only one line-to-line voltage is fed to the PLL. Therefore, the result will have a phase shift of 30° in respect to the phase voltage, which should be corrected within the reference current generator algorithm. Moreover, as it can be seen from the system schematics shown in Fig. 6, the firing angle of the thyristor based rectifier (i.e., SCR) should be applied according to the phase detected by the PLL.

IV. Results

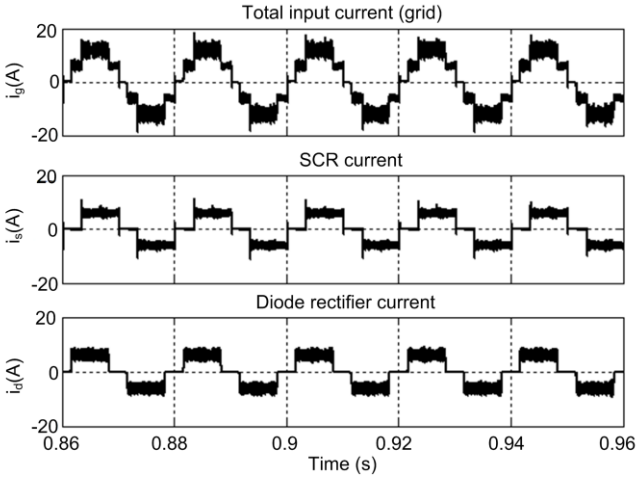
Referring to Fig. 6, the proposed approach has been validated through simulation and practical experiments. To bring simulation and experiments in a close agreement, practical parameters have been fully considered in simulation. Here the grid phase voltage is 220 V_{RMS} and the grid frequency is 50 Hz. The total output power was set at 5.5 kW and the output voltage of the boost converter is maintained at 700 V_{DC} by employing a Proportional Integrator (PI) controller and a hysteresis controller is adopted as the current controller, as shown in Fig. 6.The main component parameters of the entire systems are the same in the SCR and diode rectifier as listed in Table I.

A. Simulation Results

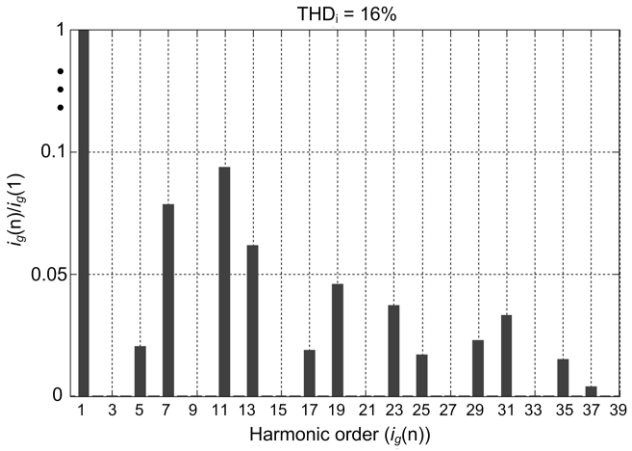
Simulations have firstly been conducted to verify the effectiveness of the proposed method. In the first study case, the effect of applying phase-shift strategy to the multisystem is tested with a simple flat current modulation, as it is shown in Fig. 3. The simulation results are presented in Fig. 7. As it can be observed in Fig. 7(a), the input currents of each unit (i_s and i_d) and the total current at the grid side (i_g) are controlled to be the desirable levels (flat currents). Theoretically, applying a phase-shift of 36° to the SCR unit should completely remove

TABLE I
MAIN CIRCUIT COMPONENTS OF THE ENTIRE MULTI-RECTIFIER SYSTEM.

Component	Symbol	Value
DC-link inductor	L_s, L_d	2 mH
DC-link Capacitor	C_{dc}	470 μF
Snubber (*RC*) across thyristor		100 Ω - 0.1 μF
Snubber (*RC*) across IGBT		82 Ω - 1 *n*F
Grid impedance	Z_g (L_g, R_g)	0.18 mH, 0.1 Ω



(a)



(b)

Fig. 7. Performance of the proposed method with flat currents applying a phase-shift of 36°: (a) current waveforms and (b) spectrum of the low-order harmonics at the total power level of 5.5 kW.

the 5th harmonic appearing in the grid. However, the presence of non-ideal parameters especially the grid impedance reduces the performance of the system slightly, and nonetheless the 5th harmonic is relatively lowered (i.e., 2.1 %), as shown in Fig. 7(b).

In order to further illustrate the influence of the phase-shift of the SCR unit on the grid current quality, the performance of the system has been analyzed by applying a wide range of the phase-shifts to the SCR unit. Fig. 8 shows the effect of applying different phase-shifts to the SCR on the grid current

THD_i, the low-order harmonics (i.e., 5^{th}, 7^{th}, 11^{th}, and 13^{th}) of the grid current i_g, and the Power Factor (PF). As it can be seen in Fig. 8(a), an increase of the firing can alter the power quality of the grid current. The lowest THD_i is observed in the case of a firing angle of 30°, where the grid current will be of 5-level with a relatively large PF = 0.952.

Moreover, mitigating of the low order harmonics (e.g., the 7^{th}) can also be achieved by introducing a phase-shift to the SCR unit (e.g., α_f = 27°). However, in return, the phase displacement increases when a large firing angle is applied, i.e. leading to a lower PF, as it is shown in Fig. 8(b). Specifically, seen from Fig. 8(a), it is better to control the firing angle within 20° to 40° in order to maintain a satisfactory THD_i while also minimize the low order harmonics. In contrast, when keeping the firing angle within 0° to 30°, the PF will be maintained between 0.95 and 0.97, as it is shown in Fig. 8(b). Therefore, for the case of applying square-wave current, the optimum firing angle (phase-shift) can be selected by applying an optimization algorithm as mentioned in Section II in order to mitigate the harmonics of interest when considering the THD_i and also the power factor. The above has confirmed that it is a flexible solution to mitigate the harmonics in multiple drive systems by using phase-shifted SCR units.

According to the simulation results, an almost-complete elimination of the 5^{th} harmonic occurs at 38° instead of 36°, which is the theoretical calculation (i.e., 180°/5 = 36°). This is due to the presence of the line impedance, which delays the charging of the DC-link inductor and therefore a slight phase shift from the theoretical value occurs [25]. However, in reality, the grid impedance is unknown and applying a real-time calculation of the grid-impedance to the proposed modulation method is not a feasible approach.

In the third case, in order to further reduce the THD_i and target at minimizing a higher number of the low order harmonics, novel current modulation has to be applied. Since only the low-order harmonics are of interest, the proposed method has been optimized according to (9)-(11) in order to attenuate the 5^{th}, 7^{th} and 11^{th} harmonics to be less than 1 % of the fundamental component (i.e., the selected optimization constraints). In addition, THD_i is also included in the objective function (THD_i < 13%). A MATLAB function – "fmincon" has been used for optimization in this case study. Fig. 9(a) presents the results of the multi-rectifier system with the proposed current modulation strategy, which confirms that a multi-level input current is achieved by the phase-shift based modulation scheme, contributing to a lower THD_i (Fig. 9(b)).

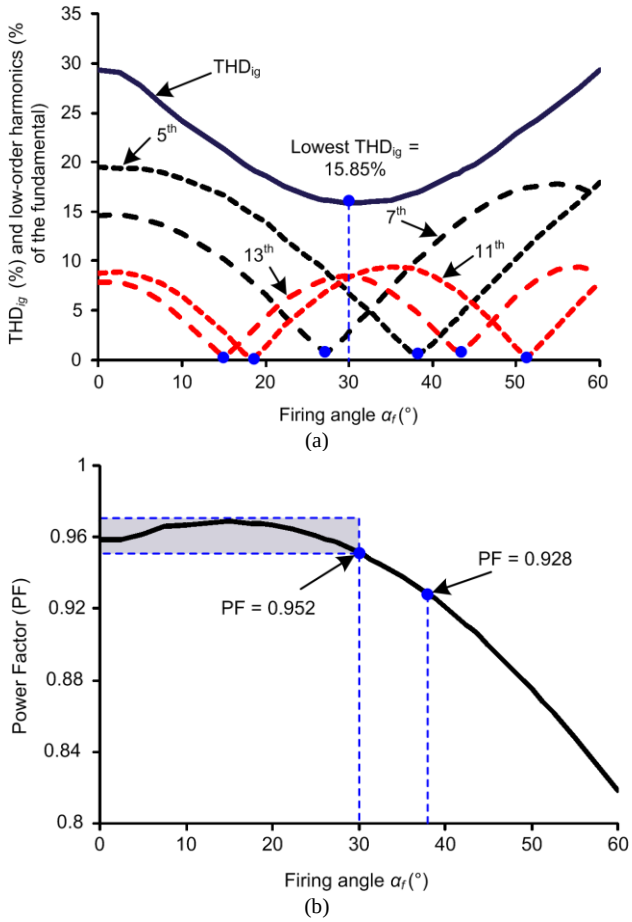


Fig. 8. Simulation results of the multi-rectifier system with different firing angles for the SCR unit: (a) total harmonic distortion and the low-order harmonic distribution of the input current i_g and (b) power factor.

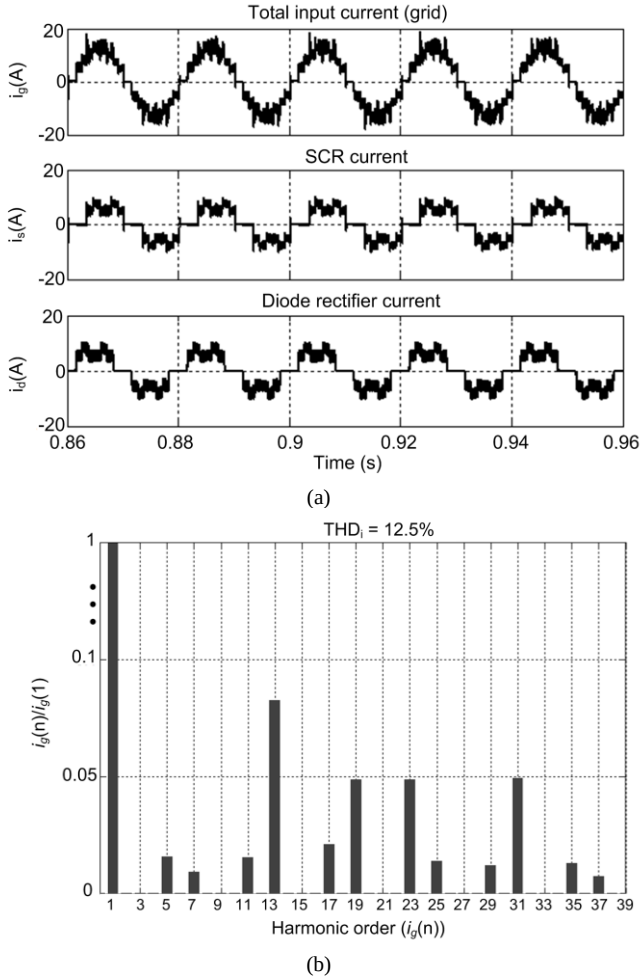
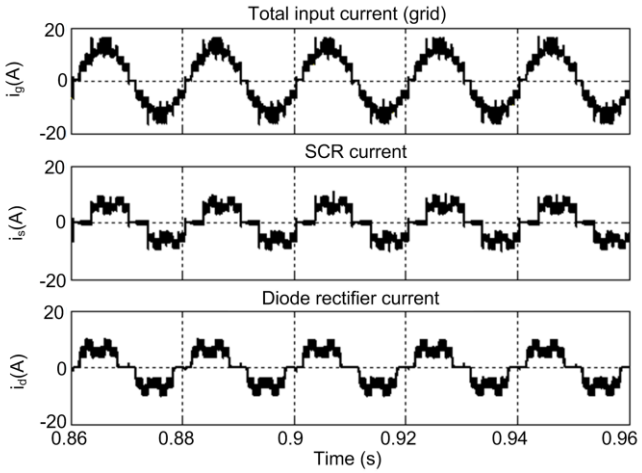
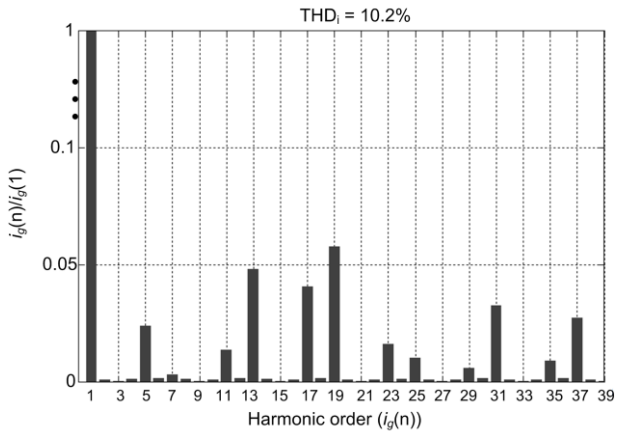


Fig. 9. Performance of the proposed method with current modulation when 5^{th}, 7^{th} and 11^{th} harmonics are optimized for reduction where the total power level is 5.5 kW: (a) current waveforms (phase a) and (b) spectrum of the low-order harmonics in the grid current.



(a)



(b)

Fig. 10. Performance of the proposed method with current modulation when THD_i is optimized where the total power level is 5.5 kW: (a) current waveforms (phase a) and (b) spectrum of the low-order harmonics in the grid current.

TABLE II
HARMONIC DISTRIBUTION OF DIFFERENT SIMULATED CASES AT A POWER LEVEL OF 5.5 KW.

Harmonic Mitigation Strategy	Harmonic Distribution and THD_i (%)				
	$\frac{i_g(5)}{i_g(1)}$	$\frac{i_g(7)}{i_g(1)}$	$\frac{i_g(11)}{i_g(1)}$	$\frac{i_g(13)}{i_g(1)}$	THD_i
Phase-Shifted Flat Current (Fig. 7)	2.1	7.9	9.4	6.2	16
[1]Optimized Novel Current Modulation (Fig. 9)	1.6	0.9	1.5	8.3	12.5
[2]Optimized Novel Current Modulation (Fig. 10)	2.4	0.3	1.4	4.8	10.2

1. Optimization objective is to minimize the low order harmonics and also a lower THD_i.
2. Optimization objective is only to achieve a lower THD_i.

TABLE III
OPTIMIZED CALCULATED CURRENT MODULATION PARAMETERS (NORMALIZED WITH $M_a = 1$).

Harmonic Mitigation Strategy	Diode Rectifier			SCR			
	I_{dc1}	I_{dc2}	α_1^o	I_{dc1}	I_{dc2}	α_1^o	α_f^o
[1]Optimized Novel Current Modulation (Fig. 9)	0.4	0.22	50	0.4	0.22	50	36
[2]Optimized Novel Current Modulation (Fig. 10)	0.41	0.2	50	0.41	0.2	49.9	38.7

1. Optimization objective is to minimize the low order harmonics and also a lower THD_i.
2. Optimization objective is only to achieve a lower THD_i.

However, due to the presence of non-ideal parameters, the 5th and the 11th harmonics are slightly higher than the optimization target (less than 1%), resulting from the effect of the grid impedance as previously discussed.

In addition, the flexibility of the proposed optimization method is also demonstrated in another case study, where the THD_i is selected as the optimization objective function, and the optimization results are shown in Fig. 10, where the grid current, the diode rectifier input current, the SCR input current, and the Fast Fourier Transform (FFT) spectrum of the total grid current are illustrated. It can be observed in Fig. 10(b) that a THD_i of 10.2 % is attained in the multi-rectifier system with the proposed method. Moreover, Table II summarizes the detailed harmonic content of the rectifier systems at a constant power level of 5.5 kW for comparison. It should be pointed out that different objectives have been included in the optimization algorithm as discussed in Section II. Following (5) and (7), Table III illustrates the estimated current modulation parameters for the two optimized cases with normalized amplitudes.

It should be noted that the aforementioned case studies were performed based on an assumption that each rectifier unit draws an equal amount of current from the grid; otherwise, the rectified voltages V_{rec_s} and V_{rec_d} (see Fig. 6) are different due to the phase-shift and thus leading to different boost conversion gain ratio and may complicate the harmonic distributions.

In addition to the effect of phase-shift, in real-world applications the two rectifier units do not necessarily operate at the same power level. Since the system is not dependent on the load profile, the power level itself is not the concern, and the ratio between output-power levels of the rectifier units are of importance. Therefore, as long as the following equation holds true, the rectifiers will draw equal amount of current from the grid; otherwise it should be reflected in the optimization process in one of the objective functions.

$$\frac{P_{o\_d}}{P_{o\_s}} \times \cos(\alpha_f) = 1 \tag{16}$$

where P_{o_d} and P_{o_s} are the output power of the diode rectifier and SCR unit, respectively.

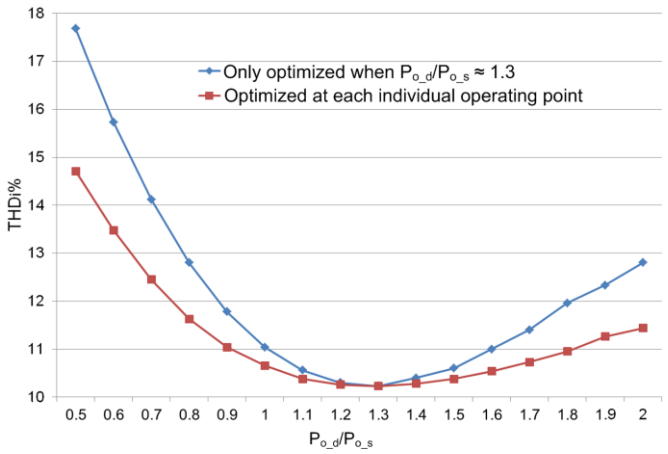


Fig. 11. Performance comparison of the multi-drive system at different output power ratios.

To examine the performance of the system when the output power of each rectifier unit is not balanced according to (16), different power ratios have been evaluated as illustrated in Fig. 11. In order to better realize this effect, the last case where the THD_i was targeted for optimization for different power level is considered again. The optimized firing angle for this case ($\cos(\alpha_0) \approx 1/1.3$) denotes that the rectifiers draw an equal amount of currents, when the output power of the diode rectifier is 1.3 times of the output power of the SCR unit; otherwise the THD_i = 10.2% mentioned in Table II cannot be obtained. This is clearly demonstrated in Fig. 11, where the system is tested at different output power ratios (blue curve). However, if this situation is considered in the optimization objective function by reflecting (16), a compensated result can be obtained (red curve).

As it can be seen, by applying a specific set of current modulation parameters at each operating point (i.e., power ratio) the increased THD_i due to the unbalanced loading of the rectifier units can be maintained at a lower level. Fig. 12 shows the estimated parameters for a wide range of power ratio variations (i.e., unbalanced loads) following Fig. 11.

Notably, to reduce computation complexity and to guarantee the smooth performance of the proposed method different pre-calculated current modulation parameters with their corresponding power ratios should be included as a look-up table in the controller. Therefore, by including a communication between each rectifier unit, suitable combinations of the input currents at the PCC can be made under variety situations.

B. Practical Verification

Experimental tests have been carried out on a 5.5-kW multi-rectifier system, which consists of two rectifier units (one diode rectifier and one SCR unit). Fig. 13 shows the prototypes used in the experimental tests, where Fig. 13(a) depicts a photograph of the three-phase diode rectifier unit and

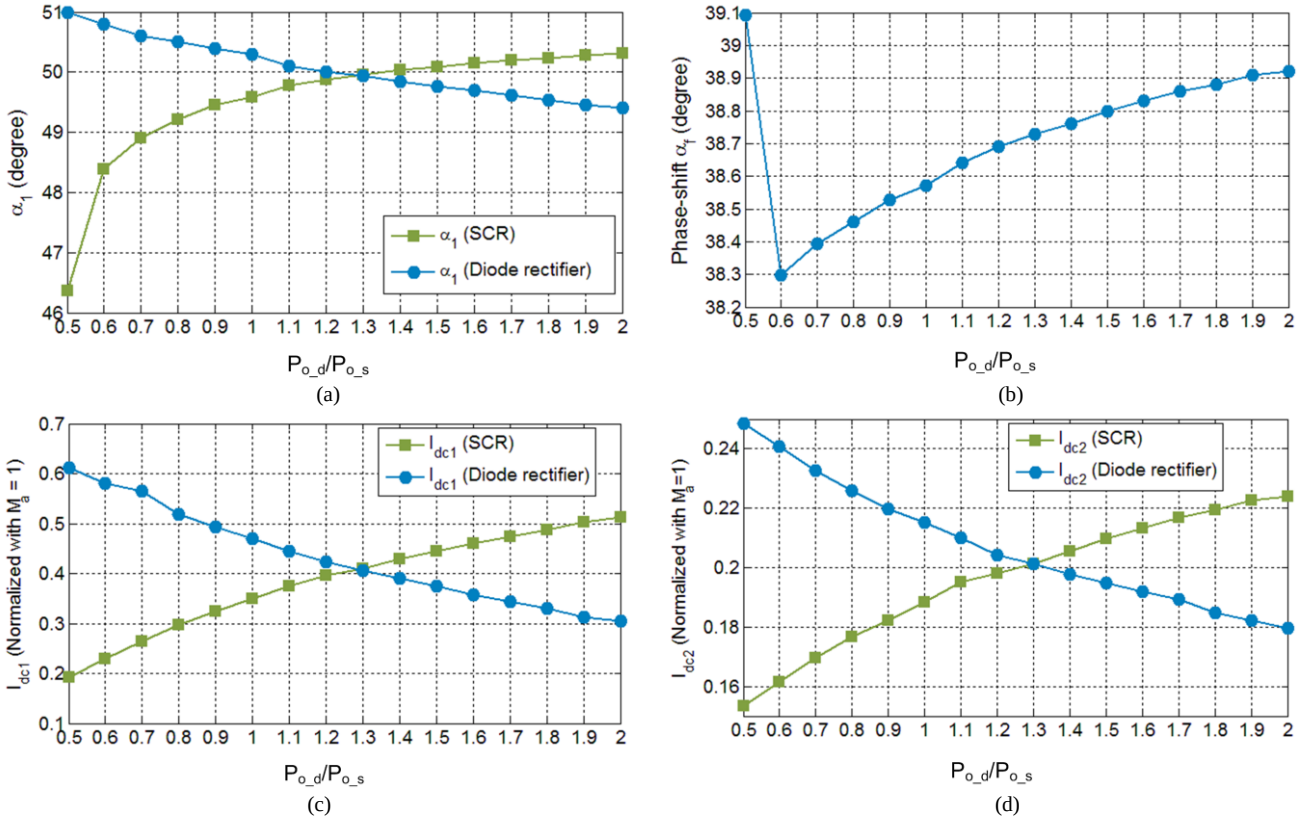
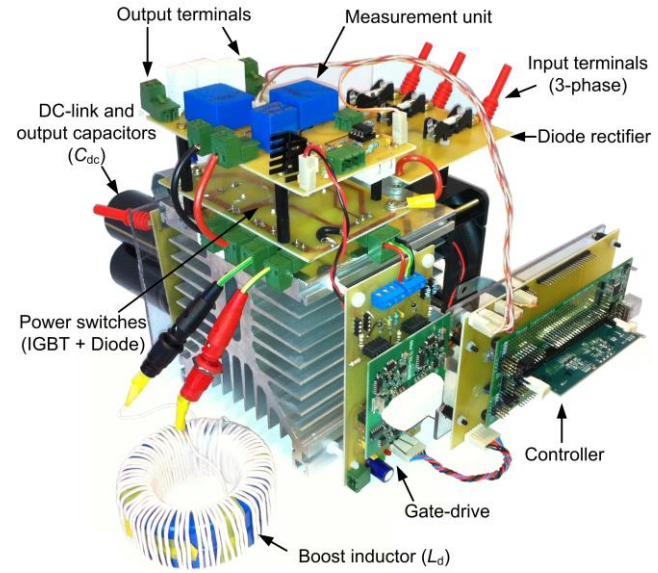
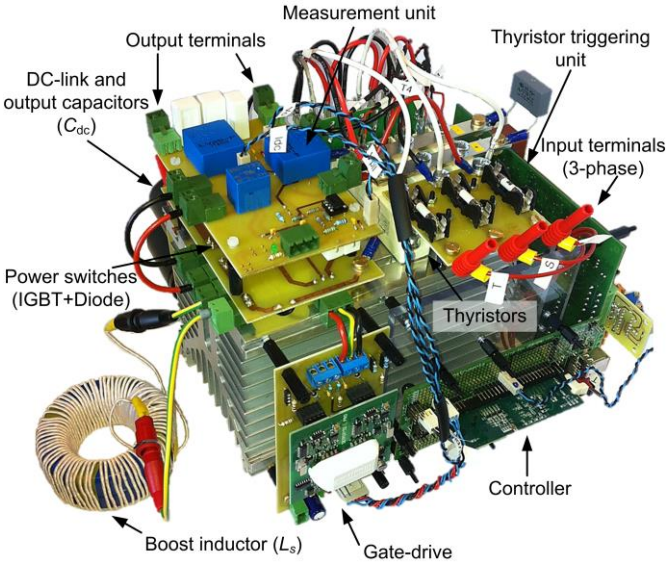


Fig. 12. Estimated modulation parameters of the rectifier units for minimizing grid current THD_i optimized for different power ratios (P_{o_d}/P_{o_s}): (a) phase angle α_1, (b) applied phase-shift between rectifiers (firing angle), (c) magnitude of the first added level (I_{dc1}), and (d) second added level magnitude (I_{dc2}) at the DC-link.



(a)



(b)

Fig. 13. Photograph of implemented single switch three-phase boost rectifier for (a) diode rectifier and (b) SCR system.

Fig. 13(b) shows the three-phase SCR unit, including the boost converter for each unit. Table IV summarizes the employed modules in the implemented prototypes.

Fig. 14 shows the performance of the two-rectifier system with a flat current modulation, where the firing angle for the SCR unit is set to 36° for comparison and the input power is also measured ($P_{in} \approx 6$ kW). It can be seen that a relatively low 5th-order harmonic (0.3 A, i.e., 2.37 % of the fundamental) is achieved by introducing a phase-shift of 36° for the SCR unit. Moreover, the THD of the input grid current is around 16.2 %. When compared with the simulations, the experimental results are in a close agreement with those shown Fig. 7.

The occurrence of the current spikes in the SCR current

TABLE IV
EMPLOYED MODULES IN THE IMPLEMENTED PROTOTYPES.

Module	Part-Number	Qty
Three-phase diode rectifier	SKD30	1
Three-phase SCR	SKKT 106/16	3
IGBT-diode	SK60GAL125	2
IGBT gate drive	Skyper 32-pro	2
SCR triggering circuit	RT380T	1
Current measurement	HX-15	2
Voltage measurement	LV25-P	4
Controller	TMS320F28335	2

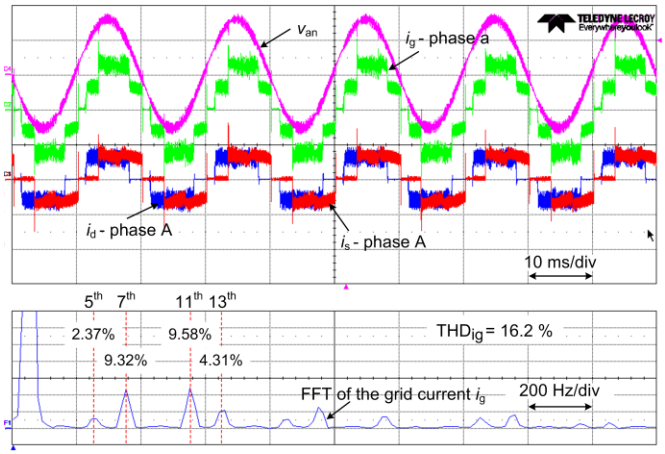


Fig. 14. Experimental results (phase a) of the multi-drive system with a flat-current modulation at $\alpha_f = 36°$, $P_{in} \approx 6$ kW, $V_o = 700$ V: grid current i_g [10 A/div], grid phase voltage v_{an} [200 V/div], diode rectifier input current i_d [10 A/div], SCR unit input current i_s [10 A/div], and Fast Fourier Transform (FFT) analysis of the grid current [500 mA/div].

(e.g., i_s) at the point of commutation is due to the presence of the snubber branches in the SCR unit. In practice, to avoid SCR unit failure and to reduce the overvoltage to a reasonable limit, an RC snubber branch is connected across each thyristor. In order to damp the current spikes, small AC-side inductors can be placed in series prior to the SCR unit.

In order to further verify the effect of phase-shifting operation of the SCR unit on the power quality of the grid currents, more tests have been conducted on the same system with different phase-shifting angles (i.e., firing angles). The results are shown in Fig. 15 and it is also compared with the simulation results shown in Fig. 8. It can be observed in Fig. 15 that the lowest THD$_i$ (i.e., 16.04 %) is achieved with a relatively large PF of 0.94 when $\alpha_f = 36°$. The results are in good consistence with the simulation results. The above tests have validated that by introducing an appropriate phase-shift to the SCR unit, a lower THD$_i$ and/or a minimization of the low order harmonics can be achieved.

Furthermore, the novel current modulation scheme is then applied to the two-rectifier system in order to increase the control flexibility in terms of minimizing the selected harmonics of interest and also the THD$_i$ (i.e., Table III). Firstly, the control objective is to lower the THD$_i$ and also to reduce the 5th, 7th, and 11th harmonics, where thus the optimization algorithm is also used. Fig. 16 demonstrates the

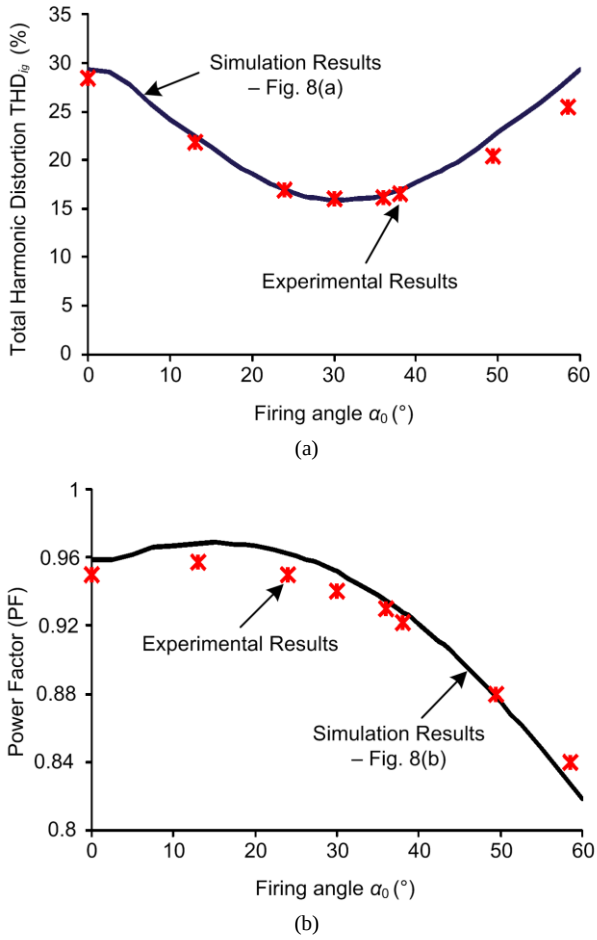


Fig. 15. Experimental results of the multi-drive system with different firing angles for the SCR unit: (a) total harmonic distortion of the input current i_g and (b) power factor.

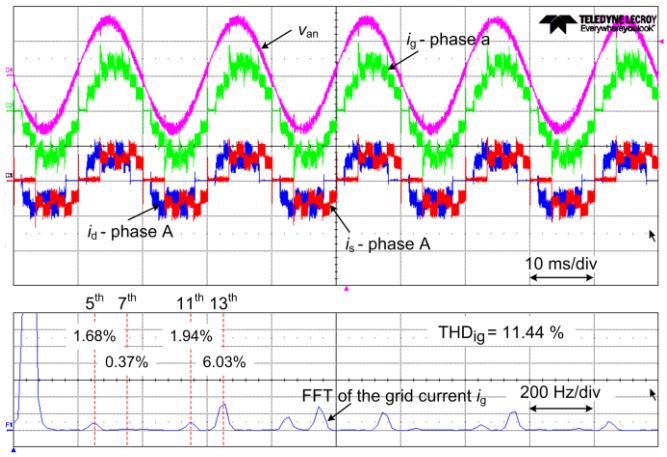


Fig. 16. Experimental results (phase a) of the multi-drive system with the novel current modulation scheme at $P_{in} \approx 6$ kW, $V_o = 700$ V, targeting at reducing the low order harmonics and also a lower THD$_i$: grid current i_g [10 A/div], grid phase voltage v_{an} [200 V/div], diode rectifier input current i_d [10 A/div], SCR unit input current i_s [10 A/div], and Fast Fourier Transform (FFT) analysis of the grid current [500 mA/div].

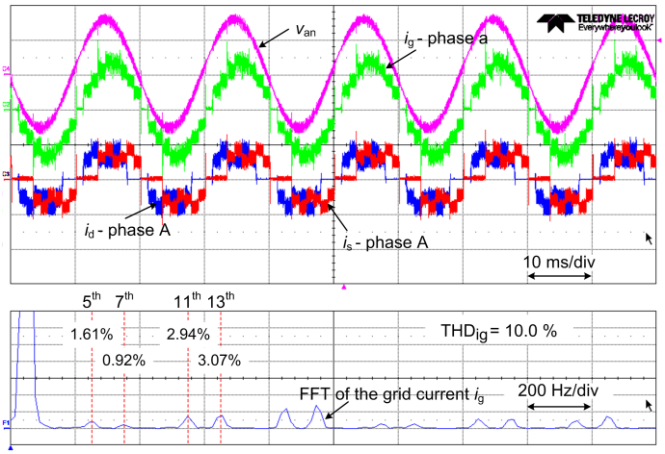


Fig. 17. Experimental results (phase a) of the multi-drive system with the novel current modulation scheme at $P_{in} \approx 5.85$ kW, $V_o = 700$ V, targeting at a minimized THD$_i$: grid current i_g [10 A/div], grid phase voltage v_{an} [200 V/div], diode rectifier input current i_d [10 A/div], SCR unit input current i_s [10 A/div], and Fast Fourier Transform (FFT) analysis of the grid current [500 mA/div].

performance of the multi-drive system equipped with the novel modulation technique, which targets not only a lower THD$_i$ but also an elimination of the low order harmonics. It can be seen in Fig. 16 that the 5th, 7th, and 11th order harmonics are almost completely eliminated, since they are considered in the optimization function as shown in (11). In addition, a THD$_i$ of 11.5 % of the grid current is also obtained when applying the novel modulation scheme to both rectifier units, which is better than the case of only using the flat current modulation.

In order to further demonstrate the flexibility of the novel modulation scheme, another test has been carried out on the system. In this case, the optimization target is to only minimize the THD$_i$. Fig. 17 presents the performance of the multi-rectifier system with a control objective to lower the THD$_i$, where it shows that around 1.5% reduction of the THD$_i$ has been achieved compared to the case shown in Fig. 16. At the same time, the low order harmonics are at relatively low levels. The results are quite in agreement with the simulations. To sum up, both the experimental tests and the simulations have validated the effectiveness of current harmonic mitigations in multi-rectifier systems by means of: a) phase-shifting the currents drawn by SCR units and b) a novel current modulation scheme at the DC-link using a DC-DC converter. Those can significantly contribute to a good power quality in both the single-drive and the multi-drive systems.

V. Conclusion

In this paper, a new harmonic elimination approach by combining different non-linear loads has been proposed for three-phase multi-drive systems, where also Silicon Controlled Rectifiers (SCR) are adopted. The proposed method can enable the selected harmonic cancellation by adjusting the phase angle of the SCR, and thus it can contribute to an improved power quality of the main grid. Moreover, in order to further reduce the harmonics, a novel modulation scheme has been applied to the DC-DC converter at the DC-link of the drive system. The modulation scheme is able to eliminate the

harmonics of interest by adding or subtracting specific current levels with respect to the conventional modulation approach. As a consequence, the combination of multiple non-linear loads with the new modulation scheme offers much flexibility as well as cost-effectiveness for the multi-drive systems in terms of harmonic elimination. A main advantage of the proposed method is that the harmonic distribution remains the same regardless of load profile variations.

In order to maximize the system efficiency, the added boost converter at the DC-link of the front-end rectifier should be optimized. Design and optimization of the traditional boost converter has been studied extensively in the past years. However, the traditional boost topology efficiency can be improved to a limited extent, as it should be designed for the total output power. Therefore, the future work will be focused on investigating alternative topologies and smart control strategies to minimize the power losses covering a wide range of power levels.

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