Modular Online Uninterruptible Power System Plug’n’Play Control and Stability Analysis

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Modular Online Uninterruptible Power System
Plug’n’Play Control and Stability Analysis

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Abstract—in this paper, a plug’n’play control strategy proposed for modular online UPS system is presented, which allows to plug the UPS modules in or out randomly. This provides a lower difficulty for the maintenance of the whole system. A two level control scheme was proposed, including local controllers to achieve active and reactive power sharing and central controllers to maintain synchronization capability, which allows the online UPS modular system having faster dynamic performance according to the standard IEC 62040-3. A detailed small signal mathematical model was developed in order to analyze the proposed modular online UPS system. Experimental results and data are presented to validate the stability analysis and support the proposed plug’n’play control feasibility.

Index Terms—modular online UPS system, phase control, stability analysis.

NOMENCLATURE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>ΔQ</td>
<td>Matrix for phase reference</td>
</tr>
<tr>
<td>Δδ</td>
<td>Matrix for phase angle of DC/AC module</td>
</tr>
<tr>
<td>Kqv</td>
<td>Matrix for phase proportional term in central controller</td>
</tr>
<tr>
<td>Kqv0</td>
<td>Matrix for phase integer term in central controller</td>
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<td>Kpp</td>
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<td>Matrix for output reactive power</td>
</tr>
<tr>
<td>ΔEδ0</td>
<td>Combined matrix of output voltage and phase</td>
</tr>
<tr>
<td>$e_{odi}$</td>
<td>d-axis component of output voltage of DC/AC #i</td>
</tr>
<tr>
<td>$e_{oqi}$</td>
<td>q-axis component of output voltage of DC/AC #i</td>
</tr>
<tr>
<td>$E_{odi}$</td>
<td>Matrix of output voltage dq component</td>
</tr>
<tr>
<td>$E_{oqi}$</td>
<td>d-axis component of reference voltage of DC/AC #i</td>
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</tr>
<tr>
<td>$E_{odi}$</td>
<td>Matrix of reference voltage dq component</td>
</tr>
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<td>$I_ n$</td>
<td>n×n identity matrix</td>
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<td>Zpi</td>
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</tr>
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</table>

I. INTRODUCTION

NOWAYS a large number of advanced electric equipment, such as medical equipment, communication facilities and data centers, are penetrating into our daily life [1]. Online UPS system is becoming an effective equipment to solve the concerns about the power quality and reliability [2], [3]. In [4] and [5], a kind of poor power factor UPS structure is proposed using rectifier and battery as the DC source of the UPS while a PFC is chosen to form the DC side in order to enhance UPS power factor performance in [6] and [7]. For the sake of smaller current and voltage stress and multi-output
functionality, structures based on dual active bridge (DAB) converter are presented in [8] and [9]. Compared with the aforementioned structures, modular parallel online UPS systems are receiving more and more attention due to their high flexibility [10]. Due to the physical parameters differences that may cause high circulating currents among the paralleled DC/AC modules, parallel algorithms, like those proposed in [11]-[31], are becoming essential technology in the implementation of a modular online UPS system. Active and reactive power sharing, voltage amplitude, frequency and phase are common basic elements that most of parallel control algorithms are taken into consideration in modular UPS systems.

By considering the existence of intercommunications, parallel technology can be categorized into two main groups [11]. With these critical communications among the modules, active and reactive power are well controlled and equally shared among different modules. For instance, centralized control [12], master-slave control [13], [14] and average load sharing control [15] are three of the main techniques that rely on inter-communications. However, these critical intercommunications bring about some serious issues, such as reduced reliability, robustness and modularity.

As a consequence, parallel control based on droop methods have been proposed [16]-[23]. Basic type of droop control (mainly a $P$-controller for power regulation) is proposed in [16]-[20]. Hereby, it is assumed that the output impedance of the DC/AC in the UPS is mainly inductive. Thus, the active power of each DC/AC module is calculated in order to modify its own output voltage frequency, while reactive power is also required to regulate output voltage amplitude. Thus output voltage of different DC/AC modules is regulated to the same value, while contributing to both active power and reactive power sharing among them. In order to analyze droop controller impact on system performance, detailed mathematical models are established [20]. Moreover, by modifying the DC/AC output impedance, the control can be simplified and improved. So virtual impedance concept is introduced by [21]. Additionally, in [22], derivative component of the active and reactive power regulation is considered in order to enhance the parallel accuracy. Accurate small-signal analysis has been achieved on both stability impacts and controller parameters selection. However, droop-controlled UPS system output voltage frequency and amplitude are inherently load-dependent. Thus, serious frequency deviations may occur under heavy-load operation, being not acceptable for bypass operation in online UPS system. On the other hand, output voltage amplitude slightly changes according to different load currents. As a result, secondary controllers are proposed to compensate such a kind of voltage and frequency deviations [27].

Furthermore, in addition of the adjust of frequency, a phase loop can be included, which allows the increasing of the gain droops to get a faster response, but keeping the system damping level, that is, it is possible to accelerate the response without leading the system to a under-damped condition [24], [25]. Additionally, active power sharing among DC/AC modules should be also taken into consideration. Instead of using only active and reactive power as the feedback for power regulation, a power reference is inserted into the regulation loop in [28] to enhance a faster dynamic performance. Moreover, a cross combination of active and reactive power feedback is considered in [29]. In order to achieve a tight control on power, a PI or PD controller for power regulation is used in [30]. Virtual impedance, mentioned in [27], shows outstanding improvements on both power sharing and harmonic current sharing performance. Since in the proposed online UPS system, inductor current is measured to achieve inner current loop, a virtual impedance loop is inserted into the inner control loop to achieve both active power and harmonics sharing. Thus a voltage amplitude drop may occur due to the virtual impedance loop. Thus special efforts must be taken to compensate the output voltage phase shift and amplitude drop. As shown in Fig. 1, two conventional PI controllers, $G_{v\_rec}$ and $G_{ph\_rec}$, are used to restore output voltage amplitude and to adjust the phase shift in order to keep the UPS system output voltage tightly synchronized with the utility grid voltage. In Fig. 1, different color lines in the CAN bus network denote different communication addresses for each phase. Each DC/AC module receives the amplitude and phase recover value through the CAN bus network. However, it can be seen that such kind of control architecture relies too much on the communication network. The central controller should be confirmed of the exact working numbers of the DC/AC modules in order to calculate the voltage amplitude and phase recovery reference. This will decrease the system reliability and increase the maintain cost of the system.

In order to achieve plug'n'play capability, an improved control architecture is proposed as shown in Fig. 2 by measuring voltage and frequency directly from the AC critical bus and removes the average blocks. Thus the central controller can operate at any time without knowing the exact numbers of
DC/AC modules. Moreover, a small signal mathematical model is established to analyze critical parameters performance on the proposed online UPS system output voltage.

This paper is organized as follows. Section II depicts proposed plug’n’play control diagram. Section III shows the small signal modeling and the stability analysis with the experimental results is shown in Section IV. Section V presents the improved control experimental results. Finally, conclusions are given in Section VI.

II. PROPOSED CONTROL

The proposed plug’n’play control diagram is presented in Fig. 2. It can be observed that the central controller measures the AC bus voltage directly without using the average block \((V_{1a}+V_{2a}+...+V_{na})/n\) used in Fig. 1. With the previous control, the exact number of the connected units must be refreshed in real-time to allow the correct calculation of the average value. For instance, if one DC/AC module plugs out and the \(n\) is kept the same, the output of average block will become smaller, which means that the feedback for the central controller will send an improper value for each unit in order to compensate the output voltage, which will affect the AC bus voltage controllability. Similarly, for phase regulation in the central controller, an improper average value calculation will imply a wrong phase compensation value, resulting in an abnormal system operation. In addition, average block depends too much on the communication network, which will decrease the system reliability.

Hereby two typical \(PI\)s are used to recover the voltage amplitude and phase,

\[
G_{v\text{-rec}} = k_{pv\text{-sec}} + k_{iv\text{-sec}} \frac{s}{s} \quad (1)
\]

\[
G_{ph\text{-rec}} = k_{ph\text{-sec}} + k_{ip\text{-sec}} \frac{s}{s} \quad (2)
\]

The inner loop for the DC/AC modules is considered in \(a\beta\) frame, which is shown in Fig. 3. References are modified in \(abc\) frame and then transferred to \(a\beta\) frame as shown in Fig. 3. Two conventional \(PR\) controllers are used for the voltage and current loop,

\[
G_v(s) = k_{pv} + \frac{k_{pv} s}{s^2 + \omega_o^2} + \sum_{h=5,7} \frac{k_{h,v} s}{s^2 + (\omega_o h)^2} \quad (3)
\]

\[
G_c(s) = k_{pc} + \frac{k_{pc} s}{s^2 + \omega_o^2} + \sum_{h=5,7} \frac{k_{h,c} s}{s^2 + (\omega_o h)^2} \quad (4)
\]

being \(k_{pv}\), \(k_{pc}\), \(\omega_o\), \(k_{h,v}\), \(h\), \(k_{h,c}\) as voltage proportional term, fundamental frequency voltage resonant term, fundamental frequency, the \(h^{th}\) harmonic voltage compensation term, harmonic order, current proportional term, fundamental frequency current resonant term and the \(h^{th}\) harmonic current compensation term respectively. The local controller has the ability of compensating harmonics due to nonlinear load, whose behavior in closed loop is shown in Fig. 4. Hereby the local controller bandwidth is designed to be around 1.5kHz
since the switching frequency is 10kHz. And the parameters range is chosen to be around the parameters shown in TABLE I- Control Parameters (DC/AC modules). At the same time, a bypass behavior is achieved at both 50Hz and harmonic frequency point (250Hz, 350Hz). Also 0dB is achieved at these frequency points.

As mentioned in [22], when the DC/AC output impedance is designed to be mainly resistance, the active power and reactive power that DC/AC module injects into the AC bus can be regulated by output voltage amplitude and phase angle respectively. Thus a virtual impedance loop and a $Q-\phi$ droop are embedded into the control scheme to realize parallel operation and power sharing as shown in Fig. 3.

\begin{equation}
\delta_{nk} = \delta_{nk\text{ref}} - k_{ph}Q_{nk}
\end{equation}

\begin{equation}
v_{nk} = v_{nk\text{ref}} - i_{Labc}R_{vir}
\end{equation}

where $n$ is the number of DC/AC module ($1, 2, 3...N$), $k$ is the phase order ($a, b, c$), $V_{nk\text{ref}}$ the nominal voltage reference, $R_{vir}$ the virtual resistor, $\delta_{nk\text{ref}}$ the nominal phase reference, $k_{ph}$ the phase regulating coefficients, and $Q_{nk}$ the reactive power of each phase of each DC/AC module. Hereby, instead of modifying frequency, the proposed control regulates the phase angle according to output power. Thus a better frequency behavior is achieved.

### III. SMALL SIGNAL MODEL AND STABILITY ANALYSIS

This Section presents the small-signal model derivation process for the proposed online UPS system. Before modeling the system, some assumptions must be kept in mind, which are described as follows:

1) Consuming that the inner loop for DC/AC modules is well tuned and working well. Also the proposed controller presented in Fig. 5 presents a lower bandwidth compared to the PR internal controllers since they include low pass filters in the phase and voltage loops, as well, the PLL naturally presents a lower bandwidth compared to its central frequency. Thus the DC/AC modules can be considered as an ideal voltage source.

2) Since local controllers are carried out in the stationary-reference-frame ($\alpha\beta$), mathematical model is fully considered in $\alpha\beta$ frame as well.

#### A. Small Signal Model for the Proposed Controller

In Fig. 5, the small signal model for the proposed controller is presented, where the $LC$ filters of the three DC/ACs are connected to the same AC critical bus.

Thus,

\begin{equation}
\Delta E_o = \Delta E_{o1} = \Delta E_{o2} = \Delta E_{o3} = \left(\Delta E_{o1} + \Delta E_{o2} + \Delta E_{o3}\right) / 3
\end{equation}

\begin{equation}
\Delta \delta_o = \Delta \delta_{o1} = \Delta \delta_{o2} = \Delta \delta_{o3} = \left(\Delta \delta_{o1} + \Delta \delta_{o2} + \Delta \delta_{o3}\right) / 3
\end{equation}

being $\Delta E_{o1}$, $\Delta E_{o2}$, $\Delta E_{o3}$ the AC critical bus voltage, DC/AC #1 output voltage, DC/AC #2 output voltage and DC/AC #3 output voltage respectively and $\Delta \delta_{o1}$, $\Delta \delta_{o2}$ and $\Delta \delta_{o3}$ the AC critical bus phase, DC/AC #1 phase, DC/AC #2 phase and DC/AC #3 phase.

As a result, the $\Delta E_{m1}$ can be derived,

\begin{equation}
\Delta E_{m1} = \frac{\omega_{fin}}{s + \omega_{fin}} \Delta E_o = \frac{1}{3} \frac{\omega_{fin}}{s + \omega_{fin}} \left(\Delta E_{o1} + \Delta E_{o2} + \Delta E_{o3}\right)
\end{equation}

\begin{equation}
\Delta E_{m1} = \frac{1}{3} \left(\Delta E_{m1} + \Delta E_{m2} + \Delta E_{m3}\right)
\end{equation}

being $\Delta E_{m1}$ the RMS voltage value of DC/AC #1. Similar equation can be obtained in DC/AC #2 and #3.

Since voltage restoration is carried out in phase and amplitude respectively, the small-signal model can be derived by considering the two main loops, namely RMS voltage restoration loop and phase regulation loops,

\begin{equation}
\Delta E_{r1} = \frac{1}{3} \left[ \begin{array}{ccc} k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \end{array} \right] \Delta E_{r2} = \frac{1}{3} \left[ \begin{array}{ccc} k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \end{array} \right] \Delta E_{r3} = \frac{1}{3} \left[ \begin{array}{ccc} k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \end{array} \right] \Delta E_{m2}
\end{equation}

\begin{equation}
\Delta E_{m3} = \frac{1}{3} \left[ \begin{array}{ccc} k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \end{array} \right] \Delta E_{m2} = \frac{1}{3} \left[ \begin{array}{ccc} k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \\
 k_{pv\_sec} & k_{pv\_sec} & k_{pv\_sec} \end{array} \right] \Delta E_{m3}
\end{equation}

\begin{equation}
\Delta \delta_{r1} = \frac{1}{3} \left[ \begin{array}{ccc} k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \\
 k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \\
 k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \end{array} \right] \Delta \delta_{r2} = \frac{1}{3} \left[ \begin{array}{ccc} k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \\
 k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \\
 k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \end{array} \right] \Delta \delta_{r3} = \frac{1}{3} \left[ \begin{array}{ccc} k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \\
 k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \\
 k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \end{array} \right] \Delta \delta_{p1}
\end{equation}

\begin{equation}
\Delta \delta_{p2} = \frac{1}{3} \left[ \begin{array}{ccc} k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \\
 k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \\
 k_{\delta\_sec} & k_{\delta\_sec} & k_{\delta\_sec} \end{array} \right] \Delta \delta_{p3}
\end{equation}

\begin{equation}
\begin{bmatrix}
\Delta \delta_{p1} \\
\Delta \delta_{p2} \\
\Delta \delta_{p3}
\end{bmatrix} = \frac{1}{3} \begin{bmatrix}
k_{ph} & 0 & 0 \\
0 & k_{ph} & 0 \\
0 & 0 & k_{ph}
\end{bmatrix} \begin{bmatrix}
\Delta \delta_{r1} \\
\Delta \delta_{r2} \\
\Delta \delta_{r3}
\end{bmatrix}
\end{equation}

RMS block is considered as a low pass filter, as shown in Fig. 5. Thus, output voltage dynamics can be expressed as,
From the perspective of small-signal analysis, the output of the phase detector is considered as $(Δδ_o−Δδ_p)$. Consequently, based on (8), phase-signal equations are derived as,

$$
\begin{align*}
\begin{bmatrix}
\dot{\Delta \omega}_p \\
\dot{\Delta \omega}_o \\
\dot{\Delta \omega}_m
\end{bmatrix} &= X_3 \begin{bmatrix}
\Delta \delta_1 \\
\Delta \delta_2 \\
\Delta \delta_3
\end{bmatrix} + X_4 \begin{bmatrix}
\Delta \delta_1 \\
\Delta \delta_2 \\
\Delta \delta_3
\end{bmatrix} \\
\begin{bmatrix}
\dot{\Delta \delta}_p \\
\dot{\Delta \delta}_o \\
\dot{\Delta \delta}_m
\end{bmatrix} &= X_5 \begin{bmatrix}
\Delta \omega_1 \\
\Delta \omega_2 \\
\Delta \omega_3
\end{bmatrix} - X_6 \begin{bmatrix}
\Delta \delta_1 \\
\Delta \delta_2 \\
\Delta \delta_3
\end{bmatrix}
\end{align*}
$$

where,

$$
\begin{align*}
X_3 &= \begin{bmatrix}
k_{pp} & 0 & 0 \\
0 & k_{pp} & 0 \\
0 & 0 & k_{pp}
\end{bmatrix}, \\
X_4 &= \begin{bmatrix}
k_{ip} & 0 & 0 \\
0 & 0 & k_{ip} \\
0 & 0 & k_{ip}
\end{bmatrix}, \\
X_5 &= \begin{bmatrix}
k_{pp} & 0 & 0 \\
0 & k_{pp} & 0 \\
0 & 0 & k_{pp}
\end{bmatrix}, \\
X_6 &= \begin{bmatrix}
k_{ip} & 0 & 0 \\
0 & k_{ip} & 0 \\
0 & 0 & k_{ip}
\end{bmatrix}
\end{align*}
$$

being $k_{pp}$ the proportional term and $k_{ip}$ the integral term in PLL scheme, respectively. As a result, a series of differential equation system is derived in a symbolic way as shown in (18)-(21) by combining (11), (13) and (17) it yields,

$$
\begin{align*}
\dot{\Delta \omega}_p &= (K_{pp} \omega_{fm} - K_{iv}) \Delta E_m - K_{pp} \omega_{fm} \Delta E_o \\
\dot{\Delta \delta}_p &= -K_{pp} \Delta \delta_p - K_{pp} \Delta \delta_o - K_{pp} \Delta \omega_p - K_{ip} \Delta \delta_p \\
\Delta \delta_p &= \Delta \omega_p
\end{align*}
$$

Considering the vectors $ΔX_r$ and $ΔX_o$ represented by,

$$
\begin{align*}
\Delta X_r &= \begin{bmatrix}
\Delta E_r \\
\Delta \delta_r \\
\Delta \omega_r \\
\Delta \delta_i
\end{bmatrix}^T \\
\Delta X_o &= \begin{bmatrix}
\Delta E_o \\
\Delta \delta_o \\
\Delta \omega_o \\
\Delta \delta_i
\end{bmatrix}^T
\end{align*}
$$

The differential equations (18)-(21) can be rewritten as,

$$
\begin{align*}
\dot{\Delta X}_r &= \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & K_{pp} & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{bmatrix} \Delta \dot{X}_r + \begin{bmatrix}
K_{pp} \omega_{fm} \\
0 \\
0 \\
0
\end{bmatrix} \Delta E_m + \begin{bmatrix}
K_{iv} \\
0 \\
0 \\
0
\end{bmatrix} \Delta \dot{Q}_{av}
\end{align*}
$$
where

\[
X_\delta = \begin{bmatrix}
-K_{p1} \phi_m & 0 & 0 & 0 \\
0 & 0 & -K_{d1} & -K_{d2} \\
0 & K_{pi} & -K_{pp} & -K_{p2} \\
0 & 0 & I_3 & 0 \\
\end{bmatrix}
\]

Here \(\Delta X_r\) and \(\Delta X_v\) are two vectors with 12 variables since \(\Delta E_{riv}, \Delta \delta_{riv}, \Delta \theta_{riv}, \Delta \delta_{riv}, \Delta E_{rvi}\) and \(\Delta \delta_{rvi}\) represent 1x3 matrices. Hence (24) can be rewritten as,

\[
\dot{\Delta}X_v = M_1 \Delta X_o + M_2 \Delta X_o + M_3 \Delta E_{riv} + M_4 \Delta Q_{av}.
\]  

(25)

As for the DC/AC inner control loops, only phase and amplitude of output voltage should be taken into consideration. However, the reactive power is calculated in a Cartesian coordinate system. So that output voltage of DC/AC is represented,

\[
\Delta E_{oi} = \Delta E_{odi} + j \Delta E_{oji},
\]

(26)

where, \(\Delta E_{odi} = E_{odi} \cos \delta_{odi} \), \(\Delta E_{oji} = E_{oji} \sin \delta_{odi} \),

\[
\delta_{odi} = \arctan(\Delta E_{oji} / \Delta E_{odi}).
\]  

(27)

Linearizing (27) at the equilibrium point,

\[
\Delta \delta_{odi} = \frac{\partial \delta_{odi}}{\partial E_{odi}} \Delta E_{odi} + \frac{\partial \delta_{odi}}{\partial E_{oji}} \Delta E_{oji}
\]

(28)

\[
= m_{odi} \Delta E_{odi} + m_{oji} \Delta E_{oji}
\]

The amplitude of the output voltage is represented as,

\[
\Delta E_{oi} = \Delta E_{odi} + j \Delta E_{oji}.
\]

(29)

Its linearization form around the equilibrium point is derived as,

\[
\Delta E_{oi} = n_{odi} \Delta E_{odi} + n_{oji} \Delta E_{oji}
\]

(30)

where \(n_{odi} = E_{odi} / \sqrt{\Delta E_{odi}^2 + \Delta E_{oji}^2} \), \(n_{oji} = E_{oji} / \sqrt{\Delta E_{odi}^2 + \Delta E_{oji}^2} \).

Thus the vector \(\Delta E_{oi}\) can be derived as,

\[
\Delta E_{oi} = \begin{bmatrix}
n_{odi} & n_{odi} & 0 & 0 & 0 & 0 \\
n_{odi} & n_{odi} & 0 & 0 & 0 & 0 \\
n_{odi} & n_{odi} & 0 & 0 & 0 & 0 \\
n_{odi} & n_{odi} & 0 & 0 & 0 & 0 \\
\end{bmatrix} \begin{bmatrix}
\Delta E_{odi} \\
\Delta E_{odi} \\
\Delta E_{odi} \\
\Delta E_{odi} \\
\end{bmatrix}
\]  

(31)

Rewriting (31) in symbolic form,

\[
\Delta E_{oi} = T_{f} E_{odi}
\]

(32)

Thus the vector \(\Delta E_{oi}\) can be derived as its vertical coordinate form \(\Delta X_{odi}\) as follows,

\[
\Delta X_o = \begin{bmatrix}
T_{f} & 0 \\
0 & I_6
\end{bmatrix} \Delta X_{odi} = T_{odi} \Delta X_{odi}
\]

(33)

and \(\Delta X_{odi}\) is,

\[
\Delta X_{odi} = \begin{bmatrix}
\Delta E_{odi} & \Delta E_{odi} & \Delta E_{odi} & \Delta \theta_{odi} & \Delta \delta_{odi} & \Delta \delta_{odi}
\end{bmatrix}
\]  

(34)

Furthermore, the same transformation process can be applied to the vector \(E_{riv}\),

\[
\Delta \delta_{riv} = m_{rdi} \Delta E_{rdi} + m_{rqi} \Delta E_{rqi}
\]

(35)

\[
\Delta E_{riv} = \begin{bmatrix}
m_{rdi} & m_{rqi} \\
0 & 0
\end{bmatrix} \begin{bmatrix}
\Delta E_{rdi} \\
\Delta E_{rqi}
\end{bmatrix}
\]

(36)

\[
\Delta \delta_{riv} = m_{rdi} \Delta E_{rdi} + m_{rqi} \Delta E_{rqi}
\]

\[
\Delta E_{riv} = \begin{bmatrix}
m_{rdi} & m_{rqi} \\
0 & 0
\end{bmatrix} \begin{bmatrix}
\Delta E_{rdi} \\
\Delta E_{rqi}
\end{bmatrix}
\]

Thus, it yields to,

\[
\begin{bmatrix}
\Delta E_{riv} \\
\Delta E_{riv} \\
\Delta E_{riv} \\
\Delta E_{riv}
\end{bmatrix} = \begin{bmatrix}
m_{rdi} & m_{rqi} \\
0 & 0
\end{bmatrix} \begin{bmatrix}
\Delta E_{rdi} \\
\Delta E_{rqi}
\end{bmatrix}
\]

(37)

Symbolically, (37) is rewritten as follows,

\[
\Delta E_{riv} = T_{f} E_{odi}
\]

(38)

and the vector \(\Delta X_{r}\) is derived as,

\[
\Delta X_{r} = \begin{bmatrix}
T_{f} & 0 \\
0 & I_6
\end{bmatrix} \Delta X_{odi} = T_{odi} \Delta X_{odi}
\]

(39)

where

\[
\Delta X_{rdi} = \begin{bmatrix}
\Delta E_{rdi} & \Delta E_{rdi} & \Delta E_{rdi} & \Delta \theta_{rdi} & \Delta \delta_{rdi} & \Delta \delta_{rdi}
\end{bmatrix}
\]

(40)

Substituting (33) and (39) in (25), it yields to,

\[
T_{odi} \Delta X_{odi} = M_1 T_{odi} \Delta X_{odi} + M_2 T_{odi} \Delta X_{odi} + M_3 T_{odi} \Delta X_{odi} + M_4 \Delta Q_{av}
\]

(41)

which describes the small signal behavior of the controller presented in Fig. 5 around a certain equilibrium point by considering \(\Delta E_{m}\) and \(\Delta Q_{av}\) as the input variables.

B. Small Signal Model for the Whole System

The load impedance and line impedances of the system can be defined respectively as,

\[
Z_{pi} = R_{pi} + jX_{pi}
\]

(42)

\[
Z_{L} = R_{L} + jX_{L}
\]

(43)

which admittances are shown as follows,

\[
Y_{pi} = 1/Z_{pi}
\]

(44)

\[
Y_{L} = 1/Z_{L}
\]

(45)

Consequently, the output currents can be derived as,

\[
\begin{bmatrix}
i_{odi} \\
i_{odi}
\end{bmatrix} = \begin{bmatrix}
G_{11} & -B_1 & G_{12} & -B_2 & G_{13} & -B_{13} \\
B_1 & G_{11} & B_2 & G_{12} & B_{13} & G_{13}
\end{bmatrix} \begin{bmatrix}
i_{odi} \\
i_{odi}
\end{bmatrix}
\]

(46)
where
\[ Y_{ij} = G_{ij} + jB_{ij} \]  
(47)

Thus (46) can be expressed in symbolic form as,
\[ i_{odi} = Y_{o} e_{odi} \]  
(48)

and by linearizing (48), it yields,
\[ \Delta i_{odi} = Y_{o} e_{odi} \]  
(49)

Since reactive power is obtained through an orthogonal system as,
\[ q_i = e_{odi} i_{odi} - e_{odi} i_{odi} \]  
(50)

Then, the small signal form of the reactive power is presented as,
\[
\begin{bmatrix}
\Delta q_1 \\
\Delta q_2 \\
\Delta q_3
\end{bmatrix} = I_o + E_o
\begin{bmatrix}
\Delta e_{odi1} \\
\Delta e_{odi2} \\
\Delta e_{odi3} \\
\Delta e_{odi3}
\end{bmatrix}
\]  
(51)

where
\[ I_o = \begin{bmatrix}
i_{odi1} & -i_{odi1} \\
0 & 0 & 0 \\
i_{odi2} & -i_{odi2} \\
0 & 0 & 0 \\
i_{odi3} & -i_{odi3} \\
0 & 0 & 0
\end{bmatrix}, \quad E_o = \begin{bmatrix}
-e_{odi1} & e_{odi1} & 0 & 0 & 0 \\
0 & -e_{odi2} & e_{odi2} & 0 & 0 \\
0 & 0 & 0 & 0 & -e_{odi3}
\end{bmatrix}.
\]

Thus the symbolic form for (50) is derived as,
\[ \Delta q = I_o \Delta e_{odi} + E_o \Delta i_{odi} \]  
(52)

By substituting (49) into (52), it yields,
\[ \Delta q = (I_o + E_o Y_o) \Delta e_{odi} \]  
(53)

Considering the first order low pass filter used to calculate the reactive power, it can be obtained,
\[ Q_{avl} = \frac{\omega_f}{s + \omega_f} q_i \]  
(54)

and the linearization form of the filter is obtained as follows,
\[
\begin{bmatrix}
\Delta Q_{avl1} \\
\Delta Q_{avl2} \\
\Delta Q_{avl3}
\end{bmatrix} = \begin{bmatrix}
\omega_f & 0 & 0 \\
0 & \omega_f & 0 \\
0 & 0 & \omega_f
\end{bmatrix}
\begin{bmatrix}
\Delta Q_{avl1} \\
\Delta Q_{avl2} \\
\Delta Q_{avl3}
\end{bmatrix}
\]
\[ + \begin{bmatrix}
\omega_f & 0 & 0 \\
0 & \omega_f & 0 \\
0 & 0 & \omega_f
\end{bmatrix}
\begin{bmatrix}
\Delta q_1 \\
\Delta q_2 \\
\Delta q_3
\end{bmatrix}
\]  
(55)

By combining (53), its symbolic form is,
\[ \Delta Q_{avl} = -\omega_f \Delta Q_{avl} + \omega_f \left( I_o + E_o Y_o \right) \Delta e_{odi} \]  
(56)

Relating the vector \( e_{odi} \) with \( X_{odi} \), we can rewrite (56) as,
\[ \Delta Q_{avl} = -\omega_f \Delta Q_{avl} + \omega_f \left( I_o + E_o Y_o \right) K_{x_{odi}} \Delta X_{odi} \]  
(57)

where
\[ K_{x_{odi}} = \begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix} \]

Thus (12) in a symbolic way and relating the vector \( \Delta E_o \) with \( \Delta X_o \),
\[ \Delta E_o = K_x \Delta X_o = K_x T_{odi} \Delta X_{odi} \]  
(58)

where
\[ K_x = \begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix} \]

Thus (12) can be rewritten as,
\[ \Delta E_m = -\omega_m \Delta E_m + \omega_m K_x T_{odi} \Delta X_{odi} \]  
(60)

Finally, an equation system composed by (41), (57) and (60) is obtained. On the other hand, there is a virtual impedance loop between \( E_r \) and \( E_o \) that can be expressed as,
\[ E_{ri} = E_{oi} + Z_v i_{oi} \]  
(61)

where
\[ \begin{bmatrix}
R_{x1} + jX_{x1} & 0 & 0 \\
0 & R_{x2} + jX_{x2} & 0 \\
0 & 0 & R_{x3} + jX_{x3}
\end{bmatrix} \]

Thus,
\[ e_{rdqi} = e_{odi} + Z_{vr} i_{odi} \]  
(62)

where
\[ Z_{vr} = \begin{bmatrix}
R_{x1} & -X_{x1} & 0 & 0 & 0 & 0 & 0 & 0 \\
X_{x1} & R_{x1} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & R_{x2} & -X_{x2} & 0 & 0 & 0 & 0 \\
0 & 0 & X_{x2} & R_{x2} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & R_{x3} & -X_{x3} & 0 & 0 \\
0 & 0 & 0 & 0 & X_{x3} & R_{x3} & 0 & 0
\end{bmatrix} \]

Substituting (48) in (62), it yields,
\[ e_{rdqi} = e_{odi} + Z_{vr} Y_o e_{odi} = (I_o + Z_{vr} Y_o) e_{odi} = K_{z_{rdqi}} e_{odi} \]  
(63)
By linearizing (63), we can obtain the following small signal approximation,

\[ \Delta e_{rdq} = K_{Z1} \Delta e_{odq} \]  

(64)

Then, relating (64) with \( \Delta X_{rdq} \) and \( \Delta X_{odq} \), it can be obtained:

\[ \Delta X_{rdq} = \begin{bmatrix} K_{ZY} & 0 \\ 0 & I_6 \end{bmatrix} \Delta X_{odq} = K_{rdq} \Delta X_{odq} \]  

(65)

\[ \Delta X_{rdq}^* = \begin{bmatrix} K_{ZY} & 0 \\ 0 & I_6 \end{bmatrix} \Delta X_{odq}^* = K_{rdq} \Delta X_{odq}^* \]  

(66)

By combining (41) and (66), it yields,

\[ T_{rdq} K_{rdq} \Delta X_{rdq} = M_1 T_{odq} \Delta X_{odq} + M_2 T_{odq} \Delta X_{odq} + M_3 \Delta E_m + M_4 \Delta Q_{av} \]  

(67)

Considering (57) and (67), we can rewrite (66) as,

\[ \Delta X_{rdq}^* = T^{-1}_{km} \begin{bmatrix} M_2 T_{odq} + M_4 \omega_f \left( I_o + Y_o E_o \right) K_{sxq} \end{bmatrix} \Delta X_{odq} + T^{-1}_{km} M_4 \omega_f \Delta Q_{av} \]  

(68)

where

\[ T_{km} = T_{rdq} K_{rdq} - M_1 T_{odq} \]  

(69)

Based on (57), (60) and (68), we can write the following state-space equation,

\[
\begin{bmatrix}
\Delta X_{rdq}^* \\
\Delta E_m^* \\
\Delta Q_{av}^*
\end{bmatrix} = A
\begin{bmatrix}
\Delta X_{odq} \\
\Delta E_m \\
\Delta Q_{av}
\end{bmatrix}
\]

(70)

where

\[ A = \begin{bmatrix}
X_8 & T^{-1}_{km} M_3 & -T^{-1}_{km} M_4 \omega_f \\
\omega_f T_{odq} & -\omega_f & 0 \\
\omega_f \left( I_o + Y_o E_o \right) K_{sxq} & 0 & -\omega_f
\end{bmatrix} \]

(71)

where \( X_8 = T^{-1}_{km} \left( M_2 T_{odq} + M_4 \omega_f \left( I_o + Y_o E_o \right) K_{sxq} \right) \).

### IV. Stability Analysis

In order to achieve the stability analysis of the system, load step was carried out in the experimental setup, which is shown in Fig. 7. The critical parameters are shown in TABLE I. Through dSpace, experimental data are extracted from the experimental setup, plotted in Matlab and compared with poles movement obtained from the mathematical model in order to analyze the six critical parameters impacts on system performance.

Fig. 8(a) presents the system dynamics in case of changing \( k_{pv, sec} \). Since the model is considered in \( \alpha\beta \) frame, rms value of the AC critical bus is processed in \( \alpha\beta \) frame, i.e. 230V rms means 281.69V in \( \alpha\beta \) frame. It can be seen that, with \( k_{pv, sec} \) being 0.5, 2.5 and 5, the system transient performance including AC critical bus voltage, active power and reactive power, is becoming more and more damped. The poles movement is drawn with the same parameter changing range are shown in Fig. 9(a). It can be observed that the poles are moving towards the real axis, which also indicates that the system is becoming more and more damped.

The system performance when \( k_{pv, sec} \) is 5, 20.5 and 50 is presented in Fig. 8(b). It can be observed that AC critical bus voltage, active power and reactive power tend to have oscillations, which indicates a less damped system. Poles movements with the same changing range, is presented in Fig. 9(b), moving away from real axis. This means that the system is becoming less and less damped, which matches the experimental result.

Fig. 10(a) shows the system dynamics when \( k_{ph} \) is 0.0001, 0.0003 and 0.0005. Actually the dynamics are almost the same.
controlled under 10% optimally, that it has small impacts on the system performance. Based on the dominating poles have slight movements, which indicate being seen that all the poles of the system is kept in the same position in the experiment. But in order to show the process clearly, three curves are made manually a bit separated. And it can be seen that all the poles of the system is kept in the same position (Fig. 11(a)), which means that it has no impacts on system performance.

In Fig. 10(b), the impacts of the virtual resistor are depicted. Small impacts are observed on the active power and reactive power. However, it has significant impacts on the voltage sag amplitude in the transient process. With $R_{vir}$ increasing, the voltage sag becomes bigger. Fig. 11(b) presents the poles distribution condition regarding the same $R_{vir}$ variation range. The dominating poles have slight movements, which indicate that it has small impacts on the system performance. Based on IEC 62040-3, the voltage sags in the transient process should be controlled under 10% optimally, being $i_o$ and $V_o$ the maximum output current and nominal output voltage.

In Fig. 12(a), it can be observed that when the $k_{p\theta_{sec}}$ is 0.2, 1 and 2, small difference is able to be seen in AC critical bus voltage transient, active power transient and reactive power transient. Poles movement in this situation is presented in Fig. 13(a). One pole is moving away from original point in the real axis and its impact on the system is becoming more and more unconspicuous. And the remaining dominating poles doesn’t move too much, which means that system performance is not affected too much. Fig. 13(b) shows the $k_{i\theta_{sec}}$ effects on the poles movement. Poles tend to remove away from real axis, which means that the system is less and less damped, as shown in Fig. 12(b) experimental data.

Besides its impacts on AC critical bus voltage transient process, $k_{p\theta_{sec}}$ and $k_{i\theta_{sec}}$ also has impact on the synchronization process divergence speed of the proposed online UPS system, which is shown in Fig. 14. In Fig. 14(a), the $k_{i\theta_{sec}}$ is 10, 20 and 30 respectively while $k_{p\theta_{sec}}$ is remained fixed. It can be
observed that the synchronization process tends to have oscillation with bigger $k_{iθ_{sec}}$. Fig. 14(b) shows the synchronization process with variational $k_{iθ_{sec}}$. While it increasing, the system is becoming more and more damped without any oscillation.

V. EXPERIMENTAL RESULTS

By using the control parameters shown in Table I, experiments were carried out to validate the feasibility of the proposed plug’n’play control strategy.

Fig. 15 presents the AC critical bus voltage restoration performance when one DC/AC is suddenly disconnected. It can be seen that the AC critical bus is tightly regulated to 230Vrms. During the transient, the voltage oscillation is kept under 15V, i.e. 8.6% of the nominal output voltage. In Fig. 15(a), the performance with previous control is presented. If one phase voltage of all modules are positive, for instance phase $a$, when one modules plug out without refreshing the DC/AC working number $n$, the average block output $(\alpha_{1a}+\alpha_{2a}+...+\alpha_{na})/n$ will become small. This means that the instantaneous input of the controller $G_{v_{rec}}$ becomes bigger. As a result, the output of the controller $v_{a_{rec}}$ is bigger, which means that a bigger voltage reference is generated. It can be observed that $v_{c_{rms}}$ had an overshoot. After some transient process, it reaches a random value that is not equal to 230V. However, with the proposed control, the AC critical bus voltage can be recovered to 230V as shown in Fig. 15(b). Also, under nonlinear load conditions, a similar AC critical bus voltage performance is obtained as shown in Figs. 15 (c) and (d). Since the voltage variation is quite serve under previous control, the $y$ axis in Fig. 15 between previous control and improved control are different.

Since there is a low pass filter in the RMS value calculation block, the voltage transient process is slowed and it cannot precisely reflect the UPS output voltage performance. So that real-time voltage performance is obtained through scope to evaluate the plug’n’play performance. At the same time, power sharing performance between modules is also presented in Fig. 16. At $t_2$, DC/AC #3 is order to plug in and plug out at $t_3$. The active power is well shared among the modules, as well as the reactive power. At $t_3$ and $t_4$, a similar operation was carried out.
Fig. 16. Power sharing performance in case of module plugging in and out. (a) Active power sharing when module #3 plug in and out. (b) Reactive power sharing when module #3 plug in and out. (c) Active power sharing when module #2 plug in and out. (d) Reactive power sharing when module #2 plug in and out.

TABLE II

<table>
<thead>
<tr>
<th>Voltage overshoot or sag (%)</th>
<th>Duration time (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>14% (overshoot or sag)</td>
<td>20-40</td>
</tr>
<tr>
<td>12% (overshoot or sag)</td>
<td>40-60</td>
</tr>
<tr>
<td>11% (overshoot or sag)</td>
<td>60-100</td>
</tr>
<tr>
<td>10% (overshoot or sag)</td>
<td>100-1000</td>
</tr>
</tbody>
</table>

Linear Load

Nonlinear Load

12% (overshoot) 27% (sag) 40-60
11% (overshoot) 27% (sag) 60-100
10% (overshoot) 20% (sag) 100-1000

Fig. 17. System output voltage transient performance in case of DC/AC module plugging in and out. (a) Transient at $t_a$. (b) Transient at $t_b$.

Fig. 18. Synchronization process. (a) Overall Process. (b) Transient at $t_e$. (c) Transient at $t_f$. (d) Transient at $t_g$.

for DC/AC #2. It can be observed that both active power and reactive power are well shared. AC bus voltage transient behaviors during this two modules operation are presented in Fig. 17 and evaluated according to IEC 62040-3 [2].

Fig. 17(a) depicts the UPS output voltage transient performance at $t_a$. It can be observed that the whole transient time duration is around 70 ms. The voltage overshoot when DC/AC #3 is reconnected is around 40V, as shown in Fig. 17(a), which is around 5.21% (605V - 575V)/575V of the nominal output voltage value. According to the standard shown in TABLE II, if the voltage overshoot is less than 10% of the nominal value, the transient duration time is in the range of
100mˢ – 1000mˢ when the load is either linear or nonlinear. Consequently, it can be concluded that the system performance meets the standard IEC 62040-3 [2].

Synchronization performance of the system was also tested as shown in Fig. 18. Line-to-line voltage of phase a and b of the utility and proposed online UPS system is presented. It can be observed that the phase errors are reduced smoothly without causing any voltage oscillation.

VI. CONCLUSION

This paper presents an improved control strategy for modular online UPS system, which aims at achieving plug n' play capability. This control feature allows the system to be maintained with less difficulty, such as serious AC critical bus voltage oscillation, unbalanced power sharing performance, synchronization problems with the utility and so on. The modules that need to be maintained can be stopped or started randomly without affecting the AC critical bus voltage. Besides the accurate active and reactive power sharing performance, the proposed control strategy presents a faster dynamic performance in case of module plugging out and in compared with the control methods proposed before according to IEC 62040-3. Moreover, a recovery and synchronization capability is achieved without using PLL. Experiments results are provided to validate the proposed control strategy. A detailed small signal model is derived to analyze the critical parameters impact on system performance using experimental data, which is able to be treated as a guidance to design the system.

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REFERENCES


VII. BIOGRAPHIES

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His research interests is oriented to different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, and optimization of microgrids and islanded minigrids. Prof. Guerrero is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and the IEEE Industrial Electronics Magazine, and an Editor for the IEEE TRANSACTIONS on SMART GRID and IEEE TRANSACTIONS on ENERGY CONVERSION. He has been Guest Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS Special Issues: Power Electronics for Wind Energy Conversion and Power Electronics for Microgrids; the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS Special Sections: Uninterruptible Power Supplies systems, Renewable Energy Systems, Distributed Generation and Microgrids, and Industrial Applications and Implementation Issues of the Kalman Filter; and the IEEE TRANSACTIONS on SMART GRID Special Issue on Smart DC Distribution Systems. He was the chair of the Renewable Energy Systems Technical Committee of the IEEE Industrial Electronics Society. In 2014 and 2015 he was awarded by Thomson Reuters as Highly Cited Researcher, and in 2015 he was elevated as IEEE Fellow for his contributions on “distributed power systems and microgrids.”

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