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Published in:
I E E E Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2016.2531631

Publication date:
2016

Document Version
Early version, also known as pre-print

A 3D Lumped Thermal Network Model for Long-term Load Profiles Analysis in High Power IGBT Modules

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***Abstract*—The conventional RC lumped thermal networks are widely used to estimate the temperature of power devices, but they lack of accuracy in addressing detailed thermal behaviors/couplings in different locations and layers of the high power IGBT modules. On the other hand, Finite Element (FE)-based simulation is another method which is often used to analyze the steady-state thermal distribution of IGBT modules, but it is not possible to be used for long-term analysis of load profiles of power converter, which is needed for reliability assessments and better thermal design. This paper proposes a novel three-dimensional RC lumped thermal network for the high power IGBT modules. The thermal-coupling effects among the chips and among the critical layers are modeled, and boundary conditions including the cooling conditions are also taken into account. It is demonstrated that the proposed thermal model enables both accurate and fast temperature estimation of high power IGBT modules in the real loading conditions of the converter while maintaining the critical details of the thermal dynamics and thermal distribution. The proposed thermal model is verified by both FE-based simulation and experimental results.**

***Index Terms*—Finite element method (FEM), insulated gate bipolar transistor (IGBT), mission profile, power semiconductor, reliability, thermal model.**

I. INTRODUCTION

POWER electronic devices, especially Insulated Gate Bipolar Transistor (IGBT) modules, are widely used in various important applications with high power rating like renewable energy production, motor drives, HVDC and automation [1], [2]. In order to push the power ratings of the devices, power semiconductor industries are trying to make new generation silicon chips with more compact area and higher power density. In addition, more semiconductor chips are integrated into the same substrate and are connected with bond-wires in order to increase current ratings of the power module. All these mentioned technologies may result in the increased complexity of geometry inside the IGBT module. On the other hand the critical mission profiles in the high power applications may introduce complicated loading conditions to the devices, consequently resulting in complicated thermal dynamics.

The thermal behaviors of the IGBT modules are very important design consideration for the whole converter system, especially in the high power range. Because the reliability of power electronic devices is closely dependent on the thermal behaviors of semiconductor devices, the adverse thermal loading and dynamics may quickly trigger the reliability problems, causing failures of IGBT modules like bond-wire lift-off or solder cracking [3]-[5]. It has been demonstrated that thermal stresses of the semiconductor devices can be mathematically correlated to the expected reliability performance of the converter, allowing a more accurate design of the semiconductor parts [6]-[9]. On the other hand, power semiconductor device may incur in catastrophic failures if the maximum junction temperature given by the manufacturer is exceeded [5]. Therefore, an accurate prediction of the chip temperature is crucial for a reliable IGBT module thermal design as well as heat sink design which affect the total converter cost.

Currently, the correct estimation of the temperature in high power semiconductors under real mission profiles is still a challenging task. A group of methods are based on thermal models composed of RC lumps given by manufacturer's datasheets which estimate temperature indirectly as detailed in [10]-[17]. In these methods, the temperature of the IGBT module is mathematically solved by the information of loss dissipation in the IGBT/diode chips as well as the thermal impedances in the form of one-dimensional RC network. However, these thermal models exhibit some limits in calculating the temperatures in different layers of the IGBT module. In other words, they only estimate junction temperature and they do not provide accurate temperatures in the middle layers. In addition, they can only estimate the average temperature of the chip area without considering the thermal coupling between the chips or temperature distribution in different layers of materials inside the module. Moreover, 2D- and 3D-boundary conditions including nonlinear cooling

Manuscript received July 8, 2015; revised November 2, 2015; accepted December 1, 2015. Recommended for publication by Associate Editor xxx.

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Digital Object Identifier 07.0246/JESTPE.2016.xxxxxxx

system are not considered in the mentioned methods.

Today, many advanced simulation tools have been introduced for the thermal behavior analysis of the high power IGBT module, such as traditional Finite Element Method (FEM), Finite Volume Method (FVM) and Finite Difference Method (FDM) [17]-[19]. All these methods provide much more accurate and detailed thermal information in both transient and steady-state operation of the device. However these methods normally require massive calculations in three dimensions. Furthermore, because of the complex structure and cooling system of high power IGBT modules, these methods normally result in very long computation time, especially in multi-physics environments – electro-thermal and thermo-mechanical – which are more and more demanded in reliable design for power electronics [20]. Indeed, many researches have been carried out to simplify and speed up the pure FEM simulation tools, such as the ones mentioned in [21]-[30], but all of these methods are difficult to be implemented in real mission profiles and, even in case of success, several of them exhibit significantly decreased the accuracy in the temperature calculation.

This paper proposes a novel, fast and accurate three-dimensional RC lumped thermal model for high power IGBT modules; it takes into account some critical geometry and material information of the devices. The obtained model is suitable to be integrated into a circuit simulator, whose execution time is much shorter than the one for an FEM-based simulation with comparable accuracy. This model includes thermal coupling effects between the chips as well as the critical sub-layers. Moreover, the 3D thermal network is adjustable according with power losses distribution and cooling system equations that means by change of these boundary conditions the thermal network is modified to fit to new conditions. Some experimental tests are presented too, which verify the proposed approach. One of the key outcomes is that the approximated temperature distribution inside the IGBT module can be obtained both vertically and horizontally, even if a circuit simulator is used. This feature is very important for lifetime calculation of the power device [31].

The paper is structured as follows: the modeling environment and operating conditions of the IGBT module under study are introduced first, together with challenges and limits of the existing thermal models. Then, the proposed method to extract the 3D lumped thermal network is described. Self-heating and thermal coupling effects inside the IGBT module are carefully included in the modeling process. Finally, the obtained thermal network is validated both by FEM simulation and experiments under the real field operating conditions in a grid-connected wind power converter.

II. Conditions and Environment for Modeling

A. Structure of IGBT Module and Conditions for Analysis

Without losing of generality, this paper focuses on a power IGBT module which is rated 1 kA and 1.7 kV. All silicon chips are placed on a Direct Copper Bonded (DCB) layer and copper baseplate respectively via solder layers. More in detail, the considered IGBT module contains 6 half-bridge converters connected in parallel, totally amounting to 12 transistors and 12 diode chips. The IGBT module is simulated using an FEM-based tool, namely ANSYS Icepak, to extract the temperature profiles. The graphical view of the IGBT module in the FEM simulation is shown in Fig. 1. The IGBT module is assumed adiabatic from top and lateral sides; so the heat propagates from the junction area, inside the chip, through several sub-layers and dissipates in the heat exchanger. Bond-wires can be removed in very good approximation as they minimum negligibly influence the thermal balance [4].

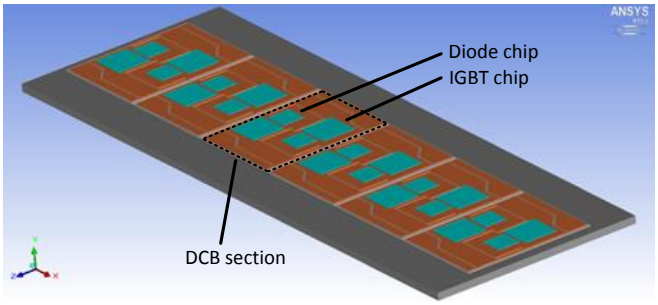


Fig. 1. Graphical view of the considered IGBT module developed in ANSYS Icepak.

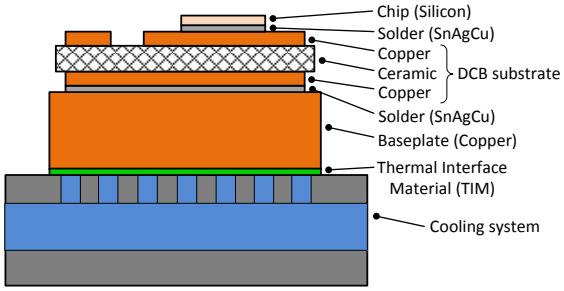


Fig. 2. Layer stack of the considered IGBT module.

TABLE I
IGBT Module Material Thermal Properties

Material	Density kg/m^3	Specific heat $J/(kg \cdot K)$	Conductivity	
			Temp. (°C)	Conductivity $W/(m \cdot K)$
Silicon (Si)	2330	705	0.0	168
			100.0	112
			200.0	82
Copper (Cu)	8954	384	0	401
			100	391
			200	389
Al_2O_3	3890	880	all	35
SnAgCu	7370	220	all	57

The layer stack in the considered IGBT module is shown in Fig. 2. In this case study, the DCB substrate layer material is chosen to be Aluminum Oxide (Al_2O_3). Of course, other interesting DCB materials such as AlN or Si_3N_4 can be studied as alternative cases. The thermal characteristics of all materials used in the IGBT module are given in Table I. It is worth to note that the conductivity of some materials is set to be temperature dependent based on [32] especially silicon and copper, which show considerably lower thermal conductivity at higher temperatures.

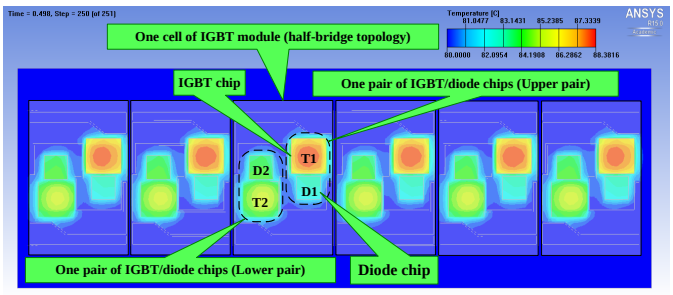


Fig. 3. Temperature distribution in 6 cell IGBT module in a real operating condition.

As an initial demonstration and reference for analysis, FEM simulation is implemented based on the given specifications of IGBT module. It has been assumed that the baseplate is mounted on a plate with fixed temperature set to 88°C in order to decrease the simulation time and to avoid the uncertain physical properties in thermal interface material and heatsink. This is a typical design target of the cooling system for the chosen IGBT modules [33]. Of course, using thermal interface material or active heatsink follows the same method of thermal modeling. Also, the ambient temperature of the simulations is fixed to 20°C. To achieve the highest accuracy in the simulation results and shorter simulation time, multi-level meshing is applied in the FEM tool. Basically, multi-level meshing consists of using finer mesh in the critical regions such as junction and solder layers rather than the thicker layers such as the baseplate and DCB. The FEM simulations are done in transient mode for 0.5 seconds which is sufficient time to ensure the temperatures inside the IGBT module under study have reached the steady-state.

B. Challenges of Accurate Thermal Modeling

The conventional thermal models calculate the junction temperature excursions for self-heating of the devices caused by single operational semiconductor chips. On the other hand, some thermal models consider thermal couplings between chips such as the thermal models introduced in [33]-[35], but they do not explain thermal coupling between different layers of the IGBT module in thermal paths between the chips. Identifying thermal coupling in sub-layers helps in accurate temperature calculation of critical layers. Indeed, any chip dissipating power will produce a temperature increase in the same chip and all other chips. So, an accurate thermal model should account for superposition of thermal couplings. This paper studies thermal coupling effect as an important factor for accurate thermal modeling. One of the key achievements of the presented approach is to make able to study the temperature cross-effects among the chips. Without losing of generality, it is assumed that power losses are generated equally in IGBT and diode chips. The surface temperature distribution of the IGBT module is shown in Fig. 3. As previously pointed out, the IGBT module under study consists of 6 cells, each cell contains a half-bridge converter including two pairs of IGBTs and freewheeling diodes, namely T1/D1 and T2/D2.

The coupling effect from other chips is related to the distance of heat sources and the magnitude of the power generated at heat sources [37]. It can be observed in Fig. 3 that

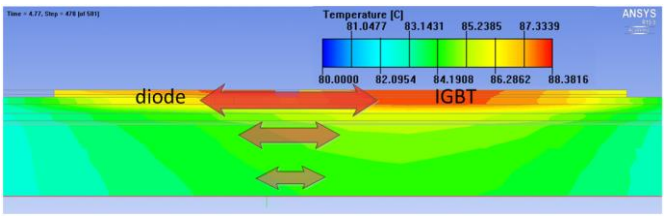


Fig. 4. Cross section view of temperature distribution in one cell of IGBT module and thermal coupling effects among layers.

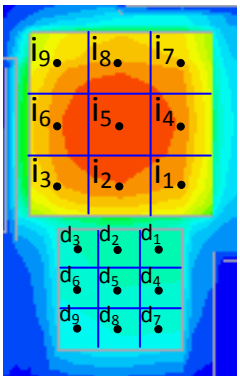


Fig. 5. Temperature monitoring points in one pair of IGBT/diode chip.

in each half-bridge cell, the thermal coupling effects among the cells are negligible since there is no significant temperature difference in the area between them. Consequently, the study can be focused on one individual half-bridge cell which is composed of four closely positioned chips (Transistors T1, T2, and freewheeling diodes D1, D2). Furthermore, for simplicity, the thermal coupling study can be focused on one pair of IGBT/diode (T1 and D1) thanks to symmetry. It is worth to note that the thermal coupling is not only among the chips, but it is also relevant among sub-layers beneath the chips. Fig. 4 shows the cross-section view of temperature distribution in the IGBT module when the IGBT chip is conducting and it can be seen that thermal coupling exist between the chips and sub-layers. In addition, a noticeable amount of heat is flowing through solder layers, which can lead to reliability problem as detailed in [3].

Since the side temperatures of the chips are critical information in solder cracks study, nine equally distanced monitoring points are considered on each IGBT/diode chips to study the self-heating and thermal coupling effects from the other chips. These monitoring points are shown in Fig. 5. It should be mentioned that thermal couplings also exist between points on same chips which are not included in this work due to their negligible effect in comparison to thermal coupling from other chips. Other monitoring points are considered under the chips and are labeled as *s1* for the chip solder, *s2* for the baseplate solder, *C* for the case and *TIM* for the thermal interface material.

In order to model the self-heating and thermal coupling effects, FEM simulations have been performed in three cases: 1. only the Transistor (T1) is switching; 2. only the freewheeling diode (D1) is switching and 3. T1 and D1 are switching alternatively. For this purpose, a power loss profile from a grid-connected converter is given to both IGBT and diode chips. The converter rated power is 500 kW, DC bus voltage is 1100 V, rated load current is 209 A_{rms}, output

frequency is 50 Hz and switching frequency is 2 kHz. The baseplate temperature is fixed to 80°C. In the simulation, we apply power losses to the IGBT and we measure the diode temperature and vice versa. The results for i_2, i_5 and i_8 monitoring points on the IGBT chip and d_2, d_5 and d_8 on the diode chip are shown in Fig. 6(a)-(f).

In these figures, transient temperatures on the selected monitoring points of the IGBT chip are shown. The IGBT chip results to be less influenced by the diode chip. On the contrary, in Fig. 6.(d), 6.(e), and 6.(f), the diode chip receives more considerable thermal coupling impact from the IGBT chip, especially for the monitoring points d_1, d_2 and d_3, which are positioned closer to the IGBT chip. This unequal thermal coupling between IGBT and diode is mainly due to the smaller size of the diode chip and much higher losses in the IGBT chip in an inverter operating mode. For what found above, it can be concluded that thermal coupling is obviously not symmetric. In thermal modeling of the IGBT modules, independence of thermal paths is not reasonable under these circumstances and thermal coupling effects should be included in the thermal networks.

On the other hand, many factors may have impacts to the loading of high power IGBT modules. These factors include variable wind speeds and temperatures, harsh environments, grid disturbances, etc. Finite Element Analysis (FEA) can be used for short-term simulations, but for long-term load profiles FEA is time-consuming and demands for huge amount of computation time and cost. Therefore, a much faster thermal model is required to estimate temperatures for loading profiles under multi-time scales, while the accuracy about the thermal coupling and distribution inside the module need to be maintained.

III. Modeling of Thermal Impedance Network

A. *Proposed Structure of 3D Thermal Impedance Network*

In order to correctly represent the thermal coupling impact, a thermal model is needed which estimates self-heating as well as thermal coupling effects from other chips in critical layers. Indeed, this model should make a superposition of self-heating and thermal coupling effects. To this aim, the self-heating effects are modeled as conventional lumped RC networks for each intended locations on the chips. The RC networks start from chip, end in the cooling system and cover critical solder layers as well as cooling system. On the other hand, thermal couplings are modeled as voltage sources between layers and controlled by other chips. These additional sub-circuits include current source from the neighboring chip and thermal coupling impedance between two layers. The sub-circuits are powered by the other chip power loss heat source.

FEM is executed for two trials in which temperatures are monitored in both chips and critical layers and distributed points on each layer. Based on this, a 3D thermal lumped network is obtained which is shown in Fig. 7. For simplicity, only the thermal branches for i_2 and d_2 monitoring points are shown; the other branches follow the same rules. The thermal branches are extracted for the critical monitoring points from junction to chip solder $Z_{th}(j-s_1)$, chip solder to baseplate solder $Z_{th}(s_1-s_2)$, baseplate solder to case $Z_{th}(s_2-c)$ case to Thermal Interface Material (TIM) $Z_{th}(s_2-TIM)$ and TIM

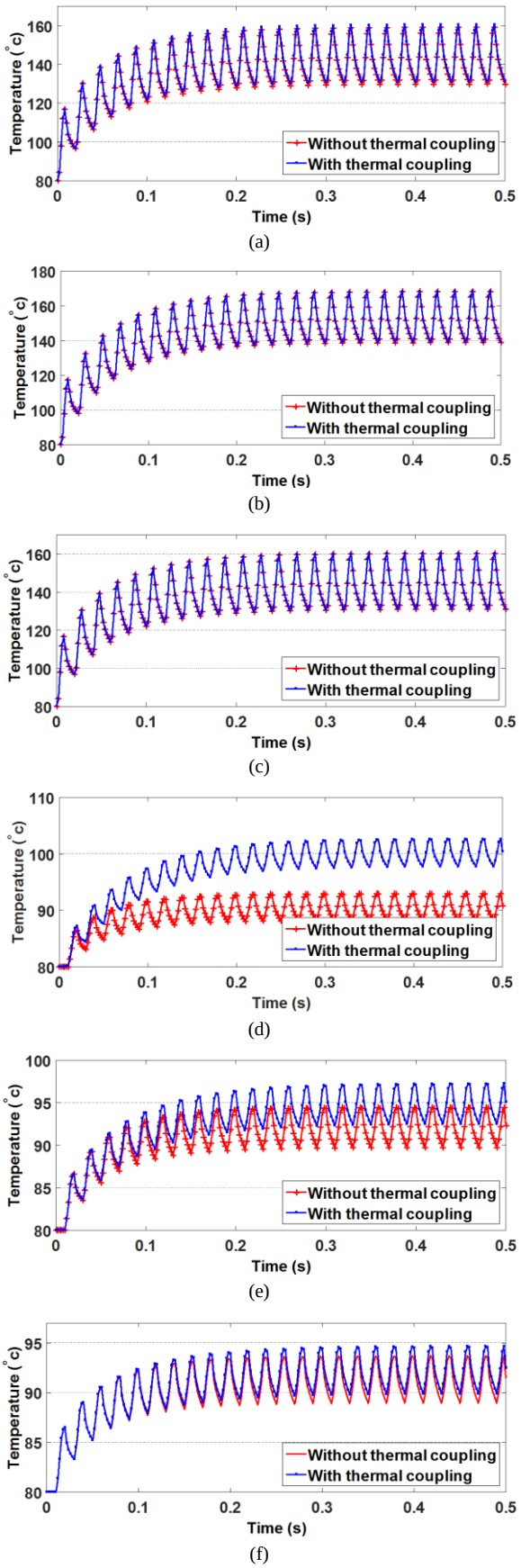


Fig. 6. Transient temperature on selected monitoring points (see Fig. 5) with and without considering the thermal coupling effect: i_2 (a), i_5 (b), i_8 (c), d_2 (d), d_5 (e), d_8 (f).

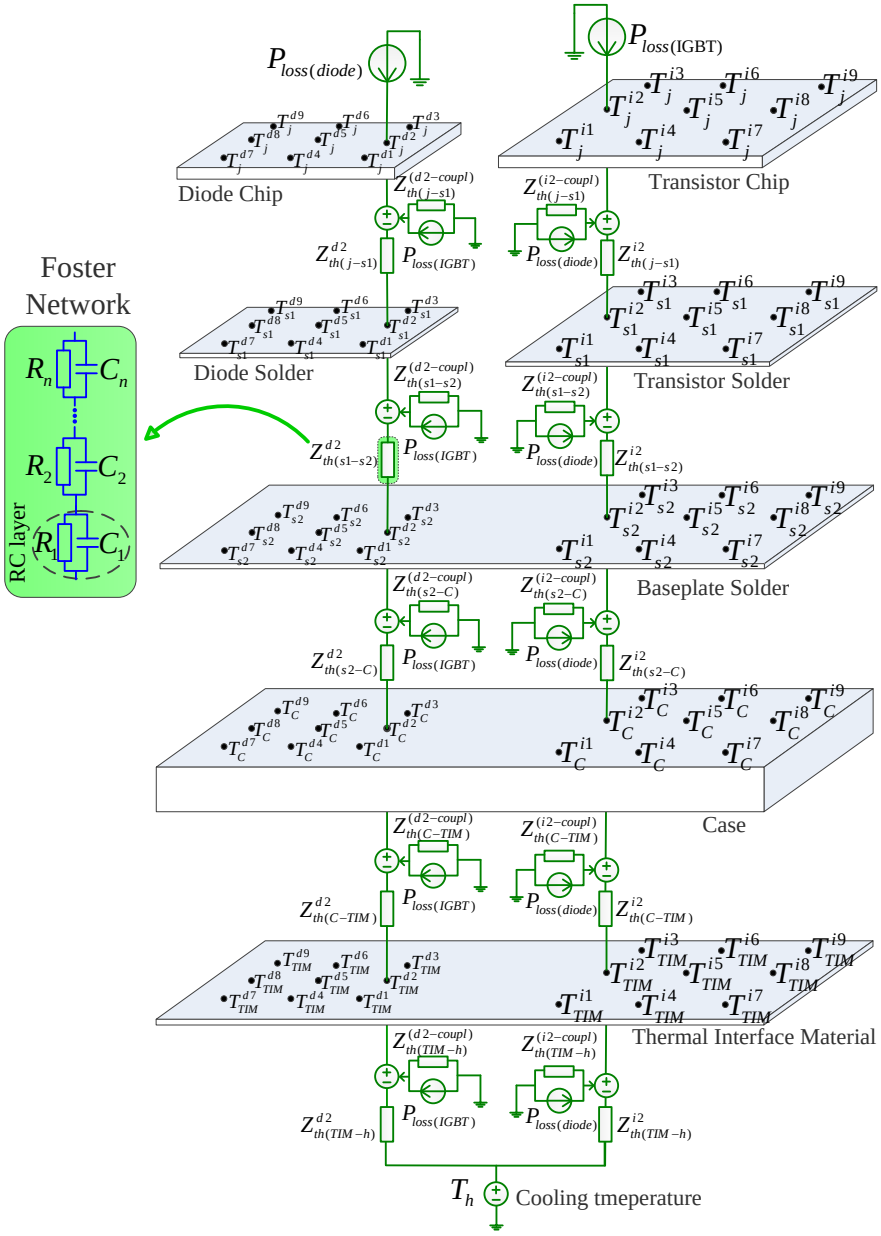


Fig. 7. 3D thermal impedance network for a pair of IGBT/diode chips (Thermal network is shown for i_2 and d_2; all other monitoring points share the same thermal network configuration).

to cooling system $Z_{th}(TIM-h)$. Z_{th} is the thermal impedance of each branch which will be described in section III.B. The thermal coupling effects are shown as controlled voltage sources, which are added to the self-heating sources.

In Fig. 7, T_j^{im} and T_j^{dm} are the chip temperature at the monitoring point *'m'*, T_{s1}^{im} and T_{s1}^{dm} are the chip solder temperature beneath the monitoring point *'m'*, T_{s2}^{im} and T_{s2}^{dm} mean the baseplate solder temperature beneath the monitoring point *'m'*. T_c, T_{TIM} and T_h are case temperature, thermal interface material temperature and coolant temperature respectively. $Z_{th}^{im,dm}$ is the self-heating thermal impedance between the two layers and $Z_{th}^{(im,dm-coupl)}$ is the coupling thermal impedance between two the two layers.

B. *Extraction of Elements in the 3D Thermal Network*

Roughly speaking, the temperature rise across the IGBT module is proportional to the power dissipation in both transient and steady-state [27]. The temperature rise in steady-state can be calculated applying thermal resistance, R_{th}, between the target point and the reference point. Similarly, the temperature in the dynamic state is calculated using the transient thermal impedance curve $Z_{th}(t)$ between the two mentioned points. The thermal resistance and thermal impedance equations are given by (1) and (2).

$$R_{th(a-b)} = \frac{T_a - T_b}{P_{self}} \tag{1}$$

$$Z_{th(a-b)}^{self}(t) = \frac{T_a(t) - T_b(t)}{P_{self}} \quad (2)$$

where T_a and T_b are temperatures in two adjacent points and P_{self} is the power losses which is generated in the same chip. Moreover the coupling thermal impedance can be written as (3).

$$Z_{th(a-b)}^{coupl}(t) = \frac{T_a(t) - T_b(t)}{P_{coupl}} \quad (3)$$

where P_{coupl} is the power losses which is generated in the neighbor chip. Typically, the power losses are not constant and also time dependent, so the temperature rise (ΔT) of the device can be calculated by (4) [33].

$$\Delta T(t) = \int_0^t P(\tau).dZ_{th}(t-\tau).d\tau \quad (4)$$

where $\Delta T(t)$ is the device temperature rise, $P(\tau)$ is the power losses profile, $Z_{th}(t-\tau)$ is the transient thermal impedance and t is the time of switching.

Indeed, in order to study the thermal coupling effects among the chips and to find the temperature rise in critical points such as solder layers, more detailed thermal impedances are needed. This information is essential for the optimized design of IGBT modules. To consider the self-heating and the thermal coupling effects, (2) and (3) can be rewritten in matrix form as (5.1):

$$\begin{bmatrix} T_1 \\ T_2 \\ \cdots \\ T_m \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1n} \\ Z_{21} & Z_{22} & \cdots & Z_{2n} \\ \cdots & \cdots & & \cdots \\ Z_{m1} & Z_{m2} & \cdots & Z_{mn} \end{bmatrix} . \begin{bmatrix} P_1 \\ P_2 \\ \cdots \\ P_n \end{bmatrix} + \begin{bmatrix} T_{ref,1} \\ T_{ref2} \\ \cdots \\ T_{ref,m} \end{bmatrix} \quad (5.1)$$

where T_i, with $i \in 1,..,m$ is the monitoring point temperature, P_j, with $j \in 1,..,n$ is the power losses on each chip, $T_{ref,m}$ is the reference temperature at the monitoring point m and Z_{mn} is the coupling thermal impedance between the monitoring point m and the reference point i. In particular, Z_{ii} is the self-heating thermal impedance. The expanded form of eq. (5.1) to the 3D thermal network can be written as eq. (5.2), where junction temperature, chip solder temperatures and baseplate solder temperature in the IGBT chip and diode chip can be calculated using the 3D thermal network.

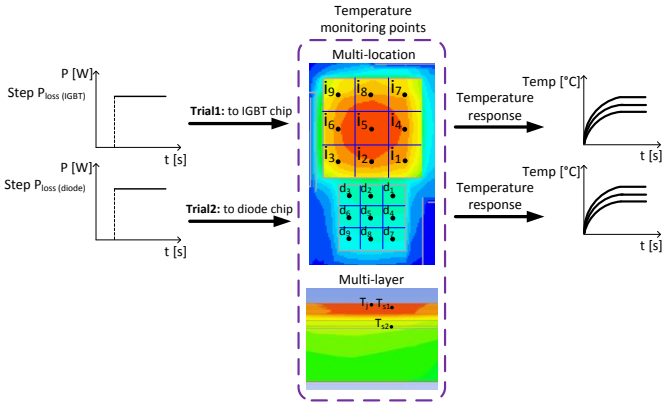


Fig. 8. Temperature responses to step power losses applied to the IGBT chip and diode chip and they are monitored in distributed locations and layers of the IGBT module.

The method used in this paper to extract thermal network is based on the extraction of transient thermal impedances from FEM analysis and transformation of these curves into equivalent thermal RC networks by using step response analysis. The RC networks can then be used in any circuit simulators like PSpice or PLECS to calculate temperatures. This will accelerate the simulation time with acceptable accuracy compared to the FEM analysis.

To extract the responses, a step power loss input is applied to each chip (T1 and D1) individually and the temperature responses from the intended monitoring points are extracted. If only the self-heating of the monitoring point is intended to be calculated, a step response analysis can be applied to extract the equivalent thermal RC network. If the thermal coupling effect is also needed to be taken into account, the transient thermal impedance for one node can be extracted by using the superposition principle as the summation of self-heated transient thermal impedance and coupling transient thermal impedances from the other chip (as another heat source). The methodology to find the thermal response of the IGBT module is detailed in the following:

1) The IGBT module geometry is drawn in FEM environment.

2) Step response analysis is performed for all chips, by applying the step power loss input to one single chip in a trial and then to monitor the temperature responses on the same

$$\begin{bmatrix} T_j^{i1} \\ T_j^{i2} \\ \cdots \\ T_j^{im} \end{bmatrix} =$$

$$\begin{bmatrix} Z_{th(j-s1)}^{i1} + Z_{th(s1-s2)}^{i1} + Z_{th(s2-C)}^{i1} + Z_{th(C-TIM)}^{i1} + Z_{th(TIM-h)}^{i1} & Z_{th(j-s1)}^{(i1-coupl)} + Z_{th(s1-s2)}^{(i1-coupl)} + Z_{th(s2-c)}^{(i1-coupl)} + Z_{th(c-TIM)}^{(i1-coupl)} + Z_{th(TIM-h)}^{(i1-coupl)} \\ Z_{th(j-s1)}^{i2} + Z_{th(s1-s2)}^{i2} + Z_{th(s2-C)}^{i2} + Z_{th(C-TIM)}^{i2} + Z_{th(TIM-h)}^{i2} & Z_{th(j-s1)}^{(i2-coupl)} + Z_{th(s1-s2)}^{(i2-coupl)} + Z_{th(s2-c)}^{(i2-coupl)} + Z_{th(TIM-h)}^{(i2-coupl)} + Z_{th(TIM-h)}^{(i2-coupl)} \\ \vdots & \vdots \\ Z_{th(j-s1)}^{im} + Z_{th(s1-s2)}^{im} + Z_{th(s2-C)}^{im} + Z_{th(C-TIM)}^{im} + Z_{th(TIM-h)}^{im} & Z_{th(j-s1)}^{(im-coupl)} + Z_{th(s1-s2)}^{(im-coupl)} + Z_{th(s2-c)}^{(im-coupl)} + Z_{th(c-TIM)}^{(im-coupl)} + Z_{th(TIM-h)}^{(im-coupl)} \end{bmatrix} \quad (5.2)$$

$$\times \begin{bmatrix} P_{loss(IGBT)} \\ P_{loss(diode)} \end{bmatrix} + \begin{bmatrix} T_h \\ T_h \\ \cdots \\ T_h \end{bmatrix}$$

chip and all other intended points on the other chip. The results are a series of curves, which are transient temperature responses. This process is illustrated in Fig. 8.

3) To obtain the self-heating transient thermal impedance between the vertical monitoring points, that means *j* to *s1*, *s1* to *s2*, *s2* to *C*, *C* to *TIM* and *TIM* to *h*, the extracted temperature curves in each monitoring point is subtracted from the adjacent vertical point and divided to the same chip power loss. As an example t self-heating thermal impedance between *j* and *s1* can be calculated as:

$$Z_{th(j-s1)}^{im} = \frac{T_j^{im} - T_{s1}^{im}}{P_{loss(IGBT)}} \tag{6}$$

where im is the monitoring point on the IGBT chip in the corresponding monitoring layer and $P_{loss(IGBT)}$ is the step power losses of IGBT chip.

To identify the coupling transient thermal impedance, the temperature difference between junction and heatsink on each monitoring point of a chip is measured, when the step power loss is applied to the other chip. Then the temperature difference will be divided to the power losses of the other chip. For example, the coupling thermal impedance between *j* and *s1* at point (I, m) can be calculated as the following:

$$Z_{th(j-s1)}^{im-coupl} = \frac{T_j^{im} - T_{s1}^{im}}{P_{loss(diode)}} \tag{7}$$

where $P_{loss(diode)}$ is the step power loss of diode chip.

4) In order to apply the transient thermal impedance in the circuit simulator for temperature calculation, the transient thermal impedance curves in each scenario are curve-fitted mathematically using a sum of exponential functions as shown in (8) in order to obtain an equivalent thermal network to the thermal impedance curve.

$$Z_{th}(t) = \sum_i R_{th_i} . (1 - e^{-t/R_{th_i}C_{th_i}}) \tag{8}$$

where R_{th_i} is the equivalent thermal resistance and C_{th_i} is the equivalent thermal capacitance.

The equivalent RC network, which is used in this paper, is a Foster network that is highlighted in Fig. 7. It is worth to mention that in Foster networks, the voltages at the intermediate nodes do not have physical meaning and only the first and the last nodes are meaningful to the adjacent temperature monitoring points. The number of RC pairs are dependent on the accuracy of the fitted curve to $Z_{th}(t)$. In this paper, the number of RC pairs varies from one layer to four layers depending on the fitted $Z_{th}(t)$ curve. It is very important to note that, although the Foster network node voltages do not have any physical meaning, the first and last nodes are located in sub-layers of the 3D thermal network, therefore they assume a physical value.

C. Curve Fitting of Thermal Impedance Curve

The R and C values in the Foster network are mathematically calculated using *cftool* in MATLAB [38]. To this aim, first the time values and thermal impedance values in the thermal impedance curve are entered as two matrices. Also for better fitting operation, it is advised that in transient times more resolution of thermal impedance values being selected rather than the steady-state. The time steps selected for this work are shown in Fig. 9.

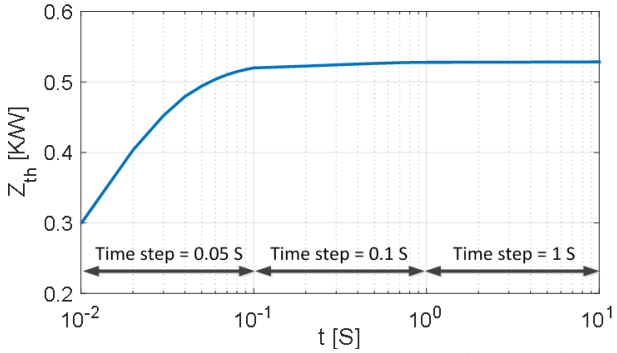


Fig. 9. Time step values which has been selected for curve fitting of transient thermal impedance curve.

The curve fitting tool creates interpolation best fit based on the eq. (8). Curve fitting tool uses nonlinear least-squares formulation to fit the nonlinear model to data extracted from the thermal impedance curve. If the number of thermal impedance values is *n* and the number of time steps is *m*, then the eq. (8) can be rewritten in a matrix form like a nonlinear model as shown in (9).

$$y = f(X, \beta) + \varepsilon \tag{9}$$

where y is an *n*-by-1 vector of responses, f is a function of β and X, β is an *m*-by-1 vector of coefficients, X is the *n*-by-*m* design matrix for the model and ε is an *n*-by-1 vector of errors. To fit the data, an iterative approach is required that follows the following steps:

1) Fitting process starts with an initial estimation for each coefficient of eq. (9). For example random values on the interval [0, 1] are provided.

2) The fitting model creates the fitted curve for the current coefficients. The fitted response value $\hat{y}$ is given by (10).

$$\hat{y} = f(X, b) \tag{10}$$

$\hat{y}$ includes the calculation of the Jacobian of $f(X, b)$ and represents as a matrix of partial derivatives of the coefficients. b is an *m*-by-1 vector of new coefficients.

3) The coefficients are adjusted and it is determined if the fitting is improved. The magnitude and direction of adjustment depend on the fitting algorithm. Since the coefficients of the fitted model (RC values) must be kept non-zero and upper limits are kept to 1000, the Trust-region algorithm is used to solve the problem. Trust-region algorithm can solve difficult nonlinear problems in a very efficient way rather than other methods.

4) The process is iterated by returning to step '2' until the fitting process is modified properly. For this purpose, the sum of squares due to error (SSE) is considered as 10^{-4} at most. The whole curve-fitting process can be found in MATLAB help documentation [38].

D. Limits and Extension of the Models

The presented thermal model is dependent on the boundary conditions of the studied geometry. As discussed before,

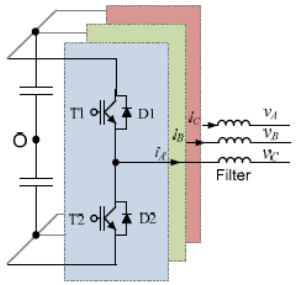


Fig. 10. Two-level voltage source DC-AC converter (2L-VSC).

TABLE II
PARAMETERS OF CONVERTER SHOWN IN FIG. 10

Rated output active power P_o	500 kW
Output power factor PF	1.0
DC bus voltage V_{dc}	1100 VDC
*Rated primary side voltage V_p	690 V rms
Rated load current I_{load}	209 A rms
Fundamental frequency f_o	50 Hz
Switching frequency f_c	2 kHz
Filter inductance L_f	1.9 mH (0.2 p.u.)
IGBT module	1700V/1000A

* Line-to-line voltage in the primary windings of transformer.

boundary conditions include ambient temperature, power losses and cooling system. It is widely shared that the ambient temperature does not affect the thermal behavior of power devices, so the IGBT module is assumed to be adiabatic from top and lateral sides. In addition, it has been proven in [39] that the loading conditions affect the accuracy of the thermal model which is due to the variation of thermal conductivities of materials in different temperatures. On the other hand, cooling conditions may affect the parameters of the thermal network. For example, if the cooling system heat transfer coefficient is increased, the heat flux spread reduces, which in turn leads to increased thermal impedance, especially in the baseplate. This phenomenon will reduce the heat spreading efficiency of the baseplate and heat transfer efficiency to the heat exchanger. So, the temperature difference between the junction and case and consequently the thermal resistance will be increased respectively. More discussion regarding boundary conditions effects on thermal impedance is presented in [39].

IV. MODEL VERIFICATION

A. FEM Verification

In this section, the presented thermal network is implemented and verified by a circuit simulator (PLECS) whose results will be compared with FEM results (ANSYS Icepak). In order to find the power loss profile, the IGBT module is loaded with a three-phase DC-AC Voltage Source Converter (2L-VSC). The circuit schematic of the converter is shown in Fig. 10 and the detailed converter specifications are listed in Table II. The IGBT/diode components and the other values in the Table II are typical values used in grid-side inverters for wind power application.

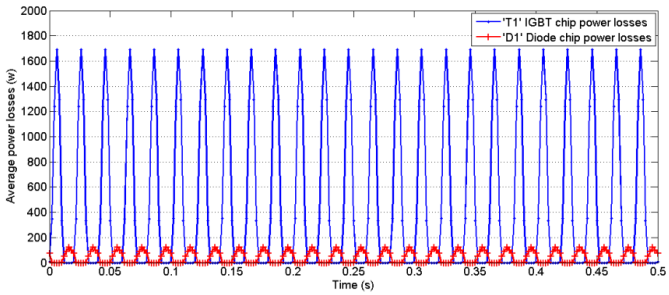


Fig. 11. Average power losses in the IGBT module calculated by PLECS for 25 cycles.

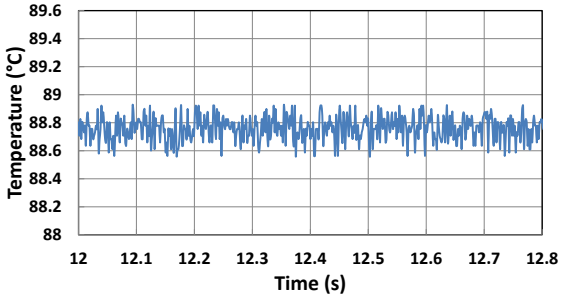


Fig. 12. Baseplate temperature measured in the experiment.

The converter conditions presented in Fig. 10 and Table II are used to design the heat sources for the IGBT/diode chips. The power losses for the power semiconductor devices are the sum of conduction losses and switching losses. The conduction losses can be calculated by (11):

$$P_{cond\mathrm{T/D_{chip}}}(t) = v_{ce/\mathrm{f-chip}}\left(i_{\mathrm{chip}}(t)\right).i_{\mathrm{chip}}(t).D_{\mathrm{T/D}}(t) \quad (11)$$

where $v_{ce/\mathrm{f-chip}}$ is the conduction voltage of IGBT/diode, $i_{\mathrm{chip}}(t)$ is the mean current flowing in each chip, $D_{\mathrm{T/D}}(t)$ is the duty ratio for the IGBT or diode. The switching losses can be calculated as follows:

$$P_{\mathrm{swT/D-Ave}}(t) = f_s.f_0\int_0^{1/f_0} E_{sw\mathrm{T/D-chip}}\left(i_{\mathrm{chip}}(t)\right).dt \quad (12)$$

where $E_{sw\mathrm{T/D-chip}}$ is the average switching energy for all IGBT or diode chips, which is a function of the current flowing in each chip. f_s is the switching frequency of the converter and f_0 is the fundamental frequency of the converter. The whole loss calculations are detailed in [40], and the instantaneous power losses generated on each IGBT and diode chip inside the module are shown in Fig. 11. It can be seen that under the specified operating conditions the power losses on the IGBT chip is significantly larger than the power losses generated on the diode chip.

The loss profile is applied to the thermal network as $P_{loss(IGBT)}$ and $P_{loss(diode)}$ and the case temperature is kept fixed around 88.8 °C as shown in Fig. 12. To model the cooling system, boundary conditions should be identified in FEM analysis. The cooling system in the experimental setup is a fixed temperature hotplate. A hot plate is not an efficient

cooling system since it is equivalent to a very high heat transfer coefficient and very low thermal resistance in the boundary of the baseplate and the heat exchanger [39]. The baseplate temperature is measured by means of thermocouple put in a heatsink hole and measuring the temperature in the closest location to the baseplate.

In the FEM simulation the equivalent heat transfer coefficient at the boundary of baseplate is adjusted to obtain the same temperature of the experiment. The heat transfer coefficient is a function of thermal resistance and the heat conduction area:

$$h = \frac{1}{R_{th}.A} \tag{13}$$

where h is the heat transfer coefficient at the boundary of baseplate and hotplate, R_{th} is the baseplate to hotplate thermal resistance and A is the effective heat conduction area between the baseplate and hotplate. From eq. (1), eq. (13) can be rewritten as:

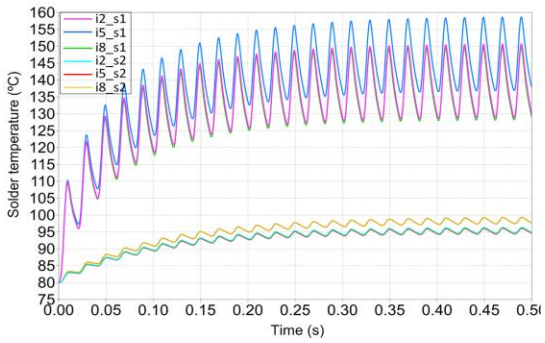
$$h = \frac{P_{loss}(IGBT) + P_{loss}(diode)}{(T_{baseplate} - T_{hotplate}).A} \tag{14}$$

The total power losses of the IGBT chip and the diode chip from the experiment is $1666\,W$, $T_{baseplate} - T_{hotplate} = 88.8 - 88 = 0.8\,°C$, and $A = 0.02\,m^2$, the equivalent heat transfer coefficient is obtained approximately as $100{,}000\ \mathrm{W/m^2}$. With this boundary condition, the FEM simulation is performed to extract the 3D thermal network RC elements.

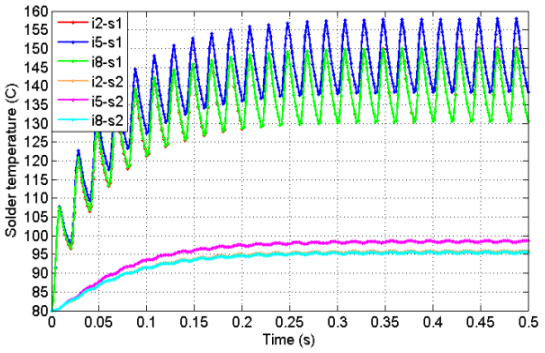
The temperature responses on i_2, i_5 and i_8 on the IGBT chip (as previously described on Fig. 5) are shown in Fig. 13.(a) and Fig. 13.(b). It can be seen that the presented method and the FEM results well track each other. The highest error is 1.3% for $i_2\_S_2$ monitoring point. It is worth to observe that the temperatures on i_2 and i_8 are very close to each other that shows no significant thermal coupling effect from the diode chip to the IGBT chip. The temperature responses on d_2, d_5 and d_8 on the diode chip are given in Fig. 14.(a) and Fig. 14.(b). It clearly appears that d_2 is the hottest point – even higher than d_5 – which shows a higher thermal coupling effect not only from the IGBT chip but also from other chips on the DCB.

To validate the 3D thermal network for other loads, another load profile is applied to the chips. The adopted load profile is given in Fig. 15. The solder temperatures for the monitoring points i_2, i_5 and i_8 are given Fig. 16.(a) and Fig. 16.(b).The maximum error between two simulation methods is 1.5% for $i_2\_S_2$. The results verify that the presented thermal network model is valid for different loss levels.

Table III shows the computer specifications and computational time needed for simulating the presented model and FEM model. It can be seen that the simulation time for the presented thermal network is significantly faster than the FEM analysis. However, one could argue that the time needed to extract the thermal network and implementation in the circuit simulator is longer than FEM model setup. It is worth to point out that to extract the 3D thermal network, the FEM simulation is just run for two simple trials with step power losses as stimuli. Afterwards, the model can be used for any long-term load profile without further FEM simulations.

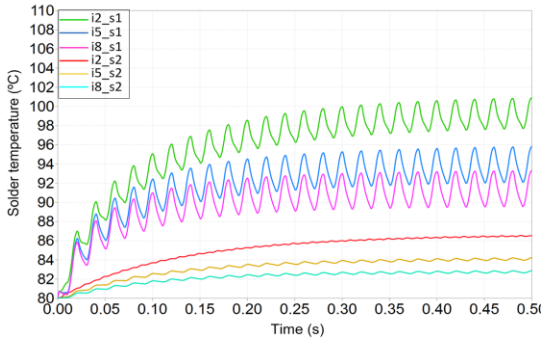


(a)

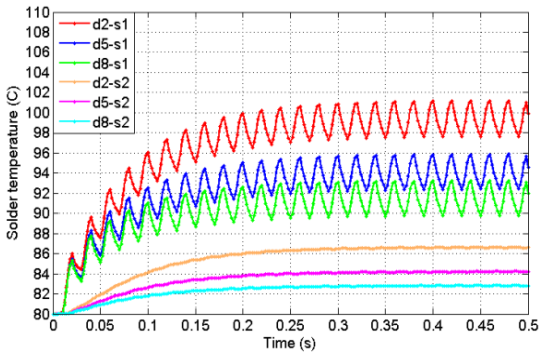


(b)

Fig. 13. IGBT chip solder temperatures on monitoring points $\boldsymbol{i_2}$, $\boldsymbol{i_5}$ and $\boldsymbol{i_8}$ for loss profile given in Fig. 11 and the baseplate fixed to 88 ℃: a) Simulated thermal model in PLECS; b) Simulated FEM model in ANSYS Icepak.



(a)



(b)

Fig. 14. Diode chip solder temperatures on monitoring points $\boldsymbol{d_2}$, $\boldsymbol{d_5}$ and $\boldsymbol{d_8}$ for loss profile given in Fig. 11 and the baseplate fixed to = 88 ℃**:** a) Simulated thermal model in PLECS; b) Simulated FEM model in ANSYS Icepak.

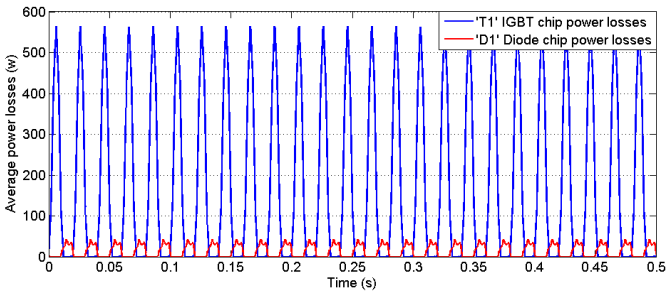
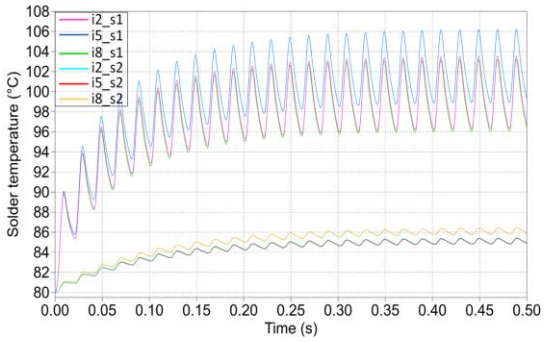
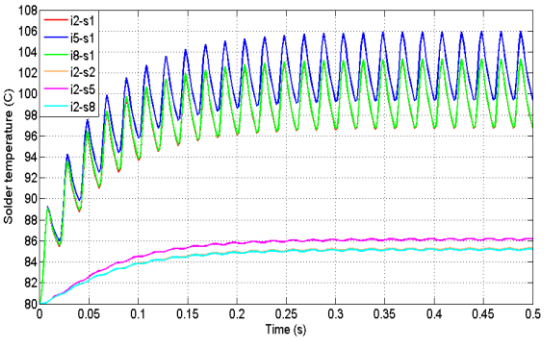


Fig. 15. Average power losses in the IGBT module calculated by PLECS for 25 cycles (power loss profile II).



(a)



(b)

Fig. 16. IGBT chip solder temperatures on monitoring points i_2, i_5 and i_8 for loss profile given in Fig. 15 and the baseplate fixed to 88 ℃. a) Simulated thermal model in PLECS; b) Simulated FEM model in ANSYS Icepak.

TABLE III
COMPUTATIONAL TIME AND COMPUTER SPECIFICATIONS.

	Thermal model in PLECS	**FEM model in ANSYS Icepak**
Computational time	15 second	30 minutes
Computer specifications	Laptop: Intel i7 3740QM, RAM 8GB	Work Station: Intel E5-2650 v2, 2.60GHz, RAM 32GB

Calculation of multi-layer temperature under the chips is one of the major contributions of the 3D thermal network approach which is not possible to be calculated from manufacturer datasheet or direct measurements due to inaccessible sub-layers. Therefore, the Therefore, the advantage of fast simulation is significant in case of very long load profile (e.g. a year load profile) and fast life-time estimation is needed based on temperature swings in the junction and sub-layers.

TABLE IV
STEADY-STATE ERRORS OF TEMPERATURE CALCULATION DIFFERENCE BETWEEN THE PRESENTED THERMAL MODEL AND FEM MODEL.

Loss profile	**Chip temperature**	**Error between PLECS and FEM results (%)**					
Loss profile in Fig. 13	IGBT chip junction temp.	i_2	0.84	i_5	0.67	i_8	0.17
	IGBT chip solder1 temp.		1.08		0.4		0.36
	IGBT chip solder2 temp.		1.32		0.94		0.81
	Diode chip junction temp.	d_2	1.39	d_5	1.75	d_8	2.36
	Diode chip solder1 temp.		0.97		1.29		2.07
	Diode chip solder2 temp.		0.1		0.04		0.07
Loss profile in Fig. 16	IGBT chip junction temp.	i_2	0.18	i_5	0.14	i_8	0.02
	Diode chip junction temp.	d_2	0.25	d_5	0.31	d_8	0.41

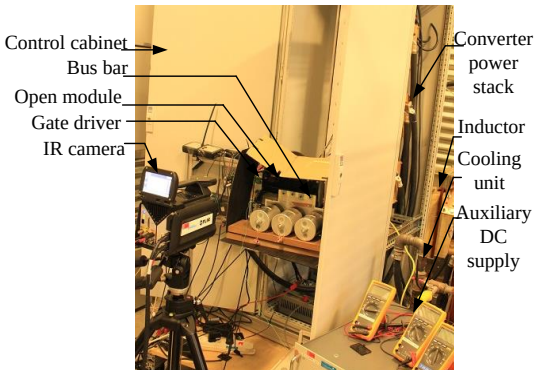


Fig. 17. Test set up featured with IR camera.

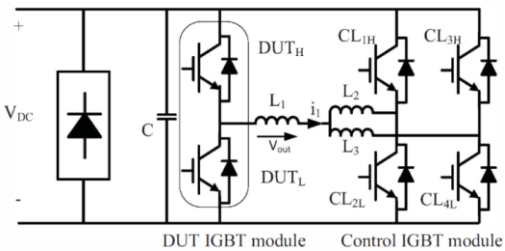


Fig. 18. The power converter set up schematic for testing IGBT modules.

To compare the results of presented 3D thermal network model in PLECS with FEM model in ANSYS Icepak, the errors are given in percent for the average temperature differences between two models on selected monitoring points in Table IV. As it can be seen the highest error is for d_8 monitoring point (2.36%) for the loss profile given in Fig. 11. Also, the lowest error is for monitoring point i_8 (0.02%) for the loss profile given in Fig. 15.

B. Experimental Verification

In this section, the simulated temperatures extracted from the 3D thermal model are compared with the measurements from the experimental setup. The test setup featured with the IR camera is shown in Fig. 17. An opened and black-painted

TABLE V
TEST SETUP SPECIFICATIONS

Converter topology	Full-bridge
Output frequency	6 Hz
Switching frequency	2.5 kHz
Input voltage	450 V
Output current	500 A (Peak)
Filter inductance *L1..3*	350 µH

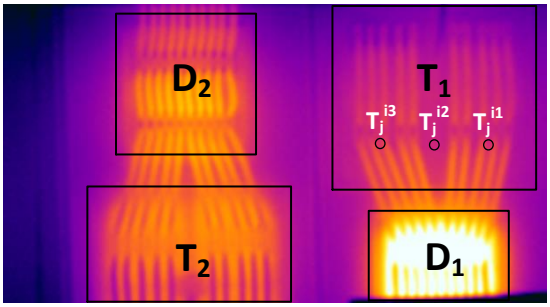


Fig. 19. Infrared thermal image of one DCB section of IGBT module.

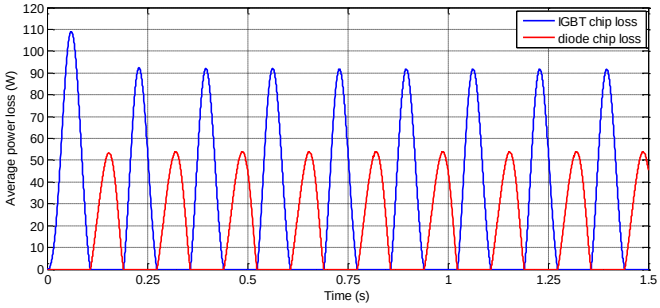


Fig. 20. Average power losses generated in the IGBT chip and diode chip in the experiment.

IGBT module is being tested in a full bridge test circuit whose schematic is shown in Fig. 18. The upper chip pairs in the IGBT module under test are shown as DUT_H and the lower chip pairs are shown as DUT_L. The test circuit specifications are given in Table V. An online temperature measurement is performed by infrared thermal camera at every five minutes in normal operating conditions to prevent oversized data collection. A hot plate is mounted under the baseplate with temperature fixed to 88 ℃ ± 0.5 ℃ throughout the test. The infrared thermal image of one DCB section of IGBT module is shown in Fig. 19. To validate the presented model, similar monitoring points as the 3D thermal networks are considered on the surface of the IGBT chip and the diode chip. The monitoring points should be considered between the bond-wires and be on the chip surfaces to prevent false bond-wire temperatures instead of chip temperature.

The instantaneous power losses which are generated in each IGBT chip and diode chip are shown in Fig. 20. The power losses are calculated using the method mentioned in [40]; where the temperature feedbacks to the loss calculation are considered. The temperature curves for three monitoring points on the IGBT chip including i_1, i_2 and i_3 are shown in Fig. 21. These monitoring points are selected since they are in

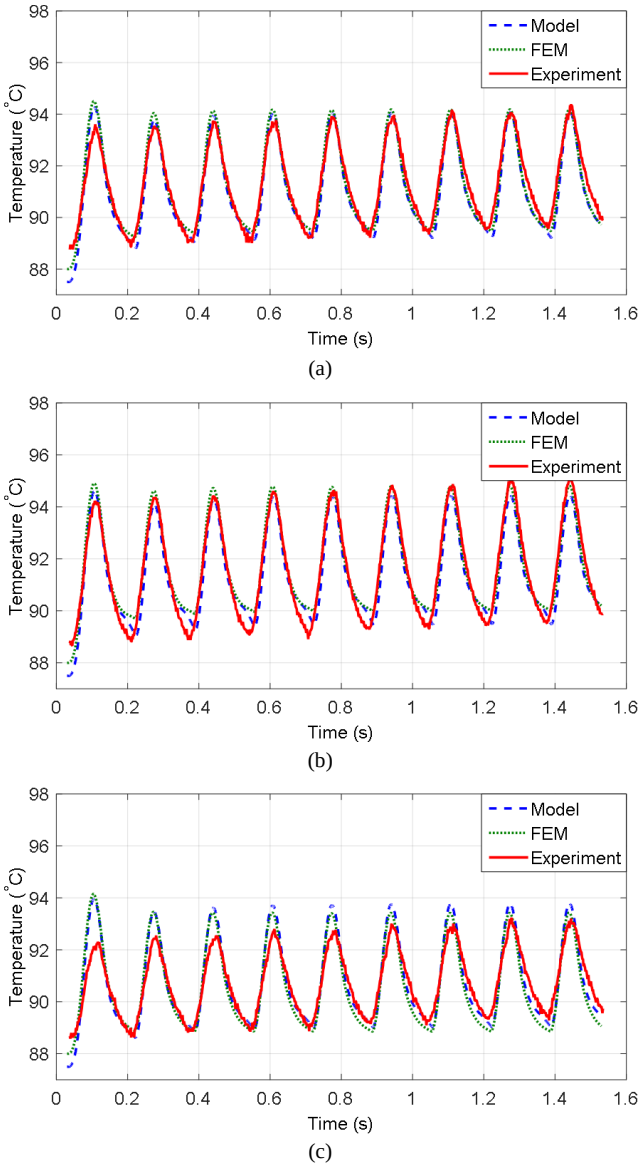


Fig. 21. IGBT chip surface temperatures calculates by model, FEM and experimental measurements, a) i_1; b) i_2; c) i_3.

the side of IGBT chip close to diode chip and suitable to validate the model in the case of high thermal coupling effects. The temperature curves are compared with the proposed thermal model, FEM simulation and experimental measurement. The amount of peak-to-peak temperature error between the results by simulated model and experimental tests are 3%, 6% and 8% for i_1, i_2 and i_3 respectively. But the simulated model results are consistent with the FEM simulation results with errors less than 1%. Therefore the obtained 3D thermal network shows satisfactory performance in comparison with FEM and experimental result.

V. APPLICATION OF 3D THERMAL NETWORK FOR LONG-TERM MISSION PROFILES

In order to show the application of proposed 3D thermal network in long-term thermal dynamics, real-field mission profiles from wind power system are selected and applied to

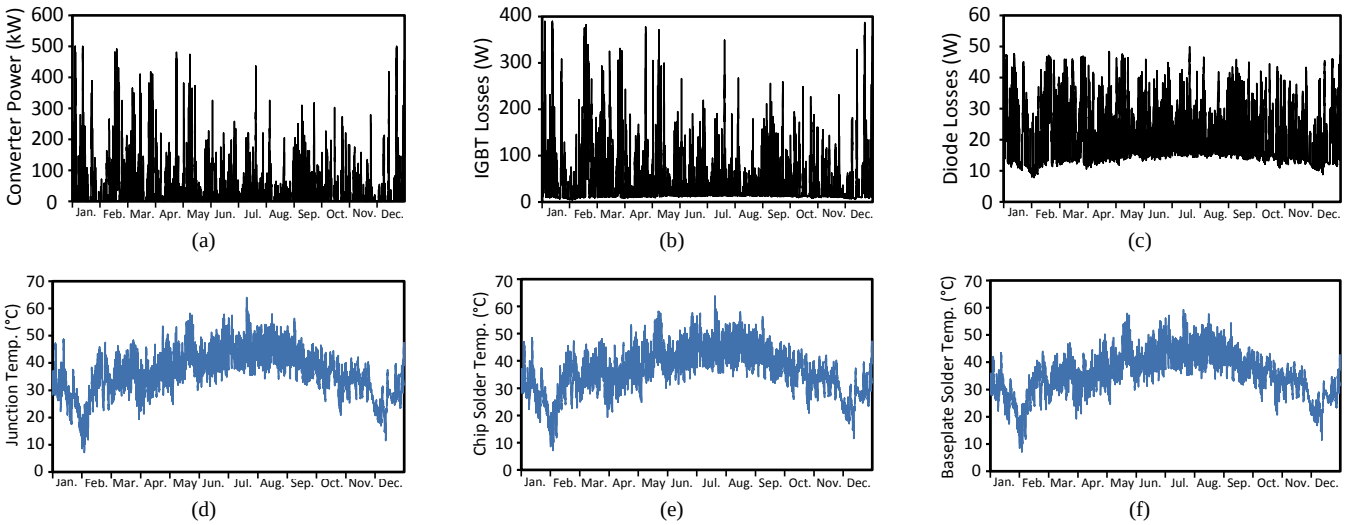


Fig. 22. Temperature calculation for one-year mission profile in i_2 monitoring point: a) Converter power; b) IGBT power losses; c) Diode power losses; d) Junction temperature; e) Chip solder temperature; f) Baseplate solder temperature.

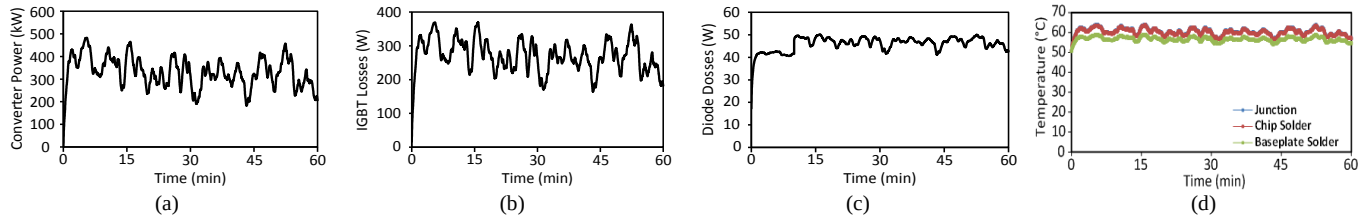


Fig. 23. Temperature calculation for one-hour mission profile in i_2 monitoring point: a) Converter power; b) IGBT power losses; c) Diode power losses; d) Junction, Chip solder, and baseplate solder temperatures.

the converter system specified in Table II. Fig. 22.(a) presents a yearly load profile in steps of one hour, IGBT and diode power losses as well as junction, chip solder and baseplate solder temperatures underneath the i_2 monitoring point are also shown. The simulation time for this mission profile was 80 minutes with the laptop system given in Table III. It is worth to point out that the FEM simulation was not capable to implement the yearly mission profile due to the memory overload of the computer systems.

Moreover, an hourly load profile with the steps of one second was applied to the IGBT module and 3D thermal network was used to identify temperatures at junction, chip solder and baseplate solder beneath monitoring point i2. Fig. 23 presents the results for the hourly load profile. The simulation time needed for this mission profile was 30 minutes with the laptop system. Using FEM simulation for the same mission profile, it took 2 days to get the same temperature result.

VI. Conclusions

In this paper, a detailed 3D thermal model of IGBT modules has been presented. The proposed thermal network contains the self-heating and thermal coupling between the chips as well as multi-locations and multi-layer thermal behaviors of the IGBT module. The lumped RC elements of thermal network are extracted by step response analysis of FEM model in different loading and cooling conditions. The extracted temperature step responses are modeled as self-heating and thermal coupling Foster networks by accurate curve fitting process. The presented thermal model is verified by a circuit simulator, FEM and experimental setup. The model is highly consistent with the FEM model and show low errors compared to experimental results. Moreover, the 3D thermal network estimates the temperatures in critical layers of IGBT module such as solders. The thermal model has been used with one-year and one-hour wind power mission profiles for fast and accurate temperature calculations in critical locations. In summary, the presented thermal model is appropriate to be applied in all circuit simulators for long-term dynamic load profiles. The fast temperature calculation can help the power electronic designer to evaluate the reliability of the IGBT module in real-field mission profiles and real converter operating conditions in a very fast and accurate way.

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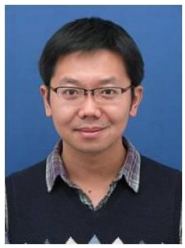

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