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Voltage Unbalance and Harmonic Compensation in Microgrids by Cooperation of Distributed Generators and Active Power Filters

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***Abstract*— In this paper, the power quality of microgrids is addressed. To achieve the desired level of power quality, a strategy based on the coordinated control between DGs and APFs is proposed. In this regard, hierarchical control is applied where primary control consists of power droop controller of DGs, selective virtual impedance and voltage/current regulators. Based on the secondary control, at first voltage harmonic compensation and voltage unbalance compensation of point of common coupling (PCC), that might includes sensitive loads, is carried out by DGs. Voltage compensation of PCC by DGs may cause severe voltage distortion at DGs terminals. Thus, the coordinated control is used to mitigate the voltage distortion to the defined maximum allowable value at DGs terminals. Evaluation of the proposed hierarchical control is carried out by a simulation study.**

***Index Terms*—Active power filter, Distributed Generator, Hierarchical control, Microgrid, Voltage unbalance/harmonic compensation.**

I. Introduction

DISTRIBUTED generators (DGs) are usually connected to microgrids (MGs) by power electronic interface converters. Regulating voltage/frequency of DG terminal is accomplishable by proper control of the interface inverters [1],[2]. Furthermore, many strategies have been suggested for improving power quality of MGs based on DGs inverters control [3]-[14].

Unbalanced voltage might be produced due to asymmetrical transmission lines or loads. It might cause serious problems such as increase of power losses in equipment, disturbing sensitive loads performance and even instability of system. As a common problem in three-phase MGs, voltage unbalance has been addressed in some previous works. A well-known strategy addresses voltage unbalance compensation (VUC) of point of common coupling (PCC) or DG terminal by proper control of DGs interface inverters [3]-[6]. To compensate unbalanced voltage of Sensitive Load Bus (SLB), an extra control loop is devised in [5] as secondary control. Although SLB voltage is improved in [5], DGs terminal might be distorted. This strategy is also applied in [6], moreover, an extra control loop is contrived to distribute the distortion rate among DGs terminal in an optimized way. However, in severe unbalance conditions, one or more DGs terminal might become distorted severely by this method.

With high penetration of nonlinear loads and power electronic equipment, harmonic pollution is considered as an important power quality problem. Many efforts have been done for voltage harmonic compensation (VHC). Like VUC, DGs inverters are usually used for VHC. The common strategy is making resistance emulation at harmonic frequencies [7]-[14]. The methods proposed in [11] and [12] address VUC and VHC of PCC while compensation sharing is considered too. Furthermore, [11] is built on selective harmonic compensation approach and in [12], transient state is regarded too. Again, DG terminal might become distorted severely by these methods. To simultaneously compensate voltage harmonics of the both points (PCC and DGs buses), coordinated control of DGs inverters and Active Power Filter (APF) is suggested in [13] and [14]. In [13], satisfactory voltage quality of multi-area MG (with different voltage quality requirement) is obtained while in [14], DGs inverters rated power is considered in the coordinated control too.

In line with previous efforts regarding power quality improvement of MG by DGs inverters and APFs, in the present paper, voltage unbalance mitigation is considered while VHC is carried out too.

II. Proposed Hierarchical Control Scheme

A typical MG is represented in Fig. 1. Note that there might be more than one DG connected to DG(s) bus. Two points are represented in the system as nodes and PCC where nodes are DGs terminals and PCC is the point that there might be high amount of loads (including sensitive loads). Note that there should be very low voltage harmonic distortion (VHD) and voltage unbalanced factor (VUF) at PCC while satisfactory power quality of nodes (according to the nodes voltage quality requirement) is considered. Meanwhile, since there is no constraint defined for voltage quality of a typical node, well-known power quality indexes should be considered.

Fig. 2 shows general scheme of the proposed hierarchical control. The proposed control contains two levels. Primary control is DGs local control that power sharing is considered in this level. Secondary control is for PCC voltage quality improvement by DGs interface inverters. However, due to PCC voltage compensation by DGs, nodes voltages might

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become distorted [14]. In this situation, APF is used for voltage distortion mitigation of nodes by making APF cooperated with DGs for PCC compensation.

According to Fig. 2, at first PCC voltage is analyzed by "PCC voltage analysis" block. In this block PCC voltage components in dq frame ($v_{dq}^{h\pm,1-}$) is extracted by synchronous reference frame-phase lock loop (SRF-PLL) [15] extraction method. Note that both positive and negative sequences of individual harmonics is considered in this block. Then $v_{dq}^{h\pm,1-}$ is transferred to secondary control by low bandwidth communication (LBC) link. As it is shown in Fig. 2, all the signals communicated to secondary control are LBC signals so secondary control as a central control can be far from DGs and APF. In secondary control, voltage distortion rate of PCC ($VDR_{PCC}^{h\pm,1-}$) is calculated. Due to nonlinear-unbalance loads in the system, both negative and positive sequences of individual harmonics ($VHD_{PCC}^{h\pm}$) and VUF of PCC (VUF_{PCC}) are considered to be very low; so these parameters are calculated in "PCC compensation rate cal.". $VDR_{PCC}^{h\pm,1-}$ is compared with its reference value, since there is any violation from the reference value, proper signals ($C_{dq}^{h\pm,1-}$) are generated and sent to primary control of DGs for removing the violation and compensating PCC. Note that $C_{dq}^{h\pm,1-}$ is the same for all DGs and sharing compensation among DGs is explained in follow.

As it is proved in Section V, PCC compensation by DGs might result severe VDR at nodes ($VDR_N^{h\pm,1-}$). This distortion is directly dependent on $VDR_{PCC}^{h\pm,1-}$; by increase of $VDR_{PCC}^{h\pm,1-}$, DG should tolerate more efforts for PCC compensation so the corresponding $VDR_N^{h\pm,1-}$ increases. In this situation, APF is active to help DGs for improving PCC and reducing $VDR_N^{h\pm,1-}$ to its reference value ($VDR_{N_{ref}}^{h\pm,1-}$). To make the cooperation, individual $VDR_N^{h\pm,1-}$ are calculated and transferred to this level by LBC (see Fig. 1). In the cooperation block, $VDR_N^{h\pm,1-}$ is compared with its reference values since there is any violation, according to the proposed cooperation policy between DGs and APF, proper signals are sent to primary control of the relative DGs ($T_i^{h\pm,1-}$) for reducing those DGs efforts. Moreover, proper signals ($T^{h\pm,1-}$) are sent to control stage of APF to include APF in compensation, partially. In follow, detailed descriptions of the hierarchical control is offered.

A. *Primary Control*

As mentioned before, in primary control power sharing is considered. Since there might be power circulation between parallel DGs, droop control is used to share fundamental component of power. As the main drawback of droop control, nonlinear and unbalance load sharing is not considered in the droop scheme. To share unbalance and harmonic current, using virtual impedance is suggested to provide resistance behavior toward harmonic components and the negative sequence of fundamental component of output current. Remember that different sequences of harmonic components should be regarded in virtual impedance since we have unbalance load condition in the system. Noteworthy that multiple second-order generalized integrator-frequency lock loop (MSOGI-FLL) is used in this paper to extract fundamental and harmonic components in stationary frameworks [15]. Note that PCC compensation by DGs is shared between them in compensation effort controller of primary control. Comprehensive explanations of different parts of primary control is available in [1], [5] and [14].

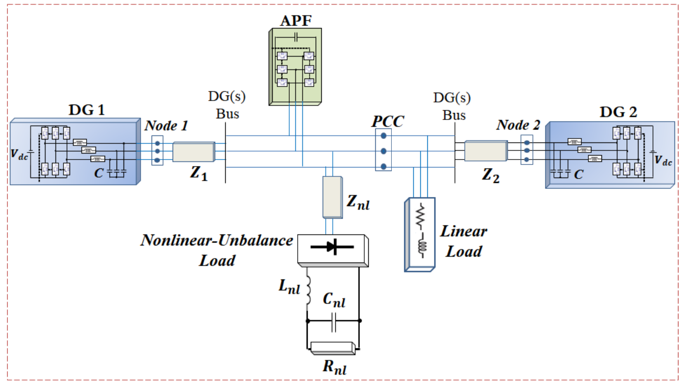


Fig. 1. General scheme of microgrid.

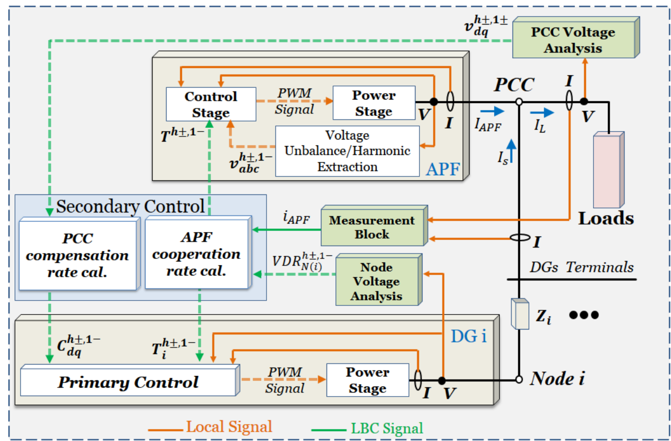


Fig. 2. General scheme of the proposed hierarchical control.

B. *Secondary(Central) Control*

As mentioned before, in secondary control PCC compensation is carried out by DGs, firstly. Fig. 3 shows PCC compensation rate calculation block of secondary control. As it is shown in Fig. 3, VDR is calculated like below:

$$VHD_V^{h\pm} = \frac{V_{rms_{o\alpha}}^{h\pm}}{V_{rms_{o\alpha}}^{1+}} \quad and \quad VUF = \frac{V_{rms_{o\alpha}}^{1-}}{V_{rms_{o\alpha}}^{1+}} \tag{1}$$

The VDR is compared with the reference value (VDR_{ref}), if there is any violation, depending on the violated rate, proper signal is produced for individual sequence of harmonics ($C_{dq}^{h\pm,1-}$) by using a Proportional-Integrator (PI) controller. Then $C_{dq}^{h\pm,1-}$ is sent to compensation effort controller of all DGs to mitigate PCC distortion to the reference value. The PI controller should be tuned so that the reference quality is achieved in short time while stability margin is considered too. It is worth noting that the "dead band" block is used to prohibit secondary control operation since PCC voltage distortion is lower that the reference value. Remember that the coordination step is also included in secondary control that is described in Section V.

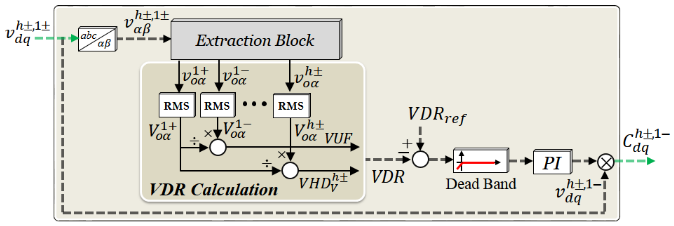


Fig. 3. Block diagram of compensation rate calculation.

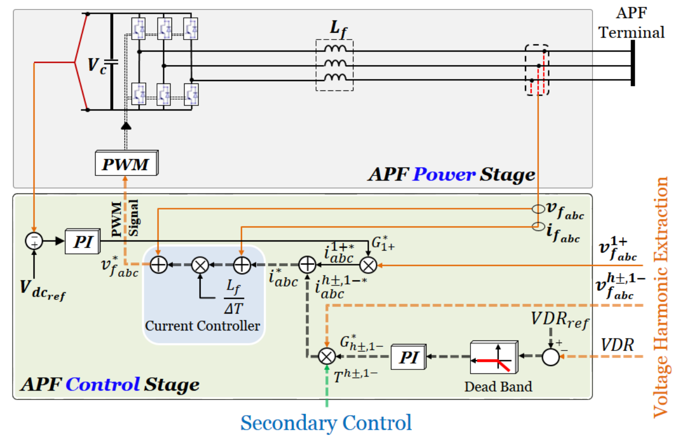


Fig. 4. APF power stage and control structure.

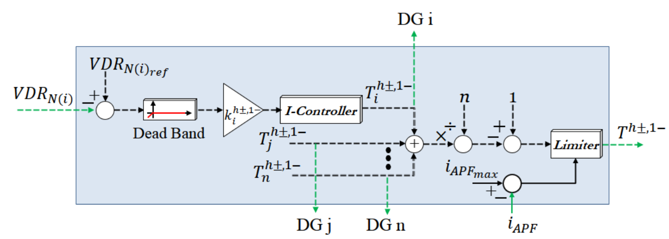


Fig. 5. Block diagram of APF cooperation rate calculation.

III. ACTIVE POWER FILTER, CONTROL SCHEME

Shunt APF is used in this paper to compensate both unbalance and harmonic distortion. The general control approach of the applied APF is extracted from [16]. The APF suppresses VDR by making resistive behavior toward fundamental negative sequence and harmonic components of current. The current command is determined as the follow equation:

$$i_{abc}^{*} = \sum_{h\pm,1-} G_{h\pm,1-}^{*} \cdot v_{fabc}^{h\pm,1-}. \tag{2}$$

where h is the harmonic order. In Eq. (2), $v_{fabc}^{h\pm}$ and v_{fabc}^{1-} are h^{th} harmonic component (including positive and negative sequences) and the fundamental negative sequence of voltage at the APF installation point (that is PCC in this paper, according to Fig. 1), respectively. Furthermore, $G_{h,1-}^{*}$ is the conductance command that might be different for fundamental and individual harmonic components. In fact, $G_{h,1-}^{*}$ is tuned based on the violation rate of VDR from the reference value by using a PI controller. As a result, APF can regulate compensation according to nonlinear/unbalance load condition. Note that the PI controller is designed exactly like that used in secondary control to make the better cooperation. Finally, the current regulator produces the following voltage command at the APF terminal [16]:

$$v_{fabc}^{*} = v_{fabc} - \frac{L_f}{\Delta T}\left(i_{abc}^{*} - i_{fabc}\right). \tag{3}$$

where L_f and ΔT are the APF inductance and sampling period, respectively [16]. According to above explanations, Fig. 3 shows the APF structure. It is worth noting that a PI controller is used for fixing the dc link of the filter and the dead band is applied to inhibit compensation if PCC compensation is not required.

IV. PROPOSED COORDINATION SCHEME

As mentioned before, the coordination is contrived for the situations that DG(s) is not sufficient for PCC compensation. As a result, the coordinated control manages compensation by using APF as auxiliary compensator. It is happened in "APF cooperation rate cal." of secondary control (see Fig. 2). The main policy of the proposed hierarchical control is that PCC compensation is carried out with the least cost investment and applying auxiliary compensator is avoided as far as possible so DGs play the main role in compensation. However, nodes voltage might become distorted severely. This can damage possible loads around nodes. Furthermore, when there is high amount of VDR at PCC, DGs have to devote high their capacities for compensation. It might diminish their efficiency as generators and even it might result instability. As a result, it is essential limiting DGs effort as compensators and provide satisfactory voltage quality at nodes.

The coordination scheme is represented in Fig. 5. As shown, at first $VDR_{N(i)}$ of all nodes is compared with the reference value; if there is any violation, proper signals ($T_i^{h\pm,1-}$) are sent to the primary control of the corresponding DG to obtain the reference voltage quality at the respective node. $T_i^{h\pm,1-}$ is tuned by using an integrator controller with the initial condition set to 1. In fact, $T_i^{h\pm,1-}$ changes between one and zero, as a result, DG compensation effort can be changed from 100% to 0%, depending on the violated rate. The integrator controller should be tuned so that the DG is able to tolerate the possible overshoot produced due to fast response while the time-response is not very long. Note that $T_i^{h\pm,1-}$ is individual for each voltage distortion including voltage unbalance of fundamental component and positive and negative sequences of voltage harmonic components. As it is shown in Fig. 5, VDR of all nodes are considered in the coordination while compensation effort reduction is carried out just for those DGs that their terminals are distorted severely. It is achieved via the dead band block in the coordination block (see Fig. 5).

However, by reducing DGs efforts for PCC compensation, PCC voltage will be distorted depending on the total compensation effort reduced by DGs. For this, APF is used to cooperate with DGs. In this line, it is needed calculating the total compensation effort reduction. Therefore, the following equation is used to determine the required cooperation rate:

$$T^{h\pm,1-} = 1 - \frac{\sum_{i=1}^{n} T_i^{h\pm,1-}}{n}. \tag{4}$$

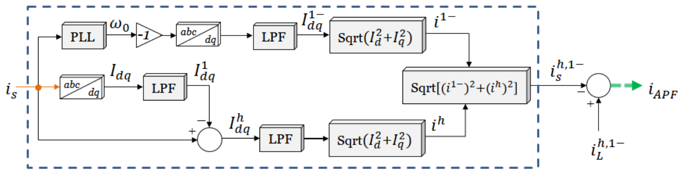


Fig. 6. APF current measurement.

where n is the number of DGs. In Eq. (4), it is assumed that PCC required compensation for achieving the reference voltage quality is 1 (or 100%). APF cooperation is obtained through multiplying $T^{h\pm,1-}$ to $G^*_{h\pm,1-}$ (see Fig. 4).

Another factor important in the cooperation is APF operation situation that can be determined by measuring its output current. Simply, since APF is overloaded, its cooperation should be limited (see Fig. 5). To measure APF current (i_{APF}), adaptive noise canceling technology (ANCT) is used [17]. According to ANCT, i_{APF} can be measured based on the following equation:

$$i_{APF} = i_L^{h\pm,1-} - i_s^{h\pm,1-}. \tag{5}$$

where $i_L^{h\pm,1-}$ and $i_s^{h\pm,1-}$ are harmonic component (including both positive and negative sequences) and fundamental negative sequence of load and DGs current, respectively (see Figs. 2&6). $i_L^{h\pm,1-}$ and $i_s^{h\pm,1-}$ extraction is taken place in measurement block of Fig. 2. This block is represented in Fig. 6. As shown, SRF-PLL extraction method is used in this block. Based on measurement block, harmonic component is measured by using Low Pass Filters (LPFs) and subtracting total current from fundamental component and the fundamental negative sequence is extracted by using PLL [18]. Note that $i_L^{h\pm,1-}$ is measured like $i_s^{h\pm,1-}$.

V. Simulation Study

The test MG is shown in Fig. 1. To provide high power quality for the loads at PCC, voltage quality requirement of PCC is set to higher levels than that of nodes (reference values $VHD_{PCC_{ref}}$ and $VUF_{PCC_{ref}}$ =0.5%). It is worth noting that compensation of 3th, 5th and 7th harmonics (the main orders) of nodes and PCC voltage is concerned in this paper.

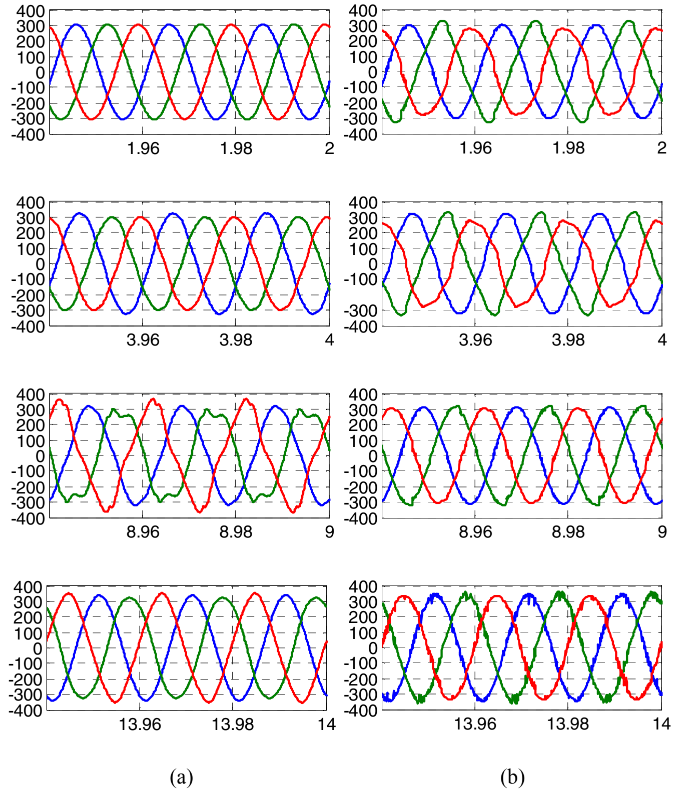
TABLE I
Test System Parameters

Power Stage Parameters								
APF Power Stage		Distribution Lines			nonlinear load			linear load
L_F (mH)	C_F (μF)	Z_1(Ω)	Z_2(Ω)	Z_{nl}(Ω)	C_{nl}(μF)	R_{nl}(Ω)	L_{nl}(mH)	Z_{l1}(Ω)
15	2200	0.2+j1.131	0.1+j0.565	0.2+j1.005	235	20	0.084	50+j6.238

Control Stage Parameters					
APF Capacitor-PI Controller		Cooperation stage			
K_p	K_i	k_1^{1-}	$k_1^{3\pm}$	$k_1^{5\pm}$	$k_1^{7\pm}$
0.16	0.02	0.5	0.45	0.4	0.35

TABLE II
Simulation Time Periods

Time (s)	0 < t < 2	2 < t < 4	4 < t < 9	9 < t < 14
Control loop	Droop Control And Power Sharing	Current sharing	Secondary Control (PCC compensation by DGs)	Secondary Control (PCC compensation by the cooperation)



Vertical axis: voltage(V), Horizontal axis: time(s)

Fig. 7. Voltage waveforms: (a) Node1, (b) PCC.

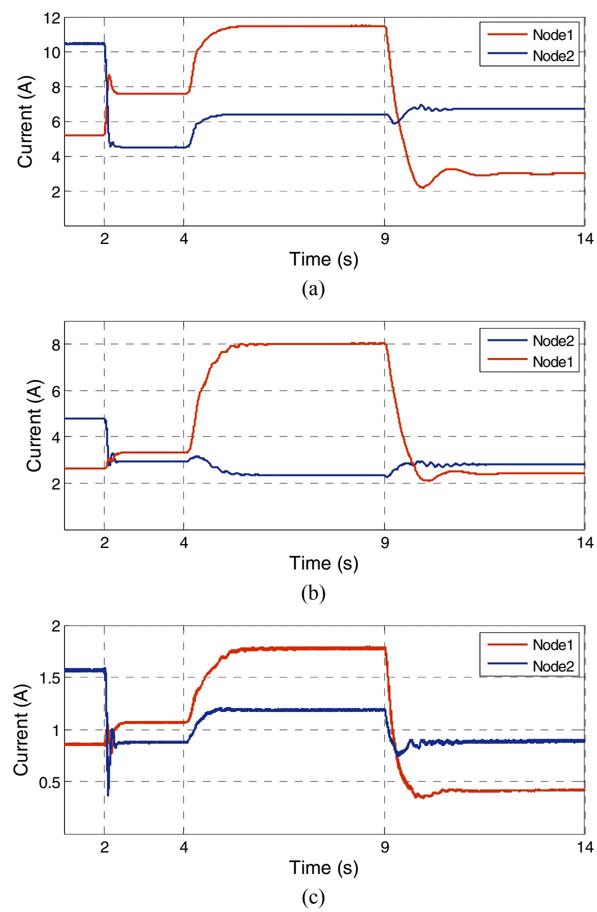


Fig. 8. Current distortion rate of nodes (RMS value in $\alpha\beta$-frame): (a) Fundamental negative sequence, (b) 3th harmonic, (c) 5th harmonic.

Required data of power and control stages of the system is available in Table I and the data concerning primary and secondary controls can be found in [11] and [14]. Based on DGs power droop characteristics, DG1 is twice of DG2.

To test different parts of the proposed hierarchical control clearly, Table II shows simulation process and the following explanations are based on this table. It is worth noting that MATLAB/Simulink is used for evaluating the proposed hierarchical control.

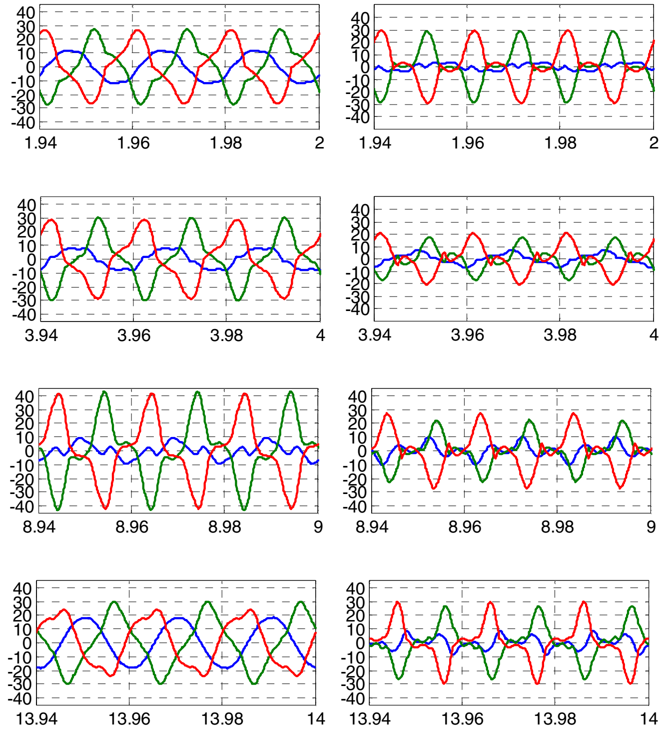
Two DGs are in the system so power, harmonic and unbalance current sharing should be considered. It is assumed that voltage quality reference of the node 1 is Total Harmonic Distortion (THD) equal to 3% ($THD_{N(1)_{ref}}$ =3%) and $VUF_{N(1)_{ref}}$ =1% while the maximum permissible VDR is considered for node 2 according to IEEE Standards 519 and 141 ($THD_{N(2)_{max}}$ =5% and $VUF_{N(2)_{max}}$ =2%) [19],[20].

Since APF is only cooperated with DG1, Fig. 7 shows voltage waveforms of node 1 and PCC according to simulation time periods (Table II). As it is represented, the node voltage is completely sinusoidal in the first period, demonstrating perfect performance and well design of droop control and selective virtual impedance. However, PCC voltage waveform is distorted. It is for the voltage drop produced through $Z_{1,2}$ (see Fig. 1). As it is shown in Fig. 7, voltage waveform of node 1 and PCC are severely distorted while current unbalance and harmonic sharing between DGs is obtained by virtual impedance (see Fig. 8). It can be seen in Fig. 8 that harmonic and unbalance components in DG2-current is higher than that of DG1 before $t = 2s$ while after this time, current sharing is happened based on DGs rated power. As shown in Fig. 7, PCC voltage is significantly improved since secondary control is initiated but node 1 voltage is severely distorted. It shows that DG1 has main role in PCC compensation. However, the cooperation is required because $VDR_{N(1)}$ is very higher than the reference value, according to Fig. 10. Since the cooperation is initiated, it can be seen that $VDR_{N(1)}$ is reduced while PCC voltage is remained unchanged. It proves that the cooperation is designed accurately.

Fig. 8 shows current distortion at nodes. As shown, since secondary control is initiated, node 1 current is severely distorted. However, as the cooperation is initiated, it can be seen that current distortion in node 1 is reduced while this parameter is nearly unchanged in node 2. It is because APF is only cooperated with DG1.

To be more illustrative, Fig. 9 shows current waveforms of nodes according to the simulation time periods. It can be seen that node2-current is more close to sinusoidal waveform since virtual impedance is initiated and current sharing is taken place. On the other hand, node1-current is more distorted. As PCC compensation is occurred by DGs, it is shown that node1-current is even more distorted than before because DG1 plays the main role in compensation. However, by initiation of the cooperation at $t = 9s$, node1-current waveform is nearly sinusoidal due to the fact that a part of PCC compensation is carried out by APF.

To test the proposed hierarchical control more accurately, Fig. 10 shows VHD curves of both positive and negative sequences of individual harmonic components and VUF of the nodes and PCC. Based on Fig. 10, nodes and PCC-VDR are



(a) (b)

Vertical axis: current(A), Horizontal axis: time(s)

Fig. 9. Current waveforms: (a) Node1, (b) Node2.

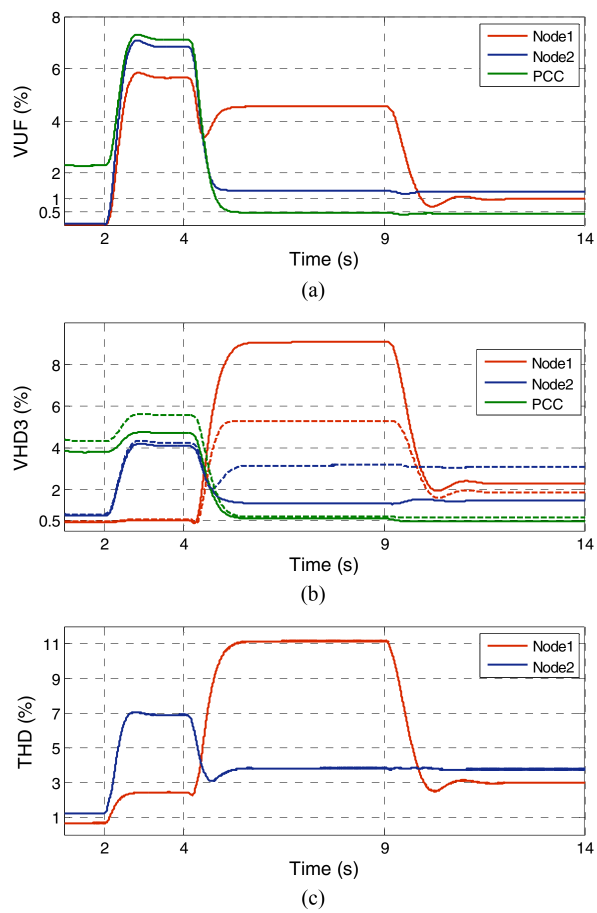


Fig. 10. Voltage Distortion Rate (dashed: positive sequence, solid: negative sequence): (a) VUF, (b) 3th harmonic, (c) THD.

increased since current sharing is happened. According to Fig. 10, when secondary control is active, PCC-VDR is significantly reduced and $VDR_{PCC_{ref}}$ is achieved but node1-VDR is severely increased and the violation from $VDR_{N(1)_{ref}}$ is occurred. In the final period, the cooperation between APF and DG1 is initiated and $VDR_{N(1)_{ref}}$ is achieved. It is shown in Fig. 10 that $VDR_{N(2)}$ and VDR_{PCC} (both positive and negative sequences of voltage harmonics and VUF) are remained unchanged when APF is participated in compensation. It shows perfect performance of the coordination and precise design of its parameters.

VI. Conclusion

A hierarchical control scheme to improve voltage harmonic distortion and voltage unbalance factor of microgrid is proposed. The hierarchical structure includes two levels. In the primary control, power and current sharing is carried out. Secondary level compensates PCC by controlling DG(s) inverters. Compensation of PCC by DG(s) might increase voltage distortion at DG(s) terminal. Thus, a coordinated control between DGs and APF is designed to share compensation. The coordinated control is based on the required power quality of each DG terminal and the APF capacity.

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