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A Secondary-Control Based Fault Current Limiter for Four-Wire Three Phase Inverter-Interfaced DGs

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***Abstract*— Fault current limiters (FCLs) are one class of solutions to cope with the upcoming challenges in microgrid protection. Considering high penetration of distributed generations (DGs) in microgrids, the necessity of designing cheap and effective FCL is getting higher. This paper attempts to fill this gap by proposing an embedded FCL operating based on modifying the secondary control of DGs. As this method is designed for four-wire system, besides cost-effectiveness, it has independency and flexibility to only limit the fault current of DG. In order to validate the proposed method, different types of faults are examined through an extensive simulation study.**

***Index Terms*— Fault current limiter, four-wire DG, Microgrid, Protection, Secondary control, SOGI PLL**

I. INTRODUCTION

In the near future structure of the power system will change from centralized to decentralized fashion. With introduction of microgrid, higher small-scale Distributed Generations (DGs) will be integrated into distribution system. Although this trend of future grid leads to lower power loss, higher reliability, and lower Carbone dioxide emission, implementation of high penetration of DGs causes new challenges for protection systems. These challenges include higher level of fault current, bidirectional nature of fault current, mechanical stress on Circuit Breakers (CBs) and transformers, miscoordination of conventional overcurrent relays, tripping of healthy feeders, sympathetic tripping, and week-infeed loop fault [1]-[3] .

Several approaches have been proposed to deal with DGs impacts on protection system. A primitive solution is replacing used CBs and transformers with higher capacity ones. This is very costly solution and not practical solution. Other solutions include limiting maximum DG capacity, enhancing conventional protection, adaptive protection, and Fault Current limiter (FCL) [1]. Limiting maximum DG capacity solution is a cheap solution but it will limit high penetration of DGs in future power system. Relay-based solutions are one of the promising solutions for the future power system; however, it needs high computation to reach the desired result.

In recent years, tremendous attention has been paid to develop FCLs for power systems. This solution allows higher penetration of DGs in the grid. The main purpose of FCL is to behave like a zero impedance in normal conditions and very high impedance in faulty conditions to limit the short-circuit current. In order to reach this goal, different types of FCLs including Passive FCL (PFCL), Superconducting FCL (SFCL), Solid State FCL (SSFCL), and controlled-based FCL were introduced to obtain the promising goal [4]-[6]. PFCLs utilize passive elements to limit the fault current. It is the cheapest and simplest type of FCL, however, the voltage drop during the normal condition is the main disadvantage of this approach. SFCL classified into two types, resistive SFCLs and inductive SFCLs. Both types have the advantages of low power loss during the normal conditions and fast response. However, high weight/size, a need for a special complex cooling system, and being expensive are their main disadvantages [7]. Recently, with the progress in semiconductor technology such as thyristor, Insulated Gate Bipolar Transistor (IGBT), and Gate Turn-Off thyristor (GTO), implementing SSFCL has become more feasible. This class of FCL has different benefits including fast response and low weight, but, the main drawbacks are commutation losses and on-state losses. Nevertheless, wide-band gap power switches are a promising technology to address these issues [8]. Converter-based approach implements FCL strategy within it by adding virtual impedance and designing switching topologies. In [9], the performance of series half-bridge DC-DC converter, full-bridge DC-DC converter, and LCL-filtered thyristor-based converters for this application are compared in terms of the fault interruption capability. In [10], the performance of multiport DC-DC converter for SSFCL is investigated under the ground and phase-phase faults. Then, [10] fault current limiting by a centralized control. Employing virtual impedance in parallel with filter is another solution to limit fault current by reducing current reference in proportion to output voltage [11]. In [12], a method based on transient virtual impedance is proposed to limit fault current by exerting high and low values of virtual impedance for the faulty and normal condition, respectively. Secondary control restores voltage and frequency. Regarding this issue, it will fight against reducing voltage during the faulty conditions applying by high value of virtual impedance.

This paper modifies the structure of secondary control to limit the fault current to twice of the nominal current value for a three-phase four-wire DG inverter in Voltage-Control Mode (VCM) and proposes a simple but effective FCL for Current Control Mode (CCM). The proposed method takes advantage of four-wire system to limit fault current in each phase without effecting on healthy phase. In addition, the proposed FCL has a very fast response and does not cause harmonic distortion

II. PROPOSED METHOD

The aim of the proposed method is having a fast response of fault current limiting for a four-wire VSI that has a secondary control to fix the voltage to its nominal value. In order to reach this goal, the secondary level is modified to generate appropriate voltage reference during the faulty and unfaulty conditions. The following subsection describes first the control system for three-phase four-wire inverter controlled in VCM and CCM, and then presents the new strategy for limiting fault current strategy.

A. Three-phase four-wire control system

Three-phase four-wire system is a common topology of DG in low-voltage microgrids to support single-phase and unbalanced loads by adding a path for zero-sequence current of the loads. Among different topologies of four-wire systems, the three-leg inverter with split dc-link capacitors is the popular one where the midpoint of the dc-link is connected to a neutral point (see Fig. 1) [13]. Compared to three-phase four-leg topology, it has lower power switch and control complexity [14].

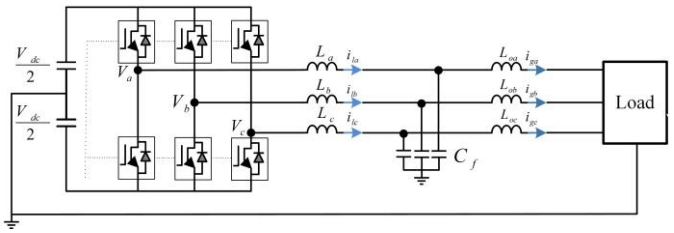

Fig. 1. Topology of three-phase four-wire with a split dc link capacitors.

In isolated microgrid, at least one DG must operate in VCM to control both voltage and frequency and other DGs could work in VCM or CCM. The controller of each DG includes primary control and secondary control. The primary level uses droop control and virtual impedance to regulate the power sharing. The secondary control restores voltage and frequency to their nominal values. The control systems for VCM and CCM VSIs are presented in Figs. 2 and 3, respectively.

The inner control loops in VCM consists of outer voltage loop and inner current loop (both based on Proportional-Resonant, PR, controllers) to regulate capacitor voltage. In CCM, the controller mainly consists of PR current controller and active damping loop.

As in natural (abc) reference frame PR controller has better performance than PI one [15], in the inner loop control, PR controllers are considered for both voltage control and current control, as mentioned before:

$$G_V = k_V + \frac{2.k_{rV}.\omega_{cV}.S}{(S^2 + 2.\omega_{cV} + \omega_0^2)} \quad (1)$$

$$G_I = k_I + \frac{2.k_{rI}.\omega_{cI}.S}{(S^2 + 2.\omega_{cI} + \omega_0^2)} \quad (2)$$

where, ω_{cV} and ω_{cI} are the cut-off frequencies for current and voltage loops, respectively. In addition, $k_V(k_I)$ and $k_{rV}(k_{rI})$ are proportional and resonant coefficients of the voltage (current), respectively. In addition, if harmonic control is required harmonic resonant should be added [16].

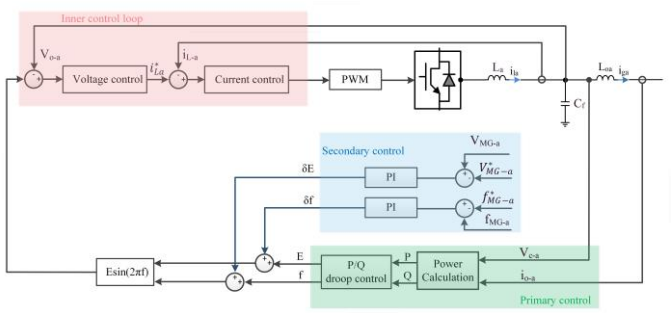

Fig. 2. VCM Scheme of phase-a of the three-phase four-wire DG with a split dc capacitors .

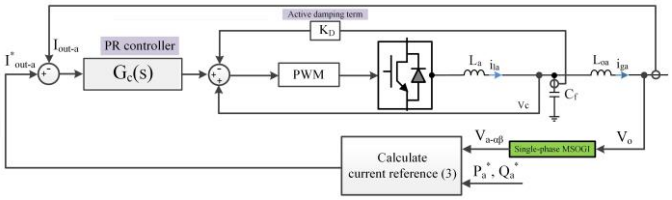

Fig. 3. CCM Scheme of phase-a of the three-phase four-wire DG with a split dc capacitors .

In secondary control level, PI controllers are applied to generate proper control signals to be followed by droop controllers and restore both frequency and voltage to their nominal values. The related equations are as follows:

$$\delta E = k_{PE}(E_{MG}^* - E_{MG}) + k_{iE}\int((E_{MG}^* - E_{MG}))dt \quad (3)$$

$$\delta f = k_{Pf}(f_{MG}^* - f_{MG}) + k_{if}\int((f_{MG}^* - f_{MG}))dt \quad (4)$$

where, $k_{PE}(k_{Pf})$ and $k_{iE}(k_{if})$ are the parameters of PI controllers. Once these correction values of voltage and frequency are obtained, these signal values are sent to primary control of each DG units.

B. Fault current limiter strategy

According to secondary control operation, , during the faulty conditions high amount of voltage amplitude is added to voltage reference of VCM VSIs to keep microgrid voltage within accepted rate. This would be at the expense of high value of VSI output current. On the other hand, DG has to protect itself from being damaged through limiting output current during the faulty conditions. In order to reach this goal, this paper proposes a multifunctional secondary control that its task is to keep voltage amplitude at nominal value in normal operation as well as to keep output current of fault fixed to twice of its nominal value.

In the proposed FCL (Fig. 4), secondary control has a distinct duty for each of normal and faulty conditions. In the normal condition, deviation of frequency and voltage are compensated by the secondary control, whereas, in the faulty condition, voltage reference is reduced in such a way that the injected current of DG is limited.

In the case of fault, the amplitude of each phase is calculated by a Multiple Second-Order Generalized Integrators Phase-Locked Loop (MSOGI-FLL). In this structure, SOGI Quadrature Signal Generations (SOGI-QSGs) are combined in

parallel to detect and extract fundamental, third, fifth harmonics individually. This method has a good disturbance rejection capability, high filter capability, fast dynamic response and medium computation burden [17].

As shown in Fig. 4, the fundamental component of current, which is obtained by MSOFI-FLL, is subtracted from twice of nominal current, and finally it passes through a deadband block and a PI controller, serially. It must be noted that the deadband block is utilized to only let PI controller be active when current amplitude is above $1.8I_n$. It must be noted that Fig.4 is for phase-a, the similar scheme us considered for other phases. In order to let proper and smooth switching between two modes of operations, the following criterion is taken into account:

$$maximum\ value\ of\ |I_m|\ during\ the\ last\ 20ms > 1.8I_n \quad (5)$$

On the other hand, a simple limiter on produced current reference would be sufficient in CCM VSI to confine current to the twice of nominal current. The structure of FCL for CCM VSI is shown in Fig. 6.

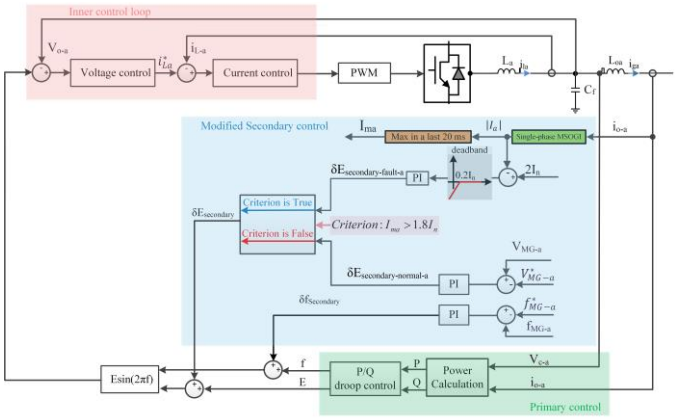

Fig. 4. Proposed FCL for voltage-control of phase-a of the three-phase four-wire DG with a split dc capacitors.

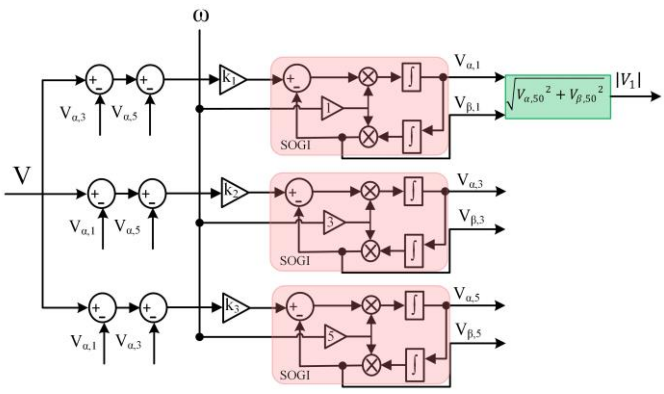

Fig. 5. Scheme diagram of MSOGI.

III. Simulation Results

The effectiveness of the proposed method is investigated in a MATLAB/Simulink model of Fig. 7 consisting of three DGs and one load.

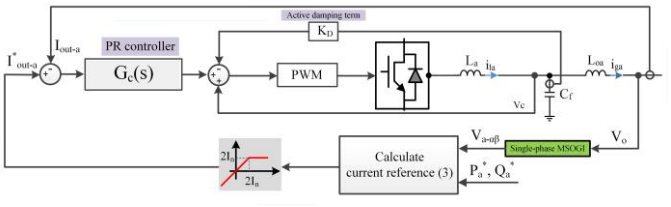

Fig. 6. Proposed FCL for current-control of phase-a of the three-phase four-wire DG with a split dc capacitors.

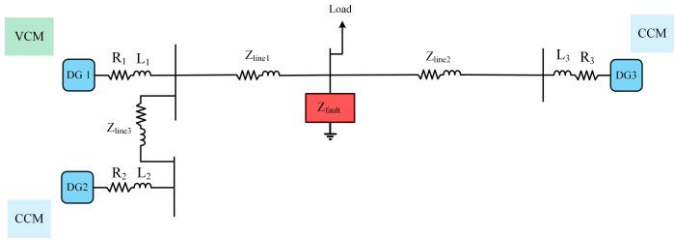

Fig. 7. System model.

TABLE I. System parameters

Type	Parameters		Value
	Symbol	Quantity	
Electrical setup	V_{dc}	DC Voltage	650 V
	V_{MG}	MG voltage	311 V
	F	MG Frequency	50 Hz
	C	Filter Capacitance	25 μF
	L	Filter Inductance	1.8 mH
	L_o	Output Inductance	1.8 mH
	P_R	Load active power	3500 W
	Z_{L1}, Z_{L2}, Z_{L3}	Line resistance	2+j0.3 Ω
Inner Loops (VCM)	k_{pV}	Proportional coefficients of voltage	1
	k_{rV}	Resonant coefficients of voltage	50
	k_{pI}	Proportional coefficients of current	20
	k_{rI}	Resonant coefficients of current	1000
	ω_{cV}	cut-off frequency of voltage loop	2 Hz
	ω_{cI}	cut-off frequency of control loop	2 Hz
Inner Loops (CCM)	k_{pII}	Proportional coefficients of current	300
	k_{rII}	Resonant coefficients of current	2500
	ω_{cII}	cut-off frequency of control loop	2 Hz
	k_D	Damping factor	300
Droop Control	k_{pP}	Active power droop term	0.0003 Ws/rad
	k_{iP}	Active power droop integral term	0.0015 Ws/rad
	k_{pQ}	Reactive power droop term	0.2 VAr/V
Secondary Control	k_{pf}	Frequency proportional term	0.001
	k_{if}	Frequency integral term	1 s^{-1}
	k_{pE}	Voltage proportional term	0.001
	k_{iE}	Voltage integral term	0.5 s^{-1}

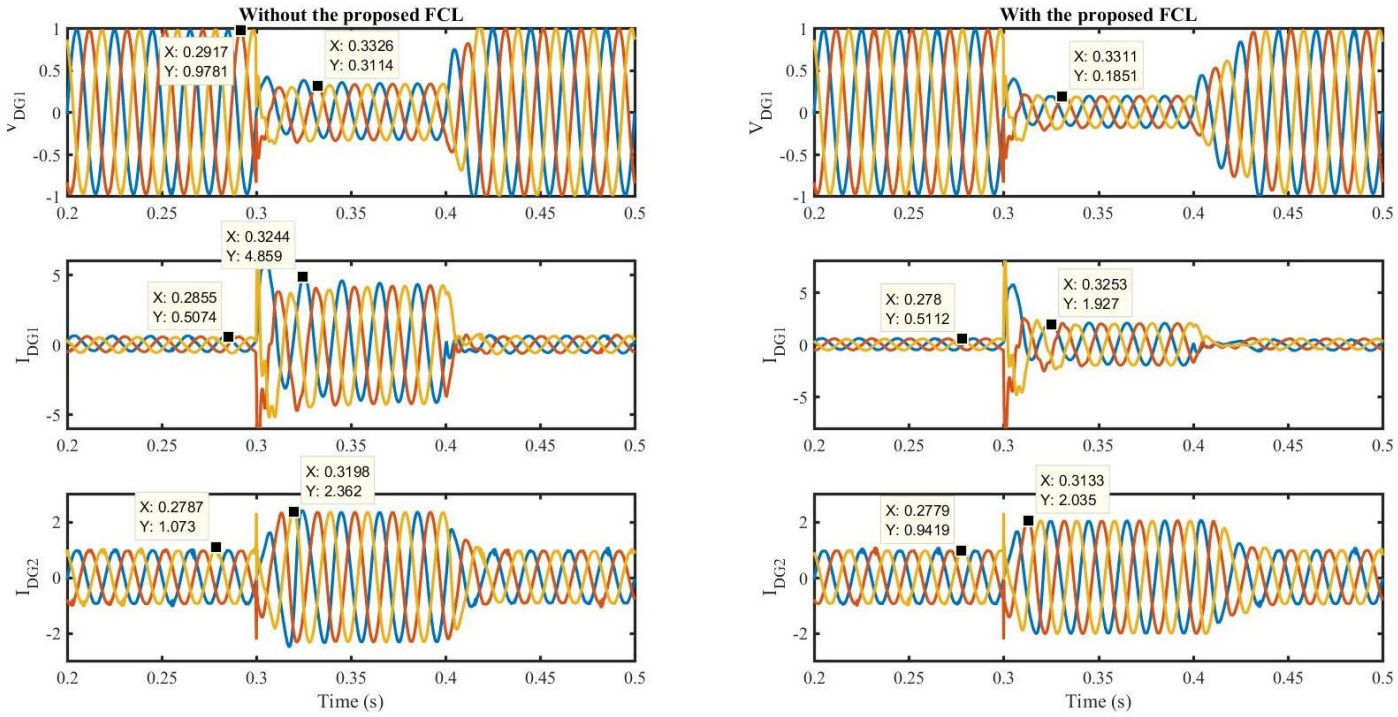

Fig. 8. Voltage of DG_1, current of DG_1, and current of DG_2 of four-wire inverter during the ABCG fault.

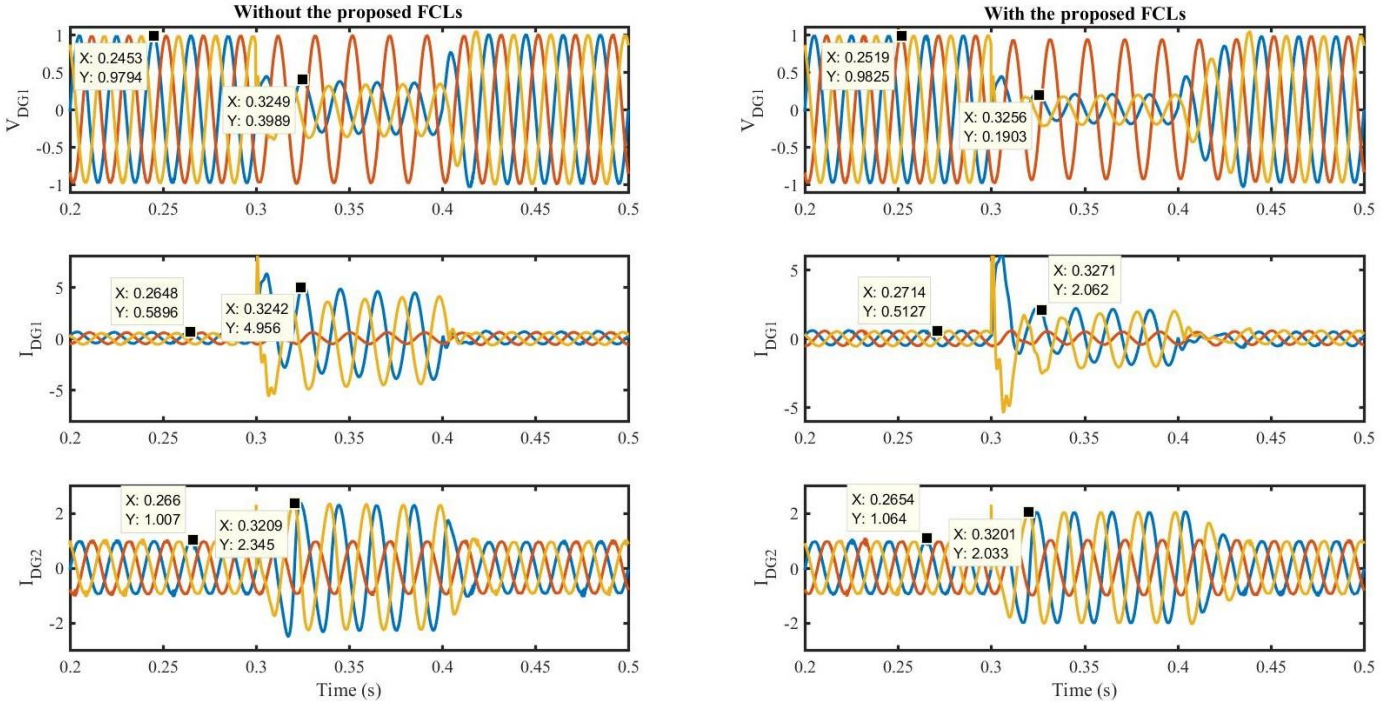

Fig. 9. Voltage of DG_1, current of DG_1, and current of DG_2 of four-wire inverter during the ACG fault.

One of the DGs operates in VCM and the others work in CCM. The parameters of this simulation system are presented in Table I. Different type of faults including ABCG (three-phase to ground), ACG, BC, and CG are examined to demonstrate the efficiency of the proposed method. In each case, the fault is placed across the load and it's the fault resistance between each phase and phase to ground are considered to be 1Ω. As shown in Fig.8, when there is no FCL for the ABCG fault, the voltage drops to 0.31 p.u. and the I_{DG1} and I_{DG2} increase up to 4.9 p.u. and 2.362 p.u., respectively. However, by using the proposed FCL, voltage of DG_1 decreases to 0.1851 p.u. to limit the fault current of DG_1 to 2 p.u. in 25 ms. On the other hand, for the CCM-VSI the limiter on current reference limits the fault current to twice of nominal current, abruptly.

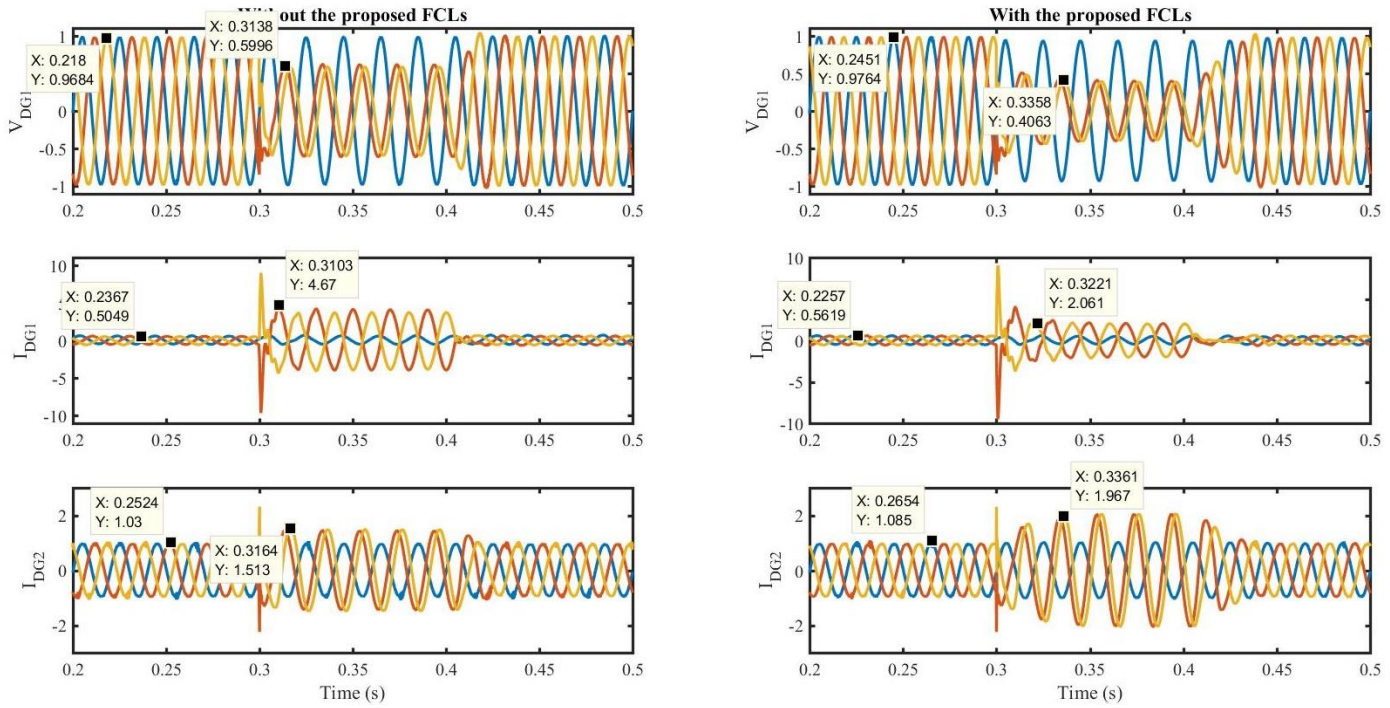

Fig. 10. Voltage of DG_1, current of DG_1, and current of DG_2 of four-wire inverter during the BC fault.

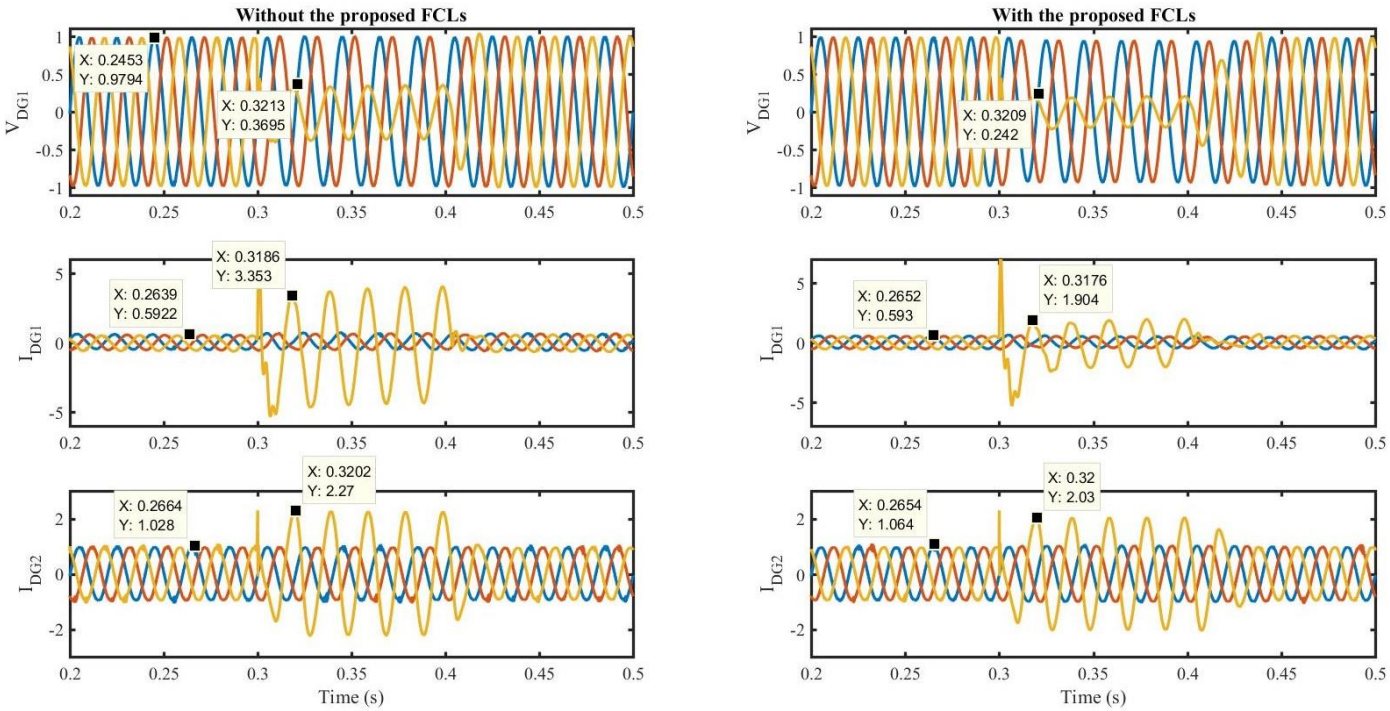

Fig. 11. Voltage of DG_1, current of DG_1, and current of DG_2 of four-wire inverter during the CG fault.

In ACG the current of DG_1 reach to around 4 times of its nominal value. The proposed FCL decreases only voltages of faulty phase of VC-VSI (A and C) by measuring the related currents. As it is shown in Fig.9, the current of DG_1 is limited to 2 p.u. in 27 ms. On the other hand, current reference limiter of CCM-VSIs (DG_2,DG_3) confines the fault current, abruptly.

As shown in Fig. 10, for BC fault, the current of faulted phase of DG_1 reaches 4.67 p.u. With applying the proposed method, only voltage references of phase-B and C reduce to 0.4063 p.u. As a result, the current fixed to 2 p.u. in around 20 ms. On the other hand, the FCL of DG_2 limit fault immediately.

Finally, a CG fault is exerted in the load bus. It can be seen that the proposed method has the same performance but even faster in limiting fault.

The summary of simulated results is presented in Table II.

TABLE II. Performance of the proposed method for four types of fault

Fault type	**THD_V** (%)	**THD_I** (%)	**V_{DG1}**	**I_{DG1}**	**Response Time**
ABCG	1.37	0.83	0.185 p.u.	1.93 p.u.	25 ms
ACG	2.30	1.21	0.33 p.u.	2.06 p.u.	27 ms
BC	2.42	0.42	0.41 p.u.	2.06 p.u.	22 ms
CG	0.33	0.44	0.24 p.u.	1.9 p.u.	18 ms

IV. CONCLUSION

In this paper, a new embedded FCL is designed to limit the current to twice of its nominal current for three-phase four wire inverter. The proposed method first measures each phase currents of DGs by the MSOGI, then based on the propose fault detection criterion, two different compensation references are transmitted to the primary control for normal and faulty conditions. According to the obtained results for different type of faults, the advantages of the proposed FCL are summarized as follows:

- Simplicity.
- Fast response (maximum 20 ms)
- Not inserting current/voltage harmonic during limiting current.
- Removing the need for an external FCL device.

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