Triangle Carrier based Discontinuous PWM for Three-Level NPC Inverters

Kai Li, Member, IEEE, Min Wei, Chuan Xie, Member, IEEE, Fujin Deng, Member, IEEE, Josep M. Guerrero, Fellow, IEEE and Juan C. Vasquez, Senior Member, IEEE.

Abstract—This paper proposes a triangle carrier based discontinuous PWM (TCB-DPWM) implement method for three-level neutral-point-clamped (3L-NPC) inverters. The function equivalent relationship of proposed TCB-DPWM and space vector based discontinuous PWM (SVB-DPWM) is mathematically analyzed in this paper. The proposed TCB-DPWM method effectively simplified the implementation of the SVB-DPWM by injecting twice common mode voltages (CMVs) to original modulation signals, where different DPWM methods can be easily obtained in a unified scheme by setting different values of proportional allocation factor for small vectors in different sectors. In addition, a TCB-DPWM based neutral point voltage balancing method is investigated to demonstrate its application. The polarity of the CMV injection is regulated according to the polarity of the proportional allocation factor to realize the neutral point voltage balancing. Finally, the proposed TCB-DPWM and neutral point voltage balancing method are both verified by simulation and experimental results. The results show that the proposed TCB-DPWM can effectively simplify the implementation of modulation and improve system efficiency.

Index Terms—Three-level neutral-point-clamped inverter, voltage source inverter, discontinuous PWM, neutral point voltage balancing.

I. INTRODUCTION

Three-level neutral-point-clamped (3L-NPC) voltage source inverters are widely used in many medium- and high-power applications. Compared with traditional two-level inverters, the 3L-NPC inverter is with better performances of efficiency, harmonics and power capability [1-3]. Recently, the T-type 3L-NPC is proposed to alternate the traditional NPC to improve the efficiency [4] [5]. The topology diagram of a T-type 3L-NPC inverter is shown in Fig.1. The main advantage of the T-type 3L-NPC inverter is the lower voltage rating of the employed devices, as the two switches of neutral point have a peak inverse voltage of half of that required in the conventional 3L-NPC inverter. Furthermore, the structure of T-TYPE 3L-NPC inverter provides lower conduction losses, compared to conventional 3L-NPC of the same ratings [6].

This work was supported in part by the National Natural Science Foundation of China (No.51707030), the Sichuan Science and technology support program (No. 2016GZ0027) and the Fundamental Research Funds for the Central Universities of China (No. ZYGX2015J075). A part of work in this paper was exhibited in the conference of APEC 2017, March 26th – 30th, Tampa, FL, USA.

K. Li, M. Wei, C. Xie are with School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu, 611731, China (e-mail:autolikai@gmail.com; 403188925@qq.com; c.xie@uestc.edu.cn).

F. Deng is with the Department of Electrical Engineering, Southeast University, Nanjing, 210096, China (dfjifa@163.com)

J. M. Guerrero and J. C. Vasquez are with the Department of Energy Technology, Aalborg University, 9220 Aalborg East, Denmark (e-mail: joz@et.aau.dk; juq@et.aau.dk).
technique implementation of general DPWM (DDT-GDPWM) was proposed in [7]. For the purpose of reducing common mode voltage (CMV), a CMV reduction DPWM (CMVR-DPWM) was proposed in [13-14]. Actually, the space vector base DPWM can be functionally equivalent to sine-triangle carrier based DPWM [15]. In most of the practical applications, the modulation strategy is implemented by a microprocessor or digital signal processor (DSP). However, it is easier to realize sine-triangle carrier based modulation in practical applications.

The four basic DPWMs in the two-level inverter, DPWM I-IV, can also be extended to three-level inverters [16-18]. For 3L-NPC inverters with DPWM, an additional option of clamping voltage level is added. The clamped phases can be clamped to positive DC bus or neutral point or negative DC bus [19]. The clamped phases, clamped voltage levels and the clamped durations can also be optimally designed according to the optimization requirements. The DPWMs aimed at reducing the switching losses [18-20], reducing the CMV [20-21] and balancing neutral point voltage [20, 22, 23] were proposed in literature. However, the existing implementation methods of above mentioned DPWMs for three-level inverters are very complex in applications, especially in the above optimization situations because they are based on space vector and requiring three procedures: sector judgment, function time calculation and pulse pattern generation. Although literature [24, 25] adopt triangular carrier based DPWM, the procedures to obtain the final modulation signals are also not easy, because the procedures to calculate CMV are divided into many situations. Furthermore, the existing relationship analysis between the TCB-DPWM and SVB-DPWM for 3L-NPC inverters is not seen in the existing literature.

In order to simplify the implementation of space vector based discontinuous PWM, this paper proposes a TCB-DPWM for 3L-NPC inverters. In addition, the relationships between the proposed TCB-DPWM and the conventional SVB-DPWM are mathematically analyzed based on [26]. Different DPWMs can be realized in a unified scheme by setting different values of proportional allocation factor for small vectors in different sectors. In order to demonstrate its applications in optimization situations, a TCB-DPWM based neutral point voltage balancing method is also proposed. The neutral point voltage can be controlled by regulating the polarity of the proportional allocation factor in TCB-DPWM. The proposed TCB-DPWM and the neutral point voltage balancing method are both verified by simulations and experiments.

This article is organized as follows: Conventional SVB-DPWMs are reviewed in Section II. In Section III, the TCB-DPWM and its implementation method for 3L-NPC inverters are proposed. In addition, the relationships of TCB-DPWM and SVB-DPWM are mathematically analyzed. Based on the proposed TCB-DPWM, a neutral point voltage balancing method is investigated in Section IV. The effectiveness of the proposed scheme is verified by simulations and experiments in Section V. Section VI summarizes the conclusions and contributions of this paper.
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2812704, IEEE Journal of Emerging and Selected Topics in Power Electronics

Table I. The values of $k$ in different sectors for SVB-DPWMs.

<table>
<thead>
<tr>
<th>SVB-DPWMs</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPWM I</td>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
<tr>
<td>DPWM II</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
<tr>
<td>DPWM III</td>
<td>-1</td>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
<tr>
<td>DPWM IV</td>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
</tbody>
</table>

Fig. 4. The unified scheme of TCB-DPWM.

Fig. 3. The clamped phases and clamped voltage levels in each sector.

vector space. Zero vectors and small vectors are redundancy vectors [27].

Conventional SVPWM adopts the nearest three vectors to synthesize the vector reference and to generate seven stages pulse patterns [28]. For a reference vector $U_{ref}$ in Fig.2(a), its pulse patterns are shown in Fig.2(b), where the vectors $poo$ and $onn$ are a couple of redundancy small vectors. In Fig.2(b), $k (-1 \leq k \leq 1)$ is defined as the proportional allocation factor for redundancy small vectors, which determines the following different situations.

1) If $k=1$: positive small vector $poo$ is used, point A in Fig.1 is clamped to positive DC bus $P$.
2) If $k=-1$: negative small vector $onn$ is used, point C in Fig.1 is clamped to negative DC bus $N$.
3) If $-1<k<1$: no phase are clamped to any voltage levels.

Normally, when $k=1$ or $k=-1$, one of the three phases will be clamped to positive DC bus $P$ or neutral point $O$ or negative DC bus $N$, thus, DPWM will be obtained. Table I shows four basic SVB-DPWMs including DPWM I–IV [16–18], where $k$ has different values ($1$ or $-1$) in different sectors.

Fig. 3(a) and Fig. 3(b) show the clamped phases and clamped voltage levels for $k=1$ and $k=-1$ respectively, where, $A+*$ means that point $A$ in Fig.1 is clamped to positive DC bus $P$; $A0$ means that point $A$ is clamped to neutral point $O$; $A-$ means that point $A$ is clamped to negative DC bus $N$. For the four basic SVB-DPWMs in Table I, the clamped phase and clamped voltage level can refer to Fig.3 according to the value of $k$ in the corresponding sector.

III. PROPOSED TCB-DPWM FOR 3L-NPC INVERTER

A. Proposed TCB-DPWM

The TCB-DPWM is proposed, as shown in Fig.4, to simplify the implementation of the SVB-DPWMs through injecting proper CMV to original modulation signals including the 1st CMV injection $u_{c1}$ and the 2nd CMV injection $u_{c2}$. Three original reference signals $u_a$, $u_b$ and $u_c$ are the output of the basic voltage/current control [29]. After twice CMV injections, the final modulation signals of $u_{mA}$, $u_{mB}$ and $u_{mC}$ will be obtained. Drive signals for switching devices are generated by comparing two phase disposition triangle carriers with final modulation signals.

In TCB-DPWM, the definition, meaning and range of $k$ are the same as SVB-DPWM, where, $k$ is the proportional allocation factor of redundancy small vectors. Different PWM methods, as well as SVB-DPWMs, can be obtained by setting different values of $k$ into the unified scheme shown in Fig.4. The functions of inverters with TCB-DPWM and SVB-DPWM are equivalent when the same $k$ are set. The procedure to realize the proposed TCB-DPWM will be interpreted in the following sections.

B. 1st CMV injection

The three reference signals $u_a$, $u_b$ and $u_c$ in Fig.4 can be expressed by:

$$u_a = U_m \cos(\omega t) = (m \times U_{dc} \sqrt{3} \cos(\omega t))$$

$$u_b = U_m \cos(\omega t + 2\pi/3) = (m \times U_{dc} \sqrt{3} \cos(\omega t + 2\pi/3))$$

$$u_c = U_m \cos(\omega t + 4\pi/3) = (m \times U_{dc} \sqrt{3} \cos(\omega t + 4\pi/3))$$

where, $U_m$ is the peak value of reference voltage, $\omega$ is the angular frequency of reference voltage, $m = \sqrt{3}U_m/U_{dc}$ is the modulation index.
In Fig.4, the 1st CMV injection \( u_{1z} \), as shown in (2), is injected to the original three reference signals to improve the modulation index (DC voltage utilization) to its maximum value 1. The maximum modulation index of the proposed method will be the same as that for SVPWM.

\[
u_{1z} = -0.5 \times \text{MAX}(u_a, u_b, u_c) - 0.5 \times \text{MIN}(u_a, u_b, u_c)
\]

(2)

where, \( \text{MAX} \) and \( \text{MIN} \) are the functions to obtain the maximum and minimum values, respectively.

After the 1st CMV injection, three modulation signals \( u_{az} \), \( u_{bz} \) and \( u_{cz} \) are given by

\[
u_x = u_x + u_{1z}, \quad x = a, b, c
\]

(3)

Fig.5 shows an example of the original modulation signal \( u_x \), the first CMV injection \( u_{1z} \) and the modulation signal \( u_x \) at the maximum value of modulation index. It can be seen from Fig.5 that the modulation signal \( u_{az} \) will be located within the reachable voltage band from \(-U_{dc}/2\) to \(U_{dc}/2\) because of the 1st CMV injection.

### 2nd CMV injection

The 2nd CMV injection is used to obtain the functional equivalent relationships between SVB-DPWM and TCB-DPWM. If the pulse patterns of SVB-DPWM and TCB-DPWM are the same, the functional equivalent relationships will be achieved.

This section also takes the reference vector \( U_{ref} \) shown in Fig.2(a) as an example; its pulse patterns are replotted in Fig.6(a). For a three-level inverter, two phase disposition triangle carriers \( u'_a \) and \( u'_b \), as shown in Fig.6(b), are used to generate the pulse patterns. The laws to generate pulse patterns are as follows [15]:

1) **Case a:** if modulation signal is bigger than positive carrier \( u'_a \), switching state \( p \) will be generated.
2) **Case b:** if modulation signal is smaller than negative carrier \( u'_b \), switching state \( n \) will be generated.
3) **Case c:** if modulation signal is bigger than negative carrier \( u'_c \) and smaller than positive carrier \( u'_a \), switching state \( o \) will be generated.

In order to generate the same pulse patterns shown in Fig.2(a), the final modulation signals of TCB-DPWM for each phase should be \( u_{max}, u_{mid} \) and \( u_{min} \) as shown in Fig.6(b).

However, it is very difficult to obtain the relationship of \( u_{max} \) and \( u_{cz} \) in the frame of two phase disposition triangle carriers. In order to simplify the procedure, a conversion defined in (4) is used to convert the frame of two phase disposition triangle carriers to the frame of one virtual common triangle carrier.

\[
u^*_x = \begin{cases} u - U_{dc}/4, & \text{if } u \geq 0 \\ u + U_{dc}/4, & \text{if } u < 0 \end{cases}
\]

(4)

As shown in Fig.7, modulation signals \( u_{max}, u_{az} \) are converted to \( u^*_{max}, u^*_a \), respectively. The two phase disposition triangle carriers \( u'_a \) and \( u'_b \) are converted to one virtual common triangle carrier \( u'_a \).

The relationships of \( u^*_{max} \) and \( u^*_a \) will be discussed in the frame of one virtual common triangle carrier to obtain the 2nd CMV injection \( u_{2z} \). In the frame of one virtual common triangle carrier, the CMV injection is labeled as \( u_{2z} \). Thus, the relationships of \( u^*_{max} \) and \( u_{az} \) are given by:

\[
u^*_{max} = u^*_a + u_{2z}, \quad x = a, b, c
\]

(5)

After the conversions, modulation signals and triangle carrier are all located in the common voltage band from \(-U_{dc}/4\) to \(U_{dc}/4\) as shown in the white background zone of Fig.6(b).

According to the virtual common triangle carrier in Fig.6(b), its mathematical equation in \( r \in [0, T_s/2] \) can be expressed as follows:

\[
u^*_t(t) = \frac{U_{dc}}{4} \times (1 - \frac{4}{T_s} \times t), \quad 0 \leq t \leq \frac{T_s}{2}
\]

(6)

where \( u^*_t(t) \) is the instantaneous value of \( u^*_a \) at the time of \( t \), \( T_s \) is the carrier wave period.

As shown in Fig.6(b), \( u^*_{max}, u^*_a \) and \( u^*_b \) are the values of \( u^*_t(t) \) at the instant of \( t_1 \), \( t_2 \) and \( t_3 \), respectively.

\[
\begin{align*}
u^*_{max} &= u^*_t(t_1), \quad t_1 = \frac{1 - k}{4} \times T_s \\
u^*_a &= u^*_t(t_2), \quad t_2 = t_1 + \frac{1}{2} \times T_s \\
u^*_b &= u^*_t(t_3), \quad t_3 = t_2 + \frac{1}{2} \times T_s
\end{align*}
\]

(7)

According to the similar triangles in Fig.6(b), the following equations can be obtained:
After the twice CMV injections, three target modulation signals of TCB-PWM \( u_{ma}, u_{mb} \) and \( u_{mc} \) can be obtained:

\[
    u_{ma} = u_a + x, \quad x = a, b, c
\]  

Fig. 8 shows the modulation signals generated by the proposed TCB-DPWM when \( m=0.4, 0.8 \) and \( k=1, -1 \). The red dash line \( u_a \) is the original reference signal of phase A. The black dotted line \( u_t \) is the total CMV injection. The blue solid line \( u_{ma} \) is the final modulation signal to drive signal generating module. The final modulation signals in Fig. 8 are consistent with the clamped phase and clamped voltage levels in Fig. 3.

D. Discussions

According to the above analysis, the procedures to realize the proposed TCB-DPWM just need a few arithmetic operations to obtain the final modulation signals and will be very easy to implement in applications. On the contrary, the procedures to realize SVB-DPWM are more complex, which require three procedures: sector judgment, function time calculation and pulse pattern generation.

In practical applications, the control and modulation strategies for inverters are realized by a microprocessor or digital signal processor. The computation burden for the proposed strategy and SVPWM are summarized in Table II.

As shown in Table II, the proposed algorithm may require about 34 machine cycles for the microprocessor in one carrier wave period. However, in the conventional SVB-DPWM methods such as \([16-18]\), it would require more than 87 machine cycles for microprocessor in one carrier wave period, which is more than two times of that in the proposed method.

IV. PROPOSED TCB-DPWM BASED NEUTRAL POINT VOLTAGE BALANCING METHOD

In this paper, neutral point voltage balancing is used to demonstrate the application of the proposed TCB-DPWM. Among different method of neutral point voltage balancing for 3L-NPC, controlling the function time of redundant small vectors is the simplest and most effective method from the space vector modulation point of view \([30]\). Based on the same basic idea and the proposed TCB-DPWM, this paper proposes an equivalent implement method as hysteresis control in \([30]\) from the triangle carrier modulation point of view. It should be noted that there is some literature \([31, 32]\) adopting DPWM to control the neutral point voltage. The DPWM in these papers is based on once offset injection. Its maximum modulation index is not as high as the proposed method.

A. Analysis of Neutral Point Voltage

As shown in Fig. 1, the voltage of \( C_F \) and \( C_N \) are \( U_{P} \) and \( U_{N} \). Thus, the voltage difference \( \Delta U_C \) of DC side capacitors is given by:

\[
    U_{C} = U_{N} + U_{P}
\]
The value of $\Delta U_C$ depends on the neutral point current $i_m$. As shown in Table III, when $i_m > 0$, current flows out of neutral point $O$, the voltage $U_N$ of $C_N$ will lower, the voltage $U_P$ of $C_P$ will rise. Thus, the difference voltage $\Delta U_C$ of DC side capacitor will reduce. Similarly, when $i_m < 0$, current flows into neutral point $O$, the voltage $U_N$ of $C_N$ will rise, the voltage $U_P$ of $C_P$ will lower, thus, the difference voltage $\Delta U_C$ of DC side capacitor will rise. The neutral point voltage can be controlled by controlling the neutral point current $i_m$.

When the switching state of one phase is $o$, its current will flow into or out of the neutral point $O$. Thus, the neutral point current $i_m$ is determined by the magnitude and polarity of the corresponding phase current and the function time of switching state $o$. As shown in Fig.6, the function time of switching state $o$ in a switching period is normally determined by the modulation signal as

$$T_o = (1 - \frac{|u_{wm}|}{U_{dc} / 2}) \times T_s, \quad x = a, b, c \tag{16}$$

where, $T_o$ is the function time of switching state $o$ caused by the modulation signal $u_{wm}$.

Suppose that the current flowing out of bridge is positive, as shown in Fig.1, the average neutral point current in a switching period can be obtained.

$$\bar{i}_m = \frac{1}{T_s} (i_m T_m + i_a T_m + i_c T_m) = i_m (1 - \frac{|u_{wm}|}{U_{dc} / 2}) + i_a (1 - \frac{|u_{wm}|}{U_{dc} / 2}) + i_c (1 - \frac{|u_{wm}|}{U_{dc} / 2}) \tag{17}$$

For a three-wire three-phase inverter, the sum of $i_m$, $i_a$ and $i_c$ is zero. Thus, equation (17) can be simplified as:

$$\bar{i}_m = \frac{2}{U_{dc}} \left( -i_m \times |u_{wm}| - i_a \times |u_{wm}| - i_c \times |u_{wm}| \right) \tag{18}$$

According to Section III, it can be observed that the modulation waves of $u_a$, $u_b$, and $u_c$ have the same polarity because the added CMV will not change the polarity of each modulation signals. For example, if $u_{wa} \geq 0$, then $u_{wb} \geq 0$ and $u_{wc} \geq 0$; if $u_{wa} \leq 0$, then $u_{wb} \leq 0$ and $u_{wc} \leq 0$. Thus, $i_m$ in (18) can be discussed according to the polarity of the original reference voltage $u_a$. According to Fig.2(a) and (18), it can be seen that the polarity of $u_a$ and the average neutral point current $\bar{i}_m$ will have six situations as listed in Table IV.

According to Table IV, (18) can be rewritten as:

$$\bar{i}_m = \frac{2}{U_{dc}} (\text{sign}(u_a) u_{wa} \text{sign}(u_a) u_{wb} \text{sign}(u_a) u_{wc} - i_m) + \frac{4}{U_{dc}} (\text{sign}(u_a) i_a u_{wa} - \text{sign}(u_a) i_a u_{wb}) \tag{19}$$

where, $\text{sign()}$ is the function to acquire the sign of input. $j (j \in \{a, b, c\})$ is the related phase that can affect the neutral point voltage, the values of $j$ in different sectors are: $j = a$, in sectors 1, 6, 7 and 12; $j = b$, in sectors 4, 5, 10 and 11; $j = c$, in sectors 2, 3, 8 and 9.

From (19), it can be obviously seen that the $\bar{i}_m$ can be regulated by $u_{wa}$, while the value of $u_{wa}$ can be decided by $k$ as:

1) $k=1$, then

$$u_{za(1-\)} = \frac{U_{dc}}{4} - \text{MAX}(u_{za}^*, u_{zb}^*, u_{zc}^*) \tag{20}$$

2) $k=-1$, then

$$u_{za(-1)} = \text{MIN}(u_{za}^*, u_{zb}^*, u_{zc}^*) - \frac{U_{dc}}{4} \tag{21}$$

The second CMV injection $u_{za}$ at different modulation index $m$ and different reference voltage angle $\theta$ are shown in Fig.9. According to (20), (21) and Fig.9, it can be obtained that the polarity of $u_{za}$ is determined by the polarity of $k$. In other words, when $k=1$, $u_{za} \geq 0$; when $k=-1$, $u_{za} \leq 0$. | Table III. The relationships between $\Delta U_C$ and $i_m$.
<table>
<thead>
<tr>
<th>$i_m$</th>
<th>$\Delta U_C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_m &gt; 0$</td>
<td>$U_N \downarrow$ $U_P \uparrow$ $\Delta U_C \downarrow$</td>
</tr>
<tr>
<td>$i_m &lt; 0$</td>
<td>$U_N \uparrow$ $U_P \downarrow$ $\Delta U_C \uparrow$</td>
</tr>
</tbody>
</table>

<p>| Table IV. The average neutral point current in different situations. |</p>
<table>
<thead>
<tr>
<th>Sector</th>
<th>Voltage relation</th>
<th>$\bar{i}_m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 &amp; 1</td>
<td>$u_{za}=0$, $u_{zb}=0$, $u_{zc}=0$, $u_{wa} &lt; 0$</td>
<td>$\frac{2}{U_{dc}} (i_m U_N - i_a U_{wb} + i_c U_{wc} - 2U_{wa} u_{za})$</td>
</tr>
<tr>
<td>2 &amp; 3</td>
<td>$u_{za}=0$, $u_{zb}=0$, $u_{zc}=0$, $u_{wa} &gt; 0$</td>
<td>$\frac{2}{U_{dc}} (i_m U_N - i_a U_{wb} + i_c U_{wc} + 2U_{wa} u_{za})$</td>
</tr>
<tr>
<td>4 &amp; 5</td>
<td>$u_{za}=0$, $u_{zb}=0$, $u_{zc}=0$, $u_{wa} &lt; 0$</td>
<td>$\frac{2}{U_{dc}} (i_m U_N - i_a U_{wb} - i_c U_{wc} - 2U_{wa} u_{za})$</td>
</tr>
<tr>
<td>6 &amp; 7</td>
<td>$u_{za}=0$, $u_{zb}=0$, $u_{zc}=0$, $u_{wa} &gt; 0$</td>
<td>$\frac{2}{U_{dc}} (i_m U_N - i_a U_{wb} + i_c U_{wc} + 2U_{wa} u_{za})$</td>
</tr>
<tr>
<td>8 &amp; 9</td>
<td>$u_{za}=0$, $u_{zb}=0$, $u_{zc}=0$, $u_{wa} &lt; 0$</td>
<td>$\frac{2}{U_{dc}} (i_m U_N - i_a U_{wb} - i_c U_{wc} - 2U_{wa} u_{za})$</td>
</tr>
<tr>
<td>10 &amp; 11</td>
<td>$u_{za}=0$, $u_{zb}=0$, $u_{zc}=0$, $u_{wa} &gt; 0$</td>
<td>$\frac{2}{U_{dc}} (i_m U_N - i_a U_{wb} + i_c U_{wc} + 2U_{wa} u_{za})$</td>
</tr>
</tbody>
</table>

<p>| Table V. The relationships between $k$ and $i_m$, in different conditions. |</p>
<table>
<thead>
<tr>
<th>$k$</th>
<th>$u_{za}$</th>
<th>$\bar{i}_m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\geq 0$</td>
<td>$\geq 0$</td>
<td>$\bar{i}_m$</td>
</tr>
<tr>
<td>$&lt; 0$</td>
<td>$&lt; 0$</td>
<td>$\bar{i}_m$</td>
</tr>
</tbody>
</table>

Fig.9. Value of $u_{za}$ at different $m$ and different $\theta$ (normalized by $U_{dc}/2$)
According to above analysis, the average neutral point current \( i_n \) can be regulated by \( k \) as shown in Table V. It can be observed that \( i_n \) can be controlled to increase or decrease by setting different values of \( k \) according to the polarity of \( u_{j,i} \). Thus, the neutral point voltage can be controlled by \( k \) according to Table III and Table V.

### B. Proposed Neutral Point Voltage Balancing Method

According to the above analysis, the TCB-DPWM based neutral point voltage control method is shown in Fig.10. The capacitor voltage balancing is controlled by the regulation of \( k \). The value of \( k \) is calculated by the proposed control strategy according to three phase currents \( i_{a,b,c} \), reference voltage signals \( u_{a,b,c} \) and the DC capacitor voltages \( u_{a,b,c} \) and \( u_p \). The reference voltages \( u_{a,b,c} \) is used to obtaining the related phase \( j \) by looking up Table IV. Then, according to the polarity of \( u_{j,i} \) and the voltage difference \( \Delta U_c \), the value of \( k \) can be obtained by the logic judgment in Fig.10. Finally, drive signals are generated by the proposed TCB-DPWM according to the value of \( k \). Note that \( U_{dc} (U_{dc}>0) \) is the threshold value and can also be seen as the acceptable deviation of neutral point voltage.

In summary, the proposed strategy for controlling the neutral point voltage is shown as follows:

1) Case a: If \( \Delta U_c > U_{dc} \) and \( \text{sign}(u_{j,i})=1 \), \( k \) is set to -1, then, the average neutral point current \( i_n \) will increase, \( \Delta U_c \) will decrease.
2) Case b: If \( \Delta U_c > U_{dc} \) and \( \text{sign}(u_{j,i})=-1 \), \( k \) is set to 1, then, the average neutral point current \( i_n \) will increase, \( \Delta U_c \) will decrease.
3) Case c: If \( \Delta U_c < U_{dc} \) and \( \text{sign}(u_{j,i})=1 \), \( k \) is set to 1, then, the average neutral point current \( i_n \) will increase, \( \Delta U_c \) will increase.
4) Case d: If \( \Delta U_c < U_{dc} \) and \( \text{sign}(u_{j,i})=-1 \), \( k \) is set to -1, then, then, the average neutral point current \( i_n \) will decrease, \( \Delta U_c \) will increase.
5) Case e: If \( \Delta U_c \) and \( \text{sign}(u_{j,i}) \) are not the above four situations, the value of \( k \) will not be changed.
of DC capacitor \(i_{AC}\) and the frequency spectrum for \(u_{AC}\) (output phase voltage to neutral star point of load) are measured in both simulations and experiments. In addition, the modulation waveform \(u_{ma}\), the output phase current \(i_{ga}\) are measured in simulations and experiments, respectively.

The waveforms \(u_{ma}\) and \(i_{ga}\) show that phase A is clamped to the positive bus or neutral point or negative bus in different sectors (refer to Fig.3). The difference of DC capacitors \(\Delta U_c\) fluctuates at the frequency of three times of the fundamental frequency. However, the phases of \(\Delta U_c\) for different DPWMs are different. For example, the waveforms of \(\Delta U_c\) for DPWM II and DPWM III have almost 180° phase shift. That means that \(k=1\) and \(k=-1\) have opposite functions on neutral point voltage. This phenomenon means that the neutral point voltage can be controlled by \(k\). Meanwhile, these results verify the analysis of neutral point voltage in Section IV. The total harmonic distortions (THDs) of output phase voltage \(u_{AC}\) are from 38.37% to 39.37%. As we know, the maximum harmonic component for SVPWM is the twice switching frequency harmonic (360°). While for the proposed strategy, the biggest harmonic component is located at the switching frequency (180°). Since filter has higher harmonic attenuation at higher frequency, the THD of grid/load side current of inverter with proposed strategy will be bigger than that of SVPWM. After the LC filter, the output phase currents \(i_{ga}\) for each DPWM methods show a good sinusoidal output wave. Both the simulation and experimental results are consistent with the theoretical analysis.

C. Validation of the Proposed TCB-DPWM based Neutral Point Voltage Balancing Method

In order to validate the proposed TCB-DPWM based neutral point voltage balancing method, simulation results are given in Fig.13. The simulations are tested in inverter mode with RL load at the DC voltage of 600V. The value of DC capacitors \(C_p\) and \(C_N\) are 4100μF(820μF×5) and 3280μF (820μF×4) respectively. \(U_{dC}\) is set as 1.5V. Waveforms in the Fig.13 from up to down are: modulation wave \(u_{ma}\), proportional allocation factor \(k\), output voltage \(u_{AC}\), output phase current \(i_{ga}\), DC capacitor voltage \(U_N\) with a \(U_{dC}/2\) shift.

At the beginning of the simulations, standard SVPWM are used. Because of the different values of DC capacitor, the neutral point voltages are unbalanced. The proposed neutral point voltage control method starts to work at 0.1s. The
Table VII. Performance comparisons.

<table>
<thead>
<tr>
<th>Test conditions</th>
<th>Parameters</th>
<th>THD</th>
<th>SLF</th>
</tr>
</thead>
<tbody>
<tr>
<td>m = 0.8, ( \varphi = 0, \tau &lt; 0.1 )</td>
<td>m = 0.8, ( \varphi = 0, \tau &gt; 0.1 )</td>
<td>1.03%</td>
<td>1</td>
</tr>
<tr>
<td>m = 0.8, ( \varphi = 0, \tau &gt; 0.1 )</td>
<td>-</td>
<td>1.96%</td>
<td>0.66</td>
</tr>
<tr>
<td>m = 0.4, ( \varphi = 30, \tau &lt; 0.1 )</td>
<td>-</td>
<td>0.43%</td>
<td>1</td>
</tr>
<tr>
<td>m = 0.4, ( \varphi = 30, \tau &gt; 0.1 )</td>
<td>-</td>
<td>1.35%</td>
<td>0.71</td>
</tr>
</tbody>
</table>

Fig.13. Simulation results of the TCB-DPWM based neutral point voltage control.

neutral point voltage can be adjusted to balance in about two milliseconds. It can be seen from the result that the neutral point voltages are controlled very well and just fluctuates in a small range of -1.5~1.5V. The output voltage \( u_{AO} \) can be clamped to positive voltage or negative voltage at \( m = 0.8 \). The output voltage \( u_{AO} \) can be clamped to neutral point voltage at \( m = 0.4 \). Thus, the switching losses will be greatly reduced because of the great reduced number of power devices switching in the clamped phase.

In order to evaluate other performances of the TCB-DPWM, the performance comparisons in THD of output current and switching losses function (SLF) [33] are shown in Table VII. It shows that the switching losses are greatly reduced (more than 29%) with the proposed method. The cost to achieve this goal is the slightly harmonic distortion increase (less than 0.93%).

In order to validate the proposed TCB-DPWM based neutral point voltage balancing method, experimental results are shown in Fig.14 and Fig.15. Fig.14 is tested in the situation of \( m = 0.8, \varphi = 0 \). While, Fig.15 is tested in the situation of \( m = 0.4, \varphi = 30 \). The experimental results are tested in grid tied inverter mode at the DC voltage of 300V. DC capacitors \( C_p \) are consisted of 5 capacitors with a rated value of 820\( \mu \)F. DC capacitors \( C_o \) are consisted of 4 capacitors with a rated value of 820\( \mu \)F. \( U_{AO} \) is set as 0.5V. Waveforms in the experimental results from up to down are: output phase voltage to neutral point \( O \), voltage of DC bus capacitor \( U_N \), output current phase \( i_{AO} \).

As shown in Fig.14(a) and Fig.15(a), standard SVPWMs without neutral point voltage control are used at the beginning of the experiment. Because the voltages of the upper capacitor are bigger than the voltage of the lower capacitor, the voltages of DC capacitors are unbalanced. The output current is greatly distorted because of the unbalance neutral point voltage. When the proposed TCB-DPWM based neutral voltage balancing method starts working, the voltages of DC capacitors become balanced. When the neutral point voltages are balancing, the waveform of \( u_{AO} \) become better, at the same time, the distortion of output current becomes smaller. As shown in Fig.14(b) and Fig.15(b), the neutral point voltages keep balancing even when the output current reference step changes. The results show the proposed method are effective in neutral point voltage balancing.

In order to validate the proposed method in low switching frequency condition, Fig.16 shows the results at \( f_s = 2k \)Hz. As shown in Fig.16, standard SVPWMs without neutral point voltage control are used at the beginning of the experiment. The output current is greatly distorted because of the
unbalance neutral point voltage. When the proposed TCB-DPWM based neutral voltage balancing method starts working, the voltages of DC capacitors become balanced. When the neutral point voltages are balancing, the waveform of $u_{AO}$ becomes better. Meanwhile, the distortion of output current becomes smaller. Although the neutral point voltage fluctuations become higher than that in high switching frequency, the neutral point voltage is acceptable.

It is worth noting that the essence of the proposed neutral point voltage balancing method is allocating redundancy small vectors. The proposed method has the same limitation as for the method of allocating redundancy small vectors. This limitation on neutral point voltage balancing is discussed in many papers, for example Fig.9 in [30] and Fig.8 in [34]. The proposed method in this paper provides another way to realize the neutral point voltage balancing. For a given value of $k$, the computation time for the proposed TCB-DPWM strategy is $6.7 \mu s$ in a DSP with CPU frequency of 80MHz. The calculation of $k$ for the proposed neutral point voltage balancing method needs $8.8 \mu s$. While for the vector base PWM without neutral point voltage balancing, the...
Factor point of view in [15], the symmetric center distribution of redundancy small vectors can minimize the harmonic flux trajectories. Thus, SVPWM will have better performance in harmonic distortion than TCB-DPWM. Thus, the cost for neutral point voltage balance and efficiency improvement is the slightly harmonic distortion increase.

VI. CONCLUSION

This paper proposed a triangle carrier based discontinuous PWM for 3L-NPC inverters. Different types of DPWM can be obtained by setting proportional allocation factor $k$ into the proposed unified scheme of TCB-DPWM. The proposed method effectively simplified the implementations of convention SVPWM and TCB-DPWMs. The proposed TCB-DPWM was verified by simulation and experimental results. In addition, a neutral point voltage balancing method was investigated based on the proposed TCB-DPWM where the neutral point voltage was controlled by controlling the polarity of $k$. The proposed neutral point voltage balancing method was also verified by both simulation and experimental results. The results showed that the proposed neutral point voltage balancing method has good performance at neutral point voltage control and switching losses reduction. Furthermore, the proposed neutral point voltage balancing method is based on logic judgment and table lookup, so it is very convenient to be implemented in applications.

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Aalborg University, Aalborg, Denmark in 2012. He is presently working as a professor in the School of Electrical Engineering, Southeast University, China. His research interests include wind power generation, high-power conversion, power electronics, DC grids, high-voltage direct-current technology, and off-shore wind farm–power system dynamics.

Josep M. Guerrero (S’01-M’12-SM’14-FM’15) received the B.S. in Telecommunications Engineering, the M.S. in Electronics Engineering, and the Ph.D. in Power Electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000, and 2003, respectively. Since 2011, he has been a full professor with the Department of Energy Technology, Aalborg University, Denmark. His research interests is oriented toward different microgrid aspects, including power electronics, distributed energy storage systems, hierarchical and cooperative control, energy management systems, smart metering, and the Internet of things for AC/DC microgrid clusters and islanded minigrids. Recently, he particularly focuses on maritime microgrids for electrical ships, vessels, ferries, and seaports.

Juan Vasquez (M’12-SM’14) received the B.S. in Electronics Engineering from the Autonomous University of Manizales, Manizales, Colombia and the Ph.D. in Automatic Control, Robotics, and Computer Vision from the Technical University of Catalonia, Barcelona, Spain in 2004 and 2009, respectively. He is currently working as an associate professor with the Department of Energy Technology, Aalborg University, Denmark. His current research interests include operation, advanced hierarchical and cooperative control, optimization and energy management applied to distributed generation in AC/DC microgrids, maritime microgrids, advanced metering infrastructure, and the integration of the Internet of things and cyber-physical systems into smart grids.