Improving the Short-Circuit Reliability in IGBTs

How to Mitigate Oscillations

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Improving the Short-Circuit Reliability in IGBTs: How to Mitigate Oscillations

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Abstract—In this paper, the oscillation mechanism limiting the ruggedness of IGBTs is investigated through both circuit and device analysis. The work presented here is based on a time-domain approach for two different IGBT cell structures (i.e., trench-gate and planar), illustrating the 2-D effects during one oscillation cycle. It has been found that the gate capacitance varies according with the strength of the electric field near the emitter, which in turn leads to charge-storage effects associated with low carrier velocity. For the first time, it has been discovered that a parametric oscillation takes place during the short-circuit in IGBTs, whose time-varying element is the Miller capacitance, which is involved in the amplification mechanism. This hypothesis has been validated through simulations and its mitigation is possible by increasing the electric field at the emitter of the IGBT with the purpose of counteracting the Kirk Effect.

Index Terms—Insulated gate bipolar transistor, short circuit, gate oscillations, parametric oscillation, robustness, Kirk Effect, TCAD.

I. INTRODUCTION

The Insulated-Gate Bipolar Transistor (IGBT) has firmly established itself in high-voltage and high-current applications, handling power outputs ranging from a few kW to several MW in the power electronics industry [1]. Despite of its great success, many challenges are ahead to meet the future high-reliability targets, in response to the ever increasing demands for more renewable energy applications. For instance, it has been said that the IGBT is one of the critical components according to a survey based on field experiences from power electronics manufacturers [2]. To improve the IGBT reliability and guarantee e.g. 20 years operation, such as in the case of renewable energy systems [3], random failures as the ones occurring during short-circuit conditions cannot be neglected. One of the failures often observed in IGBTs is related to a ringing phenomenon occurring under short-circuit events. Examples of failures caused by oscillations can be found for a trench IGBT power module in [4] and for a trench IGBT chip in Fig. 1. As shown in Fig. 1, a 3.3-kV trench IGBT chip is tested under two DC-link voltages of 1,200 V and 1,500 V, showing low and high frequency oscillations. According to the literature [4], [5], high-frequency oscillations are the precursor or a sign of IGBT failure and this has also being confirmed through experiments (see the experimental result in Fig. 1 at 1,500 V DC-link voltage).

The oscillation mechanism has been studied over the years [6], [7] showing that, under adverse combinations of large circuit stray inductance under certain operating conditions, it is likely that IGBTs exhibit high-frequency oscillations. Several experimental evidence of such phenomenon can be found in [6], [8]–[11] and, recently, also for trench-gate, field-stop IGBTs [4], [5], [12], [13]. So far, two different approaches have been followed to cope with the oscillations: circuit analysis and device analysis. The first one is related to those theories claiming that the oscillations can be solved by optimizing the external circuit parameters, for instance, by increasing the gate resistance [14], minimizing the stray inductances [8], or proposing stability criteria to avoid the unstable regions [10]. On the other hand, different studies claim that the IGBT chip itself presents some kind of instability. However, different interpretations have been given: the presence of a negative capacitance under high temperatures and high collector voltages [6], the lack of optimization of the IGBT cell design [8] and the dynamic IMPact ionization Avalanche Transit Time (IMPATT) effect [9]. It is clear that
the above works provide an extensive experimental character-
ization of the ringing phenomenon, but there has not been
a conclusive theory to explain the root cause of such an
amplifying behaviour. But what is even more important is
that such oscillations still compromise today’s IGBT reliability
[15].

The purpose of this investigation is to understand the
complex behaviour of the IGBT with both circuit and device
analysis, as presented in [16], e.g. for the diode snappy
recovery. This approach is adopted in this work to find the
interaction between the capacitive behaviour of the IGBT and
the main circuit parameters. To that end, a trench-gate and a
planar-gate IGBT structures have been simulated under short
circuit in order to reproduce the gate-voltage oscillations. The
results reveal that the oscillation mechanism does not depend
on the cell structure type (i.e., planar or trench) but on the
IGBT inherent characteristics. IGBTs have pretty low n-base
doping and high-level carrier injection features, which favours
the Kirk effect occurrence.

This paper is organized as follows: Section II presents the
description of the considered IGBT structures. Section III and
IV demonstrate the oscillation phenomenon via experimental
tests and TCAD simulations, respectively. Section V proposes
the root cause of such oscillations along with a simulation
model. Section VI proposes a possible device solution by
adopting a modification in the IGBT design. Finally, conclud-
ing remarks are given.

II. DEVICE STRUCTURE

Fig. 2 shows the two IGBT cell designs adopted, whose
blocking capability is 3.3-kV: the Soft-Punch-Through (SPT)
IGBT with a planar cell (Fig. 2a), and the Soft-Punch-Through
(SPT) IGBT with a trench cell and additional carrier enhance-
ment at the emitter (Fig. 2b) [17]. The two IGBT cells are
based on the SPT concept having the same buffer design and
drift region thickness. On the other hand, the carrier profile
distribution of each device is slightly different. The planar
IGBT has been designed with a weaker anode (i.e., lower
anode injection efficiency) in contrast with the trench IGBT.
This, in turn, leads to a lower carrier concentration at the
collector, and therefore, smaller turn-off losses. On the other
hand, the trench IGBT cell enhances the carrier concentration
at the emitter side of the IGBT by introducing an n+ layer
surrounding the p-well layer [18]. As a result, the conduction
losses in the trench IGBT are smaller in comparison with
the planar IGBT. Moreover, a floating p+ layer has been
implemented in the region between adjacent active cells in the
trench device. In this way, the gate input capacitance can be
effectively reduced, while also providing an optimum blocking
capability [19].

In this work, a traditional planar IGBT without carrier en-
hancement technology and better anode engineering, and then
a state-of-the-art trench IGBT design with carrier enhancement
technology and reduced Miller capacitance are compared with
focus on the short-circuit oscillations. Both technologies are
used to verify the proposed interpretation.

III. EXPERIMENTAL RESULTS

This section presents the experimental results on the short-
circuit capability of both planar and trench Soft Punch
Through (SPT) IGBTs rated at 3.3-kV. The measurements have
been done on a single-chip IGBT soldered on an Alluminium
Nitride (AlN) substrate. A non-destructive short-circuit tester
consisting of a high voltage power supply with a maximum
voltage of 6.5 kV has been used, which is connected to a
bank of capacitors. Two IGBT sub-modules act as circuit
breaker and the busbar stray inductance can be modified with
different inductor values up to a maximum of 2 µH. A Personal
Computer (PC) serves as an interface between a 500 MS/s, 500
MHz LeCroy LT344 oscilloscope and the two gate driving
units for device under test and series protection. The platform
to program the short-circuit sequence and to analyse the data
is based on the Laboratory Virtual Instrument Engineering
Workbench, provided by the LabVIEW software [20].

![Fig. 2. The 3.3-kV planar IGBT (a) and the 3.3-kV enhanced-trench IGBT (b). The emitter side is only represented for showing the differences between the planar and trench gate structures.](image)

![Fig. 3. Short-circuit test of a Soft-Punch Through (SPT) 3.3-kV planar IGBT at different DC-link voltages of 1 kV (red) and 1.9 kV (blue) (T = 25°C, R_{g,on} = 2.2 Ω and L_{σ} = 580 nH.](image)
The driving factors for the occurrence of the short-circuit oscillations have been previously investigated by the authors in [4], [7], [12], [22] and by others in [21], through the variation of the operating conditions, such as DC-link voltage, gate-emitter voltage and temperature. Particularly in [4], it has been pointed out that the oscillation frequency increases with the applied DC-link voltage, meaning that the Miller capacitance is involved in the oscillation phenomenon. This interpretation is confirmed later in this article.

Similarly, the 3.3-kV trench IGBT has been tested with a low DC-link voltage of 700 V. Fig. 4 demonstrates that the trench IGBT device also shows oscillations with a frequency of 20 MHz. The situation is even more critical since the gate oscillation amplitude is larger in comparison with the experiments on the planar IGBT chip. Nevertheless, this oscillation has a zero damping characteristic, which means that the oscillation is sustained and the IGBT successfully passes the short-circuit condition. On the contrary, in Fig. 1, the failure of the IGBT is unavoidable since the oscillation grows without bound.

IV. TCAD SIMULATIONS DURING SHORT CIRCUIT

A. The turn-on process under a short circuit

Finite-element device simulations have been performed by means of Sentaurus TCAD simulator [23], in order to understand the physical behaviour of both planar and trench IGBTs during a short-circuit type 1 turn-on process. Simulations have been carried out including the external circuit of Fig. 5, whose values are taken from the experimental circuit but also favoring the occurrence of the oscillation phenomenon. The collector inductance has been selected to have a large value of 1.2 μH, which is realistic in case of motor drive and other applications because of long cables. The gate parameters have been measured within the same frequency range as the oscillations, however, the input impedance during short-circuit has not been measured, as presented in [11]. The main reason is because this paper is not intended to provide a stability map of the IGBT where a combination of parameters may move the IGBT into an unstable region. Instead, the root cause of oscillations will be explained from the device physics perspective, based on a time-domain approach. Additionally, the experimental results in Fig. 3 point out that the high-frequency oscillations are not observed at high DC-link voltages. To that end, a high DC-link voltage level of 2 kV is selected, with the purpose of firstly analyze a clean short-circuit turn-on process without oscillations.

Fig. 6a shows the simulated current and voltage waveforms of the planar IGBT during its turn-on process under a short-circuit type 1, while Fig. 6b indicates the electric field variation and electron carrier distribution associated to the time instants in Fig. 6a. The cuts have been done in the vertical direction through the maximum current density region of the IGBT. The simulations show that during short-circuit, the IGBT builds up a dense electron carrier density near the emitter, while the excess electron charge density in the collector of the IGBT is slightly smaller. The importance of this charge carrier distribution is reflected on the electric field shape whose peak gradually transfers from the emitter side to the collector side, which is commonly known as the Kirk effect. Basically, the amount of electrons prevails over the sum of holes and the background concentration, therefore, the effective charge $N_{eff}$ in the drift region becomes negative ($N_{eff} = N_D + h - e$).

Fig. 7a shows the simulated electrical waveforms of the trench IGBT during its turn-on process under a short-circuit condition, while Fig. 7b indicates the electric field variation and electron carrier distribution associated to the time instants in Fig. 7a. Once again, the electron carrier density near the emitter becomes pretty dense during the short-circuit condition. Therefore, the electric field peak located at the emitter...
oscillation characteristic for both planar and trench IGBT cells and 10% maximum variation is observed, respectively. The assumed that the collector current remains constant, as a 2% cause of such oscillations. 

particular importance in order to identify which parameters simulations for both planar and trench IGBT cells. This is of phenomenon can also be reproduced via mixed-mode device be observed. Figs. 8 and 9 demonstrate that the oscillation voltage has been applied, therefore, the oscillations can now difference from previous simulations is that a lower DC-link out with the set of parameters presented in Fig. 5. The main oscillations, mixed-mode device simulations have been carried physical mechanisms taking place during the short-circuit turn into a loss of control and consequent failure. To analyze drawback coming from the Kirk effect, i.e., the electric field a higher emitter efficiency shows the benefit of minimizing the planar IGBT. It is worth to note that the trench design having the rotated-field is not as pronounced as in the case for the across the IGBT increases. However, for the trench IGBT, gradually transfers to the collector, as the collector voltage increases. However, for the trench IGBT, the rotated-field is not as pronounced as in the case for the planar IGBT. It is worth to note that the trench design having the Kirk effect, i.e., the electric field variation associated with the highlighted time instants.

Fig. 6. Short-circuit characteristic of the SPT 3.3-kV planar IGBT: (a) the voltage and current waveforms and (b) the electron carrier distribution and electric field variation associated with the highlighted time instants.

B. Analysis of the Short Circuit Oscillations

The short-circuit capability of the IGBT has been demonstrated to be limited by high-frequency oscillations, which may turn into a loss of control and consequent failure. To analyze the physical mechanisms taking place during the short-circuit oscillations, mixed-mode device simulations have been carried out with the set of parameters presented in Fig. 5. The main difference from previous simulations is that a lower DC-link voltage has been applied, therefore, the oscillations can now be observed. Figs. 8 and 9 demonstrate that the oscillation phenomenon can also be reproduced via mixed-mode device simulations for both planar and trench IGBT cells. This is of particular importance in order to identify which parameters influence the short-circuit process and later justify the root cause of such oscillations.

From the experimental and simulation results, it can be assumed that the collector current remains constant, as a 2% and 10% maximum variation is observed, respectively. The oscillation characteristic for both planar and trench IGBT cells look very similar to each other. Therefore, a time-zoom of the oscillations from the planar IGBT (see Fig. 10) is enough to show the phase-shift relation between each electrical parameter (i.e., $V_{CE}$, $I_C$, $I_g$, and $V_{GE}$). In this graph, the gate current and instantaneous input capacitance are added with respect to Fig. 8 for a clearer understanding. In Fig. 10, it can be observed that the gate current $i_g$ is leading the gate voltage $V_{GE}$ by 90°, therefore, it can be assumed that the circuit is nearly capacitive. The instantaneous input capacitance is calculated from $i_g$ and $V_{GE}$ through the formula, $C_i = i_g \times dt/dV_{GE}$. During one

Fig. 7. Short-circuit characteristic of the SPT 3.3-kV trench IGBT: (a) the voltage and current waveforms and (b) the electron carrier distribution and electric field variation associated with the highlighted time instants.

Fig. 8. Short-circuit simulation of an SPT 3.3-kV planar IGBT at $V_{DC} = 1$ kV showing oscillations during the turn-on process.
oscillation cycle, it can be observed that the IGBT exhibits a large variation of the input capacitance, which comes from the distribution of the stored excess carriers inside the IGBT, as it will be explained later. To reach a firm conclusion, one oscillation cycle is divided into two phases (see Fig. 10): phase A (charge-storage phase) and phase B (voltage build-up phase); in this way a detailed description can be given for each phase.

1) Phase A: Charge-Storage Phase: During this phase, a carrier accumulation region appears at the surface of the IGBT coinciding with an increase of the input capacitance, about 10 times higher, as it is calculated in Fig. 10. The gate voltage $V_{GE}$ takes higher values than 15 V, which in turn causes the collector voltage $V_{CE}$ to drop in order to sustain the assumed constant collector current. The electron accumulation effect is observed as soon as $V_{CE}$ drops, which is associated with a decrease in the electric field function. In short-circuit conditions, the electric field has been found to be weaker at the emitter of the IGBT, therefore, the carriers move slower in this region. The observed charge-storage effect is in agreement with the assumption of constant collector current, $J_n = qnv_n$, implying that a lower electron velocity can only result in a higher electron density driving the IGBT into the Kirk Effect mode. This behaviour is confirmed in Figs. 11 and 13 for both planar and trench cells, where a low electric field at the emitter coincides with electron accumulation effects.

From the external circuit point of view, the gate current waveform in Fig. 10 indicates that two mechanisms take place: (i) a charge period (positive $i_g$): the gate capacitance has a
large value when the capacitor is charged up, so the energy initially stored in the gate inductance is now transferred to a larger gate capacitance. The $dV_{GE}/dt$ slows down because the capacitance is increased. Once the current reaches zero, the capacitance is charged beyond the gate driver voltage ($V_{GG} = 15V$ in Fig. 5) and it starts discharging, reversing the current through the inductance; (ii) a discharge period (negative $i_g$): the voltage across the large capacitance starts falling as the current through the gate inductance begins to rise. Therefore, the energy stored in the capacitor is now transferred to the inductance. During this transition, the gate capacitance changes its value from a high to a low value causing a larger $V_{GE}$ decrease.

2) Phase B: Voltage Build-Up Phase: During this phase, the electron accumulation region at the surface of the IGBT disappears coinciding with a smaller value of input capacitance. The excess carrier concentration near the emitter is swept out as soon as the collector voltage $V_{CE}$ rises for sustaining the collector current at a lower gate-emitter voltage. Because of higher $V_{CE}$, the electric field builds-up across the n-base of the IGBT, which in turn implies an increase in the electron velocity. A higher electron velocity is associated with a reduction in the electron density and thus the Kirk Effect is counteracted. As a consequence, the rotated electric field comes back to its well-known triangular shape. This is confirmed in Figs. 11 and 13 for both planar and trench devices. By looking at the gate current, the input capacitance charges and discharges during phase B, but now the capacitance has a small value. It is also worth to look energy-wise at the proposed mechanism. In particular, the time instant when an energy increment occurs is when the surface is flooded with carriers because of Kirk effect. At that time, the collector current leaks some charge at high voltage. Such a charge is returned back to the main collector flow at low voltage, ending up in a net energy transfer from the power loop circuit (DC) to the oscillation (AC).

In summary, the evolution of the IGBT during the short-circuit oscillations varies between two situations which are represented in Fig. 15: (a) a rotated-field associated with electron accumulation effects (i.e., high capacitance) at the
emitter of the IGBT, due to low carrier velocities at low $V_{CE}$. This is observed during phase A in Figs. 12 and 14 for planar and trench cells, and (b) a non-rotated field associated with holes prevailing over electrons moving at their saturated values (i.e., low capacitance) due to high $V_{CE}$. This is observed during phase B in Figs. 12 and 14 for both planar and trench cells. As a consequence of this mechanism, the IGBT presents a time-varying gate capacitance change according to the electric field shape and position of the excess carriers. This is in fact the basis of a parametric oscillation, where the capacitor behaves as an active element. This concept is elaborated in the following.

V. PARAMETRIC OSCILLATIONS IN IGBTS

The results from the mixed-mode simulations have demonstrated that during the oscillations, the instantaneous input capacitance behaves as a time-varying element. The fluctuation of the non-linear Miller capacitance together with the series connected gate resonance circuit gives rise to an energy transfer between the IGBTs input capacitance and the gate inductance $L_g$. The amplification behaviour arises from the capacitance variation in time. Even if the IGBT acts as an amplifier at the oscillation frequency of 20 MHz [11], the observed oscillations are not caused by the IGBT’s gain, as proved later by simulations. This type of amplification has been studied in other fields, and it is commonly recognized as a parametric oscillation; similar to the operating principle of a varactor parametric oscillator, whose non-linear variable capacitor element is used to amplify [24].

The non-linear equations describing the IGBT model together with the external circuit take a complex form. On the other hand, the interpretation of such an amplifying phenomenon is more obvious through simulations. To validate the proposed hypothesis, a PSpice simulation has been built in order to justify how oscillations can diverge or being self-sustained with time. Fig. 16 shows the schematic circuit representing the gate circuit loop consisting of resistive/inductive elements connected in series with two capacitors that are switched alternatively to obtain different effective capacitances. One fixed capacitor represents the small value ($C_2$), and a switched one, mimics the capacitance increase, in case of charge accumulation ($C_1 \to C_2$). The voltage across the two capacitances is ensured to be the same with the regulated voltage supply ($V(A) = V(A')$). The gate inductance value has been selected in agreement with the value from the TCAD simulation (i.e., 40 nH), a small resistor is included to simulate circuit losses and the values of the two capacitances have been selected one 50% larger than the other. The value of the gate resistance plays an important role to dampen the oscillations, but it should be large enough to dissipate the energy increase that it is being transferred back and forth between $L_g$ and C. The collector inductance $L_C$ is excluded in this simulation because the collector current $I_C$ remains practically unchanged. However, $L_C$ affects the IGBT short-circuit process in three ways [22]: (1) with higher collector inductance $L_C$, an increased undershoot across the collector-emitter voltage is observed (this effect is disadvantageous since the electric field becomes weaker and thus the charge accumulates at the surface of the IGBT); (2) the oscillation frequency increases with decreasing $L_C$ and (3) the oscillation amplitude remains constant, meaning that $L_C$ variations do not contribute to the amplification.

The time instants at which the capacitors need to be changed are very crucial to have an amplification or attenuation of the signal. The graph in Fig. 17, representing the current and voltage waveforms of an LC circuit showing the time instants at which the capacitors need to be changed: $C_{big} = C_1 + C_2$ and $C_{small} = C_2$.

![Fig. 16. PSpice simulation circuit using one fixed capacitance ($C_2$) and a switched one ($C_1 + C_2$) mimicking the capacitance increase to model the amplification behaviour observed in IGBTs during short circuit: S - switch.](image)

![Fig. 17. Current and voltage waveforms of a typical LC circuit showing the time instants at which the capacitors need to be changed: $C_{big} = C_1 + C_2$ and $C_{small} = C_2$.](image)
capacitance is switched to a small value (i.e., time instants 2 and 4), the voltage signal will be amplified because the same energy has to be stored in a smaller capacitance.

With the aim of reproducing the same capacitance variation, as the one observed with the device simulations in Fig. 10, the small and large capacitance values are selected at the time instants 2 and 3, respectively. The use of a variable capacitance that reacts non-linearly with the mentioned time sequence is highly effective, as it is shown in Fig. 18. The current \( i \) and the voltage \( V_A \) are shown, as well as the function \( S \) that represents the switching between the low and high capacitance values, where the higher value of \( S \) corresponds with the large capacitance (i.e., \( C_1 + C_2 \)).

In sum, in the TCAD simulations, the capacitance varies as a result of the electric field variation and charge profile distribution; in the PSpice simulation the capacitance variation is controlled with a voltage supply, i.e., switch \( S \) in Fig. 18. The transition from low to high capacitance is done when the energy is being transferred from the capacitance to the inductance. This, in turn, causes the \( dV_A/dt \) to slow down because the capacitance increases; this is in agreement with the results from the TCAD simulation. On the other hand, the transition from high to low capacitance is done when the energy is transferred back to the capacitance, thus the voltage \( V_A \) increases its amplitude because a higher energy has to be stored in a smaller capacitance.

VI. PERSPECTIVE SOLUTION: SURFACE BUFFER LAYER

The primary cause for the electron carrier accumulation at the emitter of the IGBT is the weak electric field in this region, as a consequence of the Kirk effect. The carrier distribution can be adjusted by inserting an n-doped buffer layer at the surface of the IGBT. In this way, the background doping concentration at the emitter is increased, counteracting the negative effective charge. The surface buffer layer has been effectively employed in the 3.3-kV planar IGBT. Fig. 19 shows a comparison between the standard planar IGBT and the proposed one through a short-circuit simulation carried out at the same conditions and with the same stray elements. It is demonstrated that the oscillation phenomenon has been eliminated with the additional surface n-layer. However, when the n-layer is employed, the blocking capability of the IGBT is reduced. Therefore, the n-layer doping concentration must be optimized to achieve the desired carrier distribution near the emitter without substantially reducing the breakdown voltage of the IGBT.

Fig. 20 shows a cut along the vertical direction, just before the oscillations are observed for the standard IGBT at \( t = 3\mu s \) (see Fig. 19). The graph compares the simulated electric field and electron carrier concentration for both standard and proposed IGBTs. A higher electric field is built up at the pn-junction on the emitter side reducing the carrier density. The most important aspect is that the electric field does not strongly depend on the injected carriers and therefore it does not vary with increasing short-circuit time (i.e., the capacitance becomes fixed).
VII. CONCLUSIONS

A detailed study of the short-circuit behavior in IGBTs points out that a parametric oscillation takes place in the IGBT. The analysis has demonstrated that the electric field peak across the n-base is continuously changing from the emitter to the collector side coinciding with a high capacitance value when the electric field peak is located at the collector and with a low capacitance value when the electric field peaks at the emitter. The increase of gate capacitance has been correlated with charge-storage effects occurring at the surface of the IGBT at relatively low collector voltages. This hypothesis is coherent with experimental observations at higher voltages, where oscillations are not further observed. The amplification mechanism has been modeled in PSpice with the help of two capacitors (one higher than the other), which are switched alternatively together with an RLC resonant circuit, showing the typical behavior of parametric oscillators. Finally, a mitigation proposal by inserting an n-doped layer at the surface of the IGBT is given. The adoption of an n-doped surface-buffer layer has proven to be effective in IGBTs for bringing about the desired increase in the electric field at the emitter, which prevents Miller capacitance variations.

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REFERENCES

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Chiara Corvasce received her M.S. Degree in Physics from the University of Bari, Italy in 1994. In 1995 she joined the Memory Product Group of STMicroelectronics in Catania, working on non-volatile memory devices and leading the team for the development of a ferroelectric memory. In 2002 she has moved to the Integrated Systems Laboratory (IIS) of the ETH Zurich where she received the PhD in Electrical Engineering focusing on high temperature characterization and modeling of semiconductor devices. She joined the BiMOS R&D Department of ABB Semiconductors in 2006 where she has been leading numerous IGBT and diode development projects before she took over the management of the R&D chip development group in 2013. Her main research interest is design and applications of high power semiconductor devices.

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