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RELIABILITY OF METAL FILMS AND INTERFACES IN POWER ELECTRONIC DEVICES

BY
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DENMARK

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- ***M. Brincker**, K. Pedersen, and E. Skovsen, "Tunable local excitation of surface plasmon polaritons by sum-frequency generation in ZnO nanowires," *Opt. Commun.*, vol. 356, pp. 109–112, 2015.
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- ***M. Brincker**, P. Karlsen, E. Skovsen, and T. Søndergaard, "Microstructured gradient-index lenses for THz photoconductive antennas," *AIP Adv.*, vol. 6, no. 2, pp. 25015, 2016.

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ENGLISH SUMMARY

Nowadays, a large part of energy is either directly produced or consumed as electricity. Production and conversion of electricity requires power electronics. Power electronics is also used in such branches as the aerospace, railway and automotive industries. This widespread use of power devices causes high demands to robustness and reliability, as well as to lifetime estimations under very different loading cases. This can only be efficiently and precisely achieved if one has a good understanding of failure modes and degradation mechanisms involved. To complete this picture, the physics of failure approach plays very important role. It has become a widely used methodology in recent years. The study presented in this work deals with gaining this type of knowledge with focus on the physical mechanisms leading to structural and compositional changes in metal films which are used in packaging with a final goal to improve the reliability of power modules. Passive thermal and active power cycling tests are applied to accelerate the effects leading to failure. The change of electrical properties as well as structure and composition are investigated by four-point probing, micro-sectioning, optical and electron microscopy, electron backscatter diffraction, energy dispersive X-ray spectroscopy, etc. By comparing the electrical and microstructural evolution of the Al layers subjected to passive and active cycling, the main degradation factor, which is thermo-mechanical stress, is identified while other possible stressors, for example, related to electrical effects are found to play little to no role. The accelerated tests run under different atmospheric conditions suggest that the metallization layers can increase strength under thermal cycling in ambient atmosphere due to oxidation of Al surfaces constraining the dislocations movement. It is also found that the texture of the polycrystalline Al layer plays a very important role in the structural evolution under repeated compressive and tensile stresses in the films originated by thermal cycling. For the first time, it is found that the metal film texture undergoes evolution from initial (111) orientation towards (311) but not (211). The models explaining this effect are suggested. Second part of the work is devoted to the fabrication and reliability study of transient liquid phase (TLP) bonded joints. A recipe for fabrication of strong Cu-Sn-Cu bonds with superior thermal capabilities as an alternative to traditional soldering is developed. For the specific application, a novel Cu-Mo hybrid baseplate technology involving Cu-Sn-Ag-Mo TLP bonds is suggested demonstrating good structural and compositional homogeneity yielding high shear strength. Generally, the studies on TLP bonding show that this technology has very promising potential to increase reliability of power modules. However, more studies are needed to fully develop the technologies. Summarizing, the studies represent several significant contributions into the physical understanding of the restructuring mechanisms governing degradation of metal film properties as well as into the development of novel hybrid metal interfaces with superior characteristics. Both topics are of considerable importance to improve reliability of power device packaging.

DANSK RESUME

I dag bliver en stor del af vores energi enten direkte produceret eller anvendt i form af elektricitet. Produktionen og konverteringen af elektriciteten kræver effektelektronik, som også anvendes også inden for brancher som rumfart-, tog- og bilindustrien. Den omfattende brug af denne elektronik stiller store krav til både robusthed og pålidelighed, ligesom det er vigtigt at kunne estimere levetiden under meget forskellige forhold. Det kan kun opnås med en vis præcision og effektivitet, hvis man har en god forståelse af alle de fejlmekanismer og nedbrydningsmekanismer, som er involveret. I forbindelse med den forståelse spiller "physics of failure" tilgangen en meget vigtigt rolle. Den er blevet en meget anvendt metode i nyere tid. Arbejdet, der præsenteres i dette værk, beskæftiger sig med at opnå denne type viden med særligt fokus på de fysiske mekanismer, som giver anledning til strukturelle og kompositionelle ændringer i de metalliske film, man anvender i effektmoduler, med henblik på at forbedre deres pålidelighed. Passive og aktive accelererede termiske test bliver anvendt til at fremskynde de effekter, som leder til fejl. Ændringer i de elektriske og strukturelle egenskaber af prøverne er undersøgt ved hjælp af fire-punkts modstandsmålinger, mikro-sektionering, optisk og elektron mikroskopi, tilbagekastet elektron diffraktion, energidispersiv røntgen spektroskopi, osv. Ved at sammenligne den elektriske og mikrostrukturelle udvikling af aluminiumslagene, når de udsættes for henholdsvis passive - og aktive termiske tests, identificeres hovedfaktoren for nedbrydning – termomekanisk stress - mens andre mulige stressorer såsom elektriske viser sig kun at have lille eller ingen betydning. De accelererede test, som er foretaget under forskellige atmosfæriske forhold viser, at metaliseringslagene kan styrkes i den omgivende atmosfære på grund af oxidering af aluminiumsoverfladen, da denne kan virke begrænsende på dislokationsbevægelsen i metalfilmen. Derudover har det også vist sig, at teksturen af det polykrystallinske aluminiumslag har en stor betydning i den strukturelle udvikling under de termiske test. For første gang har det vist sig, at teksturen på af en aluminiumsfilm gennemgår en udvikling fra en (111) retning mod (311) og ikke (211). Modeller, som kan forklare disse effekter, er fremstillet i værket. Anden del omhandler fabrikationen og pålideligheden af "transient liquid phase" (TLP) sammenføjninger. Her er udviklet en opskrift til at fremstille stærke Cu-Sn-Cu sammenføjninger med bedre termiske egenskaber, som et alternativ til traditionelle lodninger. En simpel Cu-Mo hybrid metalkølepladeteknologi, som indeholder Cu-Sn-Ag-Mo TLP bindinger viser god strukturel og kompositionel homogenitet og høj forskydningsstyrke. Generelt viser studierne omhandlende TLP bindinger, at denne teknologi har stort potentiale til at styrke pålideligheden af effektmoduler, men det er selvfølgelig nødvendigt med flere studier til at udvikle teknologien til fulde. Opsummerende kan man sige, at studierne repræsenterer adskillige signifikante bidrag til dels den fysiske forståelse af de mekanismer, som giver anledning til strukturelle ændringer af metalfilm, men også til TLP teknologien, som kan bruges i hybrid metalkøleplader. Begge dele har stor betydning i forhold til at højne pålideligheden af effektelektronik.

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CONTENTS

CHAPTER 1. INTRODUCTION

Nowadays, a large part of the energy is either produced as electricity or converted into electricity. This tendency is stimulated by easy use and storage of electrical energy as well as by the massive production of devices and development of new technologies increasing the need for electrical energy. At the same time, due to the limited resources of the planet and the environmental pollution, the energy production moves away from the use of fossil fuels towards more sustainable energy sources such as wind- and solar power. A key component in the power generation, distribution and consumption of electrical energy is power electronics. More than 70% of electricity is processed through power electronics of different kinds, and therefore the reliability and efficiency of these devices are of great importance [1]. Reliability is defined to be the ability of a system to perform its function under a given load for specified period of time [2]. In the present work, focus is placed on the reliability of power modules, which are a key element in converter and inverter systems used to process the power generated in, for example, solar farms and wind mills, and are also used in motor drive applications in the automotive industry. Many types of different fatigue driven wear-out failures can occur in a power module such as bond wire lift-off, solder fatigue, thin film fatigue etc. [3]. Also, other failure types typically referred to as burnout or catastrophic failures, which are more related to the robustness of the power devices, can occur such as e.g. short circuits events [4].

To meet the increased demands of cost-effectiveness and reliability of the systems and components, the industry and research field are moving away from the standard empirical models and testing methods towards a Physics-of-Failure (PoF) based approach [5]–[7]. However, to apply the PoF approach a deep understanding of the physical nature of the degradation mechanisms and resulting failures is needed. A key to gain this knowledge is to reduce the complex power systems to smaller parts, sometimes even components, where main stressors more easily can be identified and physical degradation models can be obtained. The studies presented in the current work are focused on gaining this knowledge in regards to power modules – specifically by studying degradation phenomena that are related to thin metal films and interfaces of these devices. Thus, the presented work will deal with these reliability issues and examine the root physical causes of the degradation and ultimate failure of the power electronic devices. This research provides a key information for the development of physics based tools for better lifetime estimation.

The thesis is an extended summary based on scientific papers that have been published or submitted during a PhD study, which was running from 1/12-2014 to 4/01-2018 at the Physics section of the Department of Materials and Production (Department of Physics and Nanotechnology before 1/04-2017) at Aalborg University. Chapter 2 presents the state-of-the-art in the field of wear-out failures in power modules with a special emphasis on metallization degradation. Chapter 3 deals with theoretical models describing dislocation based plasticity and texture evolution in thin metal

films. Chapter 4 presents the sample preparation and characterization methods which are employed during the experimental work. Chapter 5 summarizes the scientific results obtained in the experiments on metallization degradation, while Chapter 6 presents the results about the use of transient liquid phase bonding as a novel joining technique in power modules. In Chapter 7 the main conclusions of the work are presented. The papers relevant for the thesis can be found as appendices in “Reprints of publications”.

CHAPTER 2. POWER MODULE FAILURES AND RELIABILITY

Power modules are the main switching devices in power electronic systems. They handle power, as the name implies, in a variety of ways, such as e.g. in motor drive applications, AC-DC conversion, boost/buck converters and pulse width modulated (PWM) chopper systems. Depending on the above-mentioned applications, their electrical topology can differ but they are typically configured in either a full- or half-bridge configuration. They can also be represented as simple switches in PWM applications. Today, the driving factors for research and development are decreasing the size while improving the efficiency of the power devices. The ability to do this depends on the main characteristics of power modules, namely, maximum blocking voltage, current handling capabilities and related heat dissipation. The type of semiconductor device that currently best meets these demands is an insulated-gate bipolar transistor (IGBT). An IGBT can essentially be thought of as a combination of a bipolar transistor and a metal-oxide-semiconductor field-effect transistor (MOSFET) in a way that it inherits the high current handling capabilities of a bipolar transistor and the good gate control as well as the fast switching speed of a MOSFET [8]. To handle the large currents and fulfill high demands on heat dissipation, several IGBT chips are typically put in parallel with diodes and packaged into a module. The form-factors of modules can be different depending on the application but for high power cases they typically resemble some of those shown in **Figure 1.** All these power devices operate at voltages up to 1700 V, however they are designed for different current levels. The largest one at the top can typically handle currents up 1400 A, the medium size black module in the center can handle currents up to 600 A, while the smallest white module can operate at currents up to 300 A. More form-factors exist on the market but the power modules for **Figure 1** are chosen because they have similar form-factor to those studied in this thesis.

2.1. DESIGN AND PACKAGING OF POWER MODULES

The goal of the power module packaging is to enable electrical contact to other electronics, while providing the necessary mechanical support, thermal dissipation by means of active cooling and protection against external factors (humidity, radiation, dust, chemicals etc.) which can lead to damage and malfunction. A schematic picture of the traditional structure of high power module section is shown in **Figure 2**. It can be seen that the design represents a multilayer system with numerous interfaces between different materials. From the top, the die (IGBT or diode) is soldered onto a direct-bonded-copper (DBC) substrate, which then again is soldered onto a Cu baseplate. As shown, the topside of the semiconductor dies is connected electrically to the Cu tracks of the DBC or terminals by bond wires, typically made of Al. This system along with some type of enclosure and external electrical connections constitute a power module depicted in **Figure 1**. However, when the power device is

put into application it needs a good thermal connection to dissipate the heat generated in the semiconductor devices. This is typically realized by mechanical fixation onto a heatsink with some thermal interface material (TIM) that enables effective heat transfer. The materials constituting the multilayer structure have different thermal and mechanical properties and the most common materials are listed in **Table 1**.

Figure 1. Images of three power modules with different form-factors, sizes, and current handling capabilities.

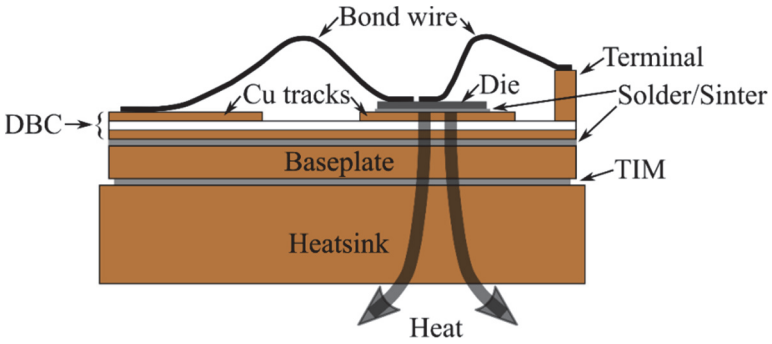

Figure 2. Schematic cross-section drawing of a power module section.

2.1.1. DBC SUBSTRATES AND BASEPLATES

The main function of the DBC substrate is to provide electrical isolation from the baseplate, while maintaining a high thermal conductivity, such that the heat can dissipate away from the semiconductor dies into the cooling system through the heatsink. DBCs are typically composed of a Cu-ceramic-Cu sandwich structure,

where the ceramic is typically either AlN or Al_2O_3 depending on the application and price range of the module. As can be seen in **Table 1,** AlN has superior thermal properties, while Al_2O_3 has a coefficient of thermal expansion (CTE) closer to that of Cu, thus reducing the thermal-induced mechanical stress in the DBC substrate. AlN is also a more expensive material and is, therefore, typically used in more demanding applications. Cu is widely used as the only material in baseplates due to low price and excellent heat transfer capabilities as well as the relative similarity of CTE to that of a Cu-based DBC substrate. Due to this difference of CTE between the baseplate and DBC, a pre-bending of the baseplate is necessary and some residual stress in the solder layer is developed which will keep accumulating under the device operation conditions (heating/cooling) finally leading to solder fatigue during power cycling.

Table 1. Relevant physical parameters of different materials which are parts of a typical packaging of power modules [8].

Material	**Thermal expansion (α)** $[10^{-6}/K]$	**Thermal conductivity (k)** $[W/(m \cdot K)]$
Al	23	237
Si	2.6	140
Cu	17	400
Al_2O_3	8.2	30
AlN	4.5	285
Sn	22	67
Ag	19	429

2.1.2. SOLDER, SINTER, AND TLPB LAYERS

Solder, sinter, and transient liquid phase bonded (TLPB) layers are used as interconnects between the semiconductor chips and the Cu tracks on the topside of the DBC and also between the DBC substrates and the baseplate of the power module. Solder layers have been used for many years in industry but the utilized materials are typically soft, which means that they are prone to creep and they also have relatively low thermal conductivity (see **Table 1**). Typically, a Sn-Ag (with ratio of 96.5/3.5)

eutectic is used in process known as reform soldering. Solder preforms are placed in between the interfaces that are to be connected and the stack is thermally treated in an oven with an inert gas mixture to prevent any unwanted oxidation of the interfaces. The temperature is increased until the solder preforms melt and join the layers.

Silver sintering is a newer technique that can produce a much stiffer interface layer with superior mechanical and thermal properties compared to solder layers [9]. This is also evident from **Table 1** where it can be seen that the physical parameters of Ag lie very close to that of Cu, thus reducing the thermal stresses while maintaining a very high thermal conductivity. Similar to soldering, a silver paste is placed between the layers that are to be joined together but with the temperature increase a large pressure is applied. The material is more expensive and the technological process is more complex, therefore, silver sintering is mainly used for some demanding applications.

TLPB joints are not yet used in any commercial power devices. But this new approach is currently under intensive investigation both in industry and academia [10], [11]. The TLPB technique can be seen as a cheaper alternative method to silver sintering that could produce joints with similar capabilities in regards to high temperature operation and high reliability. These issues will be addressed in more detail in Chapter 6.

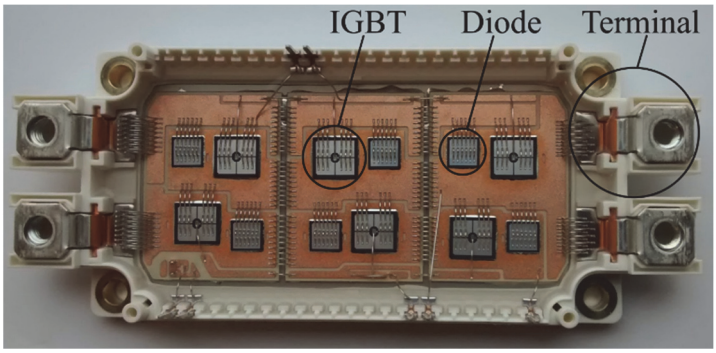

Figure 3. Top view of a 300 A power module in half-bridge configuration with three parallel sections.

2.1.3. BOND WIRES AND METALLIZATION

Semiconductor dies with IGBTs or diodes are covered by a metallization as this layer provides electrical contact to the devices of the chip. The most widely used material is Al. Thickness of the metallization varies on the scale of a few micrometers. Heavy Al wires are used to provide electrical connections between the topside of the semiconductor dies (metallization layers) and the Cu tracks of the DBC. They are bonded onto the Cu tracks, and the topside Al metallization of the semiconductor dies

via a low temperature ultrasonic procedure known as wire bonding [12]. As can be seen in **Figure 3** a number of parallel wires are used on each semiconductor chip to allow for a large current flow and to minimize joule heating in individual wires. In smaller power modules, as the one shown at the bottom in **Figure 3**, bond wires can also be used as connections to the lead terminals. Al in bond wires and metallization layers has a polycrystalline structure and typically contain small admixtures of Si and/or Cu.

2.2. FAILURES IN POWER MODULES

As can be seen in **Figure 2** and **Table 1** the multilayer stack of a power module consists of many different materials with different thermal and thermo-mechanical properties. As heat is generated in the semiconductor chips a temperature gradient is formed across the layers in the stack. This creates thermal stresses due to the difference in CTE of the materials. The stresses can lead to creep or fatigue failures due to the cyclical nature of device operation in many applications and can also lead to burnout failures such as e.g. short circuit events [3]. It is common for many of the wear-out failures that the minor degradations have tendency to accumulate, thus, accelerating the development of major failures. In the following sections, the most common fatigue and wear out failures are presented.

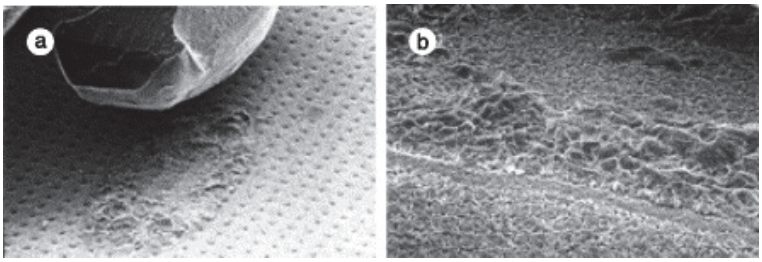

Figure 4. (a) Bond wire lift-off (SEM image, 40×). (b) Close view of the footprint edge of the bond after lift-off (SEM image, 100×). Reprinted from [3] with permission.

2.2.1. BOND WIRE FATIGUE

Bond wire related failures are the major failure mechanisms in power modules and are often the bottleneck for reliability [3], [13]–[15]. As a power module is in use, the CTE mismatch between the underlying stack of layers (metallization, Si die, solder etc.) and the bond wires cause thermal stress that results in the accumulation of plastic damage in the bond wire and especially at the wire interface with the topside metallization of the semiconductor chip. The stress development at the bond interface can eventually cause physical disconnection of a wire (lift-off) and break of electrical contact, which acts as feedback mechanism increasing the current load on the remaining wires. Rise of the current increases thermal stresses, thus, causing a quicker failure of the next wire and so on until the module loses electrical connection entirely

or fails catastrophically [16]. There is one more mechanism, which is also originated by CTE mismatch but between the entire wire and underlying stack of layers leading to wire flexure that originates heal cracking also contributing into lift-off [17].

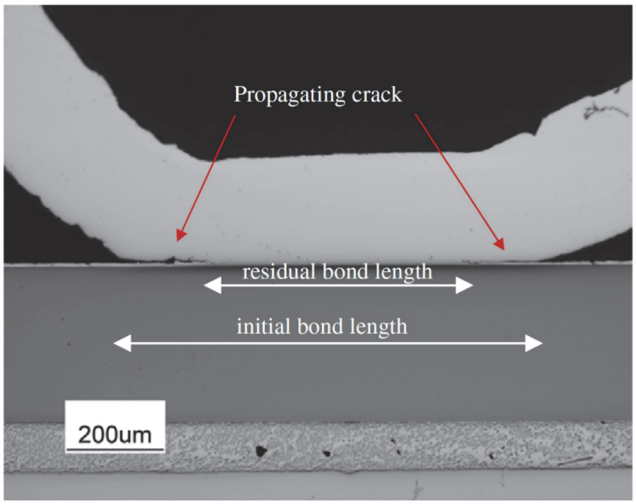

Figure 5. Crack propagation at Al wire bond during thermal cycling. Optical micrograph provides initial and residual bond length measurements. Reprinted from [18] with permission.

Bond wire fatigue has been the topic of many studies, covering the subject by active power cycling [13], [14], [19]–[28], thermal cycling [18], [29] and isothermal mechanical testing [29]–[32]. The cracks that cause the bond wire lift-off start propagating at the toe and heel of the wire bonds where the shear stresses are the highest, which have been shown experimentally [15], [18], [21]–[24], [27]–[29], [33], [34] and predicted by finite element modelling [27], [35], [36]. **Figure 4**(a) depicts SEM image of bond wire lift-off. In **Figure 4**(b) it can be seen that the cracks are developed not exactly at the interface between the wire and metallization layer but propagate through the bond wire since remnants of the wire material are present on the metallization surface. It is found that cracks typically develop through so-called refinement area of the wire which is formed under the ultrasonic bonding [21], [37]. This crack propagation is illustrated in **Figure 5**, leading to decrease of the bond length.

Using the comprehensive power cycling data and results of physical characterization of wire bond fatigue, both empirical/statistical [19], [20] and finite element based [27], [35], [36] lifetime models have been developed. Generally, wire bond fatigue in power modules can be considered as well understood and covered extensively by the literature. There are also reliable models that can provide good lifetime estimations for wire bonds.

2.2.2. METALLIZATION DEGRADATION

Degradation of topside metallization of power chips is one of the least well understood failure mechanisms in power modules and, therefore, will be one of the main focuses of the work presented in this thesis. As the CTEs of the Al metallization and the underlying Si are different, the metallization is subjected to cyclical thermo-mechanical stress during device operation or cycling in accelerated tests. These stresses can reach high values and cause plastic deformation to accumulate in the metallization in the form of micrograin reconstruction, cracks, void development, and severe surface roughening. A stress-temperature plot for an Al film on a Si substrate is shown in **Figure 6**, where the aforementioned stress development due to CTE mismatch is evident. It can be seen that the film is in tension at room temperature and it deforms elastically until the temperature reaches around 200 ºC. At this temperature the yield point is reached and plastic deformation starts. Close to this temperature, the stress undergoes a transition from tensile to compressive, which can be identified as the point where the stress-temperature curve crosses the zero line of the biaxial stress.

Further, due to the polycrystalline structure and specific crystallographic texture of Al films, the crystallographic orientation of the grains can change through a complex interaction and processes requiring minimization of the involved energies. This can either accelerate or slow down the degradation process in the layer as will be discussed in section 2.2.2.3.

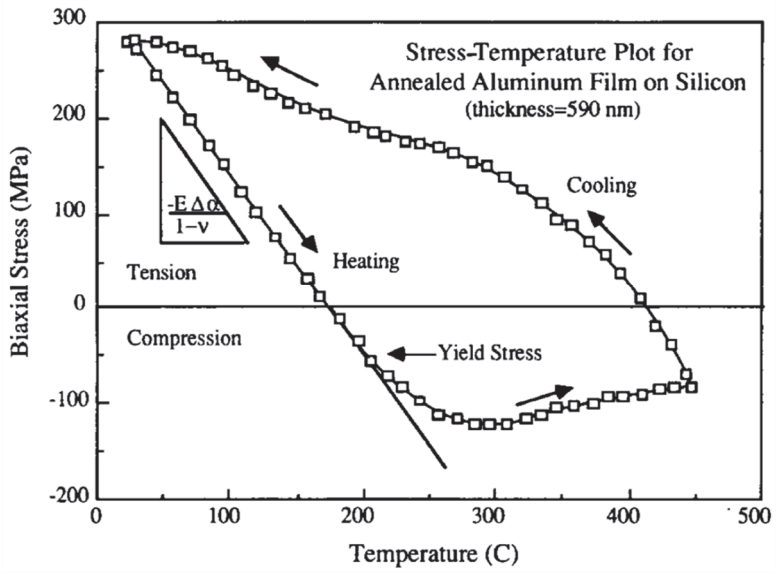

Figure 6. Stress-temperature plot for an Al film on a Si substrate. Elastic and plastic deformation occur in the film during heating and cooling. Reprinted from [38] with permission.

2.2.2.1 Topographical and microstructural evolution

The studies on topographical and microstructural changes of Al metallization of power electronic chips during accelerated test and thermal ageing have been presented in numerous studies [3], [13], [22]–[26], [38]–[73]. It should be noted that the Al layers on IGBTs, diodes and MOSFET chips are very similar in structure with only difference in thickness. The layer thickness for MOSFETs is typically 10 µm – 20 µm while for IGBTs and diodes - 3 µm – 7 µm. Therefore, one can expect that the degradation mechanisms and resulting reconstruction should be similar, thus, allowing for comparing and using data from all these devices to develop a degradation model. In [22], [23] the metallization degradation of both diodes and IGBTs is studied for half-bridge high power modules subjected to sinusoidal current load conditions with active switching of the IGBTs at 2.5 kHz. Due to the power cycling configuration, which mainly stresses the diodes, no degradation of the IGBT metallization is observed, however a clear restructuring of the diode metallization is found. A series of images for the topside metallization for diodes at different degradation stages is shown in **Figure 7**, where it is clear that the surface changes significantly as the power cycling is progressed. The nomenclature of the diodes in the figure caption refers to the stage of power cycling and to which section the diodes belong. For example, notation $C_{50\%}$ means that the diode comes from section C and it has been power cycled to 50% of the estimated lifetime. It is also observed that the surface roughening is the most severe in the center of the diodes, while the edges are less affected, which is explained by the temperature distribution across the chip. The simulations show that the highest temperature is reached in the center. The thermo-mechanical stress is, thus, proposed to be the major stressor, while it is speculated that electric phenomena such as electromigration might also have some influence.

Other studies using power cycling tests show surface roughening in the metallization layer of IGBT chips [24], [26] up to cavity formation [25]. Severe roughening of the metallization and burn marks in the source field for power MOSFET exposed to repetitive unclamped inductive switching with a $\Delta T = 160$ °C has been reported [40]. Also, repetitive short circuit power cycling of smart power switches shows degradation of the metallization layer with cracks and voids as shown in **Figure 8**. This study concludes that the temperature swing, ΔT, is probably the most important stressor in the metallization degradation. The conclusion that the temperature is the main factor is also supported by *in situ* transmission electron microscopy (TEM) indicating that the damage is not caused by electromigration [47]. Also, isothermal fatigue testing of Al [41] and Cu [42] thin films on compliant substrates shows similar damage evolution as for thermally cycled thin films, which also supports the conclusion that electromigration plays a minor role and that thermo-mechanical stress is the main driving force of the observed degradation.

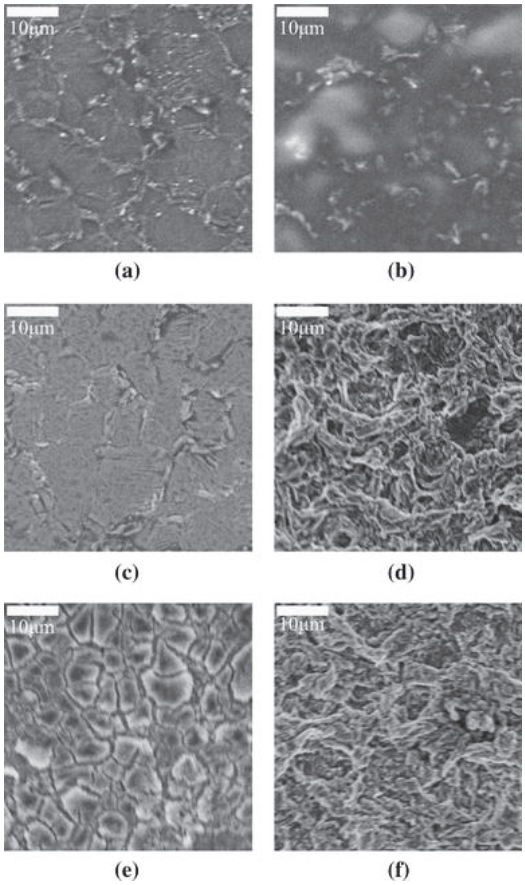

Figure 7. SEM images of diode metallization surface for power cycled modules. a) $C_{50\%}$ low-side (LS) diode edge. b) $C_{50\%}$ LS diode center. c) $D_{70\%}$ LS diode edge. d) $D_{70\%}$ LS diode center. e) $E_{90\%}$ LS diode edge. f) $E_{90\%}$ LS diode center. Reprinted from [22] with permission.

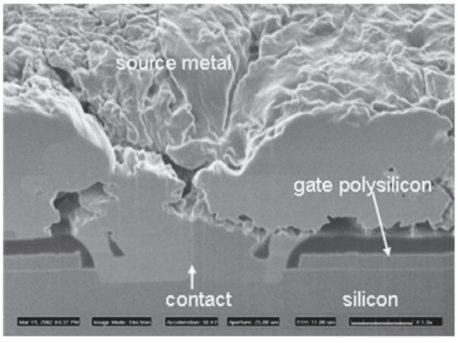

Figure 8. Metal degradation of a high side smart power switch after repetitive short circuit. Reprinted from [40] with permission.

Hillock formation is also a well-known phenomenon through which compressive stresses in thin film can relax. It has been examined extensively in many studies showing that grain boundary diffusion can cause hillock formation in Al thin films [43]–[50]. However, hillock formation is a purely diffusional mechanism and is only seen when the temperature reaches values (300 ºC-400 ºC) that lie above the operating temperatures of power electronic chips. Therefore, no additional emphasis will be put on this phenomenon.

In some works, TEM is used to investigate the dislocation movement and resulting microstructural change during thermal excursions. The temperature range of the thermal cycling in these studies is typically high (300 ºC-450 ºC) when compared to the temperature that is reached in functioning power electronic chips (up to 170ºC). However, the type of the observed dislocations and the dislocation activity can be valuable for developing better physical models for the degradation of the metallization in power chips. Different dislocation types such as threading dislocations and screw dislocation [51], [55], have been found in Al films on Si substrates. Dislocation glide have been established as the main driver through which plasticity changes occur in these thin films [51]–[56], while other effects such as dislocation pileup at the Al-Si interface and grain boundaries have also been identified as contributing mechanisms.

Some efforts have been put into simulations of the metallization fatigue using the finite element method (FEM). Crack propagation and stress levels in a MOSFET metallization have been simulated but no lifetime model has been developed due to lack of experimental results and proper physical model for degradation phenomena [74]. FEM simulation in conjunction with power cycling data has been used to develop a lifetime model for an Al chip metallization in a special test structure using a Coffin-Manson or a Norris-Landzberg approach. However, it has been concluded that neither of the models are sufficient and that better physical models for the accumulation of plastic strain and related degradation mechanisms are needed [75].

Inter-granular cracks, surface roughening, sub grain boundary formation, and grain boundary grooving have been observed in the metallization of MOSFETs and IGBTs subjected to various types of power cycling [57]–[59]. However, grain growth in the metallization of MOSFETS has also been found [60], [61], and some studies show that the grain growth primarily happens in the regions underneath wire bonds [62]. It has also been observed that the surface roughness of the Al layer, which occurs beneath wire bonds, can decrease the strength of the interface and contribute to crack formation and wire lift-off [62], [63].

In [59] a qualitative model for the metallization restructuring (degradation) is proposed, suggesting predominantly dislocation-based plasticity in the early stage, while grain boundary diffusion as the major vector at later stages of the degradation process. Dislocation glide is thought to be the main mechanism for the dislocation-based plasticity. This finding is supported by the data on sub-grain boundary

formation and dislocation movement observed by *in situ* TEM measurements. Thus, the grain boundary diffusion is proposed to be the main mechanism for the plastic deformation of the metal layer. This suggestion is based on the analytical model developed by Gao et. al. [76], [77], which describes crack-like grain boundary diffusion wedges in thin metal films and proposes that they could enhance dislocation plasticity processes. A schematic illustration of the model is presented in **Figure 9**. In the first phase (see **Figure 9**(a-c)), the stress causes dislocation-based plasticity that results in sub-grain boundary formation. When this process is exhausted and there are no more mobile dislocations allowing for easy plastic deformation, the diffusion processes takes over and leads to the formation of crack-like diffusion wedges (**Figure 9**(d-f)). As the stress cyclically alternates between compressive and tensile modes, the cracks move deeper into the film, thus destroying the film continuity and increasing the electrical resistance. This qualitative model does not predict any specific failure modes that can be used to verify its validity. However, it suggests that oxidation effects play a major role in the crack formation, thus, the degradation rate in a metallization should be sensitive to the amount of oxygen in the atmosphere. Therefore, an experiment where thermal cycling is achieved in oxygen rich and oxygen free atmosphere should show significant differences in the degradation rate and this could help to verify or falsify the validity of the model.

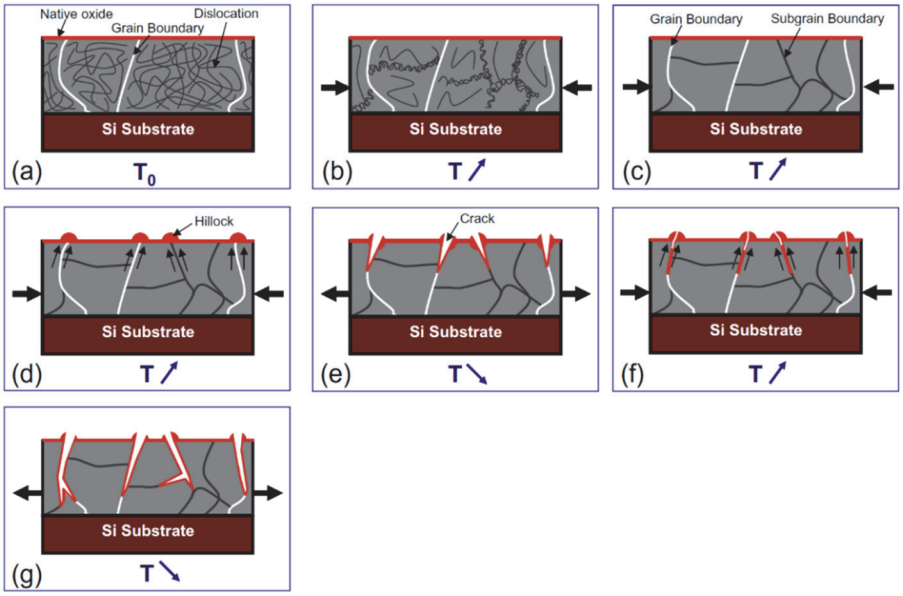

Figure 9. Gao's model extended to Al layers undergoing tension and compression stresses during thermal cycles. Panels (a–c) illustrate dislocation density decrease by recombination in sub-grain boundaries and absorption at grain boundaries and interfaces. Panels (d–g) show Al diffusion along grain boundaries, and subsequent oxidation causing crack propagation through the Al layer. Reprinted from [59] with permission.

2.2.2.2 Evolution of electrical properties

Metallization layers on high power chips such as diodes, IGBTs, and MOSFETs should be designed to provide the necessary mechanical and electrical interconnections with wires and to form a constant electrical potential across the chip area, which is especially critical for active chips (e.g. IGBTs and MOSFETs) with their planar cell structure. This means that the degradation of the metallization layer structure does not only affect the mechanical state of interconnects (e.g. wire bonds) but also can lead to drastic increase of resistance and, therefore, to electrical failures due to uneven current sharing and chip instabilities. Thus, knowledge of the evolution of chip metallization resistance not only provides a cursor for the mechanical degradation state of metallization but it can also be critical for understanding of failure mechanisms that are directly related to the change of electrical properties. Monitoring of the film resistance has, therefore, been used as a characterization technique for a part of the experimental work of this thesis and an overview of the literature on this subject is presented below.

In [64] custom packaged IGBT chips subjected to repetitive short-circuit (SC) cycling were investigated with focus on the damage and change in resistance of the chip metallization. The results on topographical changes of the metallization layer were accompanied by the data from the electrical characterization of the chips. In this specific setup, the IGBT chips featured additional bond wires that allowed for four-point resistance measurements of the chip metallization during short-circuit cycles, thus providing the continues tracking of the electrical properties. It was found that the change in metallization resistance can be partially decoupled from the rise of the on-state voltage and that three different phases of the resistance change can be distinguished. The evolution of the resistance is shown in **Figure 10(**a). The three phases are described as: 1) little to no change (0-10000 cycles), 2) significant change (10000-30000 cycles), and 3) moderate change (30000-80000 cycles). This type of behavior has also been observed in other studies as shown in **Figure 10**(b-c). In [65], a similar approach as in [64] was used to study the metallization degradation of IGBT chips. The corresponding change of resistance is shown in **Figure 10**(b). Different phases were linked to fractures in the Al layer that initiated at the surface and propagated into the layer towards the Si chip, thus causing electrical disconnections and a decrease in the effective cross-section of the metal film. In [59], the metallization degradation of actively power-cycled MOSFET chips was studied by microstructural and electrical characterization (see [58] for details about ageing procedure). The evolution of the metallization resistance of these devices is shown in **Figure 10(**c), and the same trend in the resistance change can be observed once again. The micro-structural and electrical degradation was explained by the analytical model schematically shown in **Figure 9**. In [67], an Al track on Si (4 μm thick and 1 mm wide) was thermally aged by repeatedly injection high current pulses through the layer and the relative change of the resistance was monitored using four-point voltage measurements. The evolution of the relative resistance is shown as the bottom curve

in **Figure 10**(d), and it exhibits the already established phases. In [66], severe degradation of the metallization layer of both diodes and IGBTs subjected to power cycling was found. This was seen as clear roughening, apparent grain extrusion and void development. The sheet resistance of diode was found to increase for 41% after 16800 power cycles with ΔT=160K and T_{max}=200K. The observed electrical degradation of chip metallization was coupled to the thermo-mechanical fatigue. The phenomenon, however, did not show a simple correlation to the number of cycles but rather evidenced a complex evolution with different phases as already seen in **Figure 10**.

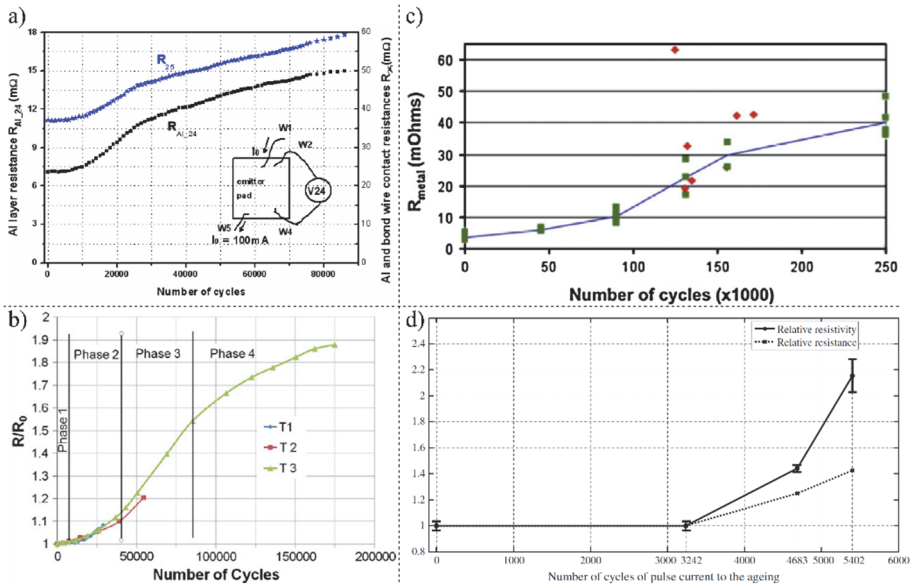

Figure 10. a) Evolution of Al layer resistance during repetition of the SC operations (600V NPT IGBT) (reprinted from [64] with permission © 2008 IEEE). b) Al resistance increase after repetition of a large number of ageing cycles (0.47 J/cycle) (reprinted from [65] with permission). c) Evolution of R_{metal} as a function of the number of cycles. Green squares represent operational devices, red diamonds failed devices. The blue curve shows the mean evolution of R_{metal} for operational devices (reprinted from [59] with permission). d) The variation of the relative resistance (r_{EC4P}) to the number of ageing cycles (reprinted from [67] with permission).

Generally, the explanation for the initial phase with almost no change in the resistance is that some dislocation-based change in film structure occurs without breaking the film continuity. The responsible mechanisms could be dislocation glide and sub-grain boundary formation. At some point, these processes come to stress accumulation at a critical value and a second phase begins where the film relaxation occurs through the formation of macroscopic cracks that are initiated at the surface of the film and propagate inwards the film. This crack formation breaks the continuity of the film and decreases the effective cross-section, thus increasing the resistance severely. The

second stage of drastic film restructuring is followed by next phase characterized by more moderate change of the resistance related to gradual growth of cracks and accumulation of other structural defects.

2.2.2.3 Change of film texture

Some studies have shown that the texture of Al thin films on Si substrates plays an important role in the degradation phenomena occurring during thermal cycling [68], [69]. Considering the complex behavior of the electrical change presented in subsection 2.2.2.2 and the proposed models that rely on dislocation based plasticity such as dislocation glide, the importance of film texture seems clear. Dislocation movement is constrained by grain boundaries, and dislocation glide is directly related to the orientation of the crystal structure since it occurs along specific crystalline planes. Thus, both the grain structure and texture of a metallic film should be taken into account when developing a physical model that can predict and explain the observed degradation.

In [68], the influence of different microstructures and texture of Al thin films in regards to the fatigue behavior was studied. The samples consisted of Si substrates with different thin Al layers were thermally cycled from 100 ºC to 450 ºC to induce thermo-mechanical fatigue in the metallization layers. Polycrystalline and epitaxial films with different thicknesses were characterized by stress-strain curves, SEM, electron backscatter diffraction (EBSD) and x-ray diffraction (XRD). It was found that the fatigue behavior and texture evolution of the epitaxial films and polycrystalline films differed significantly in the way that the epitaxial films kept their initial (111) texture and showed almost no degradation. SEM images of the surface of new and thermally cycled 2 μm thick epitaxial films along with inverse pole figures are shown in **Figure 11** demonstrating almost no change in either topography or texture. By comparing the degradation of the epitaxial film to that of the polycrystalline film, which is presented in **Figure 12**, the difference can be clearly observed. At 10000 thermal cycles the polycrystalline film (see **Figure 12**(d)) shows severe surface roughening while the epitaxial film (see **Figure 11**(b)) shows little to no change.

The texture evolution of the polycrystalline film was monitored by EBSD measurements and these results are presented in **Figure 13**. It can be seen that the film initially has a dominant (111) texture (see **Figure 13(**a)) that during thermal cycling evolves towards (211) or (311) texture (see **Figure 13(**d)). The position of (211) and (311) in an inverse pole figure can be seen in **Figure 21**(b). The difference of the fatigue behavior between the epitaxial and polycrystalline films is explained by the differences of the Al-Si interfaces and the amount of grains in the polycrystalline film that initially deviate from the exact (111) orientation. The authors propose that dislocations in the polycrystalline films disintegrate at the crystalline/amorphous interface through interface diffusion [68] thus preventing reverse slip through the

same dislocations during the cooling stage. This cannot happen in the epitaxial film due to the crystalline Al/Si interface where it is proposed that a network of misfit dislocations is formed through which the reverse slip can occur during the cooling cycle.

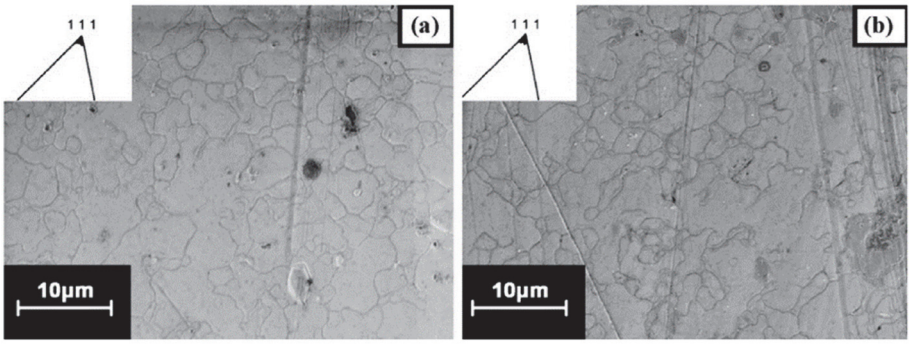

Figure 11. SEM images of the epitaxial Al film on (0001) α-Al_2O_3 at different numbers of thermal cycles: (a) initial state and (b) 10000 cycles. Inserts show the sharp texture of the epitaxial Al film even after 10000 thermal cycles. Reprinted from [68] with permission.

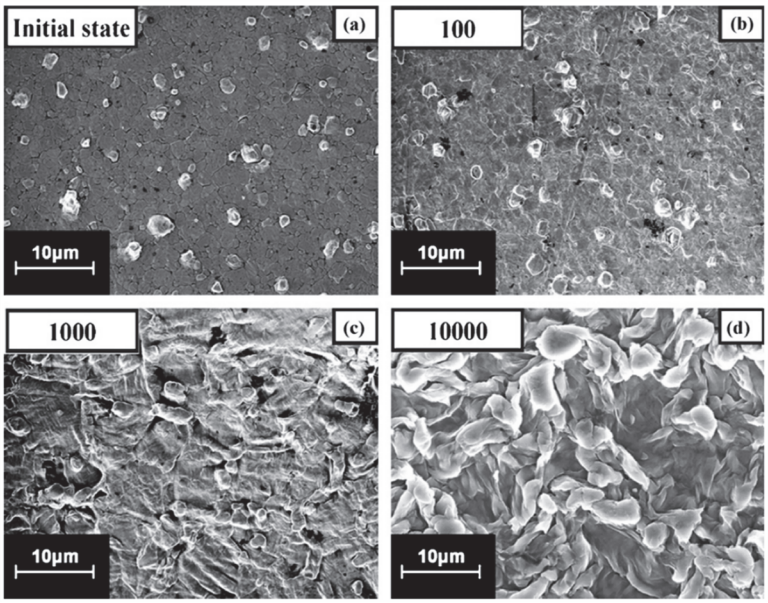

Figure 12. SEM images of a 2 μm thick Al film on oxidized (100) Si at different thermal cycles: (a) initial state, (b) 100 cycles, (c) 1000 cycles, and (d) 10,000 cycles. Reprinted from [68] with permission.

Another factor, which according to the authors can play a role, is the domination of initial (111) texture. The epitaxial films show a very sharp (111) peak with very little deviation (see insets in **Figure 11(**a)), while the polycrystalline films show a broader (111) peak with 95.5% of the grains having a misorientation of 2º or more from the exact (111) value. This can play an effect in the way that a deviation from (111) can cause the preferred activation of only a few glide systems that then due to the asymmetry causes the rotation of the grains. On the other hand, in the epitaxial film with the very sharp (111) texture, the dislocation glide can occur in a larger number of symmetric glide systems, which will not cause a rotation in any preferred direction. It is worth to stress that the above-presented explanations for the difference between the polycrystalline and epitaxial films rely on assumptions and they are not verified by any direct measurements such as e.g. *in situ* TEM or XRD measurements.

Further findings regarding the texture evolution of Al thin films during thermal cycling are reported in [69]. In this work, a thermal cycling approach similar to that used in [68] was applied to a 0.6 μm thick polycrystalline Al film on a Si substrate. It was found that single grains rotate from the initial (111) towards (211) orientation by a random walk behavior and that orientation gradients of up to 4º can evolve during the thermal cycling. The mechanism for the rotation of the grains is proposed to be a classical dislocation-based plasticity [78]. The model is based on the grain orientation evolution presented in **Figure 14** and can be explained as follows. For an unconstrained crystal in tension, slip will occur along a slip plane causing steps and terraces on the surface (see **Figure 14**(a)). However, when a constraint is introduced on one side of the crystal (e.g. a stiff Si substrate), the material cannot move in this direction, thus causing a crack to open in the topside of the film alongside with a rotation of the crystal (see **Figure 14**(b)).

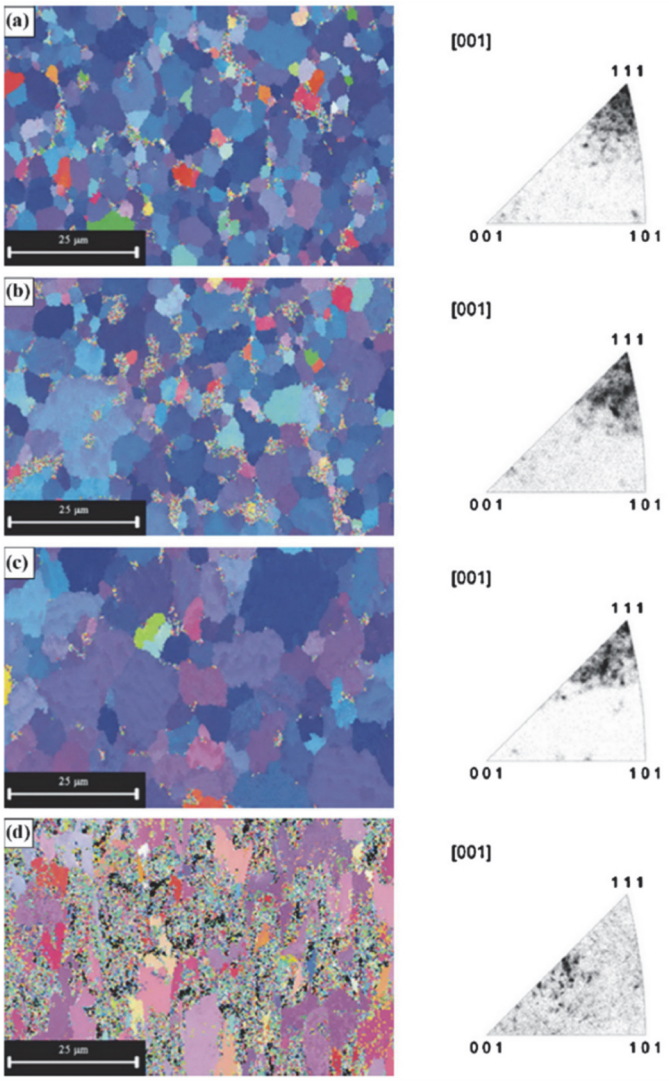

Figure 13. EBSD grain orientation maps and inverse pole figures from (a) the initial state, (b) after 100 thermal cycles, (c) after 1000 thermal cycles and (d) after 10000 thermal cycles. Reprinted from [68] with permission.

Additionally to study of texture evolution of thin Al [68], [69] and Cu [70] films, the strengthening of metal films due to the effect of low dimensionality and resulting dislocation activity is worth to be mentioned. It has been studied extensively [38], [48], [51]–[56], [71]–[73] but typically at much higher temperatures than the operating temperatures of power electronic chips. The increased temperate means that the diffusion induced plasticity plays a much larger role in the deformation process

and that the proposed mechanism and models are not directly applicable in the case of power electronic chips. Thus, it can be preliminary concluded that a better understanding of the physical processes that govern the fatigue behavior of thin Al films is needed in order to develop better models than can be used to evaluate the lifetime and reliability of power chip metallization.

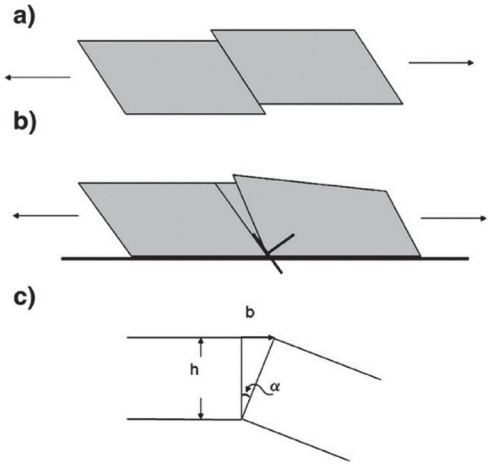

Figure 14. Comparison of (a) free dislocation glide on an inclined (111) plane causing no orientation change and (b) the constraining effect of a substrate, leading to an orientation change for the slipped portion due to the stiff substrate by storing the dislocation at the interface. (c) Orientation changes α caused by a dislocation with Burgers vector b in a material of thickness h. Reprinted from [69] with permission.

2.2.3. SOLDER, SINTER, AND TLPB LAYER DEGRADATION

Solder and sinter layers can also fail due the difference in CTE of the stack in a power module. Typically, cracks are initiated near sharp corners or voids in the solder or sinter layers where the stresses are the highest due to geometric reasons. An example of the degradation of sinter layer is shown in **Figure 15**. As the layer delaminate, the thermal conductivity is degraded, thus increasing the temperature of the semiconductor chip and the thermal gradient across the thermal stack. This acts as feedback mechanism, which accelerates the degradation of the interconnection layer itself as well as the metallization and wire bonds.

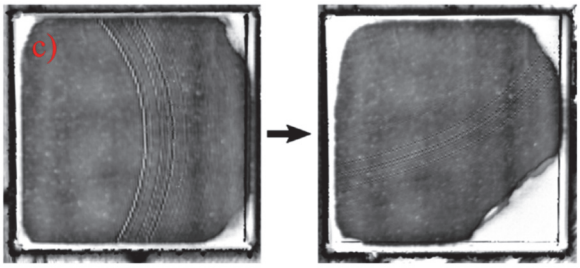

Figure 15. Scanning acoustic microscopy (SAM) image of sinter delamination after thermal cycling. The left SAM image is of the uncycled sinter layer while the right is after thermal cycling showing the lost contact in right bottom corner.

2.2.3.1 Solder fatigue

Additionally to the already described failure mechanisms in power devices, the thermo-mechanical fatigue of solder layers should be mentioned [3], [5]. It is especially pronounced for the large-area solder interconnection between the DBC and baseplate of the module [16]. Crack initiation and delamination typically occur at the edges of the solder interface since this is a place where the shear stresses reach maximum [79]. However, cracks can also initiate in voids and imperfections that are present from fabrication steps. It should also be noted that for lead-free solders used as die attach, the degradation can start in the center of the solder joint due to the occurrence of the maximum temperature in the area [66], [80], [81]. Solder fatigue in power modules has been studied extensively by power cycling [26], [27], [57], [58], [60], [61], [66], [80], [82], [83], thermal cycling [82], [84] and isothermal mechanical test [85]–[87]. Also, significant effort has been put into physics-of-failure (PoF) based finite element (FE) modelling of the damage accumulation with a purpose of lifetime prediction of theses layers [27], [81], [83], [84], [87]. The quality or degradation state of the solder layers are typically examined non-destructively by scanning acoustic microscopy (SAM) [27], [57], [58], [60], [61], [66], [84] or destructively by cross-sectioning [26], [80], [83], [86]. The SAM method has the advantage that the same solder joint can be monitored during thermal or power cycles such that the evolution of the solder degradation can be followed [27], [84]. Many experimental findings confirm that the degradation initiates at the edges of solder layers [26], [27], [80], [82]–[84] as predicted by theory [79] and FE modelling [27], [83], [84]. These studies also confirm the prediction about preferential degradation of central areas of lead-free solders [66], [80], [81]. Generally, it can be said that the solder fatigue phenomenon is quite well covered by the current literature with advanced and verified FE models allowing to simulate the degradation and provide good lifetime estimations of the solder layers in power devices.

2.2.3.2 Silver sinter fatigue

Silver sintering is a state of the art interconnect technology that can produce interface layers with excellent mechanical and thermal properties. It is currently being used in many of the top-line products from several major power electronics suppliers. The thermal properties of sintered Ag joints far exceed traditional solder joints, and this have been shown in thermal-cycling [88]–[91], power-cycling [92]–[96] and isothermal bending tests [97]. Some power cycling test have shown that power modules with silver sintered joints can have an increase in lifetime for more than 50% compared to ordinary solder ones [92]. Other tests have shown an almost two-fold increase in number of power cycles before failure [94]. After the sintering process, the Ag sinter layer has an initial porosity which affects the lifetime negatively [93]. The initial porosity depends on the sintering pressure, and a relatively high pressure is, therefore, needed to be applied during the process, which complicates the procedure since the brittle semiconductor chips and DBC substrate are prone to cracking. Furthermore, it has been shown that the porosity can increase dramatically during thermal cycling from an initial value of approximately 10% to 30% after 1000 thermal cycles (-40 ºC to 50 ºC) [98]. Eventually, the pores and cavities merge, which results in an increase in the electrical and thermal resistance of the bond along with the formation of larger cracks, which leads to the failure of the sintered joints [9]. Generally, silver sintered bonds are considered to be very reliable, however the high cost currently limits the use to premium devices only.

2.2.3.3 TLPB fatigue

It is well known that the TLPB process can produce high strength and high temperature resistant joints, which exceed the capabilities of joints produced by standard solder techniques [10], [11]. However, the fatigue properties and reliability aspects of TLP bonded joints in power electronics remain scarce as it is currently an emerging technology. Most studies examine the fabrications parameters that are necessary to produce strong joints. Among them are interlayer thickness [99]–[101] and optimal intermetallic phases [102]–[106]. Some studies have examined the fatigue properties of TLPB joints subjected to thermal ageing. They found that the joints remain stable and strong even after long time exposure to temperatures up to 500 ºC [103], [107]–[109]. Recently, interesting results on the fabrication parameters and intermetallic composition for application to Si chips in a power electronic devices are obtained both experimentally and by FE modelling [110]. It is shown that residual stresses after bonding depend strongly on the choice of chip metallization and resulting intermetallic composition and that the high residual stresses can affect the lifetime negatively [110]. A novel bonding technique based on TLPB is presented in [111]. In this work, a preform consisting of Cu particles embedded in a Sn matrix is produced and joints are created using a standard reflow process. During the reflow process, Sn in the preform matrix is fully converted into Cu-Sn compound, resulting in a joint with high shear strength and thermal capabilities. The joints produced by the

preform are compared to standard TLPB bonds using a thermal shock test in the temperature range of 55 ºC – 200 ºC. The test demonstrates high reliability of both the preform-based and standard TLP bonded joints, with the preform-based ones being the most reliable.

2.2.4. FAILURES RELATED TO BASEPLATE

The baseplate of a power module necessitates the use of large area joints to connect to the DBCs and is therefore indirectly the cause of some of the already discussed failures in solder, sinter and TLPB layers. For example, during thermal variation the baseplate will bend due to the CTE difference with the soldered DBC sections causing stress accumulation in the joining layer. To circumvent these disadvantages entirely, power modules without baseplates have been designed and investigated. They demonstrated significant increase in reliability [92].

Alternative solutions based on asymmetric hybrid-metal baseplate design are currently being investigated and, for example, described in patents [112]–[114]. These baseplates consist of an asymmetric Cu-Mo-Cu sandwich structure joined together by either silver sintering or TLP bonding technique. The asymmetric structure reduces the amount of deflection during thermal excursion and can avoid the normal pre-bending of baseplates [115], thus lowering the stress in the solder layer to the DBC and also limiting other degradation mechanisms such as TIM pump-out effect [116]–[118]. The study presented in Chapter 6 about the TLP bonding of Cu-Sn-Cu and Cu-Sn-Ag-Mo structures was initiated to examine the feasibility of using TLPB as an alternative to the existing usage of silver sintering in these hybrid-metal baseplates.

2.3. RELIABILITY OF POWER MODULES

The described failure and fatigue mechanisms significantly affect stability of operation of power electronic devices and their reliability, which are very important factors for end users. Therefore, careful consideration of failure mechanisms and operation conditions can shine light on device reliability and lifetime prediction.

To examine the reliability of a given electronic component or device, one must look at the failure distribution, $f(x)$. This distribution is a probability density function (pdf) for failure occurrence and the variable, x, is typically the operating time or number of power or thermal cycles. The reliability function, $R(x)$, is defined as

$$R(x) = 1 - F(x) = 1 - \int_0^x f(x), \qquad \textbf{(1)}$$

where $F(x)$ is the cumulative distribution function (cdf) of the failure distribution $f(x)$ [119]. Thus, the reliability function gives the probability that the component or device will be functional beyond the time or number of cycles specified by the variable

x. The hazard function, also known as the failure rate, is defined as the ratio between the pdf $f(x)$ and the reliability function $R(x)$:

$$h(x) = \frac{f(x)}{R(x)}. \quad \textbf{(2)}$$

Thus, $h(x)$ is the conditional probability that the component or device will fail at x, with the condition that failure has not already occurred. Many different pdf's can be used to model the failure distribution and this depends on the nature of the examined devices or components. For electronic devices, the failure distribution is typically described by a Weibull approach or a combination of multiple Weibull distributions [120]. The three-parameter Weibull distribution is defined as

$$f(x) = \frac{\beta}{\eta^{\beta}} x^{\beta-1} \exp\left[-\left(\frac{x-\gamma}{\eta}\right)^{\beta}\right], \quad \textbf{(3)}$$

where β is the shape parameter, η is the characteristic life, and γ is the so-called location parameter. For most practical applications the location parameter γ, which describes a failure free initial period, is zero and the distribution, thus, simplifies to a two-parameter Weibull distribution. By inserting eq. **(3)** into eq. **(1)** and performing the integration, the Weibull reliability function then becomes

$$R(x) = \exp\left[-\left(\frac{x-\gamma}{\eta}\right)^{\beta}\right], \quad \textbf{(4)}$$

and as follows from eq. **(2)**, the hazard rate becomes

$$h(x) = \frac{\beta}{\eta^{\beta}} x^{\beta-1}. \quad \textbf{(5)}$$

As it can be seen, the hazard rate can be different depending on the choice of the parameters β and η, and it will also change as the time or number of cycles increases. For real world electronic devices a combination of multiple Weibull curves must be used and the hazard rate plotted as function of time will typically result in the well-known bathtub curve [121], which is illustrated in **Figure 16**.

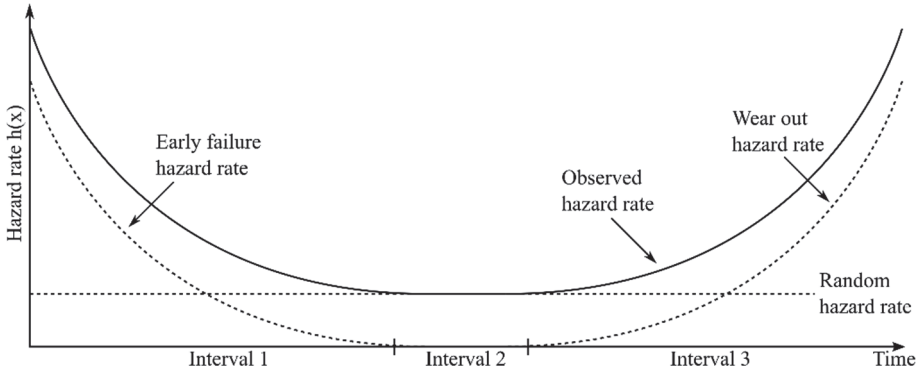

Figure 16. Bathtub curve with three intervals, 1) hazard rate is decreasing due to early failures, 2) hazard rate is constant due to random failure, and 3) hazard rate is increasing due to wear out failures.

Three intervals for the change of the hazard rate can be recognized in **Figure 16.** In the first interval the hazard rate is decreasing ($\beta < 1$) and these early failures are typically due to lack of quality control resulting in faulty devices that quickly fail during operation. In the second interval the hazard rate is constant ($\beta = 1$) and this is characterized by random failures such as e.g. semiconductor breakdown due to cosmic radiation, human error etc. In the third interval the hazard rate is increasing ($\beta > 1$), which is due to the onset of failures caused by wear-out such as thermo-mechanical fatigue.

2.3.1. LIFETIME ESTIMATION

For power electronic devices the data needed to find the true failure distribution under a given realistic load are typically not readily available. For example, in wind mill converters the lifetime of the power electronics is typically designed to last for decades and reliability testing under these realistic load conditions would therefore require unreasonable long testing and validation times. Therefore, the normal approach is to perform reliability test under much harsher load conditions that accelerate the occurrence of device failure. The data obtained from the accelerated power cycling test can then be used to extrapolate into the realistic load conditions, providing an estimation of the device lifetime. One of the most widely used lifetime estimation models is the Coffin-Manson-Arrhenius model:

$$N_f = \delta(\Delta T)^{\alpha} \exp\left(\frac{E_A}{k_b T_{max}}\right), \quad \textbf{(6)}$$

where N_f is the number of cycles to failure, $\Delta T = (T_{max} - T_{min})$, δ and α are characteristics of the material and test setup, E_A is the activation energy, and k_b is the Boltzmann constant. Thus, by fitting this model to data produced in an accelerated power cycling test at an elevated ΔT and T_{max} compared to realistic field load

conditions, the parameters δ and α can be approximated and used to estimate the lifetime of the device under normal operation. Models of the Coffin-Manson-Arrhenius type has been shown to approximate the lifetime of solders and other metallic components during repeated temperature cycling [122], however the models has clear limitations and many other more advanced models have been developed, such as e.g. the Norris-Landzberg model [123], which is only one among many.

2.3.1.1 Physics-of-failure based approach

A huge disadvantage of all the empirical/statistical models is the time and work that has to be put into the power cycling test and the fact that the results from a given test on a power module only provide a lifetime estimation for the specific type of power device. The results are not easily translatable into reliability aspects of other power modules and no knowledge is gained about the actual physical processes at play. Therefore, in recent years a move towards a PoF based lifetime modelling approach has been seen [5]–[7]. The PoF approach entails the use of advanced thermo-mechanical FE simulations to gain knowledge about different possible failure mechanisms at package, component, and sub-component levels. However, to use the PoF approach a solid physical understanding of the failure mechanism must be established as well as comprehensive and systematic failure analysis and characterization must be accomplished for verification and parameter tuning of the FE model. When this point is reached the PoF approach can provide a deeper understanding of the reliability aspects and it is easier to transfer it to different load conditions and different power devices for which the lifetime must be estimated. A good example of a solid PoF approach for the estimation of bond wire fatigue can be seen in [36]. There, a computational model for a power module is realized and the damage accumulation is predicted by a FE approach, while the model is verified by extensive physical analysis of wire bond degradation in power cycled devices [34]. Similar approaches also exist for solder fatigue as discussed in section 2.2.3.1. However, a proper physical model for the metallization degradation in power electronic chips still needs to be developed and verified.

Therefore, the one of the main goals of this project is related to developing of a solid physical understanding of the degradation mechanisms in metallization layer of power chips. This knowledge can by further used in the PoF approach in order to better predict the lifetime of power modules and also make suggestion on optimization of technologies used in the device production.

CHAPTER 3. FATIGUE IN THIN METAL FILMS

3.1. STRENGTH OF THIN FILMS

It is well known that the strength of thin films is higher than their bulk counterparts made of the same material and that in general the dimensions of samples influence the strength and plasticity [124]. For example, the yield strength of bulk aluminum is around 10 MPa [125], while **Figure 6** indicates that the yield strength of the 590 nm thick Al film on Si is about 280 MPa. Thus, the yield strength is increased by more than one order of magnitude. Since the metal films used as metallization layers in semiconductor devices typically have microgranular structure [126], the increase in strength can be partly explained by the grain-boundary strengthening described by the Hall-Petch model [127]. It states that the yield strength depends inversely on the square root of the grain size as

$$\sigma = \sigma_0 + f d^{-\frac{1}{2}}, \tag{7}$$

where σ is the yield strength, σ_0 is the yield strength for a bulk single crystal, f is a constant known as the Hall-Petch parameter, and d is the grain diameter. The model cannot, however, solely ground the effect, because monocrystalline thin films also show much higher strength than the bulk material [38]. It is also known that free-standing thin films with a fine micro-granular structure show less strength than the films that are constrained by the substrates. This is evident from **Figure 17** where a comparison of the biaxial yield strength between the freestanding and constrained Al films is presented according to the Hall-Petch relation. The constrained Al films show a much higher yield strength than predicted by the Hall-Petch relation and also than that of free-standing films.

Other studies on the relation between film thickness and grain boundary strengthening effect in Al films on Si show similar results [72], [128]. In [72] it is found that both the grain boundary strengthening and film thickness make important contributions to the mechanical properties of Al films on Si substrates. They measure the stress variations in Al films on Si as a function of the film thickness. The change in the film thickness is achieved by etching the same film, thus, making it thinner in a controlled manner. They find that the strength varies inversely with the film thickness, $\sigma \propto h^{-1}$, but not inversely to the square root as predicted by Hall-Petch theory (see eq. **(7)**). These results imply that some other mechanism must be at play and this can be understood by applying the so-called Freund-Nix model [38], [129]. This model describes the strength of thin metallic films on substrates by considering how the substrate can affect the dislocation movement and resulting plasticity of these films.

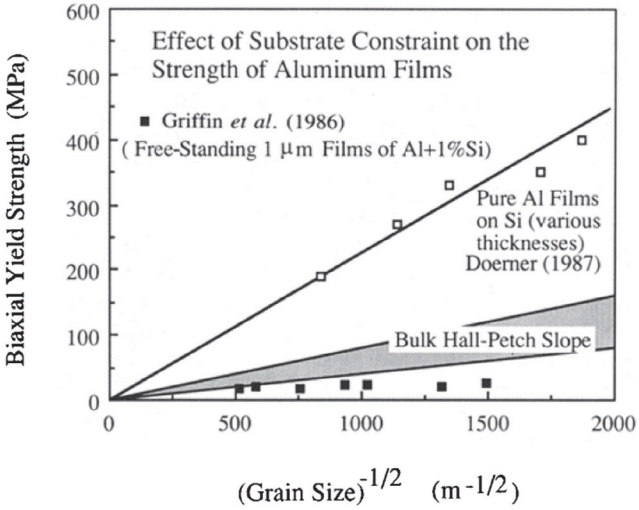

Figure 17. Comparison of the strengths of the Al films on Si substrates [130] with the biaxial strengths of free-standing films of Al + 1% Si [131], [132] in the form of a Hall-Petch plot. The constraint of the substrate causes the films bonded to the substrate to be much stronger than the free-standing films. Reprinted with permission from [38].

The Freund-Nix approach takes into account the geometry as presented in **Figure 18**. Here, the dislocation motion in an oxidized single crystal thin metal film on stiff substrate is considered. Since the substrate and oxide are brittle with very little elasticity, a dislocation that moves through the metal film will leave a misfit dislocations at the interfaces [38]. For Al on Si, there are many threading dislocations present after the growth process due to the mismatch in lattice parameters of Al and Si, and therefore dislocation motion will typically occur by threading dislocations moving in their slip planes [38].

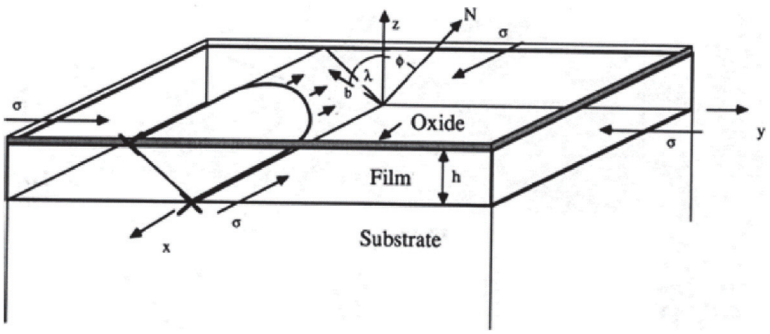

Figure 18. Dislocation motion in an oxidized film on a non-deformable substrate. Misfit dislocations are produced at the two interfaces. Reprinted with permission from [38].

Following the approach developed in [129], an expression for the work done by the biaxial stress in a thin film when a dislocation travels a unit distance for the geometry shown in **Figure 18** can be derived as [38]

$$W_{layer} = \frac{\cos\phi\cos\lambda}{\sin\theta}\sigma bh, \qquad \textbf{(8)}$$

where b is the Burgers vector, σ is the biaxial stress, and h is the film thickness. The meaning of the different angles can be seen in **Figure 18**. In order to move, the dislocation must overcome the work required to lay down the misfit dislocations at the interface. This work can be expressed as [38]

$$W_{dislocations} = \frac{b^2}{4\pi(1-\nu)}\left[\frac{2\mu_f\mu_s}{(\mu_f+\mu_s)}ln(\frac{\beta_s h}{b})+\frac{2\mu_f\mu_0}{(\mu_f+\mu_0)}ln(\frac{\beta_0 t}{b})\right], \qquad \textbf{(9)}$$

where t is the thicknesses of the oxide, μ_f, μ_s, and μ_0 are the elastic shear moduli of the film, substrate, and oxide, respectively, β_s and β_0 are the numerical constants, and ν is the Poisson ratio. By equating eq. **(8)** and eq. **(9)** and solving for σ, the minimal biaxial stress that is needed to move the dislocation in the film becomes

$$\sigma = \frac{1}{h}\frac{b\sin\phi}{2\pi(1-\nu)\cos\phi\cos\lambda}\left[\frac{\mu_f\mu_s}{(\mu_f+\mu_s)}\ln(\frac{\beta_s h}{b})+\frac{\mu_f\mu_0}{(\mu_f+\mu_0)}\ln(\frac{\beta_0 t}{b})\right]. \qquad \textbf{(10)}$$

It should be noted that the expression in eq. **(10)** is for a monocrystalline oxidized thin film on substrate. Only the constraints from the substrate and the oxide layer are evaluated and no other obstacles such as other dislocations, grain boundaries or point defects are accounted for. Further results including some of these obstacles can be found in [71]. Nevertheless, the obtained equation shows an inverse relationship with the film thickness that agrees with the earlier discussed experimental results [72], [128].

For a film without an oxide layer, and therefore a free top surface, the moving dislocation will be perpendicular to the free surface and only leave a misfit dislocation at the substrate interface. In this case, the minimal biaxial stress will be smaller and can be determined by deleting the second term in square bracket in eq. **(10)**. The prediction of the difference between oxidized and non-oxidized Al films is also supported by experimental evidence showing higher strength and different stress relaxation dynamics for Si-Al-SiO_2 multilayer films compared to Si-Al with a native oxide layer [133].

In **Figure 19** experimental results of the biaxial strength of (111) oriented Al films on Si are compared to the results obtained by the expression in eq. **(10)**. The middle curve labeled as σ_0 results from eq. **(10)** and it predicts a lower yield strength, especially for thicker films. However, by adding the contribution from grain-boundary

strengthening (see eq. **(7)**), which is shown by the curve labeled as $k_y d^{-1/2}$, the top curve labeled as σ is produced. It is then clear that the prediction of this combined model agrees reasonably well with the experimental data, although it gives the values that are still too small for thicker films.

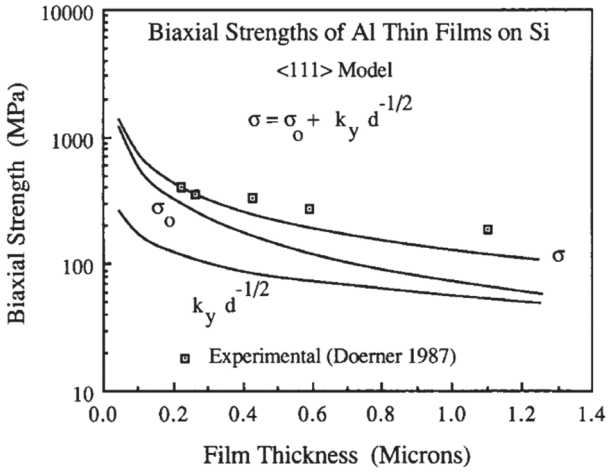

Figure 19. Experimental results on the biaxial strengths of Al thin films on Si substrates [134] are shown as squares. The prediction obtained from the misfit dislocation model for film strength is shown as bottom curve. Strength calculated according to Hall-Petch model is shown as middle curve. Combining both models leads to top curve showing good agreement with the experimental data. Reprinted with permission from [38].

One more important parameter affecting mechanical properties is temperature. For a thin film on thick substrate the change in stress value due to a change in temperature can be estimated by the formula [135]

$$\sigma = \Delta\alpha \cdot \Delta T \cdot M, \qquad \textbf{(11)}$$

where $\Delta\alpha$ is the difference in CTE, ΔT is the thermal variation, and M is the biaxial modulus of the thin film. Inserting values for Al on Si leads to a change of stress of around 20 MPa for every 10 ºC of temperature change.

Thus, the Freund-Nix model captures some of the essential mechanisms that are important to understand how the mechanical properties of thin films can differ so profoundly from similar bulk samples. It studies the energies involved in dislocation motion in the thin films and takes into account the constraints that are imposed by the stiff substrate and native oxide layers. It can be quite powerful in prediction yield strength of polycrystalline thin films when it is combined with the well-known grain-boundary strengthening effect. However, it should be noted that it does not include the dislocation density that can be very high for thin films and, therefore most likely contributes significantly to the film strength. Also, this model cannot account for the

difference in the fatigue behavior between epitaxial and polycrystalline thin films. This is discussed in section 2.2.2.3 of the thesis and in [70], where it is shown that epitaxial films experience much less structural degradation during thermal cycling. Thus, the Freund-Nix model cannot be considered to produce a complete picture of the mechanical properties of thin films, but it still develops crucial ideas and concepts for understanding the mechanics.

3.2. LATTICE ROTATION BY DISLOCATION SLIP

As discussed in section 2.2.2.3, the texture of Al thin films plays an important role in fatigue development and it evolves in non-random ways during thermal excursions. This texture evolution can be understood by considering the dynamics of dislocation slip in the polycrystalline films. In most crystals, the primary deformation mechanism is slip. It can be described as shearing of atomic planes in crystallographic directions. The displacement during slip is always an integer number of interatomic distances, which means that a crystal is left without any dislocations if slip occurs for an entire crystal plane. However, if slip only occurs for a part of the plane, a dislocation will remain. As described in the previous section, these dislocations play a very important role in the mechanical properties of thin films. The lattice rotation can be also understood by invoking a more macroscopic level and only considering the resulting slip from the dislocations. For face-centered cubic (fcc) crystals, to which Al belongs, the slip directions are in the set $< 110 >$ and slip planes are in the set $\{111\}$[1] [78]. Due to symmetry reasons, this results in a total of twelve different slip systems. It is worth to note that the slip direction is the crystallographic direction with the lowest repeat distance, and the slip planes are densely packed planes. This pattern also largely holds for other crystal structures.

When a crystal is stressed, slip begins when the critical resolved shear stress value τ_c is reached. The necessary stress conditions for a slip in crystal in a uniaxial tension test along x can be explained by Schmid's law [78]

$$\sigma_x = \pm \tau_c / m_x, \tag{12}$$

where m is the Schmid factor, $m = \cos\lambda \cos\phi$, and λ and ϕ are the angles between the slip direction and tensile axis and slip plane normal and tensile axis, respectively. The geometry with specified directions and angles is shown in **Figure 20**(a). Slip always have a tendency to follow the highest Schmid factor. For a fcc crystal with the tensile axis in the primary triangle this results in the primary slip system $[101](11\bar{1})$, where $[101]$ is the slip direction and $(11\bar{1})$ is the slip plane normal [78]. Slip in crystals can cause a gradual change of the lattice orientation. Consider a single crystal in a tension test along the $[111]$ direction as showed in **Figure 20**(a). In this case the

[1] $\{hkl\}$ denotes the set of all planes that are equivalent to (hkl) by the symmetry of the lattice, and $< hkl >$ denotes the set of all directions that are equivalent to $[hkl]$ by symmetry.

slip will occur in the primary slip system and the angles will be $\lambda = 60^{o}$ and $\phi = 30^{o}$. If the ends of the crystal were allowed to move freely during the tension test as showed in **Figure 20**(b), the observed deformation would look like that occurring when one shears a stack of cards. In this case, a rotation would occur in regards to the tensile axis of the crystal because it rotates with the long axis of the crystal. The original direction of the tensile axis is indicated by the dotted line, while the tensile axis in the deformed state is indicated by the rotated arrow. In a real tension test, the tensile axis of the crystal will remain fixed and instead the slip plane normal and slip direction will rotate in regards to the tensile axis as illustrated in **Figure 20**(c). This also holds for polycrystalline materials albeit with higher complexity because a number of neighboring grains act as constraints for a given grain [136]. It should be noted that the angles λ and ϕ change during the deformation in the way that λ decreases and ϕ increases. Thus, the Schmid factor for different slip systems changes dynamically under the crystal deformation and rotation. The simplified illustration in **Figure 20** does not take this dynamic into account, because it only illustrates a single slip system.

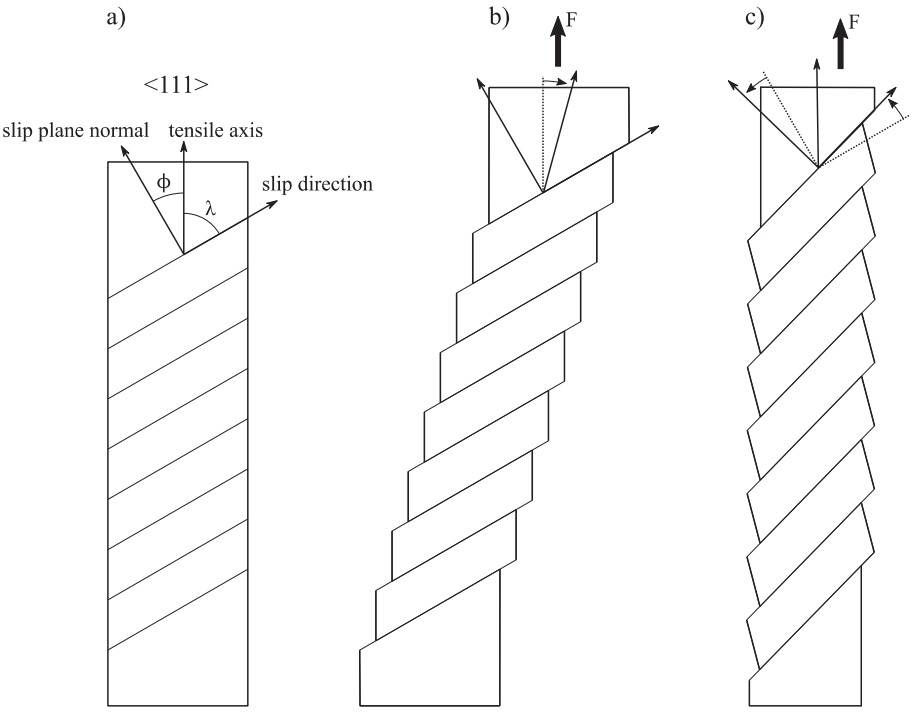

Figure 20. Illustration of rotation of fcc crystal structure by dislocation slip under a tension test with force F along tensile axis. a) Rod in rest with no applied tensile force, b) rod under tensile force with no constraint on movement in the horizontal axis, and c) rod under tensile force and constraint in the horizontal axis. Note that λ decreases and ϕ increases during the deformation.

To fully calculate the resulting rotation for a crystal in a tension test one must consider all possible slip conditions and calculate Schmid factors for all slip systems. This is not very complicated, but a time consuming and tedious procedure. Therefore, only main results of this calculation (see [78] for details) are presented in **Figure 21** showing all slip systems of a fcc crystal in a stereographic projection along with the naming convention for the different stereographic triangles. When the tensile axis of a crystal lies within the primary triangle, the situation corresponds to maximum Schmid factor, and, thus, to the primary slip system $[101](11\bar{1})$. As the primary slip propagates, the tensile axis rotates towards the $[100]-[111]$ symmetry line as shown in **Figure 21**(b). The simultaneous slip in the conjugate system $[110](11\bar{1})$ and the primary system $[101](11\bar{1})$ moves the tensile axis along the $[100]-[111]$ symmetry line, until a final and stable orientation at $[211]$ is reached (see **Figure 21**(b)). The $[311]$ orientation is also presented in **Figure 21**(b) because it plays an important role in regards to the results presented in section 5.3. The rotation towards the $[100]-[111]$ symmetry line has been verified experimentally by *in situ* measurements of grains during tensile test in an aluminum polycrystalline material [136]. The orientation of single embedded grains is measured by diffraction of focused hard X-rays. However, no results regarding the stable $[211]$ orientation is provided and it remains unclear whether this prediction is correct.

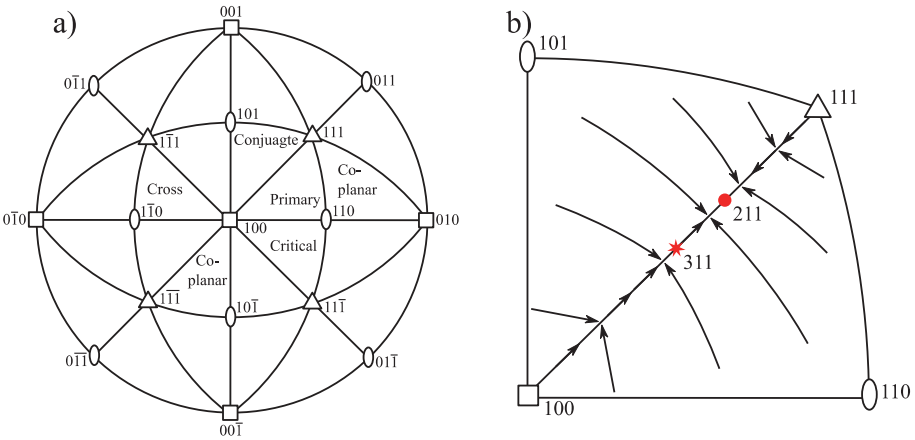

Figure 21. a) Naming convention and slip systems for fcc crystal presented in a stereographic projection. b) Conjugate and primary triangles demonstrating the tensile axis rotation towards $[100]-[111]$ symmetry line with stable orientations $[211]$ and $[311]$.

CHAPTER 4. SAMPLE PREPARATION AND CHARATERIZATION METHODS

In this work, the experimental research is mainly focused on the study of structure and composition of thin metal layers used in packaging of power electronic modules. The first topic is related to degradation of Al metallization films on top of semiconductor dies which is investigated using different accelerated tests in order to clarify the main stressors and failure mechanisms, thus, addressing reliability of such interconnects. The second main subject addresses the power module reliability related to the properties of baseplates, in particular, the development of new interconnect technologies utilizing TLP for bonding of DBC to baseplate and formation of hybrid metal baseplates.

Thus, two types of samples are under the investigation: (i) commercial silicon dies with thin Al metallization films and (ii) specially produced Cu-Sn-Cu, Cu-Sn-Mo, and Cu-Sn-Ag-Mo sandwich structures. The details about the sample preparation, used accelerated tests, and methods of the study are presented in this chapter.

4.1. TESTING AND CHARACTERIZATION OF DIODE METALLIZATION

Degradation of Al metallization is induced by passive thermal and active thermal (power) accelerated tests, which are described in details below. The change of structure and composition of the Al layers is studied using a number of characterization methods also described in this section.

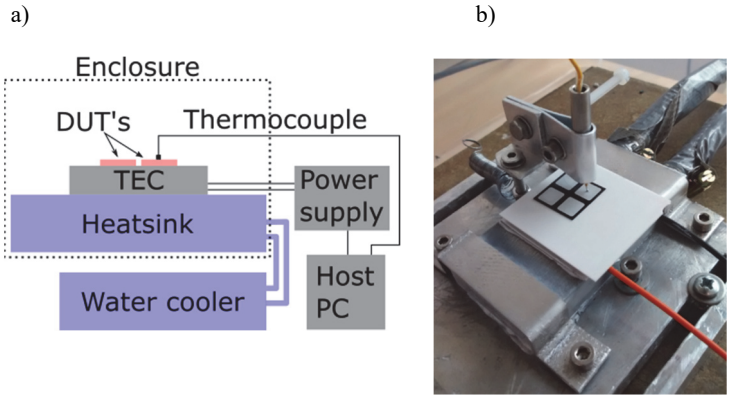

Figure 22. a) Schematic picture of the passive thermal cycling setup (reprinted from paper in appendix F with permission), and b) photo of the setup.

4.1.1. THERMAL CYCLING SETUP AND TEST CONDITIONS

As described in appendices A, B, and F, the thermal cycling setup is based on a digitally controlled thermo-electric cooler (TEC). The bottom side of the TEC is connected to a water cooled Al block and the top side is used to thermally cycle the samples. The TEC and heatsink are placed in an air-tight plastic enclosure that provides the possibility to purge the setup with different gases, for example, nitrogen which is used in the current study. A schematic picture and photo of the setup are shown in **Figure 22**. Temperature measurements are carried out by placing a thermocouple in direct contact with center of one of the devices under test (DUT) as can be seen in **Figure 22**(b). The samples are placed directly onto the TEC without any TIM to avoid contamination of the metallization during handling and measurements. The homogeneity of the temperature distribution on the surface of TEC is found to have variations within ± 2ºC across the entire surface. However, during experiments the thermocouple is attached to small central area of a DUT and no measurable temperature variations between central areas of different DUTs is found.

The control of the voltage applied to the TEC, and thus the temperature, is performed by an Arduino Uno, a L298N dual full-bridge driver, an AD623 instrumentation amplifier, a 19.5 V - 3.9 DC power supply, and a k-type thermocouple. The setup is run using a specially prepared MatLab script. The voltage from the DC power supply to the TEC is supplied through the L298N, which functions as a PWM chopper, thus allowing for both the control of the voltage level and reversal of the voltage polarity. The L298N is indirectly controlled by the Arduino Uno, which has the connection to a personal computer (PC) with MatLab script that acquires data and sets the wanted parameters. Both outputs from the L298N to the TEC features a low pass RCL filter to smooth out the PWM signal and provide the TEC with a ripple free voltage. Using a shunt resistor and the sense leads on the L298N together with the AD623 the amount of current running through the TEC is acquired by an analog input pin on the Arduino Uno and transmitted to the PC. The PC also acquires the temperature reading from the thermocouple registering the temperature of the TEC or sample surface. This allows for the total control of the temperature cycles. A simplified scheme of the electronic control is shown in **Figure 23**.

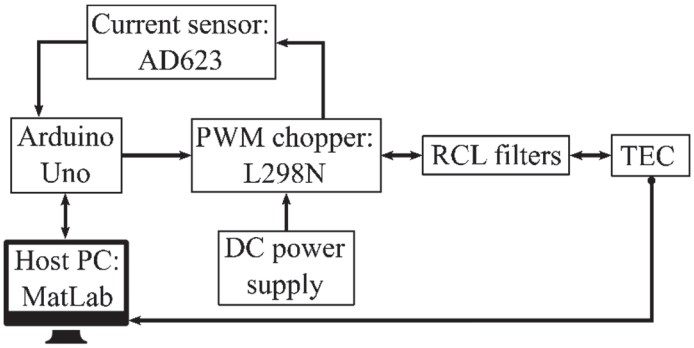

Figure 23. Simplified scheme of the electronic and thermal control of the thermal cycling setup.

For passive thermal cycling, all DUTs are high power Infineon diode chips (100 A, 1200 V). The chips have dimensions 9×9 mm and a topside Al metallization with a thickness of 3.4 μm. The thermal waveforms are chosen to be triangular with a period of approximately 26 seconds, a minimum temperature T_{min} =25 ºC, and a maximum temperature T_{max} = 105 ºC, thus resulting in mean temperature of 65 ºC and a temperature variation ΔT = 80 ºC. The profile of the thermal cycles is shown in **Figure 24**.

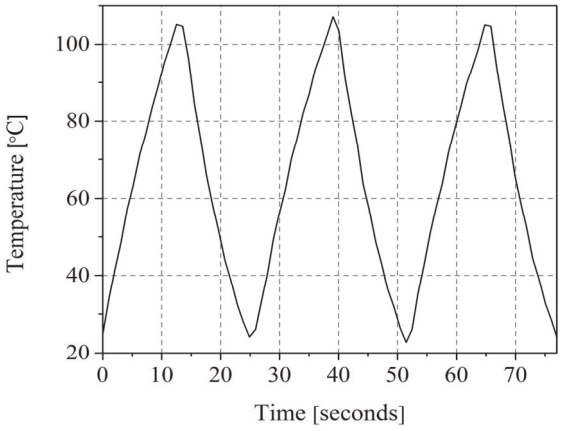

Figure 24. Typical profile of thermal cycles with T_{min} =25 ºC and T_{max} = 105 ºC. The period of one cycle is approximately 26 seconds. Reprinted from paper in appendix A with permission.

For the first series of experiments (see appendix A) the cycling is performed under a continuous flow of pure (99.999%) nitrogen into to the enclosure of the setup. The nitrogen gas substitutes the ordinary atmospheric air that decreases relative humidity (RH) to a zero value. Thus, these experiments are intendent to eliminate the effect of oxidation and possible contribution of corrosion into the metallization fatigue. In the next series of experiments, as described in appendices C, and F, the cycling is carried

out in an ordinary atmosphere with a controlled relative humidity (RH) of 50±5%. This is reached by opening the enclosure of the setup and placing it in the cleanroom where RH is under precise control. Finally, as described in appendix C, a set of data is obtained for thermal cycling in an ordinary atmosphere with RH of 95%. This is performed by placing the opened setup it in a climatic chamber (Vötsch VCL7010). During all these tests, the DUTs are taken out from the setup on reaching a certain number of cycles to perform the characterization and then returned to continue cycling.

4.1.2. POWER CYCLING ACCELERATED TESTS

For active thermal cycling, also known as power cycling, two different tests are run. Both power cycling tests are performed with assistance of Postdoc Kristian Bonderup Pedersen.

4.1.2.1 DC pulse test

The DC pulse test is a current load procedure, according to test standards described in [137], where the device is heated by ohmic losses from a DC current. In this test, the DUTs are half-bridge 300A device with 3 parallel sections consisting of two IGBT chips and two diodes each. The semiconductor devices are backside soldered to a Al_2O_3 DBC and topside bonded with heavy Al wires and the chips have a standard 3.4µm Al metallization layer. Before the test, the silicone gel is dissolved to allow for sheet resistance measurements in between the power cycling steps. The diodes are acting passively and any load variation is induced externally, thus, the current amplitude, cooling temperature, and on/off time are the primary control parameters. The DC test is performed with a set of parameters to obtain an initial ΔT of approximately 50 ºC for non-degraded devices. Additional details can be found in section II.B of appendix F.

4.1.2.2 Sinusoidal current load

The second power cycling test is carried out with a sinusoidal current load. In this test, the DUTs are standard half-bridge IGBT modules consisting of six parallel IGBT chips each with a freewheeling diode. IGBTs and diodes are topside connected with heavy Al bond wires and backside soldered to a standard Al_2O_3 based DBC substrate. These semiconductor chips also have standard 3.4 µm thick Al metallization layer. The modules are power cycled actively with a current of 890A at 6Hz switched at 2.5kHz with a DC-link voltage of 1000V. As one of the main accelerators, the baseplate of the DUT is subjected to an elevated temperature of 80 ºC. The mean temperature of the diodes is online estimated and simulated to be approximately 112 ºC with a ΔT of around 36ºC, which results in a maximum junction temperature of 130ºC. More details about the test procedure can be found in [22], [23], and section II.B of appendix F.

4.1.3. SHEET RESISTANCE MEASUREMENTS

As described in appendix A, the sheet resistance is measured using the van der Pauw method [138]. This is a well-established four-point measuring technique that removes the influence of contact resistance and ensures repeatability and very low relative uncertainties in the range of ±0.1%. When performing this type of measurement, four electrical probes are placed in each corner of the metallization. The current is applied to two probes on the same side while the voltage is measured across the two probes on the opposite side. To remove potential offsets, *I-V* curves are measured with the current varying between −100mA and +100mA in 20 steps and then the resistance is found as the slope of this curve. For all DUTs, the initial value of the sheet resistance, R_0, is determined and used to calculate the relative sheet resistance R/R_0. This is necessary since all DUTs have slightly different initial values varying between 27-29 nΩ·m. Details about the sheet resistance measurements on the power cycled samples can be found in appendix F.

4.1.4. SEM, FIB AND EDX

SEM and focused ion beam (FIB) milling is used to examine the topography and microstructure of the metallization layers, while energy-dispersive X-ray spectroscopy (EDX) is applied to study the chemical composition. All SEM, FIB and EDX are performed using a Zeiss 1540 XB system. Electron energy for SEM is in the 10kV range and the Ga ions used for FIB have an energy of 30kV. Typically, ion currents around 2 nA are used for removal of bulk material and currents of 100pA - for the final polishing step of the cross-section. EDX data capture and analysis are performed using the NSS3 X-ray microanalysis software from Thermo Fischer Scientific Inc. The accelerating voltage of the electron beam is 10 kV, which according to the simulations corresponds to a maximum penetration depth of approximately 1 μm. Each measurement is performed with a detector live time of 60 s assuring an adequate amount of data.

4.1.5. EBSD

EBSD is used to examine the texture and grain structure of the metallization layer. As described in appendix E, all EBSD measurements are performed with a step size of 0.25 μm on an area of 100 μm× 100 μm. FIB milling is used to form alignment crosses on the surface such that the same area can be found and measured in a reproducible manner. This allows to address the evolution of the same grains after the thermal cycling. The data analysis and production of pole figures is reached using the openly available MTEX Toolbox [139] for MatLab. To filter out noisy data points, a median smoothing algorithm with a 3 × 3 window is applied. For the grain analysis, the grain angle separation is chosen to be 5º.

4.1.6. XRD

X-ray diffraction (XRD) is used to examine the crystallographic texture of the metallization layer. As described in appendix E, the XRD measurements are carried out using PANalytical Empyrian X-ray diffractometer. All 2θ-scans are done in-house, while all data for pole figure plots are obtained with assistance from the X-ray center of TU Wien.

4.2. FABRICATION AND CHARACTERIZATION OF TLPB JOINTS

The study of TLPB interconnects and hybrid metal baseplates considers the necessary fabrication methods and parameters for producing strong joints using Cu-Sn-Cu, Cu-Sn-Mo, and Cu-Sn-Ag-Mo sandwich structures as well as following characterization. It is performed as a part of a three month stay abroad at the Department of Mechatronics, University of Applied Sciences Kiel.

4.2.1. SAMPLE FABRICATION

4.2.1.1 Cu-Sn-Cu samples

A detailed description of the Cu-Sn-Cu TLPB sample fabrication procedure can be found in appendix D. Using a combination of commercially available uncoated Cu and 5 µm Sn-coated Cu plates, the Sn interlayer thickness of the samples can be chosen to be either 5 µm or 10 µm. Larger Cu plates (20 mm × 20 mm × 1 mm) are populated by a number of smaller Cu plates (2.3 mm × 2.3 mm × 0.8 mm), thus, allowing for simultaneous fabrication of many samples with the same fabrication parameters. This is important for statistical reasons. After placement of nine small Cu pieces onto the larger Cu plates the samples are processed in an air-driven 100 ton TOX press (see **Figure 25**) that provides a maximum pressure of 25 MPa. To provide quasi-hydrostatic pressure at the samples, a hard bottom tool and a soft silicone top tool are used. This also alleviates any differences in the pressure due to sample alignment issues. The tools can be seen in **Figure 26(**a) before pressure is applied and in **Figure 26(**b) after pressure is applied. The tools of the press are preheated before placement of the samples and after the bonding procedure the pressure is released without an intermediate cooling stage. Thereafter, the samples are removed as quickly as possible to cool down on a metal surface. Thus, a given bonding time corresponds to both the time at which a sample was under pressure and at elevated temperature, which is illustrated in **Figure 26**(c). **Figure 26**(d) shows the different phases during the TLP bonding process (see appendix D for detailed explanation).

4.2.1.2 Cu-Sn-Mo and Cu-Sn-Ag-Mo samples

The Cu-Sn-Mo and Cu-Sn-Ag-Mo sample fabrication is carried out in the same manner as for the case of Cu-Sn-Cu samples described in the previous section. They

are produced using a combination of commercially available Sn- and Ag-coated Mo plates with lateral dimensions of 20 mm × 20 mm and thickness of 0.8 mm. Both types of Mo plates have a thin Ni interlayer for better adhesion of Sn or Ag. Small pieces of bare Cu or Cu coated by Sn with dimensions of 2.3 mm × 2.3 mm and thickness of 0.8 mm are placed on the above-mentioned large plates. The thickness of Sn layers on both the Cu and Mo plates is approximately 5 µm. The samples are bonded in an air-driven press with a pressure of 25 MPa and temperature of 255 ºC according to the procedure described in appendix D. Three sample types are fabricated: i) Cu-SnMo (using uncoated Cu on Sn-coated Mo), ii) CuSn-SnMo (using Sn-coated Cu on Sn-coated Mo) and iii) CuSn-AgMo (using Sn-coated Cu on Ag-coated Mo). To find the optimal TLP bonding parameters, the strength of the formed interconnects is measured by a standard shear test procedure applied to the small bonded pieces.

Figure 25. The 100 ton TOX air-driven press used for sample fabrication.

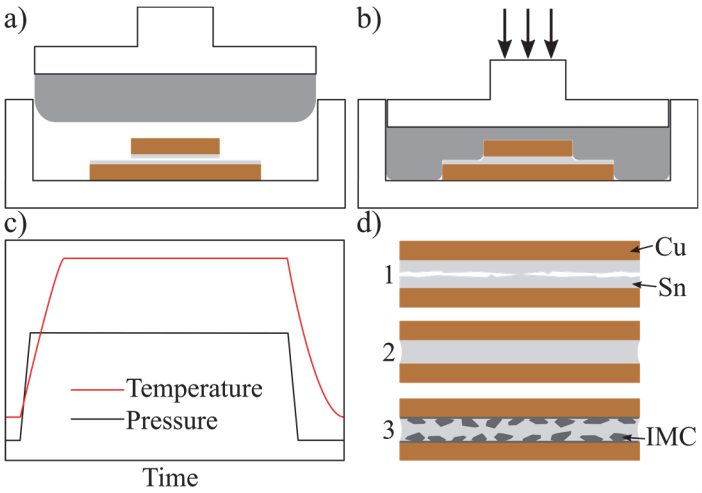

Figure 26. Schematics of the fabrication procedure. a) Samples placed on the hard bottom tool before pressure is applied, b) soft silicone (grey in color) applies hydrostatic pressure to the sample during bonding, c) illustration of the temperature and pressure profile during the bonding procedure. d) Illustrates three different phases during the TLP bonding process, 1 - contact phase, 2 - melting phase, and 3 - IMC formation and solidification. Reprinted from appendix D with permission.

4.2.2. SHEAR TESTING

To examine the strength of the fabricated bonds, a shear test is applied to the samples bonded under different conditions. Using data of these measurements the optimal TLP bonding parameters are found and used for the fabrication of final series of samples for further structural and compositional analysis. The shear testing is carried out using a XYZTEC Condor Sigma series bond tester. More details about shear test conditions and optimization procedure can be found in appendix D.

4.2.3. MICRO-SECTIONING, SEM AND EDX

To reach the interfaces of interest and perform analysis (e.g. optical microscopy, SEM, and EDX), micro-sectioning is applied. The micro-sectioning is performed using a standard in-house procedure that consists of several steps. First, the samples are molded into epoxy and then cut roughly at the interface of interest. Afterwards, several polishing steps going from large grit to fine grit sanding paper are done before a final chemical polishing step is applied. More details about the procedure can be found elsewhere [33]. SEM and EDX are applied using the same setup and procedure as described in section 4.1.4 only with a higher electron energy of 20 kV. Additional details can be found in appendices D.

4.2.4. THERMAL SHOCK CYCLING AND SAM

As described in appendix D, thermal shock cycling is performed on samples represented by TLP bonded 20 mm × 20 mm Cu plates (with Sn interface layer) on standard Al_2O_3 based DBCs. For comparison, similar samples only with silver sintered interconnects are also fabricated (see appendix D for further details). The thermal test is achieved using a standard procedure in the temperature range from -40 ºC to +150 ºC and a cycle period of 60 min. To follow the evolution of the TLP bonded interfaces before and after thermal shock cycling, scanning acoustic microscopy (SAM) measurements are carried out using a 500 MHz transducer on a KSI V8 scanning acoustic microscope. The spot size of the ultrasonic beam is approximately 100 μm at the focal plane. A trigger is set using the first reflection from the top of the sample and gates are created at the interfaces of interest.

CHAPTER 5. METALLIZATION DEGRADATION OF POWER DIODES

This chapter will cover the studies carried out on degradation of power diode metallization. The published papers presented in appendices A, B, C, E, and F will be used as the basis for the discussion.

5.1. TOPOGRAPHICAL AND MICROSTRUCTURAL EVOLUTION

5.1.1. RESULTS

Thermal cycling of the first set of samples is carried out in nitrogen atmosphere (see appendix A for details). To investigate the structural changes and to link them to the changes in metallization resistance, SEM analysis accompanied by FIB milling is performed for the samples reached a certain number of cycles. The change of the surface morphology of the metallization is presented in **Figure 27**. It can be seen that the surface roughness increases significantly with the number of thermal cycles. In the beginning, the change is mostly limited to the very surface layer (see **Figure 27**(a,b)), while at the later stages the topography is severely altered and one can see large protrusions and deep pits in the metallization (see **Figure 27**(c,d)). The surface images are supported by cross-sectional views of the metallization that are presented in **Figure 28** and **Figure 29**. It can be observed that at the initial state, the layer is crack and void free (see **Figure 28**(a)), but as the thermal cycling is in progress, cracks and voids start developing near the surface of the layer (see **Figure 28**(b,c)). As evident from **Figure 29**, these cracks and voids can reach all the way down to the Si die at the later stages (145 kilocycles), thus breaking the continuity of the film. These structural changes lead to increase of resistance as will be shown in section 5.2.

To study the influence of varying atmospheric conditions on the metallization degradation phenomena, thermal cycling in ambient atmosphere with RH=95% and RH=50% is performed (see appendices B, C, and F). It is found that the changes in topography and microstructure observed by SEM look very similar to those for the samples cycled in nitrogen. In **Figure 30**, the surfaces of the metallization and in **Figure 31**, the cross-sections are presented. With increased number of cycles, the Al layers undergo severe reconstruction showing significant surface roughening (see **Figure 30**(a,b)) as well as void and crack development (see **Figure 31(**a,b)).

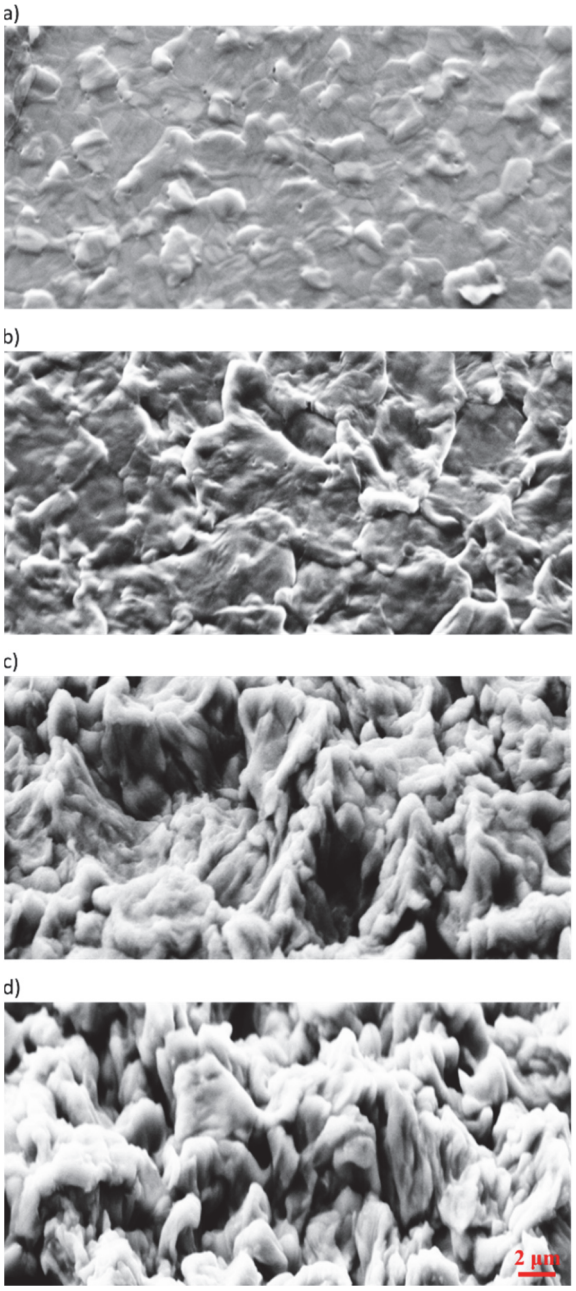

Figure 27. SEM images of diode metallization cycled in nitrogen atmosphere: a) a new diode, b) a diode after 12.5 kilocycles, c) a diode after 45 kilocycles and d) a diode after 145 kilocycles. The scale is the same for all images and shown in d). Reprinted with permission from paper in appendix A.

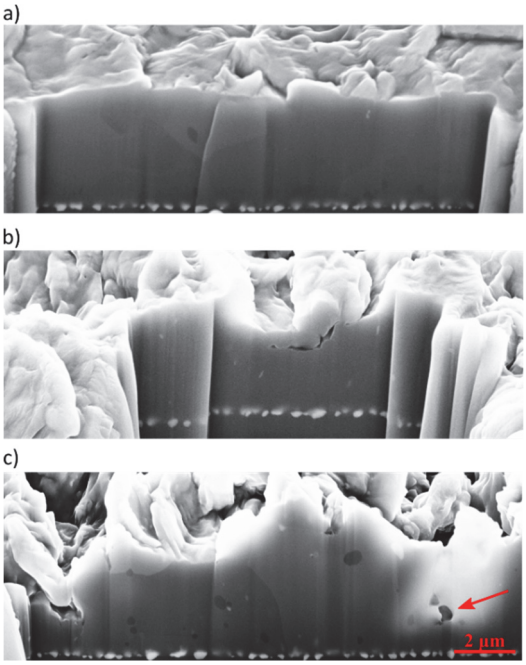

Figure 28. SEM images of diode metallization cycled in nitrogen atmosphere with wells obtained by FIB milling for a) a diode after 25 kilocycles, b) a diode after 45 kilocycles and c) a diode after 145 kilocycles. The arrow in c) indicates one of the cavities. The scale is the same for all images and shown in c). Reprinted with permission from paper in appendix A.

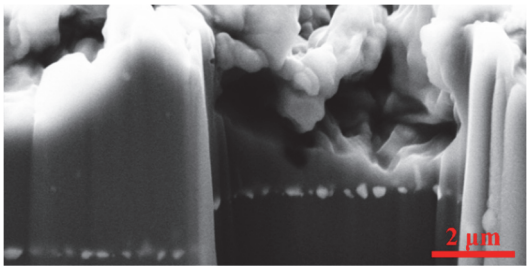

Figure 29. SEM image of diode metallization with additional milling of the area indicated by the red arrow in Figure 28(c). Reprinted with permission from paper in appendix A.

To compare the degradation under pure thermal cycling with that occurring under the electric power load, SEM images of the metallization of diodes subjected to sinusoidal current load are acquired and presented in **Figure 32**. A similar type of topographical and microstructural change to that of thermally cycled samples can be observed.

5.1.2. DISCUSSION

It is found that the passive thermal cycling under different atmospheres and the active power cycling result in a very similar change of the metallization structure. Since the passive cycling test excludes any contribution from electric current, this suggests that the dominant mechanism of the restructuring is a thermo-mechanical stress. This conclusion is also supported by the models based on dislocation plasticity that are presented in section 2.2.2.3 and Chapter 3. Since these models are based on dislocation slip as the primary deformation mechanism, one could expect to see glide steps and terraces on the surface of the metallization, as illustrated in **Figure 14**. These effects, however, are not observed and this may be explained by considering the following suggestions. First, the $T_{\max} = 110$ ºC of the passive thermal experiments is much lower compared to temperatures used in other studies (up to 450 ºC) where the glide steps have been observed [68]. Thus, in our case one should expect less pronounced glide steps, which are not clearly distinguishable. Second, in the experiments described in [68] the films were continuously and relatively slow heated up to the maximal temperature and then slowly cooled down. While in our case the heating and cooling occurs on the scale of 25 s, thus the tensile stress is followed by the compressive phase when some reverse slip could occur (see section 2.2.2.3 for details) and partly remove the initial glide step or even introduce some other type of defect. Thus, combination of these phenomena can produce much more chaotic surface structures where individual glide steps and terraces are hardly distinguishable.

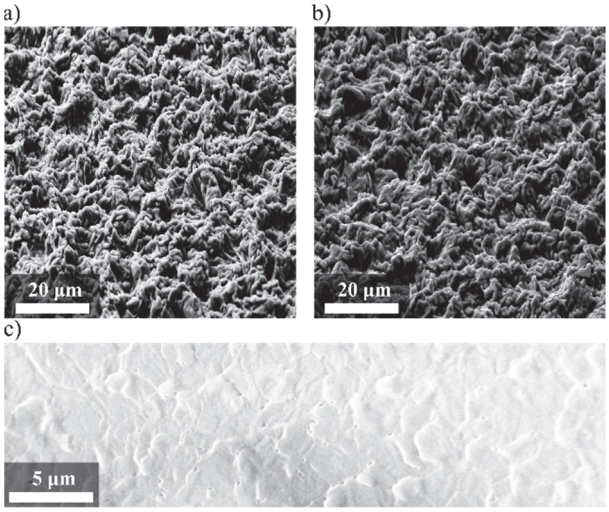

Figure 30. SEM images of diode metallization cycled in ambient atmosphere: a) after 93 kilocycles at RH=95%, b) after 110 kilocycles at RH = 50%, and c) of an uncycled sample for the comparison. Reprinted with permission from paper in appendix C.

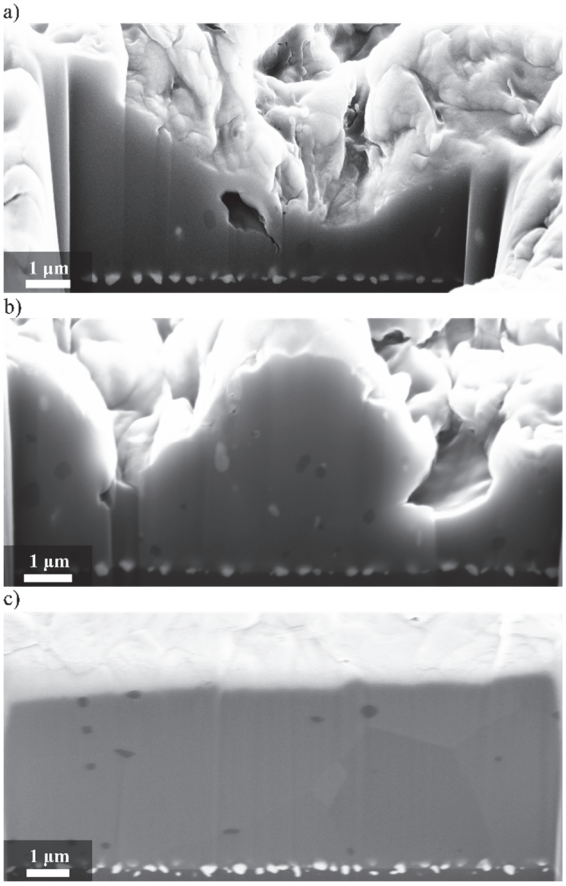

Figure 31. Cross-sectional SEM images of diode metallization with wells obtained by FIB milling for samples a) after 93 kilocycles at RH=95%, b) after 110 kilocycles at RH=50%, and c) an uncycled diode. Reprinted with permission from paper in appendix C.

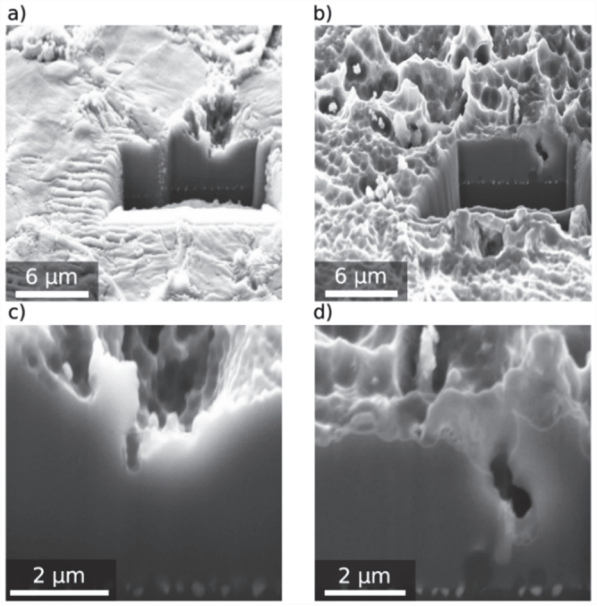

Figure 32. SEM images of metallization for diodes that are power cycled with a sinusoidal load current. a) Surface after 2.5 mega- cycles, b) Surface after 4.5 megacycles, c) cross-section after 2.5 megacycles, and d) cross-section after 4.5 megacycles. Reprinted with permission from the paper in appendix F.

5.2. DEGRADATION OF ELECTRICAL PROPERTIES

5.2.1. RESULTS

To get information on degradation of electrical properties of the diode metallization, sheet resistance measurements are carried out (see papers in appendices A, B, C, and F). The evolution of the sheet resistance for diodes cycled in the ambient atmosphere with different humidity and in nitrogen is shown in **Figure 33**. It can be seen that the sheet resistance increases in a non-linear manner with the number of cycles.

This increase can be attributed to the observed topographical and microstructural changes discussed in section 5.1. Different phases in the evolution of the sheet resistance in **Figure 33** can be distinguished. A phase 1 from 0 to 20 kilocycles shows little to no change, a phase 2 from 20 to 120 kilocycles demonstrate the most severe change, while a phase 3 above 120 kilocycles shows a more moderate change of the resistance. This type of behavior with different phases agrees with earlier results for actively cycled devices [59], [64], [65], [67] (see section 2.2.2.2 and **Figure 10**). The data imply that the cycling in dry nitrogen atmosphere yields a faster degradation rate than that in ambient atmosphere with RH=50%. For the case of RH=95% (not

presented in the figure, see for details appendix C), the results are similar to those for RH=50%.

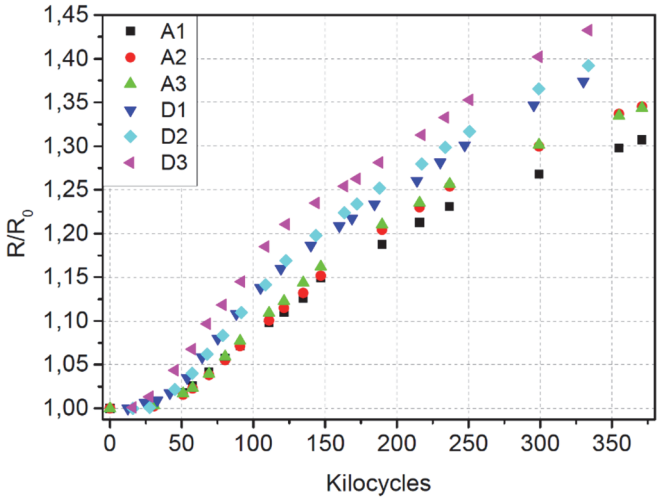

Figure 33. Relative sheet resistance of diode metallization as a function of number of cycles. A1, A2, and A3 correspond to diodes cycled in ordinary atmosphere at RH=50%, and D1, D2 and D3 correspond to diodes cycled in dry nitrogen atmosphere. Reprinted with permission from paper in appendix F.

In order to better understand the observed difference in resistance change under different atmospheric conditions, EDX measurements are carried out. In particular, the amount of oxygen in the Al layer is measured. The results for the diodes cycled in ambient atmosphere with different RH are shown in **Figure 34**. It can be seen that the oxygen content in the metal layer gradually increases with number of cycles and it rises faster for RH=95% than for RH=50%. The amount of oxygen in metallization for the diode cycled in dry nitrogen atmosphere is measured only once at the very end of cycling (after 335 kilocycles) and found to be 0.5%.

The changes in relative sheet resistance of metallization for actively power cycled diodes are presented in **Figure 35** and **Figure 36**. The results in **Figure 35** correspond to the DUTs subjected to the DC pulse load, while the data presented in **Figure 36** are for the samples cycled by the sinusoidal current load as described in section 4.1.2. The resistance evolution of DUTs under DC conditions (see **Figure 35**) resembles that of the passively cycled DUTs (see **Figure 33**) with indication of several phases. In the interval from 0 to 60 kilocycles the most severe increase can be observed, while from 60 kilocycles and above the change is more moderate. The relative increase reaches a maximum value of 23% at 360 kilocycles.

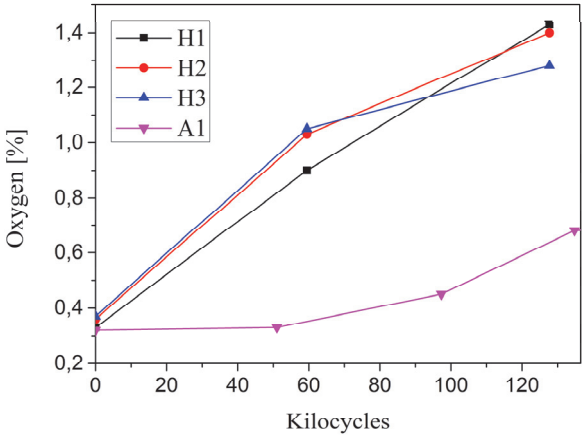

Figure 34. Amount of oxygen in the metallization of diodes cycled in ambient atmosphere. H1-H3 correspond to RH=95% and A1 to RH=50%. Reprinted with permission from paper in appendix C.

The change in the resistance in the case of sinusoidal current load can be seen in **Figure 36**. Similar to the above-discussed cases a rise in the sheet resistance can be observed. After 4.5 megacycles the value reaches a mean relative increase of 31%. It is not possible to distinguish any phases in the evolution, which is believed to be a consequence of only a few measurement points and the severe spreading in the data as the number of cycles increases. The larger spread in the values in the case of sinusoidal current load compared to the DC and passive tests is explained in the discussion section of the paper presented in appendix F and is attributed to higher system complexity under these power cycling conditions.

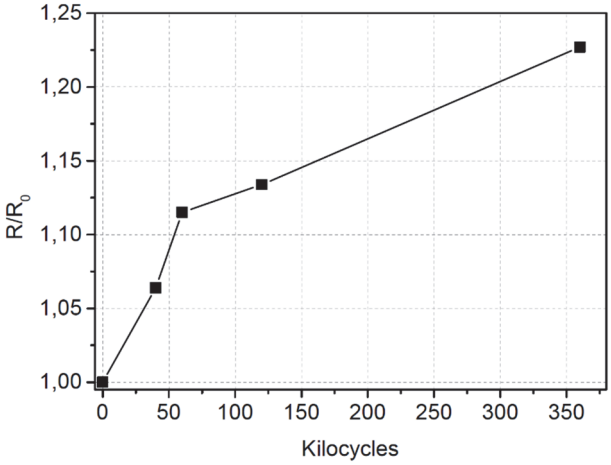

Figure 35. Evolution of relative sheet resistance of metallization for diodes cycled with DC pulse load. Reprinted with permission from paper in appendix F.

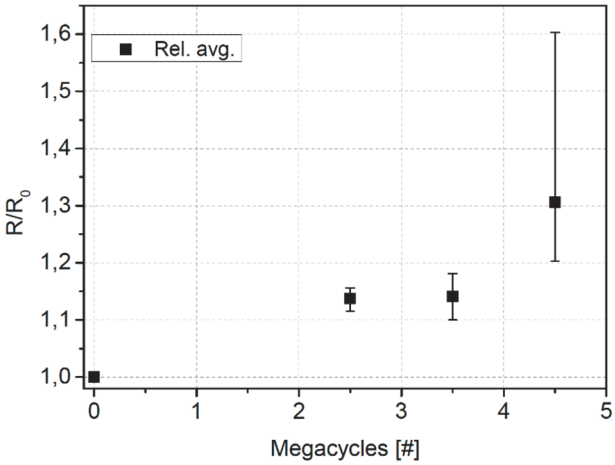

Figure 36. Evolution of relative sheet resistance of metallization for diodes under sinusoidal current load. Each solid square represents the average of the six different measured values, while the bars show the minimum and maximum of the measured values. Reprinted with permission from paper in appendix F.

5.2.2. DISCUSSION

The resistance of all metallization layers under the tests increases with number of cycles that shows good correlation with restructuring observed by SEM demonstrating surface roughening, formation and development of cracks and voids. This degradation breaks the layer continuity and decreases conductance. The resistance evolution of the thermally cycled samples shows three main phases, which are in very good agreement with those observed elsewhere and discussed in section 2.2.2.2 (see **Figure 10**). These phases correspond to different stages of structural degradation, namely: the stress accumulation in the beginning yielding small amount of defects and, thus, leading to very small rise of resistance; the phase of active formation of cracks, voids and other structural defects (for example, change of the texture which will be discussed below) causing the steep resistance increase and the last stage of gradual development of the degradation phenomena leading to further increase of resistance. These stages are well supported by multiple results obtained by SEM, some of which are presented in section 5.1 showing clear differences in structural degradation corresponding to different stages.

The above-describe general trends in evolution of resistance are also observed for our power cycled samples, except the first phase, which is not pronounced simply due to lack of analysis for the samples with low number of cycles. On the other hand, one can find a lot of data on power cycling in literature that makes no reason to repeat the already know tendencies. What was important in our case is to prove that the tendencies are the same for the passive thermal cycling and this goal is reached. This allows us to completely eliminate any major role of the degradation mechanisms of

electrical nature and to conclude that the thermo-mechanical stress is the dominant factor for the metallization reconstruction in the devices under operation.

Important insights about the role of environmental factors in metallization fatigue are obtained in the accelerated test run in different atmospheres. First, there is not any significant difference observed in the structural and electrical degradation of the layers cycled at different RH levels. This allows to conclude that presence of water vapor and related to that possibility of corrosion do not bring any considerable changes into the fatigue. Taking into account that the power modules are typically well protected by silicone gel, one can exclude the humidity factor from the stressors affecting the metallization degradation.

Cycling of the DUTs in nitrogen atmosphere brings some unexpected results, i.e. faster degradation of Al layers compared to ambient atmospheric conditions. EDX data show that oxygen value for the sample cycled in nitrogen atmosphere is significantly lower than the values found for the diodes cycled in ambient atmospheres. This low concentration value can lead us to the conclusion that oxidation of the metallization layers cycled in nitrogen occurs after the test when the samples are transferred to EDX measurements and exposed to ambient atmosphere. On the other hand, presence of oxygen during the cycling seems to affect the dynamics of structural evolution, in particular slowing down the electrical degradation.

The hypothesis is that the native oxides forming on the surface of film and at the crack tips produce a strengthening effect. This layer of native oxide constrains dislocation movement, as explained in the discussion sections of the papers presented in appendices C and F and section 3.1 of the thesis, and therefore increases the strength of the thin film. The higher strength ultimately leads to less fatigue damage and, thus a lower loss of the film continuity. However, this phenomenon requires more detailed study.

5.3. EVOLUTION OF FILM TEXTURE

5.3.1. RESULTS

To better understands the mechanisms of structural changes undergoing in polycrystalline metallization layers, the texture (crystallographic orientations of grains) is studied using XRD and EBSD. The results of the 2θ-scans by XRD for the DUTs cycled in ambient atmosphere at RH=50% and in dry nitrogen atmosphere are shown in **Figure 37**. It can be seen that in the uncycled films there is a very pronounced peak at an angle corresponding to the (111) orientation implying a dominant (111) texture of the metallization. As the number of thermal cycles increases, the peak intensity corresponding to the (111) orientation gradually decreases while other peaks corresponding to (200), (220) and (311) orientations give rise. This observation indicates that the thermal cycling has a strong effect on the

texture of the metallization. The tendency looks very similar for the cycling in different atmospheric conditions.

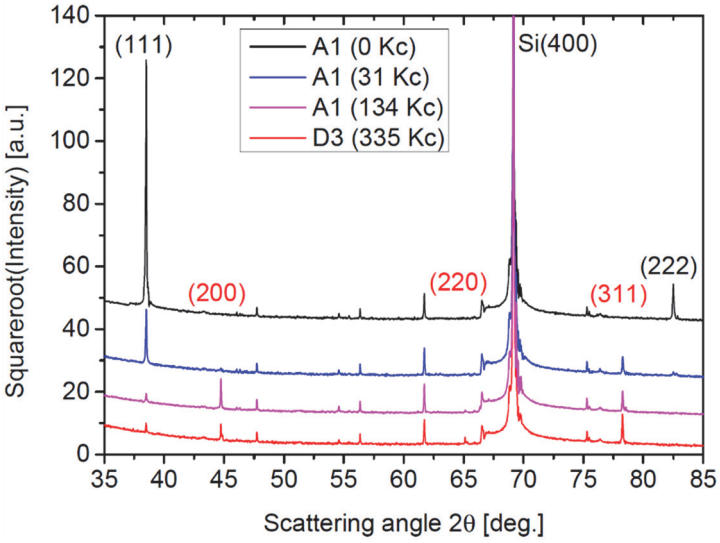

Figure 37. XRD scans for diode metallization cycled in ambient atmosphere at RH=50% (A1) and in dry nitrogen atmosphere (D3). The intensive peak at 68º and many small unlabeled peaks are related to the Si substrate. All peaks caused by the Al metallization are labeled with corresponding crystallographic planes. Black color indicates peaks that are decreasing in intensity during cycling while red color indicates peaks that are increasing. Reprinted with permission from paper presented in appendix B.

To further investigate the findings presented in **Figure 37**, which are based on the publications given in and appendices B and C, a separate study employing more advanced XRD measurements and EBSD analysis is carried out. The results from these investigations are largely self-contained in the published paper presented in appendix E and will, therefore, be only briefly overviewed below.

The XRD measurements are performed on a new diode and a diode after 317 kilocycles and shown in **Figure 38**. The data demonstrate a very clear (111) texture for the initial state of the metallization. However, when 317 kilocycles are reached this (111) texture is almost completely gone. Instead, a dominating (311) peak is evident. Earlier work [68] and the slip based model presented in section 3.2 predict a predominant evolution toward (211) texture. In order to see possible contribution of (211) orientation in our case, the pole figure for (422) is also included into **Figure 38**. The intensity in the center of the (422) pole figure stays almost constant under the cycling, which shows that no transition towards (211) texture occurs in our case.

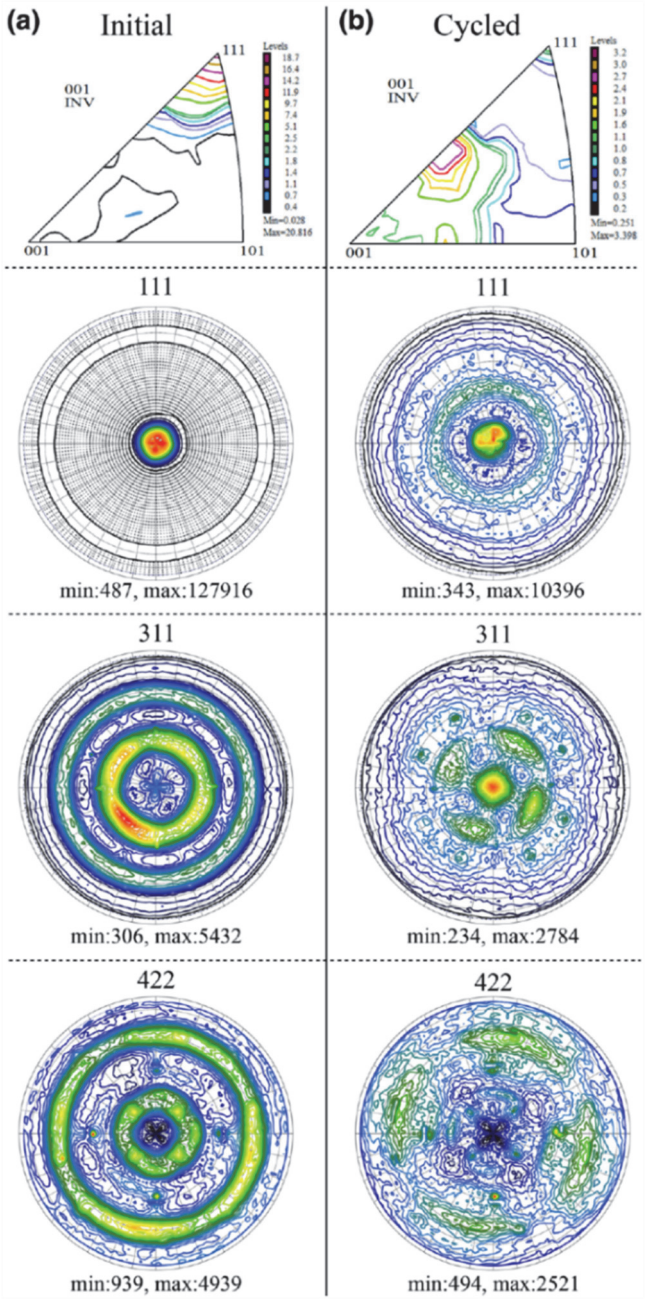

Figure 38. Inverse pole figures and pole figures extracted from XRD measurements: after a) 0 cycles and b) 317 kilocycles. The intensity of the contour plots of the inverse pole figures is given by the color bars in arbitrary units, while the minimum and maximum value are stated below every pole figure. Reprinted with permission from paper in appendix E.

To study evolution in orientation of individual grains, the same area of the metallization is studied by EBSD after a certain number of cycles. EBSD maps of the metallization can be seen in **Figure 39** showing that (111) texture dominates from 0 to 3433 cycles, although a clear change in the noise levels and microstructure can be seen as the number of cycles increases. The initial grain area distribution (grain size distribution) corresponding to EBSD map in **Figure 39**(a) is shown in **Figure 40**. Using the histogram in **Figure 40** the average grain size has been calculated to be 15 μm^2 yielding a diameter of 4.2 µm for a round shape approximation.

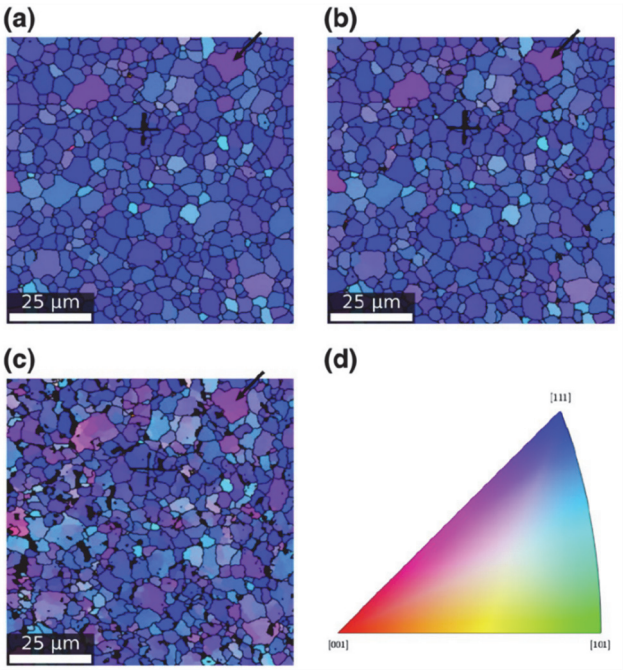

Figure 39. EBSD maps for diode metallization: after a) 0 cycles, b) 1353 cycles, and c) 3433 cycles. D) Shows the corresponding orientation coloring. The arrows in the EBSD maps indicate the grain for which the internal orientation gradients are analyzed (they are presented in Figure 42). Reprinted with permission from paper of appendix E.

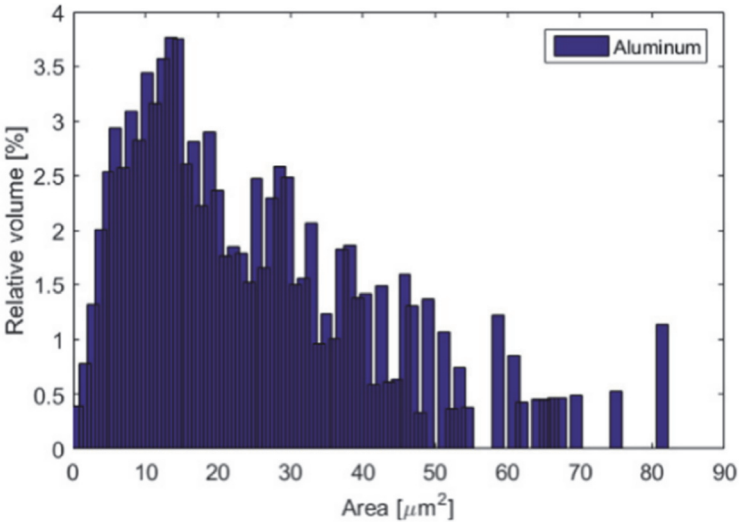

Figure 40. Histogram of the grain area for an uncycled diode extracted from the EBSD map shown in Figure 39(a). Reprinted with permission from paper of appendix C.

Pole figures and inverse pole figures extracted from EBSD measurements are shown in **Figure 41**. A pronounced (111) texture can be observed up to 5477 cycles, however the (111) signal becomes less intensive as the number of cycles increases.

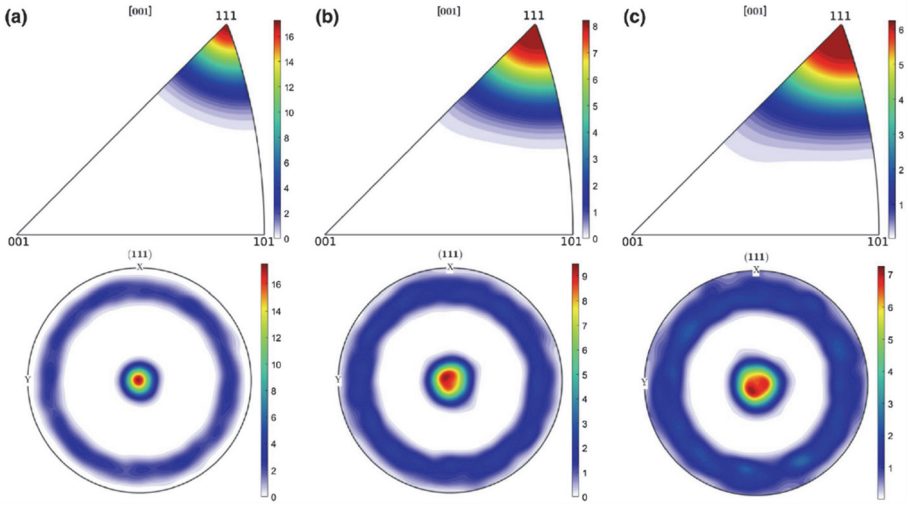

Figure 41. Inverse pole figures and pole figures extracted from EBSD maps: after a) 0 cycles, b) 3433 cycles, and c) 5477 cycles. The intensity of the contour plots is given by the color bars in arbitrary units. Reprinted with permission from paper of appendix E.

To further examine the dynamics of the reorientation, individual grains are tracked during the thermal cycling. One of the analyzed grains is presented in **Figure 42**. The grain is marked by an arrow in **Figure 39(**a-c). Initially, the grain has an internal misorientation of below 1º with respect to the mean orientation, which is indicated by homogeneous coloring in panel (a). As the number of cycles increases, the misorientation also increases, reaching values of over 8º after 5477 cycles.

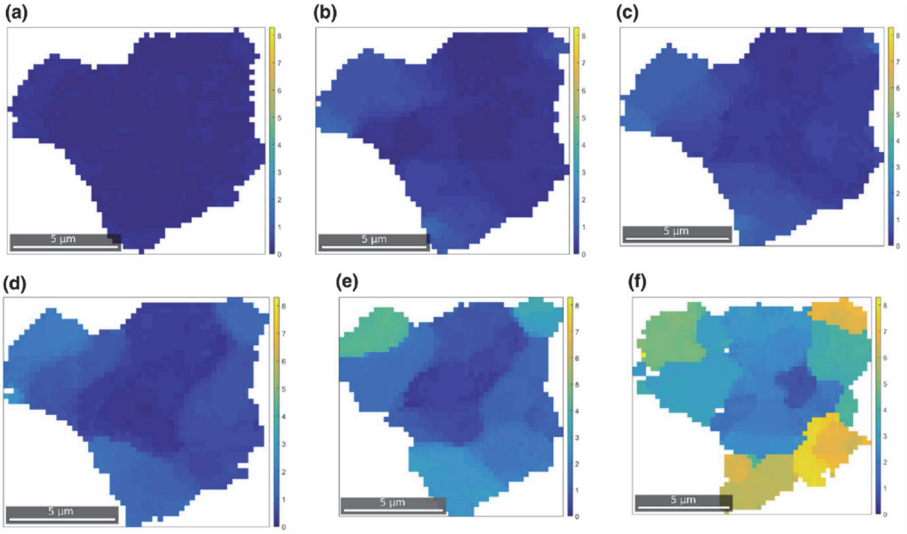

Figure 42. Orientation gradient within a single grain: after a) 0 cycles, b) 1353 cycles, c) 1985 cycles, d) 2527 cycles, e) 3433 cycles, and f) 5477 cycles. The color bar represents the misorientation angle from the mean orientation of the entire grain. Reprinted with permission from paper in appendix E.

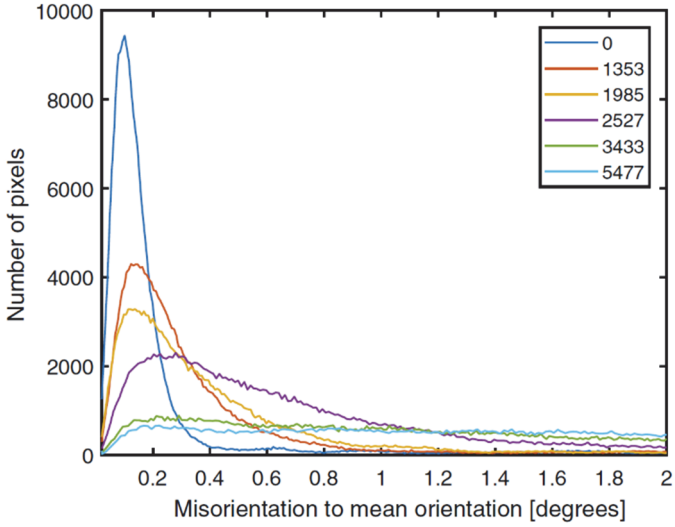

Figure 43. Change in grain misorientation to mean orientation with increasing number of cycles. The number of cycles is indicated by the legend. Reprinted with permission from paper in appendix E.

To get a more quantitative measure of the effect observed in **Figure 42**, an alternative approach is realized. This is presented in **Figure 43** as the misorientation angles from all pixels in the EBSD image with respect to corresponding grains. At 0 cycles, almost all pixels have a low misorientation of 0.1°. As the number of cycles increases, the peak significantly broadens and shifts towards higher values. After 3433 cycles an almost flat response can be observed. This indicates that all grains in area studied by EBSD undergo an evolution that is largely similar to that observed for the grain in **Figure 42**.

5.3.2. DISCUSSION

The results of texture analysis show that for the parameters used in the current thermal cycling test the mean orientation of grains in the film changes towards (311). This is not in agreement with the model presented in section 3.2 where a rotation towards (211) is expected. However, (211) and (311) spots lie relatively close and are both located on the $[100] - [111]$ symmetry line (see **Figure 21**(b)). Thus, the initial movement towards the symmetry line by the primary slip system, and the following movement along this line due to opposing slip in the conjugate slip system is in agreement with the model, and only the stable final orientation is different. One effect that is not included in the dislocation slip model is the constraint from the Si substrate. This is discussed in sections 2.2.2.3 and 3.1, and shown to play a major role in the dislocation activity, and, thus, in the strength evolution of thin films on rigid substrates (see **Figure 17**). It could, therefore, be suggested that the presence of the substrate constraint would change the dynamics of the activated slip systems in such a manner

that the stable orientation shifts from (211) to (311). This would illustratively mean that an additional constraint should be added to one of the sides of the rod in **Figure 20**(c) so that the glide is only permitted along one the sides making it similar to the illustration in **Figure 14**(b). However, further development of this new slip based model is required.

An alternative approach towards the explanation of the difference in stable dominating orientation of thermally cycled metal films can be made utilizing a simple model based on basic crystallography. This model explains the driving forces of the crystal reorientation by considering the packing density of different planes relative to {111}, which represents the highest atomic density for fcc crystals. As tensile and compressive stresses occur, the atoms will rearrange into planes with lower packing density due to lower work required to move the atoms in the plane (see discussion section of the paper in appendix E for additional details of the model). Since temperature under the test plays a defining role in the induced tensile and compressive stresses, different energy equilibrium states, and, thus, stable end orientations can occur at different temperatures. Thus, at thermal cycling in our case, which is performed up to only 110 ºC, the stresses can relax through the re-orientation to (311) plane which has packing density of 0.522 compared to (111). If the temperature rises up to higher values (400-450 ºC), as in the case presented in [68], the introduced stresses become higher requiring rotation to the orientation with even lower packing density, which is (211).

5.4. CONCLUSION

Based on the results presented in this chapter a few main conclusions about the degradation of Al metallization can be formulated.

One of the main well-grounded findings is that the restructuring and change of electrical properties of Al layers undergo in the same manner under the passive and active (power) thermal cycling tests, thus, allowing to exclude any considerable contribution of electric-related effects into the fatigue processes. The thermo-mechanical stress is the main factor affecting the metal film degradation and, thus, the reliability of this type of electrical interconnects.

The carried out research made considerable contribution into understanding of the physical mechanisms causing restructuring of the polycrystalline metal films under repeated mechanical stresses. It is found that crystallographic reorientation of individual micrograins, most probably through dislocation slips, is the main initial factor affecting the texture change of the entire film leading to high structural disorder under large number of repeated tensile and compressive stresses. The thermal cycling, which is carried out at temperatures realistic for ordinary device operation, showed for the first time that change of the Al film texture undergoes from dominating (111) orientation towards (311) but not towards (211), which is generally accepted in

literature as the end texture of polycrystalline metal films under thermal treatment. Two models are proposed for explanation of the difference considering the temperature factor and presence of substrate as a source of constraint.

It is found that penetration of oxygen into the granular Al layers under thermal cycling leads to lower degradation of electrical properties (slower resistance increase). The primary hypothesis is that the formation of thin oxide layer on Al surfaces of cracks and voids can increase the strength due to constrains on the dislocation movement, thus, slowing down reorientation of the grains, further crack development and general degradation of the film structure. However, these mechanisms require more detailed investigations.

CHAPTER 6. STRENGTH AND RELIABILITY OF TRANSIENT LIQUID PHASE BONDED INTERCONNECTS

This chapter will cover the studies carried out on TLPB as an interconnect technology in power electronics. Section 6.1 is based on the published paper presented in appendix D. The results from this investigation are largely self-contained in this paper, and will, therefore, be only briefly overviewed below. Section 6.2 presents original material on the Cu-Sn-Mo and Cu-Sn-Ag-Mo interconnects for emerging hybrid baseplate technologies.

6.1. TRANSIENT LIQUID PHASE BONDED CU-SN-CU INTERCONNECTS

6.1.1. RESULTS

Cu-Sn-Cu interconnects are produced according to the procedure described in section 4.2.1.1. One of the first steps was optimization of bonding pressure.

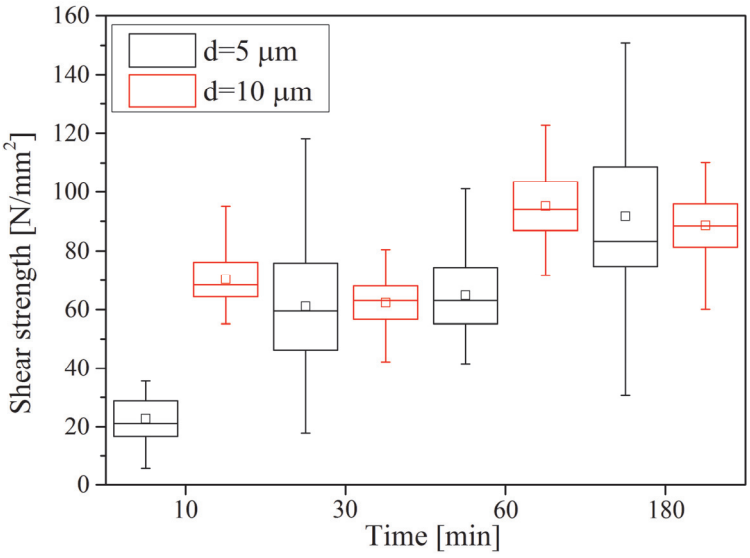

Figure 44. Shear strength of Cu-Sn-Cu samples for different bonding times, pressure of 25 MPa and temperature of 255 ºC. The squares represent the mean value, the lines correspond to minimum and maximum values and the box and line within represents the standard deviation and median value, respectively. The measurements are carried out for two thicknesses (d) of Sn layer of 5 and 10 µm. Reprinted with permission from paper presented in appendix D.

It was found that higher bonding pressure leads to stronger joints (see **Figure 3** in appendix D) with maximum shear values occurring for a value of 25 MPa. Thus, this parameter and the fixed temperature of 250 ºC are chosen for all following experiments in which the bonding time is varied. In **Figure 44,** the shear strength of the formed bonds as a function of time is presented. The shear strength increases with the bonding time reaching a maximum of 90-95 N/mm^2 after 60 min. These values are in agreement with or higher than the values published for Cu-Sn-Cu systems in literature [101], [103].

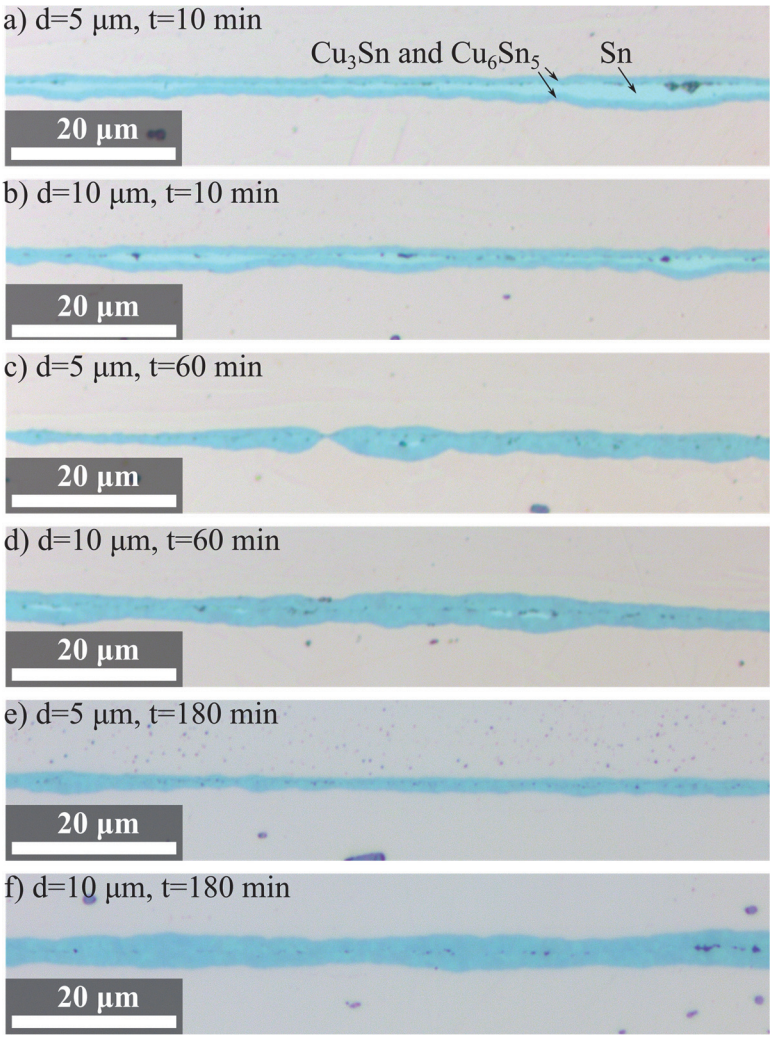

Figure 45. Optical micrographs of Cu-Sn-Cu interlayers for different bonding times (t) and interlayer thicknesses (d). Reprinted with permission from paper presented in appendix D.

Optical micrographs of the polished cross-sections of the Cu-Sn-Cu interfaces are presented in **Figure 45**. All interfaces show a number of smaller voids, which can be seen as dark spots in the bonded region. Their formation can be explained by contaminations and oxides present at the surfaces [103] or by the Kirkendall effect [140], [141] where different diffusion rates of Cu and Sn can cause voids. For the bonding time of 10 min (see **Figure 45**(a,b)) unconsumed Sn (light bluish color) can be seen in the middle of the interfaces (supported by EDX measurements). For longer bonding times (see **Figure 45**(c-f)) all Sn is consumed and only Cu-Sn IMCs are present.

EDX analysis for a sample with Sn thickness of 10 µm and a 60 min bonding time (see **Figure 45**(d)) is shown in **Figure 46**. It can be seen that the Sn rich Cu_6Sn_5 IMC are present at the center while the Cu rich Cu_3Sn IMC are predominately formed nearer to the Cu plates. Thus, the solid state diffusion process is not yet fully finished, i.e. the metals are not completely mixed. For a sample with similar bonding time but Sn thickness of 5 µm only the Cu_6Sn_5 IMC is found, that indicates good intermixing of Sn and Cu (see **Figure 5** in appendix D).

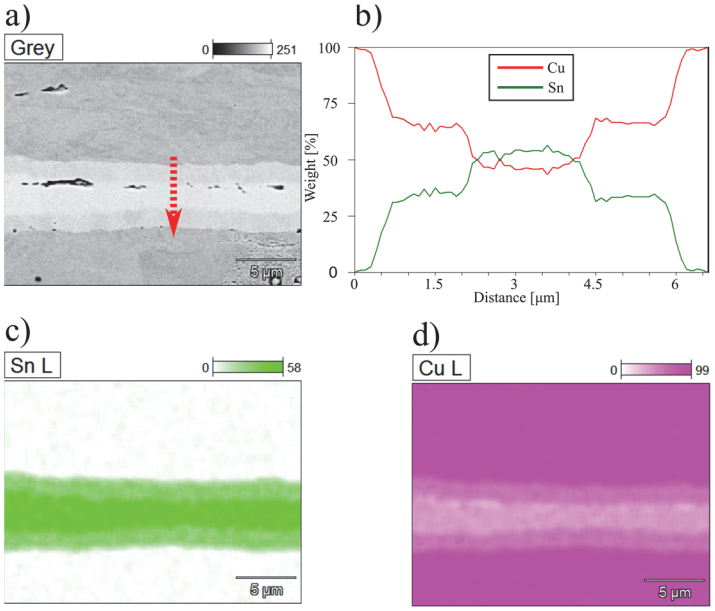

Figure 46. Results for sample with d=10 µm, bonding time of 60 min and pressure of 25 MPa. a) SEM image of the area examined by EDX, b) line scan along the direction indicated in a) showing composition of the interface, c) colour diagram for weight percent of Sn and d) colour diagram for weight percent of Cu. Reprinted with permission from paper presented in appendix D.

Results of SAM analysis of the thermally cycled samples can be seen in **Figure 47** (see section 4.2.4 for details about thermal cycling procedure and sample fabrication).

Overall, the TLP bonded samples show little to no change after 250 thermal cycles (see **Figure 47**(a,b)), thus, demonstrating higher robustness than the silver sintered samples which show delamination at corners (see **Figure 47**(c,d)).

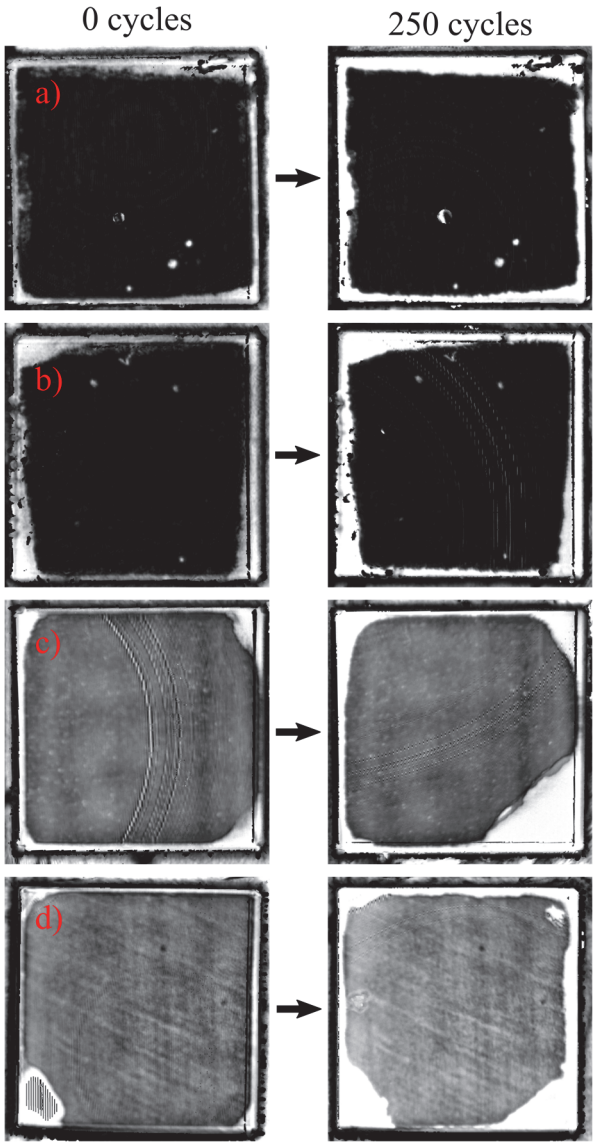

Figure 47. SAM images of two TLP bonded samples (a,b) and two silver sintered samples (c,d) at 0 and 250 thermal cycles. The arcs seen on c) at 0 cycles and b) at 250 cycles are image artefacts from the SAM measurement. Reprinted with permission from paper presented in appendix D.

6.1.2. DISCUSSION

All TLB bonded samples show development of small voids at the interface, which is well known issue for Cu-Sn bonding [99], [103], [141]. Since shear tests show high strength values, one can conclude that presence of small voids does not negatively affect the bond quality. The SAM analysis after the thermal cycling test shows that the TLP bonded interfaces demonstrate superior thermal capabilities compared to the silver sintered bonds. The attempts to extend the thermal test above 250 cycles were unfortunately unsuccessful due to the reliability issues with the DBCs used for sample fabrication (see appendix D for additional details). However, as discussed in section 2.2.3.3, TLP bonded interfaces show long term reliability at elevated temperatures [103], [107]–[109], thus, there is no reason to expect problems at larger number of thermal cycles.

6.2. TRANSIENT LIQUID PHASE BONDED CU-SN-MO AND CU-SN-AG-MO INTERCONNECTS – A NOVEL APPROACH FOR HYBRID METAL BASEPLATES

In power electronics, there is a continuous interest in devices capable to function at higher power. Use of compound semiconductors such as SiC and GaN leads to significant increase of operation temperature [142]. These tendencies cause new challenges for packaging technologies. One of the conventional techniques, soldering, experiences considerable problems to fulfil the needs in relation to thermal capability (see section 2.1.2 and 2.2.3.1). This leads to the development of new bonding approaches with better thermal performance and reliability such as silver sintering [9] and transient liquid phase bonding [11] (see section 2.1.2, 2.2.3.2, and 2.2.3.3). As described in section 2.1.1 an important part of power modules is a baseplate, typically made of Cu, on which the DBC sections with the devices are mounted. It plays a vital role in the thermal and mechanical stability of the entire module. As described in section 2.2.4 a primary concern is the baseplate shape (pre-bending) which should compensate a difference in CTE with DBC and, thus, the thermally-induced stresses at joint areas [115].

To minimize the baseplate deflection during temperature variations and avoid baseplate pre-bending, interlayers of different metals can be introduced into Cu. Mo is one of the candidates showing good promises [113] but direct bonding of Cu and Mo is not practical for industrial applications. One requires silver sintering or more complex sandwich structures involving metals allowing the formation of IMCs through the TLP process. Silver sintering is currently being used as the main joining method in the development of Cu-Mo hybrid metal baseplates at the University of Applied Sciences Kiel, however, the technique is very expensive. If TLPB joints could produce strong and reliable bonds it would be a promising and much cheaper alternative. An example of a hybrid metal baseplate joined by silver sintering method is shown in **Figure 48.** The asymmetric position of the Mo layer (closer to one side

of the plate than to another) and the difference in CTE between Cu ($17 \cdot 10^{-6}/K$) and Mo ($4.8 \cdot 10^{-6}/K$) allow to reduce deflection of the baseplate and DBC under thermal processes, thus, lowering the stress accumulation and following damage in the large area solder joints. The sections below focus on testing of TLP bonded Cu-Sn-Mo and Cu-Sn-Ag-Mo systems for novel Cu-Mo hybrid baseplates.

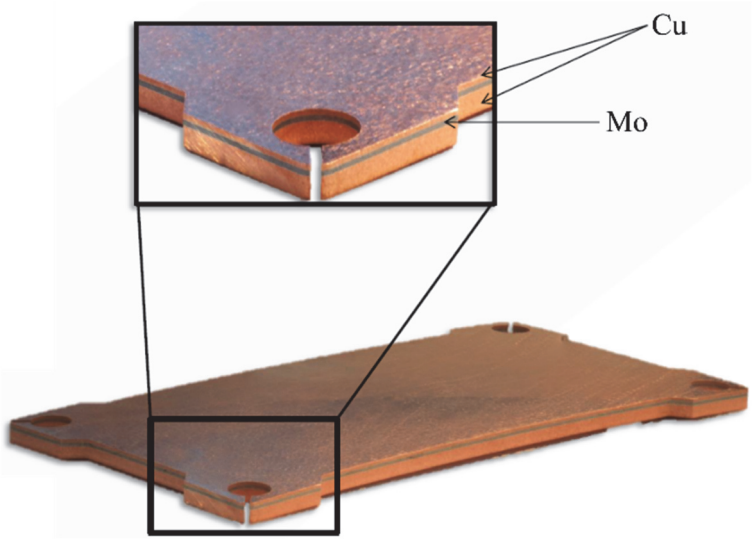

Figure 48. Picture of a Cu-Mo hybrid metal baseplate fabricated by silver sintering. Courtesy of the University of Applied Sciences Kiel.

6.2.1. RESULTS

By bonding of Sn- and Ag-coated Mo plates to bare copper or Sn-coated copper (see section 4.2.1.2 for details) three sample types are fabricated: i) Cu-SnMo (using uncoated Cu on Sn coated Mo), ii) CuSn-SnMo (using Sn-coated Cu on Sn-coated Mo) and iii) CuSn-AgMo (using Sn-coated Cu on Ag-coated Mo). Shear strength of the bonds corresponding to different structures and bonding times is shown in **Figure 49**. For longer bonding times the strength decreases in the case of Sn-coated Mo samples, while it increases for the Ag-coated Mo ones. Generally, reasonable mean shear strength values of around 40-50 MPa (comparable to literature values [101], [143], [144]) are reached for most sample, especially for CuSn-AgMo.

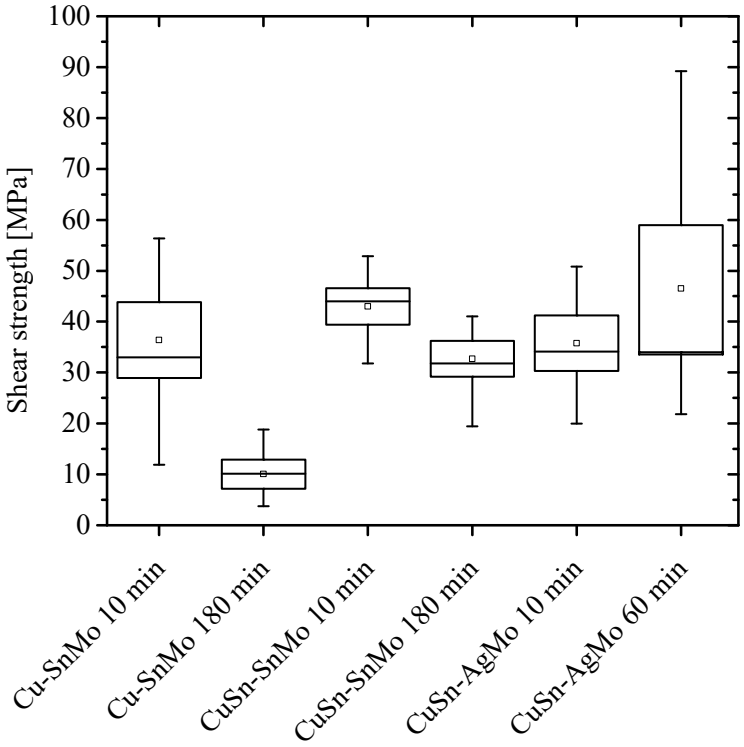

Figure 49. Shear strength of samples with different structures and bonding times. The squares represent the mean value, the lines correspond to minimum and maximum values and the box and line within represent the standard deviation and median value, respectively.

Optical images of the interface layers obtained by the micro-sectioning are shown in **Figure 50**. For all Cu samples on Sn-coated Mo (see **Figure 50**(a-c)), the interfaces show a large number of cracks and voids (dark in color), thus, representing a low quality of joints. In **Figure 50**(c), Cu precipitates (light brownish in color) are also visible in the bonded region. The interfaces for Sn-coated Cu on Ag-coated Mo (see **Figure 50**(d,e)) show much better compositional and structural homogeneity with a few small voids.

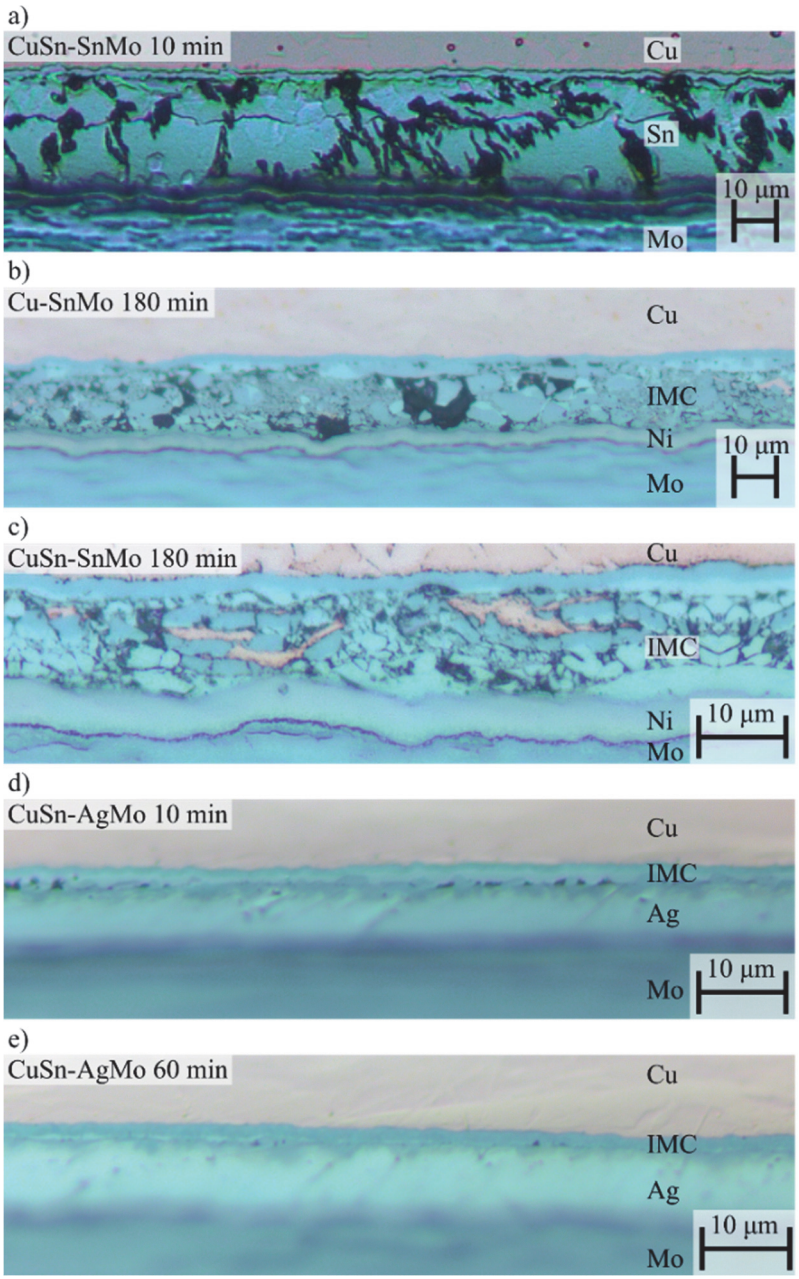

Figure 50. Optical micrographs of the interfaces for different structures and bonding times. The type of structure, bonding time, and scale are indicated for each micrograph.

EDX analysis with an acceleration voltage of 20 kV is applied to reveal the details about IMCs at the interfaces. Results of elemental analysis for CuSn-AgMo samples, which show good quality interfaces in optical images, can be seen in **Figure 51**. The line-scan in **Figure 51**(f) reveals that the solid state diffusion process has exhausted and the interface consists of both Cu-Sn and Sn-Ag IMCs.

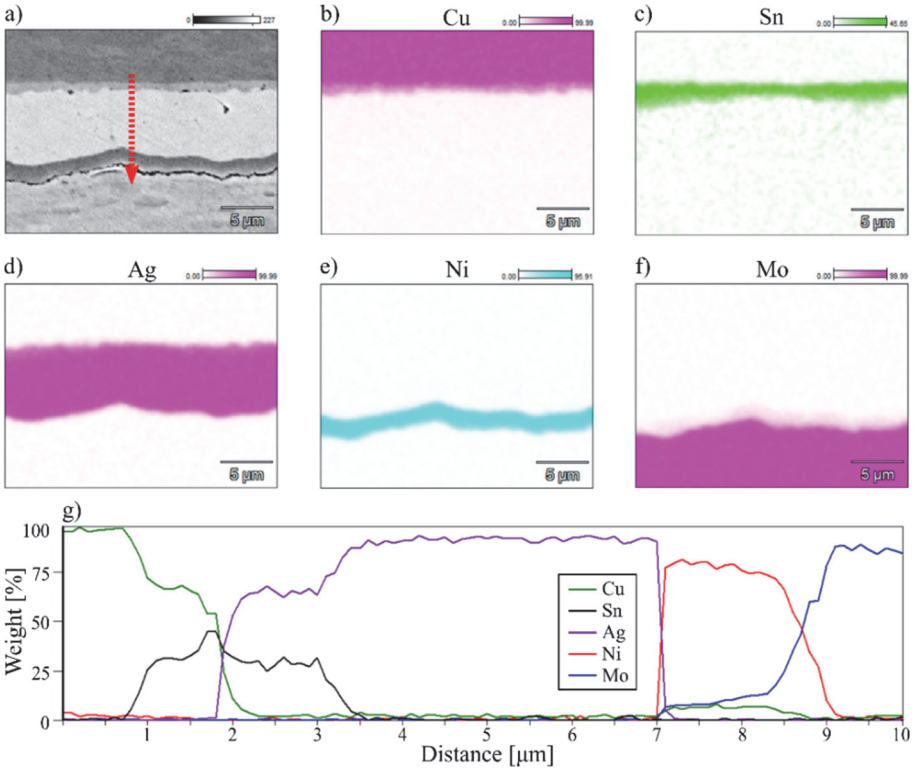

Figure 51. Results for CuSn-AgMo sample with bonding time of 10 min. a) SEM image of the area examined by EDX, b) color diagram for weight percent of Cu, d) color diagram for weight percent of Sn, d) color diagram for weight percent of Ag, e) color diagram for weight percent of Ni, f) color diagram for weight percent of Mo, and g) line scan along the direction indicated in a) showing composition of the interface.

6.2.2. DISCUSSION

Use of Sn in Cu-Mo bonds shows interfaces with numerous large voids and unwanted Cu precipitates. This may be explained by the different IMCs, which Sn can form with the Ni coated Mo [101], and also by soft nature of Sn. During the cool down process the difference in CTEs causes severe stress in the Sn layer and, thus, crack and void formation. However, to fully explain the low strength of the bonds, further investigation of the IMC formation process is needed, especially a role of thin Ni layers. Adding of Ag leads to more structurally homogeneous interfaces due to the

inter-diffusion of Ag and formation of more mechanically stable Sn-Ag IMCs that leads to better strength and performance of the bonds. Thus, TLP bonded CuSn-AgMo systems provide good promises as a novel technological solution in the Cu-Mo hybrid baseplate formation. Nevertheless, these are only the test results, which require further studies of reliability.

6.3. CONCLUSION

A few types of TLP bonded interfaces, which can be used for the bonding and formation of baseplates, have been examined. It is found that the Cu-Sn-Cu systems exhibit very good shear strengths and superior thermal cycling capabilities compared to silver sintered bonds. Important fabrication parameters are optimized and recipes for producing homogenous and strong joints are developed. The achieved results show that TLPB is promising technique, which has far superior thermal capabilities compared to traditional soldering, while simultaneously being more cost effective than silver sintering. Since Cu-Sn-Cu TLP bonds can be used as the joining technique at multiple interfaces of power modules it can be a key technique in developing the next generation of power modules with increased reliability at temperatures much exceeding what is currently possible with traditional soldering techniques. However, it is worth noting that long-term thermal reliability of these bonds still requires additional study to be able to transfer the technology to industry.

For the cases of Cu-Sn-Mo and Cu-Sn-Ag-Mo systems, the very first studied are carried out. These bonds are promising for more specific application to be used in hybrid metal Cu-Mo baseplates. It is observed that Cu-Sn-Mo are characterized by numerous voids, cracks and sometimes Cu precipitates making their performance and reliability questionable. However, the novel idea of adding an Ag interlayer is shown to improve the structural homogeneity and strength of the interfaces. Thus, the achieved results indicate that the novel TLP bonded Cu-Sn-Ag-Mo system could be a potential candidate for use as a joining technology in hybrid metal baseplates. One should stress that these are preliminary results and more studies of the structure, composition and reliability of the systems are required. However, the development of this alternative baseplate technology using the cost-effective TLPB method can lead to the development of new power modules with increased reliability and thermal capabilities.

CHAPTER 7. CONCLUSIONS

The general purpose of the studies presented in the thesis was to gain crucial physical understanding of the mechanism that lead to the degradation of thin metal films and interfaces in power modules, which play an important role in the overall reliability of power electronic systems. The work presents the results for two research areas, namely, the metallization degradation of power devices under cyclic operation and the development of novel TLP bonded interconnects.

One of the significant contributions of the work is the development of a novel type of accelerated test setup for passive thermal cycling. This simple, yet powerful approach is used to provide convincing proves on the key factors influencing the structural degradation of micrometer thick polycrystalline Al films typically used as metallization layers of commercial power electronic devices. Since the setup can reach much higher frequency of the thermal cycles compared to traditional oven based equipment, the components can be tested at thermal conditions very close to real operating temperatures while still inducing the necessary fatigue within a reasonable time frame. This novel setup is not limited to the study of metallization degradation but can easily be used to study the reliability of other important interfaces such a solder joints, wire bonds etc.

The results obtained from comparison of the metallization layers subjected to the passive thermal and active (power) cycling show very strong evidence that the main factor for metallization degradation is thermo-mechanical stress, and that electrical effects play little to no role. It is found that the grain structure and texture of micron thick Al polycrystalline films play a very important role in the degradation phenomena. In particular, it is shown for the first time that under the temperature conditions which are close to real device operation, the metal film texture undergoes an evolution from a dominating (111) orientation towards (311), but not to (211), which is generally accepted in literature. Two model mechanisms one of which is based on presence of constraints and the other one considering temperature factor in the atomic reordering are proposed to explain the finding.

The study of environmental factors, such as humidity and presence of oxygen, on the reconstruction of Al metallization layers under the accelerated test allows to conclude about importance of oxidation processes which limit the dislocation movement during the tensile and compressive phases, thus, slowing down the development of cracks and structural degradation.

Thus, new and very important knowledge about the main stressors affecting the metallization reconstruction is obtained and an increased physical understanding of the mechanisms causing degradation of thin metal films have been achieved. This knowledge is crucial for the future development of better lifetime predictions using physical modelling by considering the grain structure and texture of the metal films,

while placing special emphasis on thermo-mechanical stress as the main degradation factor leading to failure.

The studies on TLP bonded interconnects considerably contributed to the existing knowledge on the applications and reliability of these interconnects. Practical recipes for the formation of Cu-Sn-Cu TLP bonded joints providing high strengths and superior thermal capabilities are developed. These joints can substitute traditional soldering and silver sintering and help to increase the reliability and cost-effectiveness of power devices. Novel Cu-Sn-Ag-Mo structure is produced by TLP bonding and tested showing to be a promising candidate for the development of a new type of hybrid metal baseplates, which can drastically increase the robustness of these elements and, thus, the reliability and lifetime of power modules.

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REPRINTS OF PUBLICATIONS

APPENDIX A: EFFECTS OF THERMAL CYCLING ON ALUMINUM METALLIZATION OF POWER DIODES

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Effects of thermal cycling on aluminum metallization of power diodes

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ABSTRACT

Reconstruction of aluminum metallization on top of power electronic chips is a well-known wear out phenomenon under power cycling conditions. However, the origins of reconstruction are still under discussion. In the current study, a method for carrying out passive thermal cycling of power diodes in a controlled environment is developed, thus eliminating possible contribution to degradation from electric current and humidity. The focus is centered on the structural changes in the top Al metallization layer of the power diodes, correlated with the change of sheet resistance. Since the atmosphere is controlled and the device is not subjected to a current load the observed degradation of metallization and corresponding increase of resistance is purely induced by thermo-mechanical stress. A correlation between number of cycles, micro-structural evolution, and sheet resistance is found and conclusions on the dominant role of thermo-mechanical stresses are achieved. Additionally, proposals are made on how the current thermal test setup can be further developed to study the role of corrosion.

1. Introduction

In power electronic chips, Al metallization is often used as an interconnect material for wire bonding, sintering etc. The thickness of the metallization is typically on sub-micrometer to micrometer scale and the layer is deposited on top of silicon. Due to a mismatch of thermal expansion coefficients of the Si/Al structure the aluminum is subjected to thermo-mechanical stresses under thermal cycling which lead to reconstruction and degradation of the metallization [1]. Despite the simplicity of this system, real origins of the degradation are not fully understood and attract increased attention [2–4].

The reconstruction of the metallization is believed to occur as a complex interplay between electrical effects such as electro-migration and stress migration such as grain-boundary diffusion [5] as well as thermo-mechanical fatigue such as grain boundary sliding and plastic deformation [1].

To investigate metallization reconstruction in power electronic chips a passive thermal cycling setup operating in a controlled atmosphere is constructed. This approach is chosen to exclude current induced effects like electro-migration. The thermal cycling setup is enclosed in an air-tight box that is continuously pumped with nitrogen which ensures an atmosphere with low humidity and therefore limits corrosion.

2. Experimental procedure

All devices under test (DUT) are single unpackaged high power Infineon diodes (100 A/1200 V). The diodes are 9 × 9 mm squares with 3.4 μm thick Al metallization layer on the top. DUTs are subjected to the thermal cycling and characterized using measurements of sheet resistance and scanning electron microscopy (SEM) accompanied by focused ion beam (FIB) milling to obtain cross-sections. SEM measurements are carried out using Zeis 1540XB system and standard procedure.

2.1. Thermal cycling setup

The setup is based on a thermoelectric cooler (TEC). One side of the TEC is connected to a water-cooled Al block with constant temperature, while the other side is used for thermal cycling of the DUT. A current of 3 A is supplied to the TEC until the diode surface reaches the desired maximum temperature, T_{max}. This is measured with a thermocouple in direct contact with the metallization on one of the diodes. When T_{max} is reached, the current is reversed, such that the TEC rapidly cools the diodes down to the minimum temperature, T_{min}, which constitutes a single cycle. The thermal cycling profile of the setup is shown in Fig. 1. Cycling is performed with a constant ΔT and constant TEC-current, while the current direction is modulated accordingly. By modulating the current amplitude together with the current direction, temperature profiles that differ from Fig. 1 and include dwell times and more closely resemble typical operation conditions for DUT could be realized using the same setup. All DUTs are placed in direct contact with the TEC with no thermal compound, to avoid contamination of the metallization during handling and measurements. The temperature distribution across the TEC is checked and it is found to be largely homogenous with variations within ±2 °C in the center area where the DUTs are placed. The entire thermal setup is encapsulated in a plastic enclosure through which a continuous flow of pure (99,999%) nitrogen is provided

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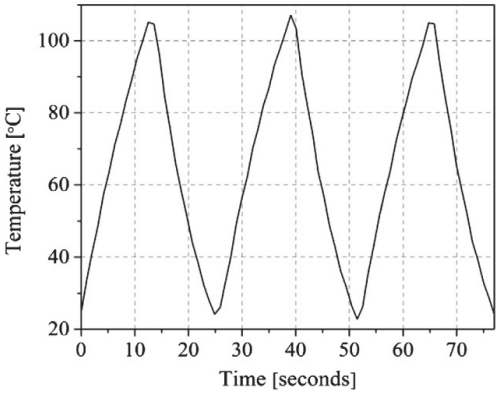

Fig. 1. Typical profile of thermal cycles with $T_{min} = 25$ °C and $T_{max} = 105$ °C. The period of one cycle is approximately 26 s.

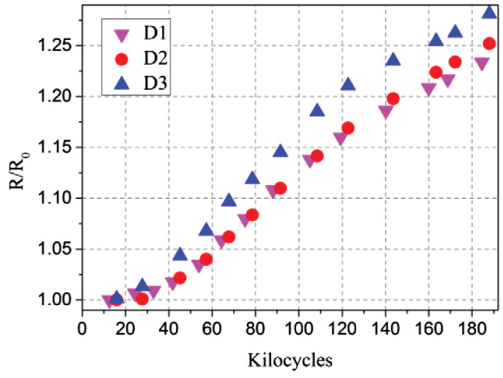

Fig. 2. Relative sheet resistance of thermally cycled diodes as function of number of cycles. D1, D2, and D3 correspond to three different diodes.

in the way that ordinary atmospheric air is pushed out and humidity drops down to a zero value.

The setup is not limited to the study of diodes and it can also be used to study thermo-mechanical degradation of other power devices such as IGBT or MOSFET chips, etc. The small size and ability to precisely control various parameters that might influence degradation such as absolute temperature, temperature slope, dwell time, and atmosphere make it a versatile setup that could be used to isolate and study numerous correlations in regard to thin film fatigue.

2.2. Sheet resistance measurements

The sheet resistance is measured according to the van der Pauw method [6]. Probes are placed in each corner of the diode and the *I–V* measurements are used to calculate the sheet resistance by van der Pauw formula. When measuring the *I–V* curve the current varies between −100 mA and +100 mA in 20 steps. Electrical characterization is carried out ex situ, i.e. the devices are temporarily removed from the thermal cycling setup.

The resistivity for a new diode was measured to be 28.8 nΩ · m, while the literature value for bulk Al is 26.6 nΩ · m. The slightly larger resistivity of the Al metallization is expected since it contains a small admixture of Si and has a granular structure [7]. A sheet resistance measured on each new diode, R_0, is used to calculate the relative sheet resistance for the cycled diodes as R/R_0.

3. Results

3.1. Sheet resistance evolution

The evolution of the relative sheet resistance is shown in Fig. 2. It can be clearly seen that the relative sheet resistance starts increasing after approximately 16 kc. From the figure three different phases in the sheet resistance evolution can be distinguished. In the first phase, which spans from 0 to 16 kc, no significant change in the sheet resistance is observed. In the second phase, which spans from 16 to approximately 120 kc, the most severe increase of sheet resistance occurs. In the third phase, which spans from 120 to 190 kc, the change is lower than in phase two, but still a significant increase can be seen. This non-trivial evolution corresponds well to earlier results regarding the sheet resistance of Al metallization during accelerated tests [7,8,9] and microstructural evolution during passive thermal cycling [10], albeit the rise in sheet resistance is less severe in our case.

There can be several factors explaining the apparently slower and less severe degradation in our experiment compared to the results presented in [7,8]. The relatively low ΔT of 80 °C and T_{max} of 105 °C as well as pure nitrogen atmosphere are the factors that influence the rate of degradation. In addition, with no current passing through the samples no hotspots occur, which might be an accelerating factor of the non-homogeneous degradation under active power cycling. Also, since the diodes in our experiment are unpackaged the thermal impedance is low. It is decided to limit the dwell time to increase cycling frequency. These conditions might limit degradation since stress migration mechanisms have less time to evolve.

At 188 kc, the largest observed increase of the relative resistance reaching 28% can be seen for diode 3 (D3). This corresponds well to the result in [7] where a relative change of 41% is found for the sheet resistance of an IGBT metallization with a strong reconstruction. A possible explanation for the faster degradation of D3 compared to D1 and D2 can be that D3 is placed onto the TEC without any fixation mechanism in contact with the metallization. Thus, no heat reservoir will limit the temperature extrema, which might result in a slightly higher ΔT.

3.2. Microstructural analysis

To investigate structural changes causing the observed increase in sheet resistance, SEM accompanied by FIB cross-section have been performed. Fig. 3 shows SEM images of the metallization at different number of cycles. It can be seen that with rising number of cycles the surface roughness increases. From Fig. 3b–c it is clear that the metallization have undergone severe reconstruction at 12.5 and 45 kc. However, when comparing to Fig. 2 the relative sheet resistance is not seen to vary considerably until reaching 24 kc. Thus, the reconstruction shown in Fig. 3b probably affects only the very surface layer and does not have impact on the resistance. From Fig. 3c–d it can be seen that the metallization layer is significantly degrading that well correspond to the steep rise of resistance in the second phase.

To get more information about the structure of the metallization, cross-sections were made using FIB. Fig. 4a shows a cross-section of the metallization after 25 kc. As expected from the sheet resistance measurements, no cracks or voids are present, and the layer is continuous with only a slightly corrugated top. As can be seen from the image this corrugation is originated by the protruding grain boundaries. In Fig. 4b the metallization after 45 kc is shown. The surface has reconstructed, and cracks propagating from the surface into the bulk of the metallization can be seen. These cracks lead to the formation of cavities and breakage of the layer continuity that cause an increase of resistance. Fig. 4c shows a cross-section after 145 kc. Cavities and cracks that protrude deeper towards the Si interface can be observed. The arrow in Fig. 4c indicates a hole that reveals a behind-lying cavity. This area is

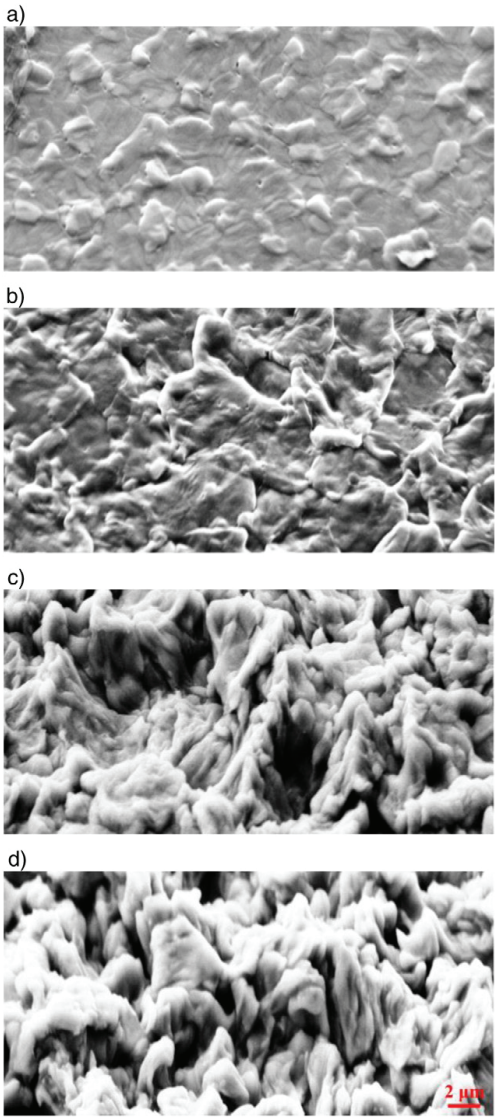

Fig. 3. SEM images of metallization for a) a new diode, b) a diode after 12.5 kilocycles, c) a diode after 45 kilocycles, and d) a diode after 145 kc. The scale is shown in d).

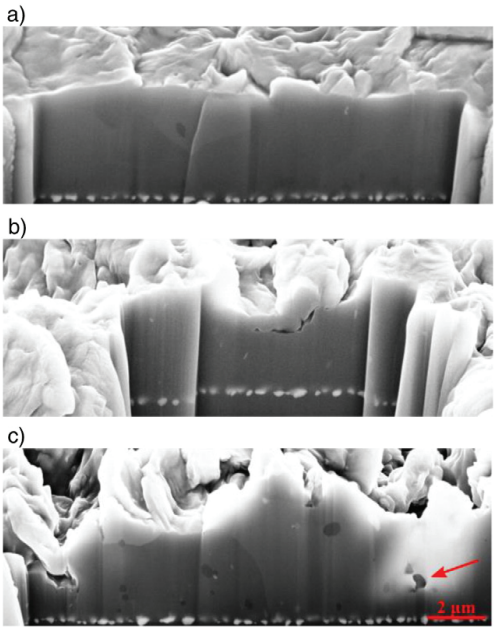

Fig. 4. SEM images of metallization with wells obtained by FIB milling for a) a diode after 25 kc, b) a diode after 45 kc and c) a diode after 145 kc. The arrow in c) indicates a behind-lying cavity. The scale is shown in c).

further explored in Fig. 5, where the cavity is opened by additional milling and it is seen to propogate into the metallization layer almost down to the Si interface. The thickness of the remaining Al is measured to be approximately 0.4 µm. A network of such cavities severely limits the conductivity and can therefore explain the rise in relative sheet resistance of 23% (see Fig. 2) at this number of cycles.

4. Discussion

Based on the approach suggested by Gao et al. [5], Martineau et al. [11] have recently proposed a qualitative model to explain the degradation observed in Al metallization layers. They concluded that the degradation is an interplay between thermal fatigue induced stress and stress migration in the form of diffusion of Al along grain boundaries onto the surface. The presented microstructural analysis results are in good agreement with this mechanism. However, in the model the self-passivation of grain boundary grooves through oxidation plays an important role in the crack propagation mechanism. Since the oxidation process is limited in our case due to the nitrogen atmosphere, this could be an explaining factor for the relatively slow and less severe degradation compared to the results of other research [7,8,10,12].

If one compare the level of degradation achieved in the present experiments with that of a device subjected to 4.5 million power cycles under the conditions described in [13] (see Fig. 6), it is clear that the metallization reconstruction achieved by passive thermal cycling closely resembles the degradation seen in actively cycled devices. This is a

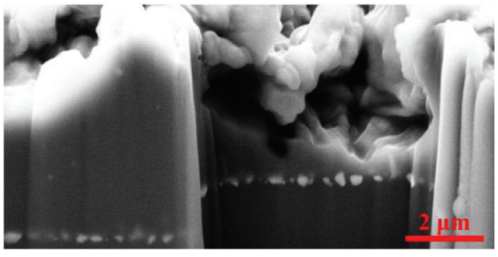

Fig. 5. SEM images of metallization with wells obtained by FIB milling of a diode at 145 kc in the area indicated by the red arrow in Fig. 4c.

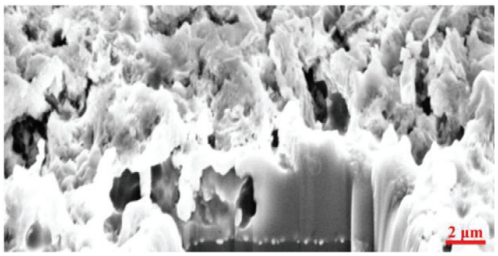

Fig. 6. SEM image of metallization with well obtained by FIB milling for a diode that underwent 4.5 million power cycles under the conditions described in [13].

strong indication about the dominant role of thermo-mechanical stress in the degradation of Al metallization.

5. Conclusion

To investigate reconstruction of Al metallization a passive thermal cycling setup is developed and applied for testing of metallization on Si based power diodes. One of the advantages of the setup is in the possibility to exclude two factors that might contribute to the degradation of the metallization, namely electro-migration and moisture induced corrosion.

Characterization of the degradation is carried out both electrically through sheet resistance measurements and microstructurally by SEM and FIB. A clear tendency of increased metallization reconstruction at higher number of temperature cycles is observed with good correlation to sheet resistance measurements. This set of data allows one to make a conclusion about the dominating role of thermo-mechanical stress in the metallization degradation.

Future works will take advantage of the versatility of the thermal cycling setup to focus on the role of oxygen and humidity in the metallization degradation by replacing the dry nitrogen gas with atmospheric air. In this way, the rate of electrical degradation and microstructural changes can be compared and the influence of oxidation and corrosion effects can be revealed.

Acknowledgments

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APPENDIX B: PASSIVE THERMAL CYCLING OF POWER DIODES UNDER CONTROLLED ATMOSPHERIC CONDITIONS – EFFECTS ON METALLIZATION DEGRADATION

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Passive thermal cycling of power diodes under controlled atmospheric conditions - effects on metallization degradation

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Abstract

Degradation of Al metallization on Si based semiconductor chips subjected to power cycling is a well known problem, but the mechanisms of this phenomenon are not fully understood. To quantify contributions of different possible effects, a passive thermal cycling setup has been developed and thermal cycling of power diodes is performed, which results in electrical degradation and microstructural reconstruction of the Al layer. The degradation is characterized by sheet resistance measurements and scanning electron microscopy (SEM). Since the passive thermal cycling induces degradation very similar to what is observed for actively power cycled devices, it can be concluded that the dominating effect for the metallization reconstruction is due to the thermal-induced stresses. To examine the role of oxidation and corrosion effects, cycling tests in nitrogen environment and ordinary atmospheric conditions are compared. This comparison shows that the presence of the continuously self-passivating surface oxide limits the electrical degradation of the metallization compared to the case with no native oxide layer. Energy-dispersive X-ray spectroscopy (EDX) shows that the metallization contains more oxygen when cycling in the ordinary atmospheric conditions and X-ray diffraction (XRD) measurements gives clear evidence that the texture of the metallization layer changes significantly during cycling.

1 Introduction

Power converters with silicon based semiconductor chips are common devices in numerous applications ranging from consumer electronics to high power energy systems. In high power modules the conventional assembly approach is to mount semiconductor chips on the supporting Cu plates using a solder paste on the backside, while heavy Al wires are bonded to the topside to provide electrical contacts. The topside of the Si chips is typically terminated by Al metallization layers with a thickness of 1-6 μm. This provides good electrical contact across the entire chip surface and allows for the bonding of Al wires. Since the materials used in the packaging (Cu, Al and Si) have different coefficients of thermal expansion, they are subjected to thermo-mechanical stress, under thermal cycling, which leads to degradation of the Al metallization, and other interfaces and materials [1, 2].

The fatigue degradation mechanism of chip metallizations has been the goal for several studies applying different loading methods such as active power cycling [3, 4, 5, 6, 7], passive thermal cycling [8, 9, 10, 11, 12, 13, 14], and cyclical bending on compliant substrates at room temperature [15, 16]. However, the degradation of the Al metallization is not fully understood and effects such as electromigration, grain-boundary diffusion [17] aided by oxidation [6], hillocking [18], and dislocation slip might contribute to the observed cumulative plastic deformations. So far no comparison has been made for thermal cycling under different atmospheric conditions.

In order to gain further insights into this subject, a passive thermal cycling setup that can operate in different controlled atmospheres has been build and the results of electrical and microstructural characterization of the metalization layers on the top of diode chips are presented.

2 Experimental procedure

2.1 Passive thermal cycling

The passive thermal cycling setup is based on a digitally controlled thermo-electric cooler (TEC), which is connected to a water cooled Al block on one side, while the other side is used to thermally cycle the power diodes. All active elements of the setup is enclosed in an air-tight enclosure that provides a possibility to control the surrounding atmosphere. A schematic of the setup is shown in **Figure 1**. Temperature measurements are carried out by placing a thermocouple in direct contact with the center of one of the devices under test (DUT).

For the current experiments, one set of data is obtained for cycling in a pure nitrogen atmosphere with zero relative humidity (RH). For the remaining experiments, thermal cycling is carried out in an ordinary atmosphere with a controlled RH=50%. The temperature waveforms are triangular shaped with a period $P_{N2} = 26\,s$ for the cycling in nitrogen atmosphere and a period $P_{air} = 24\,s$ for the cycling in ordinary atmosphere, see **Figure 2**. Other parameters, such as minimum and maximum temperature, $T_{min} = 25\,°C$,

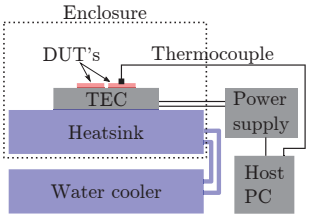

Figure 1 Schematic of the passive thermal cycling setup.

$T_{max} = 105\,°C$, and the mean temperature of 65 °C are identical for both experiments. The DUT are high power Infineon diodes (100A/1200V), that are 9×9 mm squares with a measured topside metallization thickness of 3.4 μm.

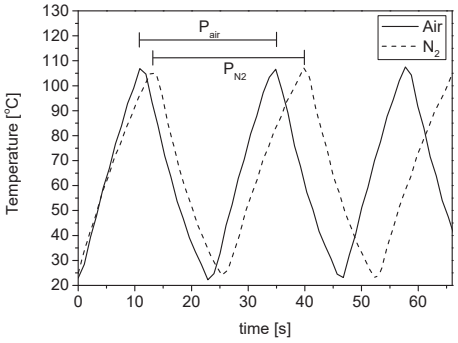

Figure 2 Profile of thermal cycles with $P_{air} = 24\,s$ being the period for cycling in atmospheric air, and $P_{N2} = 26\,s$ being the period for cycling in nitrogen atmosphere.

2.2 Electrical characterization

For the electrical characterization, the diodes are temporarily removed from the cycling setup and sheet resistance measurements are done using the van der Pauw method [19], according to the procedure described in [14].

The relative change in sheet resistance for the case of thermal cycling in both nitrogen and normal atmosphere is shown in **Figure 3**. A clear degradation of the sheet resistance can be seen for the diodes cycled in nitrogen atmosphere, with an increase of 43% at 330 kilocycles. In this case, three phases with different degradation rates can be distinguished: phase 1 for 0-20 kilocycles that shows almost no change in sheet resistance, phase 2 between 20-120 kilocycles that demonstrate the most severe change, and phase 3 above 120 kilocycles that shows moderate change. This type of curve with different phases agrees with earlier results obtained for actively cycled devices, [4, 5, 6]. The data for the diodes cycled in ordinary atmosphere show slower increase compared to the diodes cycled in nitrogen. At 147 kilocycles the average increase in sheet resistance for the diodes cycled in ordinary atmosphere is 15%, while the average rise for diodes cycled in nitrogen atmosphere is 21%. Similar to the diodes cycled in nitrogen, a phase with low change in sheet resistance, between 0-20 kilocycles, can also be seen for the diodes cycled in air, and a second phase is ongoing at 147 kilocycles, which is the number of cycles reached by now.

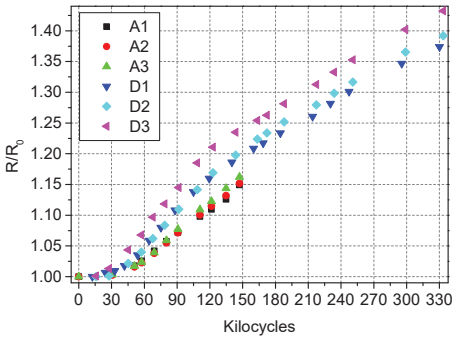

Figure 3 Relative sheet resistance of diodes at different number of cycles. A1, A2, and A3 correspond to diodes cycled in ordinary atmosphere, and D1, D2 and D3 correspond to diodes cycled in nitrogen atmosphere.

A contributing factor for the apparent slower degradation for the diodes cycled in air compared to those cycled in nitrogen could be the change in the period of the thermal cycles, which is shown in **Figure 2**. It is well known that the duration of a cycle is related to the degree of plastic deformation that can occur within that cycle, in the way that longer cycle times increase the deformation, [20]. However, it is unlikely that an increase of period from 24 s to 26 s (8.3% increase) can account for the difference in increase of resistance of 15% and 21% (40% increase), respectively. Instead, some other mechanism related to the continuous formation of a native oxide on the Al metallization may strengthens the metallization, thus limiting the amount of reconstruction. This will be addressed in the discussion section.

2.3 Microstructural characterization

To correlate the change in sheet resistance to the microstructural evolution of the Al metallization, SEM study accompanied by FIB cross-section milling is performed.

In **Figure 4** SEM images of the metallization cycled in nitrogen atmosphere are presented. **Figure 4(a)** shows the surface of the metallization after 250 kilocycles demonstrating severe reconstruction. **Figures 4(b-c)** show cross-sections obtained by FIB milling after 145 and 250 kilocycles and it can be seen that the reconstruction is not limited to the surface of the metallization. Cavities and cracks propagate deep into the metallization and the disorder of the Al layer increases with number of cycles. These observations correlate well with the sheet resistance measurements, which show an increase of relative resistance from 1.25 to 1.35 for D3 for the interval 145-250 kilocycles, see

Figure 3. **Figure 4(d)** visualizes that smaller cracks and cavities propagate all the way down to the Al/Si interface, i.e. the continuity of the metallization layer is broken.

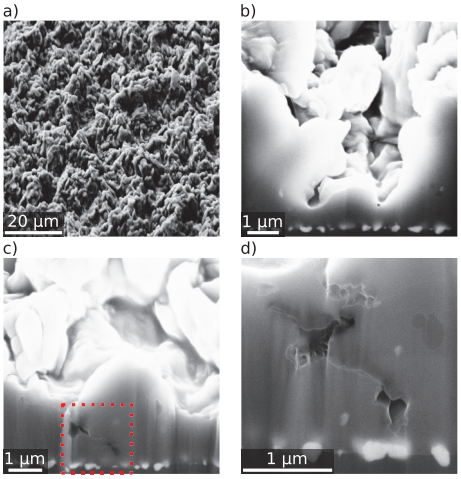

Figure 4 SEM images of metallization of D3. a) Surface after 250 kilocycles, b) cross-section after 145 kilocycles, c) cross-section after 250 kilocycles, and d) magnification of area indicated by the dotted box in c).

In **Figure 5** SEM images of the metallization cycled in ordinary atmosphere is presented. **Figure 5(a)** shows the metallization surface in the center of a diode. There is a clear reconstruction similar to that seen in **Figure 4(a)**, albeit less severe. **Figure 5(b)** show a cross-section in the center of the metallization. It can be seen that the cavities and cracks propagate into the bulk of the metallization. **Figures 5(c-d)** presents surface and cross-section images at the edge of a diode. By comparing with **Figures 5(a-b)** it becomes obvious that the reconstruction is not homogeneous, but most severe in the center of the diode. Lower reconstruction at the edges can be explained by less confinement, which leads to lower stresses.
Comparing the reconstruction for the cycling in nitrogen and ordinary atmosphere, one can not conclude about apparent differences.

2.4 Texture analysis

To examine the grain texture of the metallization XRD measurements were performed. XRD measurements can be used in thin film analysis to determine the orientation of the micro-crystals that constitute the polycrystalline film, [21]. Measurements presented in **Figure 6** correspond to the Bragg diffraction of crystal lattice planes that are parallel to the surface of the metallization. It can be seen that grains with crystallographic planes (111) dominate in new diodes. Low intensity peak corresponding to (222) plane is also resolved. This spectrum corresponds well to earlier results regarding the texture of Al thin films on Si substrates,

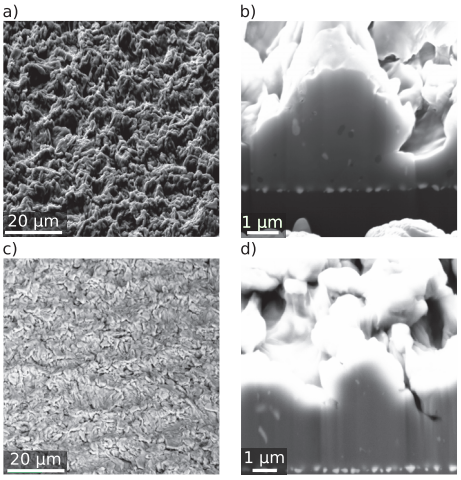

Figure 5 SEM images of metallization of A2 after 110 kilocycles. a) Surface in the center, b) cross-section in the center, c) surface at the edge, and d) cross-section at the edge.

[8, 12, 22, 23]. As the number of cycled increases, the (111) and (222) peaks are decreased in intensity and peaks corresponding to the (200), (220), and (311) crystal lattice planes are growing for both types of cycling. The transformation of the grains may be explained by dislocation glide of the inclined (111) planes that are constrained by the Si substrate [12, 24].
The significant decrease in intensity of the (111) peak under initial cycling stage (up to 31 kilocycles) is not followed by any significant change of resistance (see **Figure 3**) or any considerable reconstruction of metallization [14]. The simple explanation is in that XRD measurements are sensitive to even a very slight misorientation of crystallographic planes.
Tendencies in the change of XRD spectra are found to be very similar for both types of samples. However, it can be seen in **Figure 6** that the diode cycled in air for 134 kilocycles has almost the same XRD scan as the diode cycled in nitrogen at 335 kilocycles. This implies that the grain reorientation phenomena might only be influential until a point where no more relaxation can occur through this mechanism, while other degradation mechanisms (crack and void development) continue to influence the reconstruction process.

2.5 Oxide layer analysis

EDX measurements were performed to monitor the amount of oxygen present in the film, thus allowing to track the formation of aluminum oxide. In **Figure 7** the amount of oxygen is shown as the number of cycles increase. The accelerating voltage of the EDX measurement was 10 kV, which according to simulations corresponds to a maximum

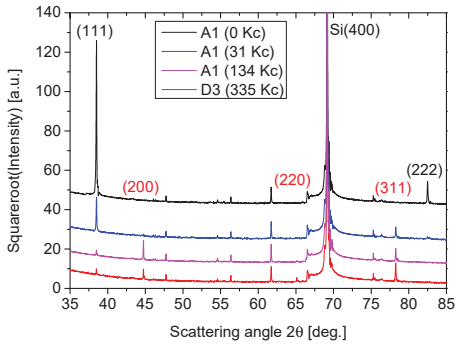

Figure 6 XRD scans for A1 and D3. The intensive peak at 68° and many small unlabeled peaks are related to the Si substrate. All peaks caused by the Al metallization are labeled with corresponding crystallographic planes. Black color indicates peaks that are decreasing in intensity during cycling and red color indicate peaks that are increasing.

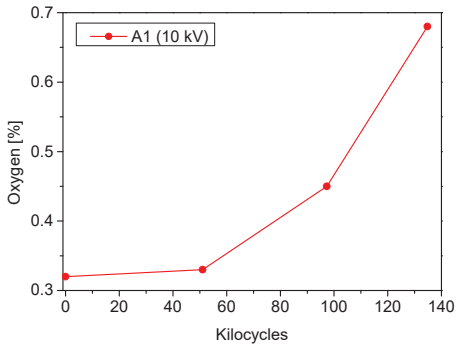

Figure 7 Amount of oxygen in the metallization of A1, measured by EDX.

penetration depth of 1 µm. It can be seen from the data presented in **Figure 7** that the amount of oxygen in the metallization of A1 increases significantly, in an non-linear manner, as the number of cycles increase. The amount of oxygen increase for diode D3 (nitrogen atmosphere) at 335 kilocycles was found to be at 0.5% which is much lower compared to A1 diode at 135 kilocycles.

This agrees with a qualitative diffusion model for the reconstruction of Al metallizations on power MOSFET's by Martineau et al [6]. They hypothesize that micro-cracks form during the tensile phase (cooling) of a thermal cycle, and the sidewalls in these cracks self-passivate, through surface oxidation in the ordinary atmospheric air, leaving them unable to heal in the following compressive phase (heating). In the next tensile phase, these cracks will travel further into the substrate, causing an electrical disconnection across the crack. In this way, the self-passivation by surface oxidation would have an impact on the sheet resistance in two ways. It will accelerate the crack propagation into the metallization towards the Si substrate, effectively decreasing the effective cross-section of the film. Also, it will leave behind a 3D network of oxidized channels that due to the low conductivity of aluminum oxide will increase the sheet resistance.

However, this mechanism should cause an acceleration of the electrical degradation when the cycling is performed in air compared to a nitrogen atmosphere, which is the opposite of what is observed in the series of experiments presented here. This might be due to an interplay between other mechanism arising from the oxidized surfaces, and this is discussed below.

3 Discussion

The results from the electrical characterization of sheet resistance and EDX analysis have showed two interesting features. The electrical degradation of the diodes that are cycled in air is seen to be slower compared to the diodes that were cycled in nitrogen atmosphere. At the same time, the EDX measurements shows that the amount of oxygen in the diodes that where cycled in ordinary atmosphere is higher than in the diodes cycled in nitrogen atmosphere, indicating a continuous self-passivation through surface oxidation during thermal cycling. This mechanism is expected to accelerate crack formation and increase the sheet resistance. However, this oxidation mechanism might be counteracted by a strengthening mechanism also arising from the presence of the native oxide.

Native oxide on Al films might constrain the dislocation motion in the film, thereby increasing the strength of the film and making it less prone to plastic deformation [25], in a similar way that a compressive layer, e.g. polyimide or silicon dioxide, has been shown to suppress the reconstruction phenomena [1, 26, 27]. However, these compressive layers are much thicker than the native oxide of Al, which is only around 3 nm to 6 nm [28], and their effect must therefore be expected to be much greater. Another example is that dislocation motion in thin Cu films which have been found to be very different compared to self-passivated Cu-1%Al films. In pure Cu films a parallel to the surface dislocation glide was observed to dominate while in the passivated films a transition to threading dislocation motion is found [29]. Also, the mechanical properties and microstructure of Al-0.5%Cu have been seen to depend on the presence of a native oxide, and it was speculated that the oxide layer might constrain the dislocation motion causing the observed behavior [8]. These results indicate that the presence of a native oxide on the metallization, despite its small thickness, might have an influence on the dislocation motion and thereby on the type of degradation and degradation rate. This model can help to explain the results presented in the current paper, however, more studies are required to quantify the role of oxide formation. It is also necessary to continue cycling the diodes in air in order

to see how the reconstruction will develop and how it will correspond to the change of resistance.

4 Conclusion

To gain insights into the dominant physical mechanisms governing the degradation of Al metallizations, a passive thermal cycling setup that can operate in different atmospheres, have been constructed. Both cycling in pure nitrogen atmosphere and ordinary atmosphere, have shown electrical degradation and microstructural reconstruction very similar to that seen in actively power cycled devices. This is a strong indication that thermo-mechanical stresses is the dominant mechanism responsible for the degradation of Al metallizations for Si based power components.

To examine the role of oxidation and corrosion effects, the degradation originated by cycling carried out in an ordinary atmosphere with controlled humidity was compared to the degradation caused by thermal cycling carried out in a nitrogen atmosphere. It was found that the degradation occurred slower in the ordinary atmosphere, and it was proposed that this could be caused by a strengthening mechanism due to the native oxide acting as a dislocation movement constraint. Comparisons between the amount of oxygen in the metallization cycled in ordinary and nitrogen atmospheres supported a model where self-passivation of micro-cracks can accelerate the degradation process.

To reach confidence in this question, passive thermal cycling experiments will be continued and more characterization techniques will be employed.

5 Literature

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APPENDIX C: MECHANISMS OF METALLIZATION DEGRADATION IN HIGH POWER DIODES

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Mechanisms of metallization degradation in high power diodes

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ABSTRACT

Under operation the topside metallization of power electronic chips is commonly observed to degrade and thereby affecta device's electrical characteristics. However, the mechanisms of the degradation process and the role of environmental factors are not yet fully understood. In this work, we investigate the metallization degradation by passive thermal cycling of unpackaged high-power diode chips in different controlled atmospheres. The electrical degradation of the metallization is characterized by sheet resistance measurements, while the microstructural damage is investigated by scanning electron microscopy (SEM) and X-ray diffraction (XRD). To study the evolution of the chemical composition of the metallization, energy dispersive X-ray spectroscopy (EDX) is also applied. Since the degradation depends on the initial microstructure of the metallization, the film texture and grain size distribution is determined using electron backscatter diffraction (EBSD). The obtained data show that the type of atmosphere plays a minor role in the degradation process, with a slight tendency that cycling in dry nitrogen atmosphere accelerates the degradation compared to the experiments in ambient atmosphere with a controlled relative humidity of 50 and 95%.

1. Introduction

Silicon based electronic chips with thin aluminum metallization layers are widely used for power converters. The conventional assembly method of power modules requires this Al metallization to allow the bonding of heavy Al wires and to provide good electrical contact across the entire chip surface. However, due to the difference in the thermal expansion coefficient between Al and Si, the metallization experiences mechanical stress when subjected to temperature cycling, which leads to structural degradation and loss of functional properties [1,2]. The degradation of chip metallizations has been investigated in a number of studies, see for example [3–12], however a systematic approach to the influence of varying atmospheric conditions has not yet been applied. To investigate this and the thermo-mechanical degradation mechanism, a series of passive thermal cycling experiments is performed on unpackaged high-power diodes under different atmospheric conditions.

2. Experimental procedure

The passive thermal cycling of the high-power Infineon diodes (100 A/1200 V) is carried out in a setup based on a thermo-electric cooler that can be placed under different atmospheric conditions. Further details about the thermal cycling setup can be found in [3,4]. The thermal cycling is performed at $T_{min} = 25$ °C, $T_{max} = 105$ °C and a period of approximately 25 s. Three sets of data are compared, namely cycling performed in pure nitrogen atmosphere, cycling in ambient atmosphere with a controlled relative humidity (RH) of 50%, and cycling in a climatic chamber in ambient atmosphere with RH = 95%. For each atmospheric condition three diodes are thermally cycled and studied. During cycling, the diodes are temporarily removed from the setup to apply various characterization techniques such as sheet resistance measurements, SEM and XRD analysis. The initial microstructure of uncycled diodes has been examined by EBSD to reveal the grain texture and grain size distribution.

The sheet resistance measurements are performed using a four point probing technique in a Van der Pauw configuration [13]. This approach removes the influence of contact resistances and ensures a very high repeatability with relative measurement uncertainties of approx. 0.1%.

3. Results

3.1. Sheet resistance evolution

The evolution of the sheet resistance is shown in Fig. 1. It can be seen that the sheet resistance increases with the number of cycles and follows a nonlinear dependence. The cycling performed in nitrogen atmosphere on average yields a faster electrical degradation compared to the cycling in ambient atmosphere. The results for the cycling in ambient atmosphere at high humidity (H1 − 3) show a relatively large spread in the measured values. Though all the diodes are taken from a single wafer, this spread of the data might stem from different manufacturing qualities of the metallization across the wafer. For example, the metallization structure can be slightly different in the middle of the wafer compared to the edges. However, there is a general tendency that the

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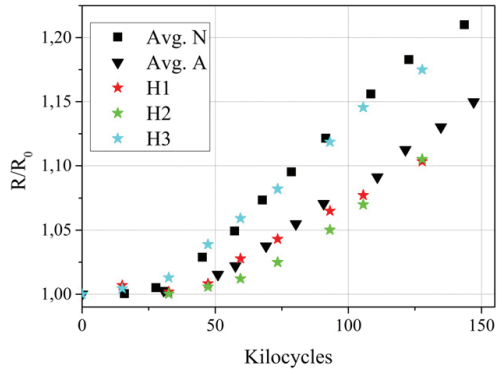

Fig. 1. Relative change in sheet resistance during thermal cycling. Avg. N and A refer to the average values for diodes cycled in nitrogen atmosphere (RH = 0%), and ambient atmosphere (RH = 50%), respectively. H1–3 refers to diodes cycled in ambient atmosphere under RH = 95%.

cycling in nitrogen accelerates the degradation compared to the cycling in ambient atmospheres. Increasing RH up to 95% does not seem to affect the degradation mechanism. But more cycles need to be performed to substantiate this.

3.2. Microstructural analysis

To correlate the evolution of the sheet resistance with the change of the microstructure of Al metallization, a SEM study is performed. The surface of the metallization after thermal cycling can be seen in Fig. 2(a–b). Compared to the initial surface of the metallization, shown in Fig. 2(c), it is clear that the metallization undergoes significant plastic deformation during thermal cycling. To get more detailed information about the reconstruction, cross-sectional SEM images are obtained and shown in Fig. 3(a–b). For comparison, a typical image for the metallization of an uncycled diode is shown in Fig. 3(c). It can be seen that the metallization degrades dramatically: cracks and cavities protrude into the metallization layer towards the silicon substrate. This decreases the effective cross-section of the film, thus leading to the observed increase in sheet resistance (see Fig. 1). The microstructural evolution for diodes cycled in pure nitrogen shows very similar features and more details can be found in [3,4]. No distinguishable difference in the microstructural evolution between the diodes cycled in ambient atmosphere at RH = 50% and RH = 95% is found.

3.3. Texture analysis

An EBSD map displaying the initial microstructure of the surface of Al metallization can be seen in Fig. 4, demonstrating a dominant (111) texture. The grain size distribution of the metallization is presented in Fig. 5. It shows a maximum occurring at approximately 15 μm^2. This corresponds to a mean diameter of 4.2 μm for a circular grain which is slightly larger than the metallization thickness of 3.4 μm. Both the observed grain texture and grain size distribution corresponds well to the typical texture of Al films on Si [9,10,14–16]. EBSD is a highly surface sensitive technique. Therefore, it is not possible to obtain EBSD data of cycled diodes due to the severe surface roughening occurring during cycling. In this regard, XRD can be used as a complementary method for acquiring information about the texture of the metallization as the number of cycles increases.

In Fig. 6 XRD measurements of the metallization before and after cycling are presented. It can be seen that during cycling, the texture changes from a strong (111) orientation towards a more randomly oriented polycrystalline film. The intensity of the (111) peak decreases significantly during cycling in a similar manner both for RH = 50% and RH = 95%, while peaks corresponding to the (200) and (311) crystallographic planes appear and increase in intensity with the number of cycles. When comparing to earlier XRD results for the cycling in nitrogen (see ref. [4]) it can be concluded that the overall tendency of the texture

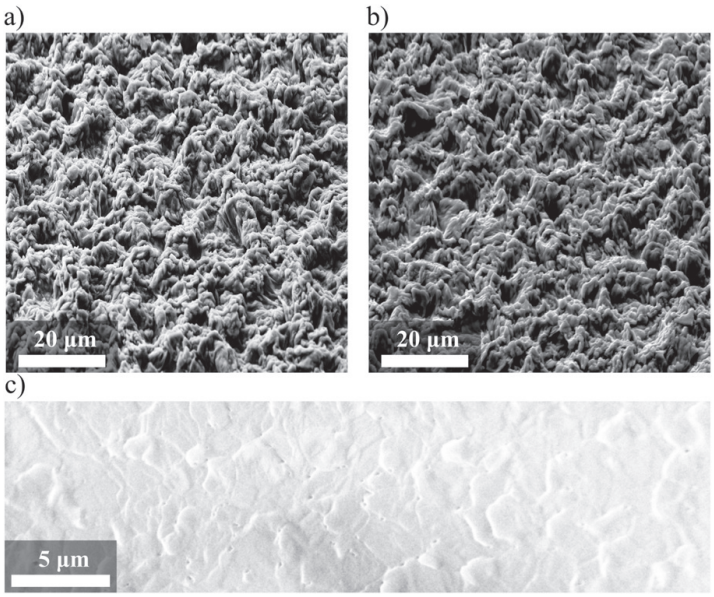

Fig. 2. SEM images of the metallization surface of diodes cycled in ambient atmosphere a) after 93 kilocycles at RH = 95%, b) after 110 kilocycles at RH = 50%, and c) the metallization surface of an uncycled diode.

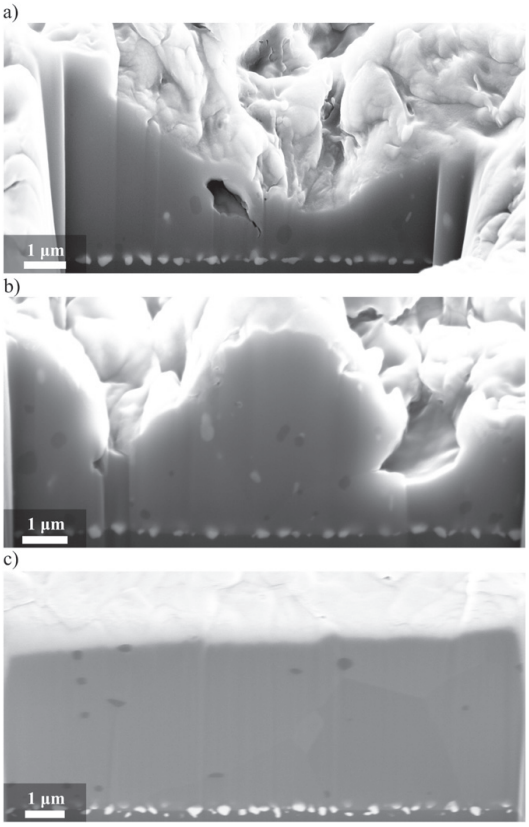

Fig. 3. Cross-sectional SEM images of metallization with wells obtained by focused ion beam milling a) after 93 kilocycles at RH = 95%, b) after 110 kilocycles at RH = 50%, and c) for an uncycled diode.

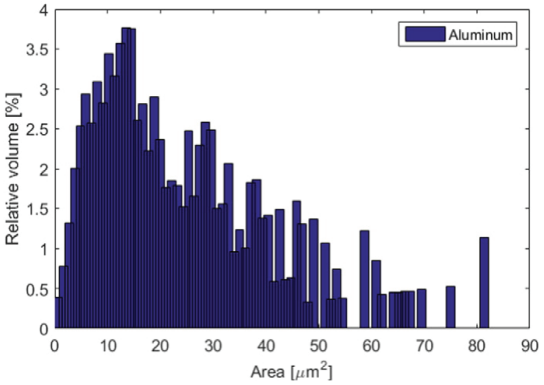

Fig. 5. Histogram of the grain area for an uncycled diode extracted from the EBSD map shown in Fig. 4(a).

change during cycling appears to be similar in all cases. The changes observed in the XRD spectra seen in Fig. 6 originate from the observed severe strain and plastic deformation of the films (see Figs. 2, 3), which can cause rotations in the orientations of the grains [17].

3.4. Analysis of oxide layer

During thermal cycling, EDX measurements were performed to monitor the amount of oxygen in the metallization as the number of cycles increases. This allows for tracking of aluminum oxides and hydroxides which might form due to reactions with atmospheric oxygen and water vapor. The results are presented in Fig. 7. It can be seen that the amount of oxygen increases significantly during cycling and it rises at faster rates for the diodes cycled in ambient atmosphere at RH = 95% (H1 − H3) compared to diodes cycled at RH = 50% (A1). The difference in the amount of oxygen between the two RH values might be explained by the additional formation of hydroxide and transformation of the oxide to hydroxide [18]. The thickness of natural oxides on aluminum is known to be around 3–6 nm [18], which means that the oxide layer itself will not notably increase the sheet resistance by decreasing the effective cross-section of the metallization.

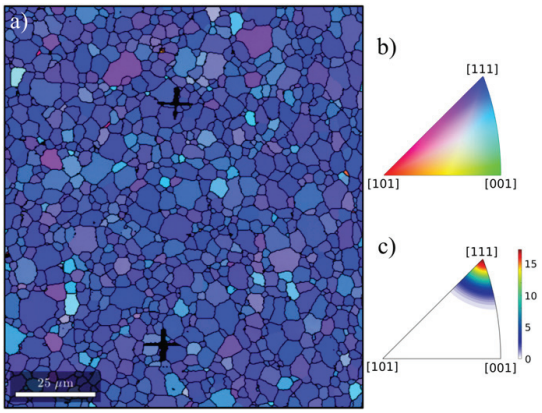

Fig. 4. a) EBSD map of Al metallization for an uncycled diode, b) the corresponding orientation coloring, and c) an inverse pole figure. The black crosses in a) are marks for alignment purposes.

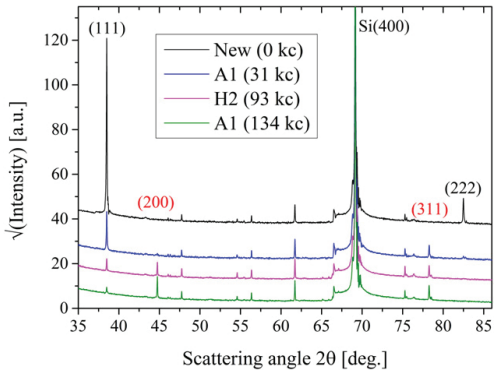

Fig. 6. XRD scans for a diodes cycled in ambient atmosphere at RH = 50% (A1) and RH = 95% (H2). The broad and intensive peak at 68° and other smaller unlabeled peaks are related to Si. All peaks related to the Al metallization are labeled according to crystallographic planes, such that black corresponds to peaks with decreasing intensity during cycling, and red corresponds to peaks with increasing intensity.

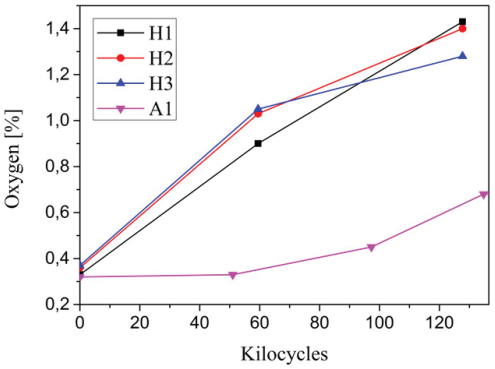

Fig. 7. Amount of oxygen in the metallization of diodes cycled in ambient atmosphere, measured by EDX at an acceleration voltage of 10 kV. H1–H3 correspond to RH = 95% and A1 to RH = 50%.

A single measurement for a diode cycled in pure nitrogen was made after 335 kilocycles corresponding to a relative change in sheet resistance of $R/R_0 = 1.43$. This measurement showed an oxygen amount of 0.5%, which is significantly lower than the diodes cycled in ambient atmosphere. The diode had at the time of the measurement been stored in ordinary atmosphere for a prolonged time, such that the entire surface of the metallization was covered with naturally forming oxides. This could indicate an oxidation mechanism where the material along the cracks that are forming during the tensile phase of the thermal cycle oxidizes, thus making a layer of oxide penetrate into the film along the crack boundaries. A degradation model based on such a mechanism has recently been proposed by Martineau et al. [7]. From this model, which is based on an analytical diffusion model by Gao et al. [19], one might expect a higher rate of degradation under cycling in ambient atmosphere compared to pure nitrogen. However, this is in contradiction with the results reported in this paper, where an opposite tendency is observed. This contradiction is discussed below.

4. Discussion

Results from the electrical and microstructural characterization show a tendency that the degradation of Al metallizations occurs slower in ambient atmospheres than in nitrogen. Also, it is observed that the diodes cycled in ambient atmosphere have noticeably higher amounts of oxygen present in the metallization than diodes cycled in pure nitrogen. The apparent contradiction between these observations might be explained by the mechanical properties of the aluminum oxide residing in the cracks propagating into the metallization. It has been reported in earlier studies that such oxide layers can act as constraints on the dislocation movement in thin metal films [20–22] and severely change the dominant type of dislocation movement. This type of dislocation constraint from the naturally forming oxide layers might lead to a more mechanically stable metallization, thus resulting in an overall increased reliability in spite of the non-conducting properties of the involved oxides.

A relatively large spread in the sheet resistance measurements for the diodes cycled in ambient atmosphere under high humidity probably indicates a spread in production quality of the Al film across the wafer. However, to draw final conclusions, the thermal cycling under high humidity must be continued and statistics needs to be improved. Until this point, corrosion effects stemming from higher humidity levels in ambient atmosphere have not been observed to affect the sheet resistance or microstructural evolution, and it can be concluded that corrosion plays a minor role at earlier stages of the metallization degradation.

It is known that the initial microstructure of Al metallization plays an important role in the degradation process [9], and this has been examined by EBSD measurements. The data show that the metallization initially has a strong (111) texture with a mean grain diameter of approximately 4 μm. From XRD measurements, it is seen that the (111) peaks gradually and quickly decrease in intensity, while peaks corresponding to (200) and (311) appear and increase in intensity with the number of cycles. It can be concluded that the structural changes, as follows from XRD studies, are overall similar for all the three different cases of atmospheric conditions.

5. Conclusion

To examine the influence of environmental factors on the degradation of Al metallization, high power diodes have been cycled under different atmospheric conditions. The first conclusion which can be drawn is that for all types of cycling the thermal degradation and film reconstruction undergo in a similar way, i.e. the mechanisms are essentially the same. Nevertheless, the experimental data show a tendency that cycling in ambient atmosphere yields a slower degradation compared to cycling in pure nitrogen. A possible reason could be the formation of an aluminum oxide layer on the grains that might constrain the dislocation formation and their following development into cracks.

The thermal cycling under high humidity conditions indicates that moisture does not affect much the degradation process in regard to sheet resistance and microstructural evolution, i.e. corrosion does not play any major role at the initial stage of the metallization reconstruction. However, further study with an increased number of cycles will be performed to clarify the role of humidity.

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APPENDIX D: STRENGTH AND RELIABILITY OF LOW TEMPERATURE TRANSIENT LIQUID PHASE BONDED CU-SN-CU INTERCONNECTS

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Strength and reliability of low temperature transient liquid phase bonded Cu—Sn—Cu interconnects

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ABSTRACT

As power electronic devices have tendencies to operate at higher temperatures and current densities, the demand for reliable and efficient packaging technologies are ever increasing. This paper reports the studies on application of transient liquid phase (TLP) bonding of Cu—Sn—Cu systems as a potential technology that could enable the realization of stacks with better thermal performance and reliability than those can be achieved using conventional soldering techniques. Low temperature TLP bonded Cu—Sn—Cu samples are fabricated, and the strength of the achieved bonds is measured by shear testing. Micro-sectioning and optical microscopy studies of the samples reveal that the TLP bonds show good homogeneity with a small number of voids at the interface. Energy dispersive X-ray analysis is applied to examine at what rates Sn is converted into Cu—Sn intermetallics since a full conversion is critical for achieving a strong and high temperature resistant bond. Finally, initial results from a thermal cycling test are presented and it is concluded that the achieved TLP bonding is a promising candidate for the fabrication of reliable interconnects in power electronics.

1. Introduction

As Si-based power devices today tend to be used at higher current densities and new semiconductor materials such as SiC and GaN are more widely used in power electronics, thermal capability of the packaging becomes a key limiting factor in producing reliable power electronic devices. One way to improve the thermal capability and reliability of the thermal stack is to apply new bonding techniques such as silver sintering [1] or transient liquid phase (TLP) bonding [2, 3] as alternatives to the conventional reflow soldered joints.

This paper focuses on the fabrication and characterization of low temperature TLP bonded Cu—Sn—Cu systems, which are applicable in power electronic packaging as a potentially superior alternative for soldered interconnects. In the low temperature range, the stable Cu—Sn intermetallics (IMCs) are the Cu rich Cu_3Sn and the Sn rich Cu_6Sn_5 [4–6]. A total conversion of the Sn into these compounds is an important point for the thermal stability and strain relaxation in the bonds and ultimately to achieve a strong and reliable bond [7–9]. To address these issues, TLP bonded Cu—Sn—Cu sandwich-like structures are fabricated and investigated using shear tests and various characterization techniques. Furthermore, to give insights into the reliability of the TLP bonds, initial results from a thermal cycling test of the fabricated structures are presented.

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2. Experimental procedure

2.1. Sample fabrication and shear testing

Samples were fabricated using a combination of commercially available Sn coated Cu and non-coated Cu plates with lateral dimensions of 20 mm × 20 mm and thickness of 1 mm. Several small pieces of Sn coated Cu were placed on larger Cu plates. These pieces had dimensions of 2.3 mm × 2.3 mm and thickness of 0.8 mm. The coating thickness of the Sn layers was 5 μm, thus allowing for an interlayer thickness of 5 μm or 10 μm depending on the choice of the larger Cu plates (uncoated or coated with Sn).

After initial rinsing and placement of nine small Cu pieces onto Cu plates the samples were bonded in an air-driven press that could provide a maximum pressure of 25 MPa. A hard bottom tool and a soft silicone top tool were used, so that the samples experienced hydrostatic pressure and such that any small misalignment of the press and samples would not influence the pressure distribution between samples, as illustrated in Fig. 1(a, b). The bottom and top tools of the press were preheated to the desired temperature before the placement of the samples, the pressure was released without an intermediate cooling stage, and the samples were quickly removed after the pressing for cooling down on a metal surface. This means that a given bonding time corresponds to both the time at which a sample was under pressure and at elevated temperature, as illustrated in Fig. 1(c). The main reason to ensure a high heating rate of the samples was to avoid void formation at

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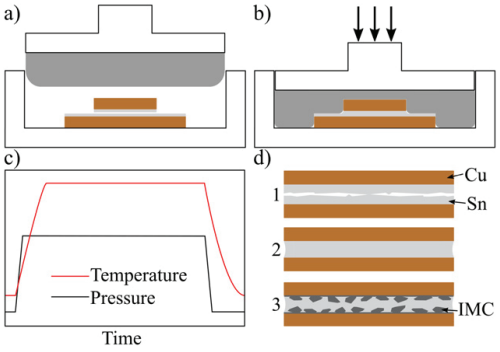

Fig. 1. Schematics of the fabrication procedure. a) Samples placed on the hard bottom tool before pressure is applied, b) soft silicone (grey in colour) applies hydrostatic pressure to the sample during bonding, c) illustration of the temperature and pressure profile during the bonding procedure. d) Illustrates three different phases during the TLP bonding process, 1 - contact phase, 2 - melting phase, and 3 - IMC formation and solidification.

the interface due to premature IMC conversion of the thin Sn layer [10]. Fig. 1(d) illustrates the different phases during the TLP bonding process. In phase 1 the samples are in contact but Sn is still solid, in phase 2 Sn melts and bond is forming, and in phase 3 the isothermal solidification and growth of the IMC's at the Cu—Sn interfaces occur.

To find the optimal TLP bonding parameters, the strength of the bonds was tested by shearing the small pieces located on the larger Cu plates. The shear test was performed using a standard procedure on a XYZTEC Condor Sigma series bond tester. For every fabrication parameter, a minimum of nine bonded pieces were sheared.

2.2. Interface analysis

After the initial fabrication and shear tests at a broad variety of parameters, a narrow set of fabrication conditions was found and samples for cross-sectioning analysis were produced. The cross-sectioning was performed by epoxy moulding, cutting and polishing until the interface of interest was reached using a similar procedure as described in [11]. Then, different characterization techniques such as optical microscopy, scanning electron microscopy (SEM) and energy dispersive X-ray analysis (EDX) were applied.

2.3. Thermal cycling

The goal of the thermal cycling test was to address the reliability aspect of the TLP bonded interfaces. The samples were 20 mm × 20 mm Cu plates that were TLP bonded onto a polished standard Al_2O_3 based direct bonded copper (DBC) substrate. Eight TLP bonded samples were fabricated with a bonding time of 60 min, temperature of 255 °C, and pressure of 25 MPa. The use of a DBC was to ensure a mismatch of the thermal expansion coefficients such that the TLP bonded interfaces were severely stressed during the thermal cycles. Additionally, eight otherwise similar samples only with silver sintered bonds and a process time of 10 min were fabricated. The point of these samples was to serve as a reference and comparison for the TLP bonded samples, since a larger body of literature already exists demonstrating a good reliability of silver sintered interconnects [12–15]. The thermal cycling was performed using a standard thermal shock test in the temperature range from −40 °C to +150 °C with a cycle period of 60 min. After 250 cycles the samples were removed and analyzed by scanning acoustic microscopy (SAM). At this number of cycles, it was unfortunately found that the DBCs had prematurely failed by cracks in the ceramics and delamination of the bottom copper layer, which is a known problem for DBC's under high temperature cycling conditions [16,17].

3. Results

3.1. Shear test

The shear strength for different bonding times is shown in Fig. 2. For longer bonding times the strength of the interlayer is seen to increase, with mean values reaching 90–95 N/mm^2 for both times above 60 min. These values are in good agreement with other TLP bonded Cu—Sn—Cu system reported earlier [18]. The shear values for different bonding pressures can be seen in Fig. 3. Higher pressures result in stronger bonds and the maximum shear values are reached at the maximum pressure of 25 MPa used for the press. Samples with a bonding temperature of 280 °C were also fabricated but revealed little to no difference in shear strength compared to 255 °C.

3.2. Optical microscopy

The cross-sectioning was carried out on six different samples. For all samples the bonding pressure was 25 MPa while the varying parameters were the bonding time and interlayer thicknesses. This choice of parameters allows to analyse the formation of the Cu—Sn intermetallic compounds and its dependence on different fabrication conditions.

The optical micrographs of the polished interface layers are shown in Fig. 4. For all the interfaces a small number of voids can be observed as dark spots at the interface. They can most likely be attributed to contaminations and remaining oxide films [18] in combination with the surface roughness of the Cu plates. For the bonding time of 10 min (see Fig. 4(a, b)) it can be observed that there remains unconsumed Sn in the middle of the interfaces indicated by light bluish colour. Cu_3Sn and Cu_6Sn_5 IMCs are shown in darker bluish and these compounds dominate at the interfaces shown in Fig. 3(c–f). Thus, for the bonding times of 60 min and 180 min the Sn is fully consumed and only the IMCs are present at the interface.

3.3. EDX analysis

EDX analysis with an acceleration voltage of 20 kV was applied to reveal the details about IMCs and their ratio at the interfaces, which could not be distinguished in the optical micrographs. The EDX results for the interlayer thickness of 5 μm and bonding time of 60 min can be seen in Fig. 5. The line-scan in Fig. 5(b) reveals that the solid-state diffusion process has exhausted and the interface purely consists of the Cu rich Cu_3Sn IMC having Sn weight percent of 38 [10]. The results for the interlayer

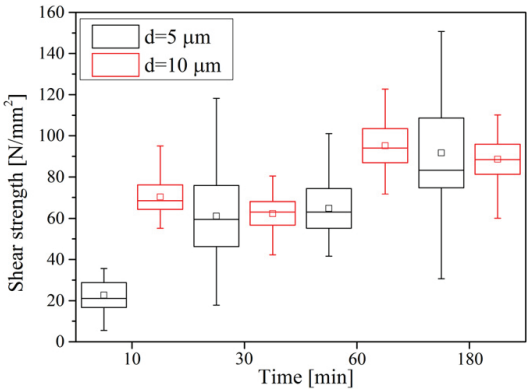

Fig. 2. Shear strength of Cu—Sn—Cu samples for different bonding times, pressure of 25 MPa and temperature of 255 °C. The squares represent the mean value, the lines correspond to minimum and maximum values and the box and line within represent the standard deviation and median value, respectively. The measurements are carried out for two thicknesses (d) of Sn layer of 5 and 10 μm.

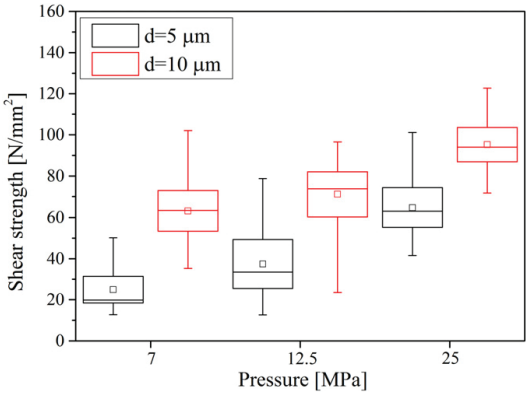

Fig. 3. Shear strength of Cu—Sn—Cu samples with different bonding pressures, time of 60 min and temperature of 255 °C. Squares, boxes and lines have the same meaning as in Fig. 1.

thickness of 10 µm are shown in Fig. 6. Here, it can be seen that the solid-state diffusion process has not been exhausted and the Sn rich Cu_6Sn_5 IMC with a weight percent of 60 [10] is still present in the middle of the bond where it is surrounded by the Cu rich Cu_3Sn IMC.

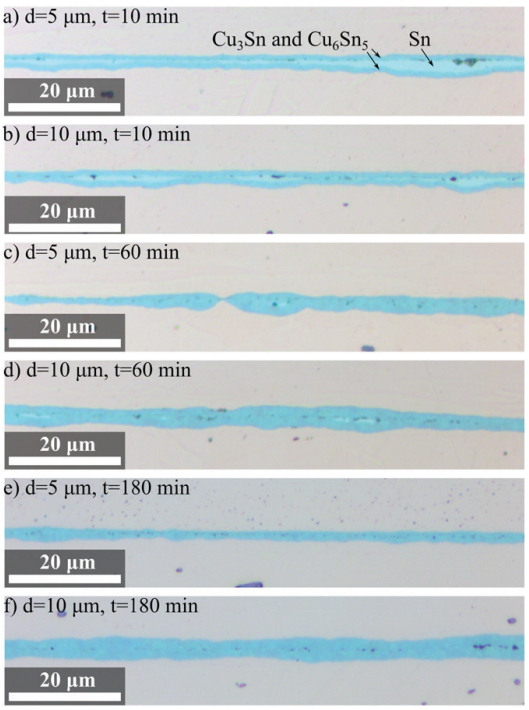

Fig. 4. Optical micrographs of the Cu—Sn—Cu interlayer for different bonding times (t) and interlayer thicknesses (d) with a constant temperature of 255 °C and pressure of 25 MPa.

3.4. Thermal cycling and SAM analysis

SAM analysis was performed on the samples before thermal cycling and after 250 cycles. Results from the SAM analysis can be seen in Fig. 7. The almost black colour in the fully bonded region of the TLP bonded samples (see Fig. 7(a, b)) is a result of the very small reflection at the TLP interface, which is due to the lack of any rapid changes of the density due to the diffusion of the materials during the bonding process. For the silver sintered samples (see Fig. 7(c, d)) the fully bonded region can be seen as a dark grey colour, which is due to the abrupt change in density from the Cu to the sintered silver layer and can therefore not be attributed to a lower quality of the bond region compared to the TLP bonded samples. At both 0 cycles and 250 cycles the TLP bonded samples show good-quality homogenous bonds, albeit some edge effects are present and a very small number of minor voids in the bonds can be seen. The main change after cycling is that the not fully bonded areas near the edges (grey in SAM image) seen at 0 cycles can be seen to change into fully detached areas (white in SAM image) after 250 cycles. A decrease of the dark area that was fully bonded before the thermal cycling began cannot be observed after 250 cycles, thus showing an apparent good thermal cycling capability of the fully TLP bonded region. The bonds of the silver sintered samples can be seen to change significantly during the cycling, since after 250 cycles larger areas are delaminated along the edges and sides of the samples, resulting in a notable change of the effective area of the remaining bond region.

4. Discussion

The fabricated samples show a small number of voids in the interface areas, which are visible both in the optical micrographs and in the SEM images presented in Fig. 5 and Fig. 6, respectively. Interfaces without voids are not achieved, and this is typical issue for TLP bonding of Cu—Sn—Cu systems [10,18]. These voids, however, do not seem to severely degrade the shear strength of the obtained bonds because the shear values are found to be comparable to the values from literature. SAM measurements reveal that large in area homogenous bonds can be achieved but getting the bond to extend all the way to the edges of the sample can be challenging.

Unfortunately, the thermal cycling of the samples had to be prematurely stopped due to failures related to the DBC substrate but not the TLP bonded interfaces. For future examinations, this could be prevented by choosing a DBC that is more reliable under thermal cycling than the standard Al_2O_3 type used here or by confining the backside of the DBCs by bonding them onto a thicker baseplate to avoid any bending of the DCBs during cycling. The results from the thermal cycling test, although not definitive, shows that the TLP bonded samples reveal very good resistance to the cycling test and in our case exhibit better thermal cycling capabilities than the silver sintered bonds.

5. Conclusion

To examine the strength and reliability of TLP bonded Cu—Sn—Cu systems, samples with different fabrication parameters have been produced and characterized. After optimization of the bonding process, the samples are analyzed using several experimental methods demonstrating overall good homogeneity of the bonds both across the area and through the cross-section of the interfaces with only a small number of voids, which are typical for this type of process. These voids are not found to affect the bond strength significantly, which is comparable with the literature values for the state-of-the-art industrial interconnects. Investigation of the composition shows the ratio of different IMCs and their dependence on the interlayer thickness as well as on the fabrication parameters providing clear recipes for the good-quality bonding.

The thermal cycling test reveals that homogeneity of the TLP bonds preserves after 250 cycles with no additional defects formed on the

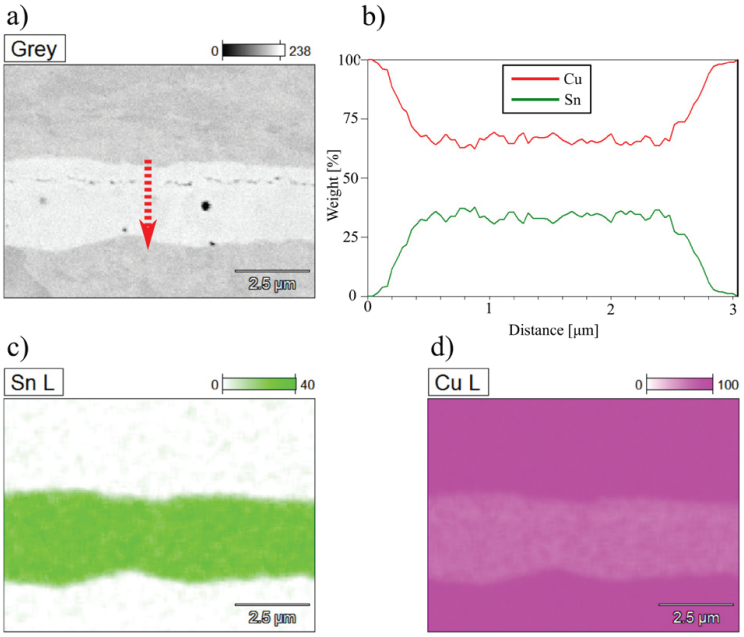

Fig. 5. Results for sample with d = 5 µm, bonding time of 60 min and pressure of 25 MPa. a) SEM image of the area examined by EDX, b) line scan along the direction indicated in a) showing composition of the interface, c) colour diagram for weight percent of Sn and d) colour diagram for weight percent of Cu.

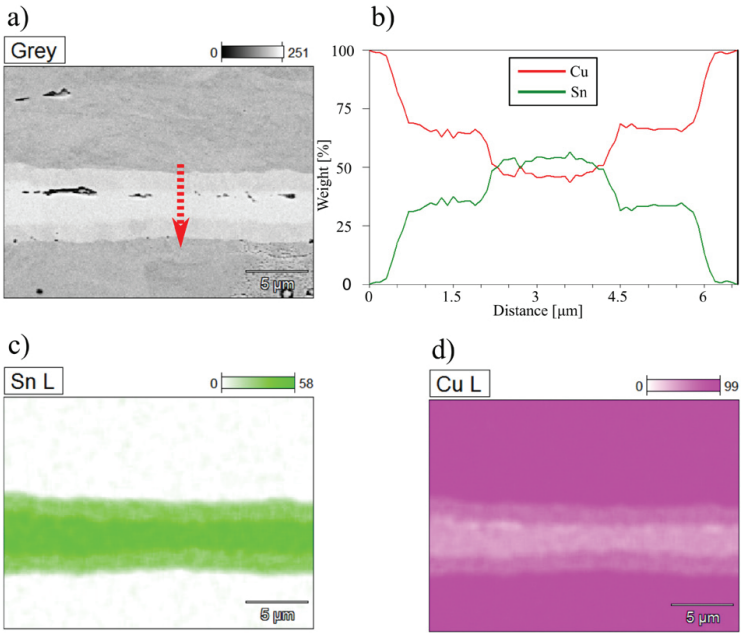

Fig. 6. Results for sample with d = 10 µm, bonding time of 60 min and pressure of 25 MPa. a) SEM image of the area examined by EDX, b) line scan along the direction indicated in a) showing composition of the interface, c) colour diagram for weight percent of Sn and d) colour diagram for weight percent of Cu.

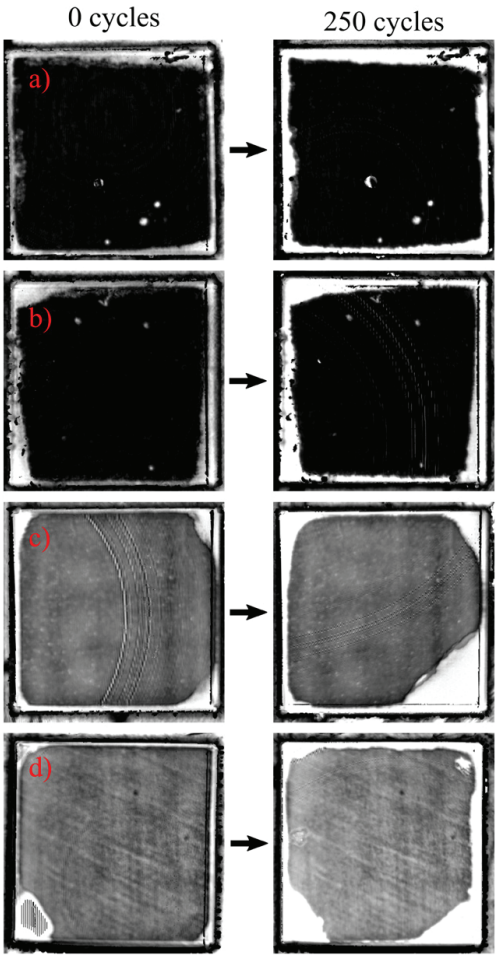

Fig. 7. SAM images of (a, b) two TLP bonded samples and (c, d) two silver sintered samples at 0 and 250 thermal cycles. The arcs seen in c) at 0 cycles and b) at 250 cycles are image artefacts from the SAM measurement.

micron scale. Unfortunately, thermal cycling of TLP bonds until damage was not realized due to the failure of DBC substrates. However, comparison of the TLP bonded Cu—Sn—Cu systems with the bonds formed by standard silver sintering after the thermal test shows that the former ones are more robust. These results allow to conclude that the suggested approach on TLP bonding using Cu—Sn—Cu is a promising method for the fabrication of reliable interconnects in power electronics. However, a deeper study of reliability of this type of bonds is required.

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APPENDIX E: THERMO-MECHANICALLY INDUCED TEXTURE EVOLUTION AND MICRO-STRUCTURAL CHANGE OF ALUMINUM METALLIZATION

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Thermo-mechanically induced texture evolution and micro-structural change of aluminum metallization

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Abstract
During operation of high power electronic chips the topside metallization is subjected to cyclic compressive and tensile stresses leading to unwanted thermo-mechanical fatigue of the metallization layer. The stress is caused by the difference in the thermal expansion coefficients of the metallization and the semiconductor underneath that can lead to a severe structural degradation of the layer changing the electrical characteristics of the electronic chips, finally causing a failure. Although this problem is well-known, the underlying physical mechanisms governing this fatigue phenomenon are not yet fully understood. In this work, we investigate the microstructural evolution of an Al metallization on high power diode chips subjected to passive thermal cycling between 20 and 100 °C. The texture of the Al film is analyzed ex-situ by a combination of electron backscatter diffraction and X-ray diffraction. It is found that the initial dominating (111) orientation of Al grains in the film changes towards a (311) texture as the number of cycles increases. A simple model explaining the driving mechanism behind the crystallographic re-orientation is proposed. Also, large orientation gradients within individual grains are found to arise during thermal cycling, which results in sub-grain formation. These processes are the dominant mechanism for the degradation of the Al layer structure leading to the formation of voids and significant increase of the surface roughness.

1 Introduction

Aluminum is widely used as the topside metallization in power electronic chips. Due to the differences in coefficients of thermal expansion between the silicon composed chips and aluminum, the metallization is subjected to cyclical thermo-mechanical stress during the life time of the device operating under AC conditions or on-off DC conditions. This typically leads to severe surface roughening and void formation in the film reducing the reliability and expected life time of the device [1, 2]. Several studies have examined metallization fatigue covering different cases like cyclical bending on compliant substrates at room temperature [3, 4], passive thermal cycling [5–13, 15], and active power cycling [16–20]. Depending on the temperature range of the thermal cycling different combinations of diffusion induced mechanisms and models based on dislocation movement have been proposed to explain the degradation of aluminum metallizations. Grain growth has been observed and studied by transmission electron microscopy (TEM) when cycling at high temperatures up to 450 °C [5, 6]. Other studies have shown that dislocation-based plasticity can cause formation of sub-grain boundaries followed by diffusion driven grain boundary grooving and surface roughening when cycling in the same temperature range [19]. Hillocking have also been observed as one more relevant phenomenon even at a relatively low temperature of 220 °C [10] becoming more dominant at higher temperatures [25, 26]. Severe surface roughening, void formation and texture change have been found for passive thermal cycling in the temperature range from 20 to 100 °C [13, 15]. It has been shown in [15, 21] that atmospheric conditions (cycling in dry nitrogen or air with 95% relative humidity) do not play a dominating role in the degradation process.

Studies covering the texture evolution of aluminum metallizations are not very many in literature but using electron backscatter diffraction (EBSD) it has been observed that an initial dominating (111) texture of polycrystalline aluminum films evolves towards (211) under thermal cycling from room temperature to 450 °C [9]. When analyzing individual

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grains, it is found that larger ones can have orientation gradients of up 4° already after 25 thermal cycles [11]. The findings of [9, 11] are explained by a combination of dislocation glide and diffusion-induced interfacial dislocation core spreading. Generally, a consistent model and interpretation of the physical mechanisms governing the degradation of aluminum metallizations are not yet fully realized partially due to the fact that many results available in literature are obtained for much higher temperatures than those typical for ordinary operating conditions of power electronic devices.

This work will analyze the micro-structural change and texture evolution of the aluminum metallization of power diode chips during passive thermal cycling between 20 and 100 °C using a combination of EBSD and XRD analysis. This temperature range is close to the normal operating conditions of typical power electronic devices, and the results should therefore be directly applicable to the degradation and reliability predictions of power electronic chips. EBSD is very sensitive to surface roughness because it decreases the quality of the electron diffraction pattern and therefore also the indexing probability. Thus, EBSD can only give insights into the subtle micro-structural changes in the beginning of the thermal cycling before significant surface roughening occurs. XRD, however, can give information about grain orientation of the metallization even after severe surface roughening occurring at high number of cycles. It should also be noted that while EBSD gives access to information about individual grains, XRD is an ensemble method measuring many grains simultaneously. Thus, combining these two techniques provides a more complete picture of the texture evolution and micro-structural change of the metallization.

2 Experimental procedure

High power commercial diode chips rated for 100 A and 1200 V were thermally cycled in ambient atmosphere using a custom setup based on a thermo-electric cooler [21]. The area of the square metallization was approximately 81 mm^2 and the thickness of the layer was around 3.4 µm [13]. The thermal cycles were run between 20 and 100 °C with a period of approximately 30 s and a triangular thermal waveform. The change in stress value can be estimated by the formula $\sigma = \Delta\alpha \cdot \Delta T \cdot M$, where $\Delta\alpha$ is the difference in thermal expansion coefficient between the film an substrate, ΔT is the temperature variation, and M is the biaxial modulus of the film [14]. This results in a change of the stress value σ of approximately 171 MPa, using standard values for (111) oriented aluminum on silicon and $\Delta T = 80$ K. The running time of the thermal cycling experiment exceeded several months with a total cycling time of the most stressed sample (314 kilocycles) reaching approximately 110 days. After a certain number of cycles the chips were removed from the setup and EBSD or XRD analysis was performed ex-situ. The EBSD measurements were done using a step size of 0.25 µm on an area of 100 µm × 100 µm. Using focused ion beam milling, alignment crosses were formed on the surface such that the same area could be measured after different number of cycles allowing to address evolution of the same grains. The alignment crosses can be seen in Fig. 1a–c. For data analysis and for producing pole figures from the EBSD measurement, the commercial software MatLab was used in conjunction with the openly available MTEX Toolbox [22]. To remove noisy pixels from the EBSD datasets, a median smoothing algorithm with a 3 × 3 window was applied. The grain angle separation was set to 5° for the data analysis. XRD measurements were performed using a PANalytical Empyrian X-ray diffractometer and pole figures were calculated using the supplied software package.

3 Results and discussion

3.1 Results

EBSD maps of the metallization can be seen in Fig. 1a–c. Using the orientation coloring presented in Fig. 1d it can be observed that (111) orientation dominates from 0 to

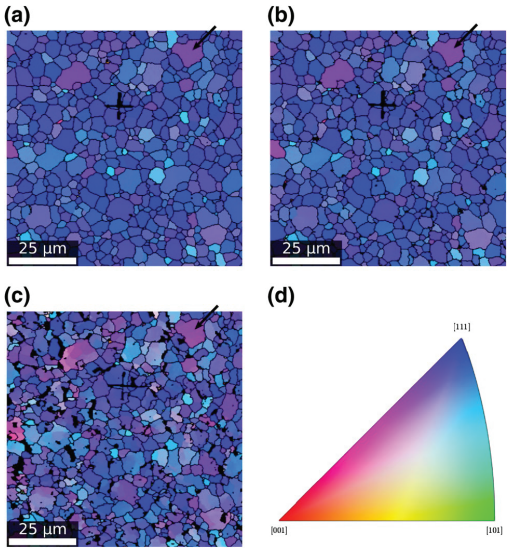

Fig. 1 EBSD maps for diode metallization: after **a** 0 cycles, **b** 1353 cycles, and **c** 3433 cycles. **d** Shows the corresponding orientation coloring. The arrows in the EBSD maps indicate the grain for which the internal orientation gradients is analyzed in Fig. 4. (Color figure online)

3433 cycles. The average grain size has been calculated to be 15 μm^2 which corresponds to a mean grain diameter of 4.2 µm for a circular shape. It was also found that there was a large spread in the size of grains and we refer the reader to our earlier work [15] for a grain size histogram. Comparing 0–1353 cycles shows almost no difference, however, at 3433 cycles a micro-structural change can be clearly seen along with added noise due to surface roughening. All grains including those being completely homogeneous at 0 cycles can be seen to have an increase in internal orientation gradients.

In Fig. 2 inverse pole figures and pole figures extracted from EBSD measurements are shown. A strong (111) texture can be seen in Fig. 2a at 0 cycles and it persists until the maximum number of cycles reached in these experiments (5477) where EBSD measurements could still be performed (see Fig. 2c). However, the (111) signal becomes less pronounced. Its maximal intensity of around 16 in the pole figure for 0 cycles decreases to approximately 7 in the pole figure for 5477 cycles.

To examine the evolution of crystallographic orientation of the metallization and the apparent movement away from the initial (111) orientation, XRD measurements are performed. An evolution of XRD spectra for passive thermal cycling under the same conditions as those used in the current work were earlier discussed in [14] demonstrating that the peak related to (111) gradually disappears while peaks of (200) and (311) increase in intensity. We find the same tendency for the current experiments and, therefore, we present only the data for the samples run to the very high number of 317 kilocycles. These results are shown in Fig. 3 as pole figures and inverse pole figures. In Fig. 3a corresponding to 0 cycles, the same strong (111) texture as observed by EBSD (see Fig. 2a) can be seen. However, when 317 kilocycles are reached the initial (111) texture is almost completely gone (see Fig. 3b). Instead, a dominating (311) orientation is evident. It is known from earlier works, for example [9], that the texture of Al films on Si substrates tends to evolve towards a (211) orientation under thermally-induced stresses. To examine if there is a similar tendency in our case, (422) pole figures are also measured. Substitution of (211) by (422) is necessary because the (211) reflex is forbidden for X-ray diffraction from structure factor considerations of a face-centered cubic (fcc) crystal. However, a (422) pole figure shows qualitatively the same as a (211) pole figure would and it can, therefore, be compared for the initial and cycled sample and used to determine a transition towards a (211) texture. The study shows that there is no such transition because the intensity in the centre of the (422) pole figures stays more or less constant during cycling. It should be noted that the intensity axis for inverse pole figures and pole figures are different for panel a and b. The (111) signal goes from a maximum intensity of 127916 in the pole figure for 0 cycles to 10396 for 317 kilocycles, thus

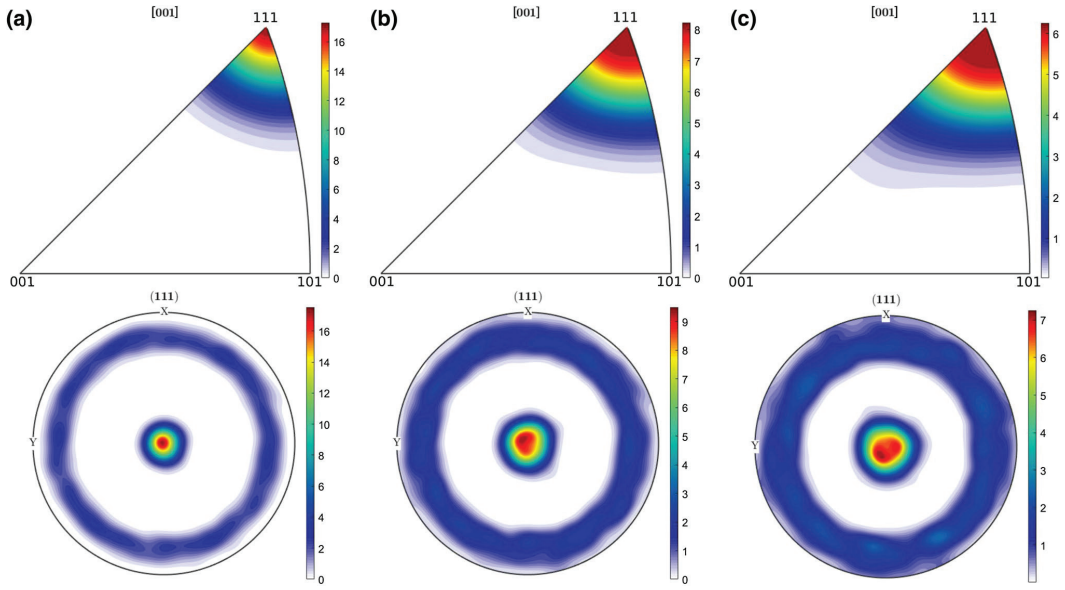

Fig. 2 Inverse pole figures and pole figures extracted from EBSD maps: after **a** 0 cycles, **b** 3433 cycles, and **c** 5477 cycles. The intensity of the contour plots is given by the color bars in arbitrary units. (Color figure online)

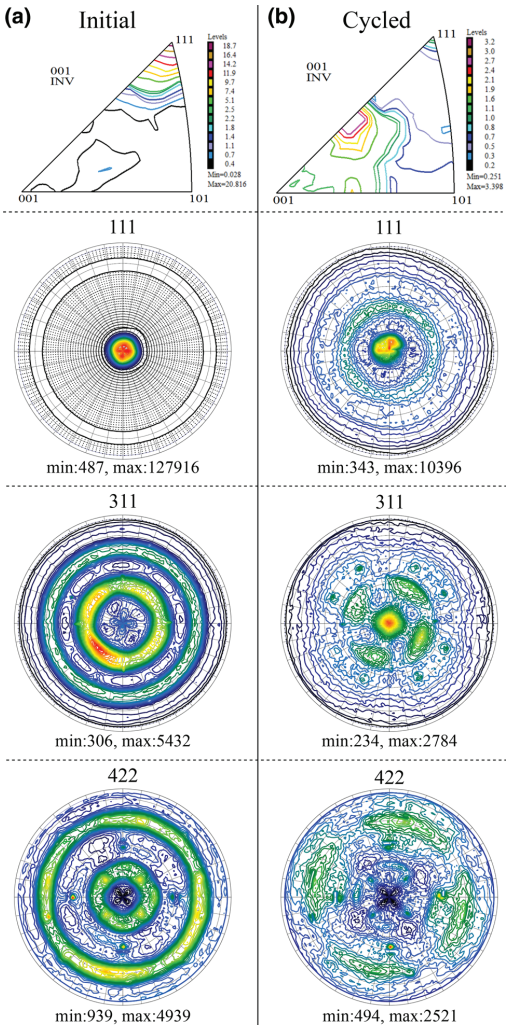

Fig. 3 Inverse pole figures and pole figures extracted from XRD measurements: after **a** 0 cycles and **b** 317 kilocycles. The intensity of the contour plots of the inverse pole figures is given by the color bars in arbitrary units, while the minimum and maximum value are stated below every pole figure. (Color figure online)

decreasing more than one order of magnitude. Conversely, the (311) signal clearly increases from around 0 for 0 cycles to 2784 for 317 kilocycles.

To further examine the reorientation dynamics, individual grains are tracked at different number of cycles and the orientation gradients within the grains are measured using EBSD. A significant number of individual grains are analyzed and results for one of these grains are shown in Fig. 4. This particular grain was chosen due to its size and low noise level in the images. The position of this grain is indicated by the black arrows in Fig. 1a–c. Initially, as can be seen from Fig. 4a, the grain has internal misorientation of below 1° with respect to the mean orientation of the grain but as the number of cycles increases, distinct areas of the grain start reorienting away from the orientation of the mother grain. By analyzing how the grain shown in Fig. 4 is positioned relative to its neighbor grains (see Fig. 1), it can be seen that the orientation first changes near the grain boundaries and especially the triple junctions and then the changes affect the interior of the grain during the later stages of cycling. As for the texture change (see Fig. 2) the reorientation happens slowly in the beginning of the thermal cycling (from 0 to 1985 cycles, see Fig. 4a–c), but from 3433 to 5477 cycles (see Fig. 4d–f) is accelerates and becomes very clear. At 5477 cycles some areas have a misorientation of up to 8°, hence exceeding 5° that is chosen as the grain separation angle in the data analysis. This means that the mother grain has effectively been split up into a number of smaller grains. The above-described observations are representative for all the grains in the area examined by EBSD, which can be confirmed by careful inspection of Fig. 1a–c.

A more quantitative approach to analyze the EBSD data and the aforementioned misorientations for all grains presented in Fig. 1 has been realized. This is done by finding misorientation angles from all pixels in the EBSD image and the mean orientation of the corresponding grains for increasing number of cycles. The obtained dependencies for different number of cycles are presented in Fig. 5. They represent the distribution of the number of pixels misoriented by a given angle from the average orientation of the grain. At 0 cycles the deviation from the mean orientation for all grains is around 0.1°. As the number of cycles increases the width of the misorientation peak increases and the peak position shifts towards higher values. At 5477 cycles an almost flat response from 0.1° to 2° can be observed indicating that all grains analyzed by EBSD undergo reorientation.

3.2 Discussion

Results from the EBSD analysis of the initial stages of thermal cycling show that the metallization undergoes significant micro-structural changes on the scale of individual grains and by producing pole figures it can be seen that the texture of the metallization gradually evolves away from the initially strong (111) orientation. As shown in Fig. 5 all grains undergo misorientation and it increases with number of cycles. By studying individual grains with EBSD it is found that the evolution can be attributed to the sub-grain formation and atomic reorientation within the grains where misorientation angles as high as 8° are found already after approximately 5500 cycles. We believe that this can be

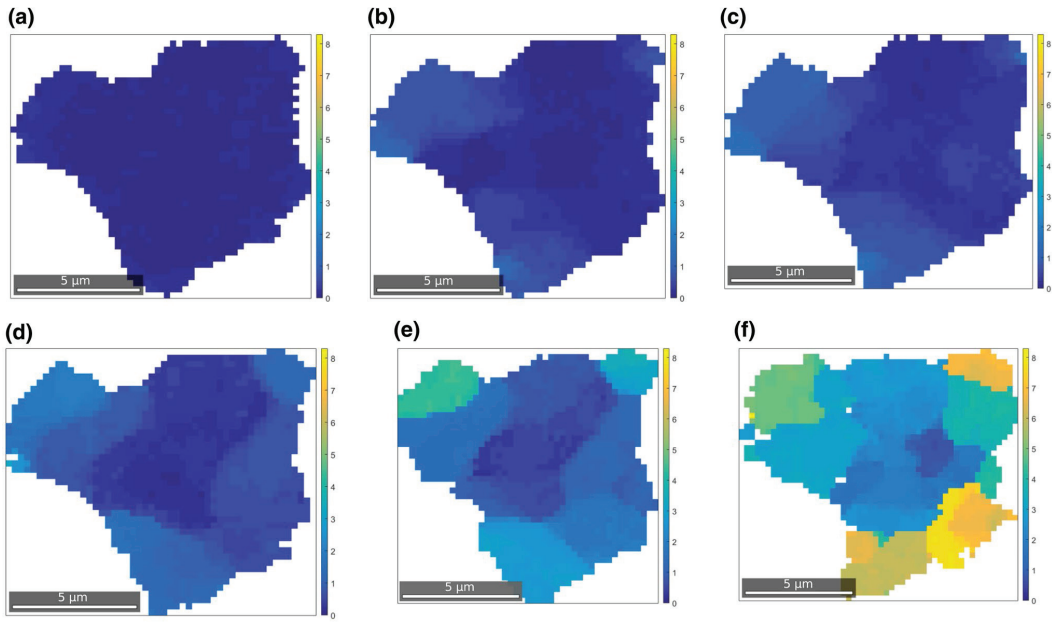

Fig. 4 Orientation gradient within a single grain: after **a** 0 cycles, **b** 1353 cycles, **c** 1985 cycles, **d** 2527 cycles, **e** 3433 cycles, and **f**) 5477 cycles. The colorbar represent the misorientation angle from the mean orientation of the entire grain. (Color figure online)

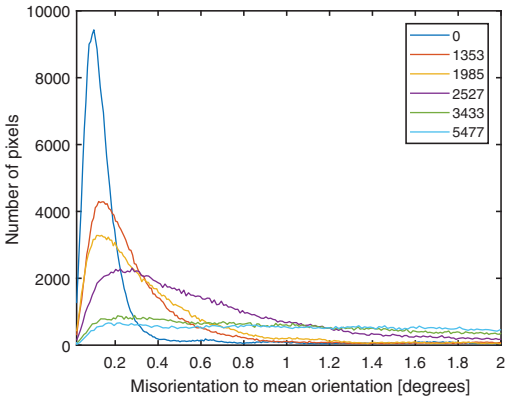

Fig. 5 Change in grain misorientation to mean orientation with increasing number of cycles. The number of cycles is indicated by the legend

explained solely by dislocation plasticity since any diffusion-related processes like hillocking, surface or grain boundary diffusion [23] should not play a significant role because of the low temperature range of the thermal cycling. This statement is also supported by our earlier studies focusing on the change of surface topography for the same temperature cycling range, where none of the aforementioned diffusion-related phenomena have been observed [13, 15, 21].

The splitting of grains into smaller distinct areas with different orientations could be explained by dislocation glide of the inclined (111) crystal planes when constrained by the silicon substrate as suggested in [9, 11]. This model is also consistent with other results showing a large impact of constraining passivation layers on the dislocation movement and, thus, the resulting degradation mechanics [5, 6, 27]. The explanation for the texture evolution from the initial orientation of (111) towards particular (311), as found by the XRD measurements after 317 kilocycles, requires special attention and it is discussed below. In [9] under the cycling at temperatures up to 450 °C a restructuring from (111) texture towards (211) was found and explained by the dislocation glide mechanism in conjunction with the diffusion-induced interfacial dislocation core spreading. The movement towards a (211) texture is also consistent with the well known fact that tensile deformation of unconstrained fcc crystal cause a lattice rotation towards a stable (211) orientation, which have been confirmed experimentally and explained by simultaneous slip in primary and conjugate slip systems [24]. This also holds for a Al film on a Si substrate since it will be in a tensile state from room temperature up

to temperatures around 200 °C [27]. Thus, the Al layer in our case should experience predominantly tensile stresses. It could then be speculated that the introduction of a backside constraint on the system analyzed in [24] (which would make it similar to our case) could lead to the activation of other slip systems for which a final (311) orientation is more energetically favorable. However, such conclusions can not be drawn from the current work and would require further investigation.

To explain the driving force of the crystal re-orientation we propose an alternative and simple model based on basic crystallography. It is known that packing density of atoms is the highest for (111) planes in fcc to which Al belongs. Under the tensile and compressive stresses in the plane parallel to the surface it is energetically favorable for the atoms to reorder to a structure with lower packing density providing better ability for atoms to move within the plane. The reordering of the atoms can occur as a combination of dislocation glide and diffusion processes depending on the temperature range of the experiment. From simple crystallographic calculations it can be found that relative to the packing density of (111) the density ratio for (211) is 0.354 and for (311) it is 0.522 [28]. Thus, the thermal cycling should ideally lead to the packing with the lowest density, i.e. (211). However, in our case the films are cycled only up to 100 °C and this relatively low temperature does not provide enough increase in plasticity or/and low thermal assistance for diffusion processes to fully exhaust the reorientation process. Hence, after 317 kilocycles the grain orientations has not evolved into the ideally optimal (211) texture but rather a (311) texture with a bit higher packing density. Thus, the proposed simple model can explain the driving force for the change in the crystallographic orientation of the grains during thermal cycling. Deeper understanding of the mechanisms governing the evolution towards (311) or (211) requires considering the strain developing in the crystalline grains under the tensile and compressive stresses along with dislocation movement, diffusion processes and resulting plasticity. This will depend strongly on the local conditions for each grain such as grain boundaries, and orientation of neighboring grains and would require a deeper analysis such as e.g. the slip plane analysis performed by Hosford [24] and considerations of the strain energy density, surface energy and interface energy of the film [14].

4 Conclusion

The micro-structural change and texture evolution of the aluminum metallization on top of a standard silicon chip subjected to passive thermal cycling between 20 and 100 °C have been studied by EBSD and XRD analysis. It is found that the initial (111) texture of the aluminum metallization evolves towards a (311) texture with increasing number of cycles. The evolution occurs through gradually increasing misorientation within individual grains leading to the formation of sub-grain boundaries. Eventually the grains split up into separate areas where the misorientation angle can reach 8° already at around 5500 cycles. The internal reorientation in the grains is proposed to be the dominant mechanism causing the degradation of the metal film and a simple crystallographic model explaining the driving force behind the restructuring is developed. It is suggested that the thermally-induced tensile and compressive stresses along the (111) plane, which has the highest atomic density in fcc crystals, force the atoms to rearrange towards crystallographic planes with lower packing densities (higher Miller indices) in order to accommodate the stresses. The tracking of individual grains using EBSD at the earlier degradation stage combined with XRD measurements to observe the metallization restructuring at larger number of cycles provides a powerful approach for understanding of the fatigue phenomena of metallic films on electronic chips.

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APPENDIX F: COMPARATIVE STUDY OF AL METALLIZATION DEGRADATION IN DIODES UNDER PASSIVE AND ACTIVE THERMAL CYCLING

Comparative study of Al metallization degradation in power diodes under passive and active thermal cycling

Mads Brincker, Kristian B. Pedersen, Peter K. Kristensen, and Vladimir N. Popok

***Abstract*—Degradation of Al metallization on Si-based semiconductor chips under operation is a reliability problem known for many years but the mechanisms of this phenomenon are not fully understood. To quantify contributions of different possible effects, a passive thermal cycling setup has been developed allowing for accelerated tests by varying the device temperature on a short time scale without applying electrical power. The setup is also capable of testing devices in different atmospheres. The results obtained by the thermal tests of diode chips are compared to those from power cycled diodes with focus on degradation of the top metallization layer. The data on structural and electrical characterization of the samples show that the passive thermal cycling induces metallization degradation very similar to that found for the power cycled devices. Thus, it can be concluded that the thermal-induced stresses are the dominating mechanisms for the metallization fatigue and following failure. The role of oxidation and corrosion effects is also studied in the experiments on passive thermal cycling using different environmental conditions. It is suggested that the formation of self-passivating aluminum oxide under ordinary atmospheric conditions can play a positive role limiting the structural, and electrical degradation of the metallization layers. The obtained results represent a considerable contribution into understanding of major failure mechanisms related to metallization fatigue and reconstruction.**

***Index Terms*—Aluminium, metallization, semiconductor device metallization, reliability, semiconductor device reliability, environmental factors, power semiconductor devices.**

I. Introduction

A common stressor for semiconductor dies is oscillating temperature originated by changes in the active losses e.g. from alternating currents or pulsed conditions. The same type of semiconductor die may experience short and long load cycles with varying amplitude depending on particular operation conditions [1]–[3]. Thermal factors are especially crucial for power electronic devices where the currents can reach tens or hundreds of amperes leading to very significant thermally induced stresses [4]. An example for such case can be high power modules used in wind power generators [5]. Thermal stresses can also originate from the device location as, for example, in power electronic devices used in hybrid electric vehicles where their cooling system is shared with that of the combustion engine [3]. Additional stressors are related to environmental conditions, for instance, high relative humidity (RH) or presence of chemically active gases, which can interplay with the thermal phenomena in a complex manner leading to change of the degradation mechanisms [6].

Consideration of the thermally-induced degradation is particularly important for interfaces and interconnects where a difference in coefficients of thermal expansion (CTE) between the components made of different materials is large causing significant mechanical stresses on compaction or expansion of the materials under temperature variation. One of the practically important cases for power electronics is fatigue of topside Al metallization on Si dies. These layers are typically between $1\,\mu\mathrm{m} - 6\,\mu\mathrm{m}$ thick and have microgranular structure. The films are needed to provide good electrical contact across the entire chip surface as well as allow for bonding of Al wires to interconnect the devices in the circuit. Due to difference in CTE between Al and Si, thermo-mechanical stresses are developed at the interface and lead to fatigue of the metallization layers causing a change of the granular structure and formation of voids and cracks. These phenomena negatively affect continuity of the film leading to increase of electric resistance and also provoking wire bond degradation and lift-off [7], [8]. Thus, a thorough understanding of the fatigue behavior of Al metallization and its interplay with wire bonds would give an important knowledge impacting the quality improvement of individual components as well as whole power devices.

The metallization fatigue has been a goal for several studies where different loading methods such as active power cycling [5], [9]–[12], passive thermal cycling [13]–[22] and cyclical bending on compliant substrates at room temperature [23], [24] were used. These investigations suggest a number of effects leading to the structural and compositional modification of Al films, among which are electromigration, grain-boundary diffusion [25] aided by oxidation [12], hillocking [26] and dislocation slip. Hence, the failure mechanisms can be of different nature involving thermo-mechanical, electrical and environmental reasons. In order to resolve the role of every effect and its importance for overall degradation, one needs to provide conditions for accelerated test separating different origins.

The current paper presents and analyses the data obtained under passive thermal cycling of diode chips under different atmospheric conditions, thus, studying the role of pure thermal phenomena isolating them from any electric effects. Thermal tests under different environmental conditions allow to justify an importance of RH and oxidation factors as well as their

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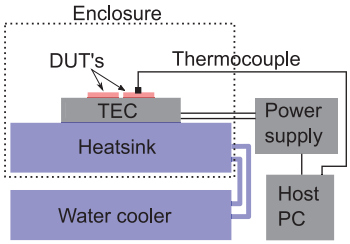

Fig. 1. Schematic picture of the passive thermal cycling setup.

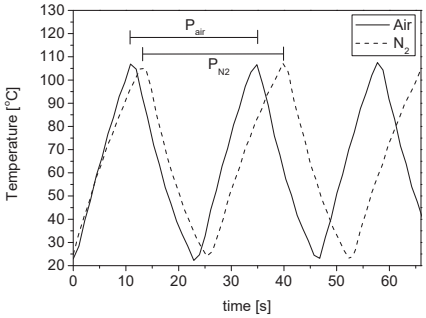

Fig. 2. Profile of thermal cycles with $P_{air} = 24\,s$ being the period for cycling in atmospheric air, and $P_{N2} = 26\,s$ being the period for cycling in nitrogen atmosphere.

interplay with the thermally-induced stressing. Comparison of topographical, microstructural, and resistance changes of the metallization layers under the above-mentioned tests with those obtained under traditional power cycling provide clear insights into the major degradation mechanisms and related failure modes.

II. Experimental procedure

A. Passive thermal cycling

The passive thermal cycling setup is based on a digitally controlled thermo-electric cooler (TEC), which is connected to a water cooled Al block on the bottom side, while the top side is used to thermally cycle the samples. All active elements of the setup are put in an air-tight enclosure that provides a possibility to control the surrounding atmosphere. A schematic picture of the setup is shown in **Figure 1**. Temperature measurements are carried out by placing a thermocouple in direct contact with the topside metallization layer on one of the devices under test (DUT).

One set of data is obtained for cycling in a pure nitrogen atmosphere allowing to reach RH close to zero and exclude effect of oxidation, while another one in an ordinary atmosphere with a controlled RH=50%. This is done to examine if humidity and oxidation effects play any major role in the degradation phenomena. The temperature waveforms are triangular shaped with a period $P_{N2} = 26\,s$ for the cycling in nitrogen atmosphere and a period $P_{air} = 24\,s$ for the cycling in ordinary atmosphere, see **Figure 2**. Other parameters, such as minimum and maximum temperature, $T_{min} = 25\,°C$, $T_{max} = 105\,°C$, and the mean temperature of $65\,°C$ are identical for both experiments. The DUT are high power Infineon diodes ($100\,A/1200\,V$) that are 9×9 mm squares with a measured topside metallization thickness of $3.4\,\mu m$. Three diodes are thermally cycled in nitrogen and in ambient atmosphere labeled as D# and A#, respectively.

B. Active power cycling

In order to compare the change in sheet resistance as well as the microstructural evolution of the passively cycled samples, a set of samples is subjected to power cycling, which is often also referred as active thermal cycling.

1) DC pulse test: The DC pulse test is a current load procedure, according to test standards [27], where the device is heated using only ohmic losses from a DC current. The investigated DUT is a half-bridge $300\,A$ device with 3 parallel sections consisting of two IGBT chips and two diodes each. The semiconductor devices are backside soldered to a Al_2O_3 DCB and topside bonded with heavy Al wires. The chips have a standard $3.4\,\mu m$ Al metallization layer. Before the test, the silicone gel is dissolved to allow for sheet resistance measurements in between the power cycling steps. Only the low side diodes are tested in the present setup, while the top side diodes are used to measure the reference value of the sheet resistance, in order to calculate the relative change for the cycled diodes. Since the diodes are acting passively, any load variation is induced externally (water cooler, power supply, etc.), and therefore, the current amplitude, cooling temperature, and on/off time are the primary control parameters. In accordance with ordinary accelerated tests of chip level interconnects, the on time is kept at $1\,s$ and the off time is varied to reach the desired ΔT. Chip junction temperature is monitored using calibrated small current injection. The test is run as a constant current test and not a constant ΔT test. This means that the device loading increases when the DUT degrades. In general, this is considered to be a much harder test than that at constant temperature load but closer to real life operation [1], [2], [4]. The accelerated test is performed with a load current per chip between $75\,A - 85\,A$, a water cooling temperature of $80\,°C$, and on/off times of $1\,s/2.3\,s$. This set of parameters is chosen to obtain an initial ΔT of approximately $50\,°C$ for non-degraded devices.

2) Sinusoidal current load: The DUT are standard half-bridge IGBT modules consisting of six parallel IGBT chips each with a freewheeling diode. IGBTs and diodes are topside connected with heavy Al bond wires and backside soldered to a standard Al_2O_3 based DCB substrate. The modules are power cycled actively with a sinusoidal current load of $890\,A$ at $6\,Hz$ switched at $2.5\,kHz$ with a DC-link voltage of $1000\,V$. As one of the main accelerators, the baseplate of the DUT is subjected to an elevated temperature of $80\,°C$. Under these conditions the mean temperature of both IGBTs and diodes is

online estimated and simulated to be approximately 112 °C, while the ΔT of IGBTs is found to be around 29 °C, and the ΔT of the diodes around 36 °C, thus resulting in a maximum junction temperature of 127 °C for the former and 130 °C for the latter. The reason why the modules have been tested at a workpoint far from the passive test conditions is to avoid too early failure from bond wire lift-off or solder fatigue prior to observing the metallization degradation. More details about the test procedure can be found in [5], [28].

C. Electrical characterization

For the electrical characterization, the van der Pauw method [30] is used according to the procedure described in [19].

In the case of the passive test, the resistivities of the new diodes are measured to be $28.9\pm0.2\text{n}\Omega\,\text{m}$ and the exact individual values are then used to calculate the relative change of the sheet resistance for each cycled diode. For the resistivity measurements, the samples are temporarily removed from the test setups and then returned for further cycling.

In the DC pulse load case, the sheet resistance of individual low side diodes is measured after reaching a certain number of cycles. For that, the module is removed from the power cycling setup, and one diode is electrically disconnected by mechanical removal of the bond wires. After the measurement of the sheet resistance, the module is reinstalled in the setup, re-calibrated for a ΔT of 50 °C, and the power cycling is continued on the remaining low side diodes. The procedure of electrical measurements is repeated on the next diode after reaching next step in the cycling. In order to collect sufficient number of cycles, two power modules are used for this accelerated test. Since resistivity values of different uncycled diodes are found to be very close to each other, $27.5\pm0.4\text{n}\Omega\,\text{m}$, the average value is used as a reference for the loaded diodes.

In the sinusoidal current load case, the power modules are taken from the setup and the silicone gel as well as bond wires of diodes are removed to provide electrical contact to the metallization of the diodes. The relative change in sheet resistance for the individual diodes at every number of cycles is calculated using the average value obtained from the uncycled module, which is found to be $27.6\pm0.2\text{n}\Omega\,\text{m}$. For each power cycling step, three sections with two diodes per section are examined, thus resulting in six readings for every number of cycles.

III. Results

A. Sheet resistance

The relative change in sheet resistance for the case of thermal cycling in both nitrogen and ambient atmospheres is shown in **Figure 3**. A clear increase of the sheet resistance can be seen for the diodes cycled in nitrogen atmosphere reaching up to 43% at 330 kilocycles. In this case, three phases with different degradation rates can be distinguished: phase 1 for 0-20 kilocycles that shows almost no change in the sheet resistance, phase 2 between 20-120 kilocycles that demonstrates the most severe increase of resistance, and phase 3 above 120 kilocycles that shows moderate increase. This

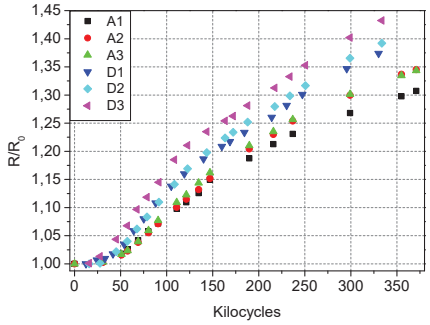

Fig. 3. Relative sheet resistance of diodes at different number of cycles. A1, A2, and A3 correspond to diodes cycled in ordinary atmosphere, and D1, D2 and D3 correspond to diodes cycled in nitrogen atmosphere.

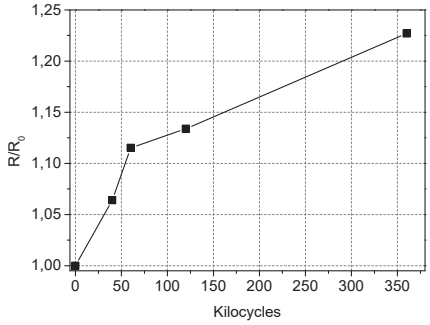

Fig. 4. Relative sheet resistance of actively cycled diodes under DC pulse load at different number of cycles.

type of curve with different phases agrees with earlier results obtained for actively thermally cycled devices [10]–[12].

The data for the diodes cycled in ambient atmosphere show three phases with different degradation rates similar to those found in nitrogen but with slower increase of resistance. At 300 kilocycles the average increase in sheet resistance for these diodes reaches only 28%, compared to 37% for the devices cycled in nitrogen atmosphere. It is suggested that the formation of a native aluminum oxide may strengthen the metallization, thus slowing down the degradation under ambient atmospheric conditions. This hypothesis will be addressed in more detail in the Discussion section.

The relative change of sheet resistance for the case of active power cycling under DC pulse load is shown in **Figure 4**. The evolution of the sheet resistance resembles that for the passively cycled diode chips, shown in **Figure 3**, in the way that distinct phases can be recognized. The interval of up to 60 kilocycles demonstrates the most severe increase of resistance, while after that the change is more moderate. The increase of resistance reaches 23% at 360 kilocycles, which is lower than the mean value of the passively cycled samples.

The change of sheet resistance for the case of active power cycling under sinusoidal current load is shown in **Figure 5**.

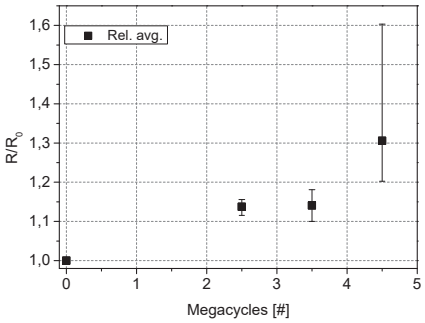

Fig. 5. Relative sheet resistance of actively cycled diodes under sinusoidal current load at different number of cycles. Each solid square represent the average of the six different measured values, while the bars represent the minimum and maximum of the measured values.

Similar to the passively cycled diodes and those under active cycling with DC pulses, a clear rise of the sheet resistance can be observed. After 4.5 megacycles this value reaches a relative increase of 31%. As the number of cycles increases a wider spread of the sheet resistance values is observed, which is indicated by vertical bars.

B. Microstructural characterization

To correlate the change in sheet resistance to the microstructural evolution of the Al metallization, a scanning electron microscopy (SEM) study accompanied by focused ion beam milling (FIB) is performed according to the procedure described elsewhere [28].

In **Figure 6**, SEM images of the metallization cycled in nitrogen atmosphere are presented. **Figure 6(a)** shows the surface of the metallization after 250 kilocycles demonstrating severe restructuring. One can compare this image with **Figure 6(b)** for the uncycled device where one can see a part of the surface which is relatively flat. This figure also indicates that the film is initially crack free, while from **Figures 6(c,d)** it can be seen that the deformation occurring during cycling is not limited to the surface of the metallization. Cavities and cracks are formed in the layer bulk and propagate deep into the metallization. The total disorder of the analyzed layers increases with number of cycles. These observations correlate well with the sheet resistance measurements, which show an increase of relative resistance from 1.25 to 1.35 for diode D3 in the interval 145-250 kilocycles, see **Figure 3**.

In **Figure 7**, SEM images of the metallization cycled in ambient atmosphere are presented. **Figure 7(a)** shows the surface in the center of a cycled diode. There is a clear microstructural change similar to that seen in **Figure 6(a)**. **Figure 7(b)** shows a cross-section in the center of the metallization with severe plastic deformation of the layer. **Figures 7(c-d)** present surface and cross-section images at the edge of the diode. By comparing with **Figures 7(a-b)** it becomes obvious that the degradation is not homogeneous but most significant in the center of the diode. Lower degradation at the edges can be explained by less confinement, which leads

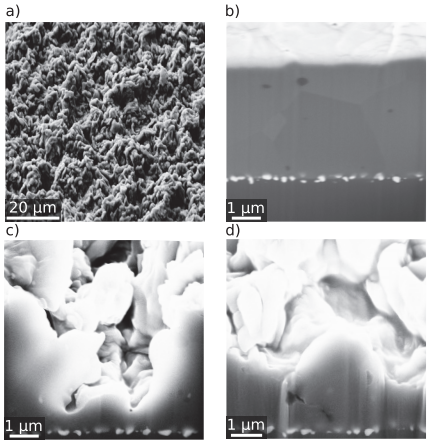

Fig. 6. SEM images of metallization for diode D3. a) Surface after 250 kilocycles, b) cross-section at 0 kilocycles, c) cross-section after 145 kilocycles, and d) cross-section after 250 kilocycles.

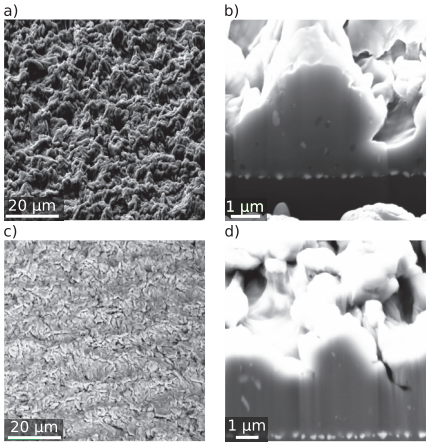

Fig. 7. SEM images of metallization for diode A2 after 110 kilocycles. a) Surface in the center, b) cross-section in the center, c) surface at the edge, and d) cross-section at the edge.

to lower stress. Comparing the metallization degradation in different atmospheres, one can conclude that the restructuring occurs in a similar way in nitrogen and ambient atmosphere.

In **Figure 8**, SEM images of the metallization for the power cycled diodes are presented. **Figure 8(a)** shows the surface of the metallization after 2.5 megacycles. One can see plastic deformation of the surface, but the cracks do not protrude deep into the layer (see **Figure 8(c)**). This level of structural degradation agrees well with the moderate increase in the sheet resistance that can be found in **Figure 5**. **Figure 8(b)** shows the surface of the metallization after 4.5 megacycles. In this case, the restructuring of the surface is dramatic, and as can be seen in **Figure 8(d)** the cracks and cavities penetrate almost all the way to the Si substrate, thus

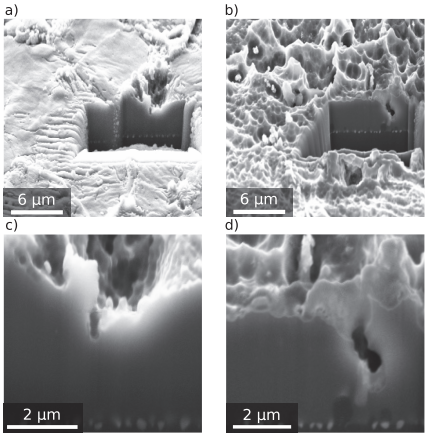

Fig. 8. SEM images of metallization for diodes that are power cycled with a sinusoidal load current. a) Surface after 2.5 megacycles, b) Surface after 4.5 megacycles, c) cross-section after 2.5 megacycles, and d) cross-section after 4.5 megacycles.

leading to the observed high increase in sheet resistance (see **Figure 5**). It is worth mentioning that under the conditions of active cycling it is primarily the diodes that are subjected to the significant power load [5]. Therefore, metallization of IGBT chips does not undergoes any considerable degradation. However, if a load profile is designed to stress IGBTs one observes considerable degradation of the metallization similar to that found for the diodes [29]. Overall, it can be concluded that the microstructural evolution of the metallization on the actively cycled devices is very similar to that found for the diodes under passive thermal tests.

C. Texture analysis

To examine the texture of the metallization, X-ray diffraction (XRD) measurements are performed on the passively cycled diodes. XRD measurements can be used in thin film analysis to determine the orientation of the micro-crystals that constitute a polycrystalline film [32]. It is found that grains with crystallographic planes (111) dominate in new Al metallization layers and these data correlate well with the results published elsewhere regarding the texture of Al thin films on Si substrates [13], [17], [22], [33], [34]. As the number of thermal cycles increases, spectral peaks corresponding to (200), (220), and (311) crystal lattice planes appear for both types of cycling (in nitrogen and ambient air). The obtained tendency is in good agreement with our earlier published results [21], and therefore, we do not present the spectra here. The transformation of the grains may be explained by dislocation glide of the inclined (111) planes that are constrained by the Si substrate [17], [35].

Tendencies in the change of XRD spectra are found to be very similar for the samples cycled in nitrogen and air. However, the diode that reached 134 kilocycles in air has almost the same XRD scan as the diode having 335 kilocycles in nitrogen. This implies that the grain reorientation phenomena might only

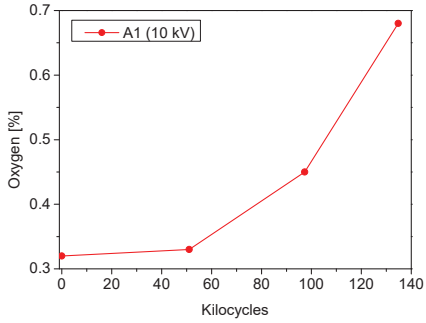

Fig. 9. Amount of oxygen in the metallization of A1, measured by EDX.

be influential until a point where no more relaxation can occur through this mechanism, while other mechanisms (crack and void development) continue to affect the degradation process. More studies are being carried out on this topic [22], which is not the focus of the current paper.

D. Oxide analysis

Energy-dispersive X-ray spectroscopy (EDX) measurements are performed on the passively cycled diodes to monitor the amount of oxygen present in the film, thus allowing to track the formation of aluminum oxide. The accelerating voltage of the EDX measurement was 10 kV, which according to simulations corresponds to a maximum penetration depth of 1 µm. It can be seen from the data presented in **Figure 9** that the amount of oxygen in the metallization of diode A1 (ambient atmosphere) increases significantly and in a non-linear manner with the number of cycles, while the oxygen increase for diode D3 (nitrogen atmosphere) at 335 kilocycles is found to be at only 0.5% which is lower compared to diode A1 at 135 kilocycles (see **Figure 9**). Oxidation of the metallization films cycled in nitrogen atmosphere most probably occurs during storage and when the samples are taken from the setup and exposed to ambient atmosphere while transferred to EDX. Thus, one may conclude about a significant oxidation of the metallization under thermal cycling in ambient atmosphere.

IV. Discussion

The results on sheet resistance and EDX analysis have showed two interesting tendencies. The electrical degradation of the metallization cycled in air is slower compared to that cycled in nitrogen atmosphere. At the same time, the EDX measurements show that the amount of oxygen in the metallization tested in ambient atmosphere is higher than in those run in nitrogen atmosphere. The increase in the amount of oxygen agrees with a qualitative diffusion model for the degradation of Al films suggested by Martineau et al [12]. They hypothesized that sidewalls of micro-cracks, formed during the tensile phase (cooling) of a thermal cycle, self-passivate through surface oxidation in ambient atmosphere, thus leaving these cracks unable to heal in the following compressive phase (heating). In the next tensile phase, these cracks will then develop deeper

into the layer causing electrical disconnections. Initially, this mechanism is expected to enhance crack formation, introduce higher disorder in the layer, and therefore increase the sheet resistance. However, this process might be counteracted by another phenomenon also arising from the oxidation.

Native oxide of Al, with a thickness of about 3 nm to 6 nm [36], could constrain the dislocation motion, thereby increasing the strength of the film and making it less prone to plastic deformation [37] in a similar way to that a compressive layer, e.g. polyimide or silicon dioxide, has been shown to suppress the degradation phenomena [7], [38], [39]. Such strengthening mechanism affecting mechanical properties and microstructure of metal thin films is suggested for Al-0.5%Cu with native oxide [13]. It is also observed for self-passivated Cu-1%Al films that the dislocation glide, which is parallel to the surface in pure Cu layer, is converted to threading dislocation motion in the oxidized films [40]. These results indicate that the presence of a native oxide, despite its low thickness, may have an influence on the dislocation motion, and thereby on the type of degradation and degradation rate. Thus, one can suggest that the formation of native aluminum oxides can play a positive role in the evolution of metallization structure through slowing down of the mechanisms leading to the loss of film continuity.

Comparing the evolution of sheet resistance for the samples under passive thermal cycling and the active power cycling with DC pulse load one can conclude about very similar character of the dependences (compare **Figure 3** and **4**). One does not clearly see the phase 1 for the power cycled samples, which is probably related to only very few measurements of the resistance for low number of cycles but then in both cases one can observe a very similar relatively steep resistance increase with following slowing down. The number of cycles leading to the increase of resistance is also comparable but the passively cycled devices degrade faster showing the rise of relative resistance up to 34% at 360 kilocycles while those under the DC pulse load reach only about 23% for the same number of cycles. Several factors may account for the higher degradation observed in the passively cycled diodes but the main reason is most likely the difference in ΔT, which is 80 °C for the passive test, and 50 °C for the DC pulse test.

Since the devices under the sinusoidal current load are expected to have much lower ΔT (around 36 °C on diodes) compared to the above-discussed cases, the increase in the sheet resistance undergoes much slower dynamics reaching a relative value of about 31% after 4.5 megacycles (**Figure 5**). It is quite difficult to distinguish between different phases of the degradation because with the increase of number of cycles we observe a wide spread of the sheet resistance values. These large variations are well explained by higher complexity of the systems under the sinusoidal current load conditions compared to those used in the passive and DC pulse cycling. In the two latter cases, individual elements or sections are under the load while for the former test the whole module is cycled. In this case, the temperature increase for each diode is caused by the passing current but it is also affected by the state of the other thermal paths, i.e. neighboring diodes, solder layers, etc. For example, uneven current sharing between individual sections originated from the degradation of solder and wire bonds cause different stresses for each diode. This spread becomes wider with the number of cycles due to the diversity in degradation of individual devices, thus, increasing the deviation in the electrical degradation of the entire power module. Nevertheless, the observed general dynamics in the increase of resistance under this accelerated test is in good correlation with both the passive thermal cycling and active one with DC pulses. The microstructural changes of the device metallization under the three different types of cycling also demonstrate close similarity.

The role of the metallization restructuring in degradation of wire bond interfaces is not directly studied in this work. But one can suggest that re-orentation of grains, formation of cavities and cracks in Al films should significantly affect the bonded area, thus, accelerating wire lift-off, which is one more major failure mechanism limiting reliability of electrical interconnects.

V. Conclusion

To gain insights into the dominant physical mechanisms governing the degradation of Al metallizations, a passive thermal cycling setup that can operate in different atmospheres have been constructed and the results obtained on the metallization degradation under passive thermal tests have been compared with those found in actively power cycled devices. Both passive cycling in pure nitrogen and ordinary atmosphere have shown electrical and microstructural degradation of the metallization films very similar to that observed for the actively power cycled devices. Since the passive thermal test excludes any contribution from electric current, the obtained results present a strong indication that thermo-mechanical stress is the dominant mechanism responsible for the restructuring and related fatigue of Al metallizations in Si based power components.

To examine the role of oxidation and corrosion effects, the degradation originated by cycling in ambient atmosphere with controlled humidity is compared to that in a nitrogen atmosphere (close to zero RH). It is found that the metallization restructuring occurs slower in the ordinary atmosphere, and it is proposed that this could be caused by a strengthening mechanism due to the formation of native oxides acting as a constraint on the dislocation movement, thus limiting the dislocation-based plasticity. Comparisons between the amount of oxygen in the metallization cycled in ordinary and nitrogen atmospheres supports the model where self-passivation of micro-crack walls can lead to the change of the involved physical mechanisms, thus, slowing down the breakage of the film continuity. No evidences for corrosion are found for the metallization cycled in ordinary atmosphere with RH = 50%. We do not extend the role of oxidation effects on the modules that are power cycled with sinusoidal current because the test are run on the packaged modules and any significant penetration of oxygen through the silicon gel is rather unlikely.

Presently, there is a general tendency in substituting Al wires by Cu-based ones and soft solders by sintered connections in order to improve the technologies in respect to

such failures as bond wire lift-off and solder fatigue [41]–[43]. Thus, one can argue that the study presented in this paper is of limited interest. However, even in this new architecture, the used Si chips are standard ones still containing Al metallization films with an additional layer of Cu on top. Moreover, Al metallization will still be a widely used industrial approach in the future due to well established technologies and lower expenses compared to Cu. This situation, therefore, leaves the Al metallization to be a bottleneck in component operation range and lifetime. Since the obtained results clarify a picture of the physical origins behind the metallization degradation, they can pave a way for further optimization on component level, and the construction of devices with improved reliability.

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