A multi-port thermal coupling model for multi-chip power modules suitable for circuit simulators

Wang, Zhongxu; Wang, Huai; Zhang, Yi; Blaabjerg, Frede

Published in:
Microelectronics Reliability

DOI (link to publication from Publisher):
10.1016/j.microrel.2018.06.031

Publication date:
2018

Document Version
Early version, also known as pre-print

Link to publication from Aalborg University

Citation for published version (APA):
Title: A Multi-Port Thermal Coupling Model for Multi-Chip Power Modules Suitable for Circuit Simulators

Article Type: SI: ESREF 2018

Keywords: Thermal model, multi-chip power module

Abstract: This paper investigates two compact thermal model representations for multi-chip power modules, namely the thermal impedance matrix model and the thermal admittance matrix model. The latter can shape a multi-port thermal network without controlled temperature sources, and can be readily implemented in circuit simulators from the electrical engineer point of view. The mutual transformation between the two models and their relationship to parameters in the multi-port network are revealed. In addition, practical tips regarding the temperature recording and the curve-fitting in the process of the thermal model parameter extraction is discussed. The multi-port thermal model is verified by simulations and experimental results. It confirms that accurate temperature estimation can be achieved compared with the thermal model without the thermal coupling effect.
A Multi-Port Thermal Coupling Model for Multi-Chip Power Modules
Suitable for Circuit Simulators

Z. X. Wang, H. Wang, Y. Zhang, F. Blaabjerg

Department of Energy Technology, Aalborg University, Aalborg, Denmark

Abstract

This paper investigates two compact thermal model representations for multi-chip power modules, namely the thermal impedance matrix model and the thermal admittance matrix model. The latter can shape a multi-port thermal network without controlled temperature sources, and can be readily implemented in circuit simulators from the electrical engineer point of view. The mutual transformation between the two models and their relationship to parameters in the multi-port network are revealed. In addition, practical tips regarding the temperature recording and the curve-fitting in the process of the thermal model parameter extraction is discussed. The multi-port thermal model is verified by simulations and experimental results. It confirms that accurate temperature estimation can be achieved compared with the thermal model without the thermal coupling effect.

Preferred track (please, tick one or number 1 to 3 tracks in order of preference: 1 = most suiting, 3 = least suiting)

[ ] A - Quality and Reliability Assessment Techniques and Methods for Devices and Systems
[ ] B1 - Si Technologies & Nanoelectronics: Hot Carriers, High K, Gate Materials
[ ] B2 - Si Technologies & Nanoelectronics: Low K, Cu Interconnects
[ ] B3 - Si Technologies & Nanoelectronics: ESD, Latch-up
[ ] C - Progress in Failure Analysis: Defect Detection and Analysis
[ ] D - Reliability of Microwave and Compound Semiconductors Devices
[ ] E1 - Power Devices Reliability: Silicon and Passive
[ ] E2 - Power Devices Reliability: Wide Bandgap Devices
[ ] F - Packaging and Assembly Reliability
[ ] G - MEMS, Sensors and Organic Electronics Reliability
[ ] H - Photonics Reliability
[ ] I - Extreme Environments and Radiation
[ ] K - Renewable Energies Reliability
[ ] L - Modeling for Reliability
[ ] SS1 (Special Session) - Reliability in Traction Applications

*Corresponding author

zho@et.aau.dk  Tel: +45 9356 2257
A Multi-Port Thermal Coupling Model for Multi-Chip Power Modules Suitable for Circuit Simulators

Z. X. Wang, H. Wang, Y. Zhang, F. Blaabjerg

1. Introduction

In order to overcome the size constrain and to increase the power density, power electronics is moving towards a more compact multi-chip package [1], which inevitably leads to more serious thermal and corresponding reliability concerns [2]. Thus, thermal behaviour has to be carefully evaluated through thermal modelling. The thermal modelling of discrete device has been extensively studied [3]. However, for power modules with multi-chips, the thermal coupling effect has to be taken into account [4-5]. This issue can be addressed by compact thermal model (CTM) [6], which can be represented by two means. One is the thermal admittance matrix [7] as a general form of star-shaped models, and its fully mathematical criteria is reported in [8]. Another approach is the thermal impedance matrix [9]. One of their differences is that the thermal admittance matrix can shape a "topology" for that thermal system with a multi-port thermal network shown in Fig. 1, and all power losses behave just like the current flowing from one driving point to another. While for the thermal impedance matrix as shown in Fig. 2, controlled temperature sources have to be used. Thus, thermal network shaped by thermal admittance matrix is easier to implement in circuit simulators from electrical engineer point of view. On the other hand, the thermal model defined by thermal impedance matrix is more suitable for large-scale analytical calculation, such as the temperature estimation for long term mission profile. However, until now, no literature explains how to get the thermal parameters in the thermal network shown in Fig. 1. Thus, it will be one of the focus of this paper.

In addition, as mentioned in [10], the thermal impedance matrix can be fully defined by a $N \times N$ matrix while the dimension is $N+1$ for the thermal admittance matrix with $N$ being the number of temperature nodes. This one additional dimension is mainly caused by the ambient temperature. As a matter of fact, if a linear thermal system dominated by thermal conduction is assumed, the ambient temperature will be just a potential reference, and has no impact on the thermal description of the thermal system. In this case, the thermal system can be fully defined by any $N$ order impedance or admittance matrix through the temperature rise from ambient instead of the actual temperature. Thus, the focus of this paper is: how the two thermal matrices can be transformed between each other, and how to interpret them into the multi-port network shown in Fig. 1.

2. Two thermal model representations

Taking a thermal system with 4 nodes for example, all nodes can be fully coupled and be characterized through a $4 \times 4$ thermal impedance matrix expressed as $\Delta T = \mathbf{Z} \mathbf{P}$ in (1). The impedance matrix shapes a multi-port thermal network as shown in Fig. 2. It can be seen that, as a matter of fact, each temperature node has its own thermal model with the
coupling point of the ambient. Moreover, controlled temperature sources are needed in this model.\[
\begin{bmatrix}
\Delta T_1 \\
\Delta T_2 \\
\Delta T_3 \\
\Delta T_4
\end{bmatrix} =
\begin{bmatrix}
\psi_{11} & \psi_{12} & \psi_{13} & \psi_{14} \\
\psi_{21} & \psi_{22} & \psi_{23} & \psi_{24} \\
\psi_{31} & \psi_{32} & \psi_{33} & \psi_{34} \\
\psi_{41} & \psi_{42} & \psi_{43} & \psi_{44}
\end{bmatrix}
\begin{bmatrix}
P_1 \\
P_2 \\
P_3 \\
P_4
\end{bmatrix}
\tag{1}
\]

where \(\psi_{ij}\) is the thermal impedance between node \(i\) and the ambient \(T_a\); \(P_j\) is power applied on node \(i\); \(\psi_{ij}\) is the thermal impedance between node \(i\) and node \(j\) representing the thermal coupling effect between them; \(\Delta T_i\) is the temperature difference between node \(i\) and the ambient.

It should also be noted that the thermal impedances \(\psi_{ij}\) do not correspond to the parameters \(Z_{ij}\) in the multi-port thermal network defined by thermal admittance matrix. Specifically, the power dissipation \(P_j\) totally goes through \(\psi_{ij}\) to generate the temperature rise of node \(T_j\) in the thermal impedance matrix. However, in the multi-port thermal network shown in Fig. 1, the power is transferred through all available paths in a 3D manner. Thus, the parameter \(\psi_{ij}\) is a combined effect of all elements in the multi-port thermal network, and vice versa. To explore the relationship between the two matrices, matrix transformation has to be conducted. For simplification, thermal conductance \(Y_{ij}\) is used instead of the thermal impedance \(Z_{ij}\), which is simply the reciprocal of \(Y_{ij}\).

Taking node \(T_j\) in Fig. 1 for example, the heat flow balance equation is\[
(T_j - T_a)Y_{j1} + (T_j - T_i)Y_{j2} + (T_j - T_i)Y_{j3} = P_i
\tag{2}
\]

where \(Y_{ij}\) is the thermal conductance between node \(i\) and \(j\), and \(Y_{ji} = Y_{ij}\). Rearrange (2) to make sure that all temperatures are referred to the same reference \(T_a\).

\[
\begin{cases}
(Y_{i1} + Y_{i2} + Y_{i3})\Delta T_i - Y_{i4}\Delta T_a - Y_{j4}\Delta T_a = P_i \\
-Y_{i4}\Delta T_a - Y_{i4}\Delta T_a - Y_{j4}\Delta T_a = P_i
\end{cases}
\tag{3}
\]

Taking heat balance equations of all 4 nodes into account, and the matrix below can be obtained\[
\begin{bmatrix}
P_1 \\
P_2 \\
P_3 \\
P_4
\end{bmatrix} =
\begin{bmatrix}
K_{11} & K_{12} & K_{13} & K_{14} \\
K_{21} & K_{22} & K_{23} & K_{24} \\
K_{31} & K_{32} & K_{33} & K_{34} \\
K_{41} & K_{42} & K_{43} & K_{44}
\end{bmatrix}
\begin{bmatrix}
\Delta T_1 \\
\Delta T_2 \\
\Delta T_3 \\
\Delta T_4
\end{bmatrix}
\tag{4}
\]

where \(K_{ii} = \sum_{j=1}^{N} Y_{ij}\), \(K_{ij} = -Y_{ij} (i \neq j)\). The matrix equation can be further simplified as \(P = K\Delta T\), in which \(K\) is the thermal admittance matrix, and the relationship \(\Psi = K^{-1}\) can be easily derived. It can be extended to thermal systems with \(N\) nodes by only changing the range of subscripts \(i\) and \(j\) to \(N\).

Based on the analysis above, the relationship between the parameters \(\Psi\) and \(Z\) of the two multi-port thermal networks can be expressed in the following,

\[
K = \Psi^{-1} =
\begin{bmatrix}
\Psi_{11} & \Psi_{12} & \ldots & \Psi_{1N} \\
\Psi_{21} & \Psi_{22} & \ldots & \Psi_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
\Psi_{N1} & \Psi_{N2} & \ldots & \Psi_{NN}
\end{bmatrix}
\]

\[
Y_{ij} = \frac{1}{Z_{ij}} = \frac{1}{\psi_{ij}} (i \neq j)
\tag{5}
\]

Note that none of the parameters \(\psi_{ij}, K_{ij}\), and \(Z_{ij}\) have physical meaning. All of them are general thermal description between nodes. In addition, thermal parameters \(Z_{ij}\) may contain negative values if Foster RC model is used to fit the thermal transient, which could lead to convergence issues [11].

Moreover, to distinguish the two multi-port thermal coupling networks and their potential applications, their features are summarized as below:

1) The multi-port thermal network defined by thermal admittance matrix can be easily implemented without controlled temperature source, and the power can be transferred in a more "realistic" manner like current. Thus, it is a better option for engineers who prefer thermal model realization with thermal resistor and capacitor only.

2) The multi-port thermal network derived from the thermal impedance matrix can shape independent thermal model for each temperature node, and no coupling exists among nodes. Thus, it is suitable for fast temperature estimation with large-scale data processing, such as the junction temperature estimation for long-term mission profile.

3. Thermal impedance matrix extraction

The thermal impedance matrix is usually obtained from either simulation or experiment. The approach is to apply a step power on each chip of interest until the thermal steady-state is achieved. The on-state voltage drop and the current going through the device under test (DUT) are measured for power loss calculation before switching off the power supply. Then the temperature cooling curves of all chips are recorded simultaneously. In this paper, a four-chip half-bridge IGBT module F4 50R12KS4 from Infineon is used as the DUT. Note
that to facilitate the temperature measurement by thermal camera as shown in Fig. 2, the IGBT has to be black painted. Based on the tested power loss and temperature responses, the self and mutual thermal impedances can be calculated by the temperature rise over the constant power dissipation. They can be further fitted into a series of Foster RC network and finally get the thermal impedance matrix $\Psi$. Based on $\Psi$ and the thermal model transformation method in section 2, the thermal admittance matrix $K$ can be obtained. Fig. 3 and Fig. 4 show part of the thermal parameters of $\psi_{ij}$ and $Z_{ij}$. As can be seen, different from the thermal impedance matrix with all values of its Foster model being positive, certain negative values can be expected for the Foster model of the thermal admittance matrix parameters. In addition, the thermal impedance matrix ($t = 1000$ s) is illustrated in (6), in which the symmetrical characteristics ($\psi_{ij} = \psi_{ji}$) can be observed with a negligible difference caused by the measurement and the nonlinearity in the system.

$$
\Psi_{t=1000s} =
\begin{bmatrix}
0.5880 & 0.2244 & 0.3058 & 0.2961 \\
0.2228 & 0.5353 & 0.2466 & 0.2452 \\
0.2974 & 0.2512 & 0.6172 & 0.2933 \\
0.2954 & 0.2466 & 0.3092 & 0.5995
\end{bmatrix}
$$

(6)

Moreover, several practical tips are listed for the parameter extraction through experiments:

1) Cooling curve is preferred since a constant power dissipation is difficult to achieve due to the temperature-dependent output characteristic of power devices in the heating process.

2) It is sufficient to select a 4th or 5th order Foster model for main diagonal elements and 2nd or 3rd Foster model for non-diagonal elements, which depend on the characteristic of baseplate and heatsink with a relatively large time-constant [12].

4. Simulation and experiment validation

A series of simulations and experiments are conducted based on the multi-chip IGBT module mentioned in section 3. Its power loss characteristics are measured by power device analyzer under different temperature conditions. The tested on-state voltage and switching loss under different current are used in simulation thermal models.

To evaluate the accuracy of the two thermal model representations, the multi-chip IGBT module is set to operate under the same current and blocking voltage condition in both simulations and experiments. A sinusoidal current profile with a dc
offset is applied to the device under test (DUT) to
temperature being 20 °C.

Fig. 6 shows the simulated and experimental steady state junction temperature of the most stressed device S2 under current profiles with different frequencies. It can be seen that junction temperature waveforms obtained from the two thermal matrices coincide with each other, but shows a higher temperature than the experimental results. This confirms the equivalence of the two thermal model representations. In additional, the thermal model without considering the thermal coupling effect underestimates the temperature as indicated by the green line, and the estimation error becomes larger with the decrease of the current frequency. However, the error is about 1 °C and is small enough.

generate an unbalanced power dissipation among the
four chips (4.3 W dissipated in S1, 19.9 W for S2, 3.5
W for D1, and 0.6 W for D2), which leads to more
severe thermal coupling issue [13]. Fig. 5 shows the
circuit topology of test bench made up of two half-
bridges and one inductor. One half-bridge converter
serves as the DUT, it is controlled by switching
profile obtained from simulations. Another half-
bridge converter functions to regulate the current
going through the DUT. The main operating
parameters are listed in Fig. 5. In this paper, three
current profiles with different frequencies, namely 50
Hz, 10 Hz and 1 Hz, are utilized. Temperatures of
the four devices under different current conditions
are recorded and compared with the corresponding
simulation results. Note that all temperatures are
tested under the steady state with the ambient

Fig. 6. Simulated and experimental steady-state junction
temperature of device S2 under different current profiles. a) 50 Hz, b) 10 Hz, and c) 1 Hz. (Black: experiment, red: simulation with Ψ matrix, blue: simulation with Z matrix, and green: simulation without thermal coupling.)

Fig. 7. Simulated and experimental steady-state junction
temperature of the other three devices under 1 Hz current profile. a) S1, b) D1, and c) D2. (Black: experiment, red: simulation with Ψ matrix, blue: simulation with Z matrix, and green: simulation without thermal coupling.)
Fig. 7 shows the simulated and experimental steady-state junction temperature of other three device (S₁, D₁ and D₃) under the same current profile with the frequency being 1 Hz. It can be clearly observed that the junction temperatures obtained by simulations based on the thermal impedance matrix \( \mathbf{\Psi} \) are in well agreement with that from the thermal model represented by \( \mathbf{Z} \) and experiments in terms of both average temperature and temperature variation. It further validates the equivalence of the two representations in linear thermal system applications. However, if the thermal coupling is neglected, the junction temperature of the three devices are all greatly under estimated with the error being up to 7°C. The reason is that in addition to the thermal coupling, the power dissipated in each node also has a great impact on the junction temperature. It means that S₁ dissipating the most power has the greatest thermal impact on the other devices, and the thermal impact of the other devices with less power loss on S₁ are negligible.

5. Conclusion
Two thermal model representations for multi-chip power modules and their mutual transformations are investigated in this paper. Based on this, two multi-port thermal networks are defined. The one shaped by the thermal admittance matrix can be easily implemented without controlled temperature source, and it could be a better option for engineers who prefer the thermal model realization with thermal resistor and capacitor only in circuit simulators. The multi-port thermal network defined by the thermal impedance matrix is characterized as independent thermal model for each node without coupling inside, it is suitable for temperature estimation with large-scale data processing. Simulation results obtained from the two multi-port networks and the experimental results validate the effectiveness and equivalence of the two methods.

References

Two multi-port thermal coupling networks are derived.
Transformation between two thermal matrixes are conducted.
Thermal matrixes are transferred into the thermal multi-port coupling network.
Answers to the reviewers’ comments are marked in red.

----------------------- REVIEW 1 -----------------------

PAPER: 163
TITLE: A Multi-Port Thermal Coupling Model for Multi-Chip Power Modules Suitable for Circuit Simulators
AUTHORS: Zhongxu Wang, Huai Wang, Yi Zhang and Frede Blaabjerg

Overall evaluation: 2 (accept)

----------- Overall evaluation -----------
The paper proposes to compare two approach to model thermal coupling.
In section 1
It is not obvious to understand why the dimension of the thermal admittance matrix is N+1.
A: The author is so sorry for unclear description, and thanks the reviewer to point it out. The further explanation is given in the following.
Actually, if a linear thermal system is assumed as in this paper, the ambient temperature will be just a potential reference. In this case, the ambient temperature value will have no impact on the thermal model description of the thermal system, which can be fully defined and described through the temperature rise from ambient as done in this paper in the following.

\[
\begin{bmatrix}
\Delta T_1 \\
\Delta T_2 \\
\Delta T_3 \\
\Delta T_4 \\
P_1 \\
P_2 \\
P_3 \\
P_4
\end{bmatrix} =
\begin{bmatrix}
\psi_{11} & \psi_{12} & \psi_{13} & \psi_{14} \\
\psi_{21} & \psi_{22} & \psi_{23} & \psi_{24} \\
\psi_{31} & \psi_{32} & \psi_{33} & \psi_{34} \\
\psi_{41} & \psi_{42} & \psi_{43} & \psi_{44}
\end{bmatrix}
\begin{bmatrix}
P_1 \\
P_2 \\
P_3 \\
P_4
\end{bmatrix}
\]  
(Thermal impedance matrix: N order)  \hspace{1cm} (1)

\[
\begin{bmatrix}
\Delta T_1 \\
\Delta T_2 \\
\Delta T_3 \\
\Delta T_4 \\
P_1 \\
P_2 \\
P_3 \\
P_4
\end{bmatrix} =
\begin{bmatrix}
K_{11} & K_{12} & K_{13} & K_{14} \\
K_{21} & K_{22} & K_{23} & K_{24} \\
K_{31} & K_{32} & K_{33} & K_{34} \\
K_{41} & K_{42} & K_{43} & K_{44}
\end{bmatrix}
\begin{bmatrix}
P_1 \\
P_2 \\
P_3 \\
P_4
\end{bmatrix}
\]  
(Thermal admittance matrix: N order)  \hspace{1cm} (2)

However, previous papers considers the actual temperature instead of the temperature difference from the ambient. In this case, the dimension of the thermal admittance matrix and thermal impedance matrix will be N+1 and N respectively, where the additional dimension results from the ambient temperature. The differences can be told from the matrixes below clearly

\[
\begin{bmatrix}
T_1 \\
T_2 \\
T_3 \\
T_4
\end{bmatrix} =
\begin{bmatrix}
\psi_{11} & \psi_{12} & \psi_{13} & \psi_{14} \\
\psi_{21} & \psi_{22} & \psi_{23} & \psi_{24} \\
\psi_{31} & \psi_{32} & \psi_{33} & \psi_{34} \\
\psi_{41} & \psi_{42} & \psi_{43} & \psi_{44}
\end{bmatrix}
\begin{bmatrix}
P_1 \\
P_2 \\
P_3 \\
P_4
\end{bmatrix}
\]  
+ \[T_a\]  
(Thermal impedance matrix: N order)  \hspace{1cm} (3)

\[
\begin{bmatrix}
P_1 \\
P_2 \\
P_3 \\
P_4
\end{bmatrix} =
\begin{bmatrix}
K_{11} & K_{12} & K_{13} & K_{14} \\
K_{21} & K_{22} & K_{23} & K_{24} \\
K_{31} & K_{32} & K_{33} & K_{34} \\
K_{41} & K_{42} & K_{43} & K_{44}
\end{bmatrix}
\begin{bmatrix}
T_1 \\
T_2 \\
T_3 \\
T_4
\end{bmatrix}
\]  
(Thermal admittance matrix: N +1 order)  \hspace{1cm} (4)

Where \[T_a\] is the ambient temperature, \[K_{ai} = K_{ia} = -Y_{ii}, \sum_{j=1}^{4} Y_{ii} \].

Equ (4) can be derived by following the procedure below.
1. The heat balance equation for node 1 is
In section 2
Figure caption of fig 1 must be checked.
A: Thanks for the comment. The caption is now checked and revised from “Multi-port thermal coupling network with 4 nodes.” to the “Multi-port thermal coupling network derived from the thermal admittance matrix with 4 driving nodes.” The author hopes the new caption gives a better explanation for this figure.

The theoretical part in section 2, can be extended to make it more accessible.
A: The author is sorry to make the reviewer confused by the simplified equation derivation. As the answer to the question 1, some detailed equation deviation are listed above, and hope it can help the reviewer understand a little bit.

As the two methods give the same results, it can be useful to give advices about the best method in accordance with particular circuit or configuration.
A: Comparison between the two methods is really an important part to highlight the contribution of this paper, and make it clearer to show the differences of the two matrix. Thus thanks very much for this very nice suggestion, and revision about this point is added in this final paper in section 2 and 3.
- The end goals and impacted applications are missing. This point would make the originality of this work.

A: The potential applications do matter for a clear description of the contribution of this work. This part is now added in section 2 and section 5. Thanks very much for this very kind and important suggestion.

- Images and figures are unreadable because they are too small
- A representation of the DUT would help to understand the approach

A: Thanks very much for the kind comments. Font size in some figures are indeed small, thus Fig. 2 is enlarged and Fig. 6 and Fig. 7 are rearranged for a better view.

For the DUT, a more detailed description about the test setup and measurement method are made in this final version.

--------------------------- REVIEW 3 ---------------------------

PAPER: 163
TITLE: A Multi-Port Thermal Coupling Model for Multi-Chip Power Modules Suitable for Circuit Simulators
AUTHORS: Zhongxu Wang, Huai Wang, Yi Zhang and Frede Blaabjerg

Overall evaluation: 2 (accept)

------------- Overall evaluation ------------- Interesting paper. Proposes a novel approach to modelling complex with multi-source thermal problems, including cross-couplings.

I think the paper can have good reference value and surely good use within the specialist reliability community.

I find it better suited for poster presentation in view of its nature.

Thanks very much for the kind evaluation and recommendation for poster presentation. Since the final paper is revised for better illustration and explanation of the idea, further evaluation and support from this reviewer are needed. Thanks again.

--------------------------- REVIEW 4 ---------------------------

PAPER: 163
TITLE: A Multi-Port Thermal Coupling Model for Multi-Chip Power Modules Suitable for Circuit Simulators
AUTHORS: Zhongxu Wang, Huai Wang, Yi Zhang and Frede Blaabjerg

Overall evaluation: 2 (accept)
--- Overall evaluation ---

The paper deals with circuit simulator modeling of multi-chip power modules, a reliability related topic, hot for power modules designers. The paper is well organized. Good simulation and experimental results.

Some description should be improved for the reader’s better understanding:
- Section 3, lines 11-14: it is not clear to the reader where the negligible difference can be observed in the symmetrical characteristics

\[ \Psi_{t=100s} = \begin{bmatrix} 0.5880 & 0.2244 & 0.3058 & 0.2961 \\ 0.2228 & 0.5353 & 0.2466 & 0.2452 \\ 0.2974 & 0.2512 & 0.6172 & 0.2933 \\ 0.2954 & 0.2466 & 0.3092 & 0.5995 \end{bmatrix} \]

- Figs. 6 and 7: what is the ambient temperature? Only the temperature excursion should be taken into account for error estimation

\[ \text{A: The ambient temperature is 20 degree for all experiments and simulations, and as this reviewer mentioned, temperature difference or rise from the ambient temperature is only considered.} \]

- Section 4: how the dissipated power for every chip is measured?

\[ \text{A: Actually, the power of each chip is not measured from the experiment, but from the simulations. Since the on-state characteristics of IGBT used in the experiments are tested by the power device analyzer in the lab, and the test results are further used in the simulation. When the operating condition in the simulation is set the same as the one in the experiment, then the power loss of each devices can be approximately estimated.} \]

- Section 4: how the chip temperature is acquired?

\[ \text{A: The author is sorry to confuse this reviewer for unclear illustration of the experiment details due to the limit of the pages. Now the experiment part is more clearly illustrated in the final paper, and hope it is clear now. Moreover, the chip temperatures are measured by thermal camera as shown in Fig. 2. The item 1 is the thermal camera.} \]

Detailed comments and suggestions:
- Ref [6] is not cited in the text

\[ \text{A: Thanks a lot for this kind reminder. Now Ref [6] is cited.} \]


\[ \text{A: Thanks for the nice suggestion, and it is a good and relevant paper regarding multi-source thermal system, and it is cited in the final paper.} \]

- Pag. 1, column 1, line 16 “is” -> “are”
- Pag. 1, column 1, line 18 “the” -> “that”
- Pag. 1, column 1, line 20 “Fig. 1. While” -> “Fig. 1, while”
- Pag. 1: there is likely an editing problem which create inconsistency in the text between the end of column 1 and the begin of column 2, please revise
A: Thanks for the detailed comments, and they are very important for a good paper. Now all of them are revised as shown in the final paper.

------------------------ REVIEW 5 ------------------------
PAPER: 163
TITLE: A Multi-Port Thermal Coupling Model for Multi-Chip Power Modules Suitable for Circuit Simulators
AUTHORS: Zhongxu Wang, Huai Wang, Yi Zhang and Frede Blaabjerg

Overall evaluation: -2 (reject)

-------- Overall evaluation -------- It is not clear to this reviewer how this paper advances the state of the art. What is new?

A: The main contribution of this work is to explore the relationship between the two multi-port thermal network and the two thermal matrix (impedance and admittance). The thermal parameters in the multi-port network defined by admittance matrix is quite different from the normal thermal impedance, which contains only positive RC values. It actually contains negative RC values. Moreover, the multi-port network can be easily implemented with thermal resistor and capacitor only and without controlled temperature sources, and the power/heat is transferred in a more realistic manner like the current in electrical circuit. This seems more familiar for the electrical engineer.