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***Abstract*—Due to the increased cost, and time-demanding approach of conventional reliability improvement procedures, the transition towards model-based reliability assessment of power electronics becomes more and more crucial. Although important steps have been taken in this direction, the resulting lifetime prediction is still subject to different assumptions and uncertainties (e.g. mission profile data, modeling errors, lifetime models, etc.). Thus, this paper aims at investigating and quantifying the impact of the mission profile resolution on the reliability estimation of power IGBT modules and DC-link capacitors. For a 10 kW PV application case study, three mission profile sampling rates (1 minute/data, 30 minutes/data, and 60 minutes/data) are considered and benchmarked, with respect to the predicted lifetime of the power electronic components/system. Finally, an uncertainty analysis is performed for the resulting reliability metrics, and some initial guidelines for mission profile resolution selection are provided.**

***Index Terms*—Mission profile resolution, power IGBT module, DC-link capacitor, system-level reliability, uncertainty analysis.**

I. Introduction

Nowadays, due to the high integration of power electronics in many mission-critical applications, the reliability requirements of power converters, and the capability to withstand long operating hours under harsh environmental conditions are becoming more and more demanding.

However, a survey presented in [1] concluded that approximately 37% of the total unexpected failures of a 3.5 MW photovoltaic (PV) plant have been caused by the PV inverter, and thus classifying the power converter as the "bottleneck" of the system with respect to reliability. Moreover, a component-level reliability survey has been carried out in [2], and it has been found that the power semiconductor devices and the capacitors are the most prone-to-failure components of the power electronic system. Consequently, the unexpected wear-out failures of the power electronic components will lead to an increase in maintenance cost, and a cutback in the total energy production of the system (due to downtime), and thus resulting in a higher cost of energy conversion.

In order to address the issues related to reliability and to the high failure rates of power electronics, conventional reliability improvement approaches (e.g. power cycling testing, component over-design, FMEA analysis, etc.) are usually employed. However, due to their increased cost and time-demanding processing time, a strong paradigm shift towards model-based reliability assessment has been seen in recent years. As a result, many mission profile based reliability assessment procedures have been proposed throughout the literature, for various applications (e.g. PV [3], wind power generation [4], motor drive systems [5], etc.). According to the input system specifications and mission profiles, the thermal loading which occurs on the power electronic components can be derived, and inherently a more accurate lifetime estimation (in comparison with conventional statistics-based methods) can be achieved.

Unfortunately, the accuracy of the resulting reliability metrics is subject to many factors, such as: environmental / operating mission profiles [6], loss and thermal modeling, cycle counting method, damage accumulation method or the lifetime model itself [7]. All of these factors will introduce a certain degree of uncertainty. Thus, by understanding the underlying uncertainties and assumptions behind the model-based reliability assessment analysis, a more confident lifetime estimation can be achieved.

An initial step towards investigating the impact of mission profile data on the reliability of IGBT modules has been taken in [6], for an offshore-based Modular Multilevel Converter (MMC) application. However, the influence on the system-level reliability and on the DC-link capacitor, which is known to have a much larger thermal time constant and inherently a different thermal behavior than the power devices [8], have not been considered.

Therefore, in this paper, the impact of mission profile resolution on the reliability evaluation of the power semiconductor devices and DC-link capacitor used within a single-stage grid-connected PV application, is studied and quantified. Initially, a generic reliability assessment procedure is presented and the employed electro-thermal, and lifetime models are briefly introduced. Afterwards, the annual solar irradiance and ambient temperature mission profiles, under three different sampling rates (1 minute/data, 30 minutes/data and 60 minutes/data), are used in order to investigate the reliability performance of the PV inverter power stage, and its active/passive components. Finally, the resulting reliability metrics are benchmarked and the uncertainties related to the PV mission profile resolution are quantified.

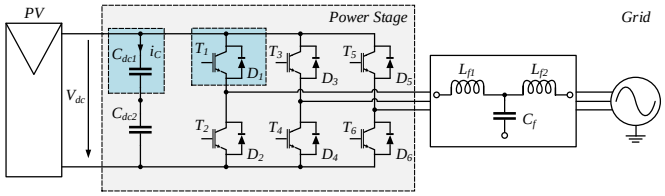


Fig. 1. Single-stage grid-connected PV application.

II. Mission profile based reliability evaluation of power electronics in PV applications

A. Single-stage grid-connected PV application case study

A typical PV application is first designed as a study case, which is shown in Fig. 1, and its parameters are presented in Table I. The system consists of a 10 kW PV plant connected to the grid through a single-stage three-phase PV inverter. Additionally, by using an LCL-filter on the grid-side of the inverter, the unwanted harmonics can be reduced.

In order to meet the DC-link voltage requirements two Nippon Chemi-con 400 V aluminum electrolytic capacitors are connected in series on the DC-bus. The power module choice is an Infineon FS50R12KT with a rated current of 50 A and 1200 V rated voltage.

The input mission profiles for the PV system are the solar irradiance and ambient temperature as shown in Fig. 2. The mission profiles have been recorded during the course of one year with an original sampling rate of 1 minute/data, in Aalborg, Denmark. The mission profiles corresponding to the 30 minutes/data and 60 minutes/data resolutions have been obtained by down-sampling the original data set by an integer factor of 30, and 60, respectively.

B. Mission profile translation to component thermal loading

An application-independent reliability assessment procedure has been proposed in [9] and it is employed in order to determine the component-level and system-level reliability of the PV inverter power stage, under the given mission profiles and operating conditions. Before, analyzing the lifetime estimation of the components of interest, the input mission profiles need to be translated into the main stressors that lead to the wear-out failure of the components: temperature and voltage.

TABLE I. Parameters for study-case PV application.

Parameter	Symbol	Value	Unit
PV array rated power	P_o	9.88	[kW]
Inverter rated power	P_{inv}	10	[kW]
DC-link voltage	V_{dc}	600	[V]
Switching frequency	f_{sw}	18	[kHz]
Grid frequency	f_h	50	[Hz]
Grid voltage	V_g	230	[$V_{\text{ph, rms}}$]
Filter inductance 1	L_{f1}	4.05	[mH]
Filter inductance 2	L_{f2}	4.05	[mH]
Filter capacitance	C_f	4.3	[μF]

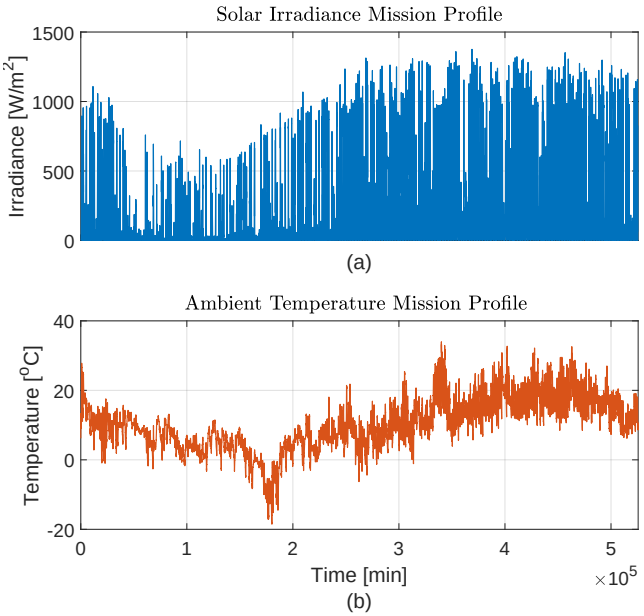


Fig. 2. Typical PV environmental mission profiles: (a) solar irradiance, and (b) ambient temperature.

As shown in Fig. 3, the environmental mission profiles and the system specifications will represent the inputs for the system-level models [10], in which the electro-mechanical dynamical behavior of the PV application study-case will be analyzed, and thus the converter-level electrical loading can be determined.

Afterwards, the resulting electrical loading can be introduced in the component-level models. Within this stage of the reliability assessment procedure, the loss and thermal characterization of the components will take place, and the voltage and current loading of the power devices and DC-link capacitors are translated into the corresponding thermal stress.

1) Power Semiconductor Devices: The current flowing through the devices will be fed into the power loss model [11], where the conduction losses of the transistor/diode are determined based on the conduction voltage (transistor) and forward voltage (diode) characteristics. Similarly, the switching losses are calculated as a function of the switching energy (transistor), and reverse recovery energy (diode) characteristics. The loss characteristics are usually provided by the manufacturer in the datasheet or it can be determined by means of experimental tests. A detailed description of the power loss model and of the equations used to describe the thermal dependency of the power device losses can be found in [12, 13].

The total losses generated by the power semiconductor devices will represent the input to the thermal model. A 4-layer RC Foster model is used in order to characterize the junction-to-case thermal impedance ($Z_{(\text{j}-\text{c})}$) of the devices, as presented in the following equation:

$$Z_{(\text{j-c})} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{1}{\tau_i}}\right) \tag{1}$$

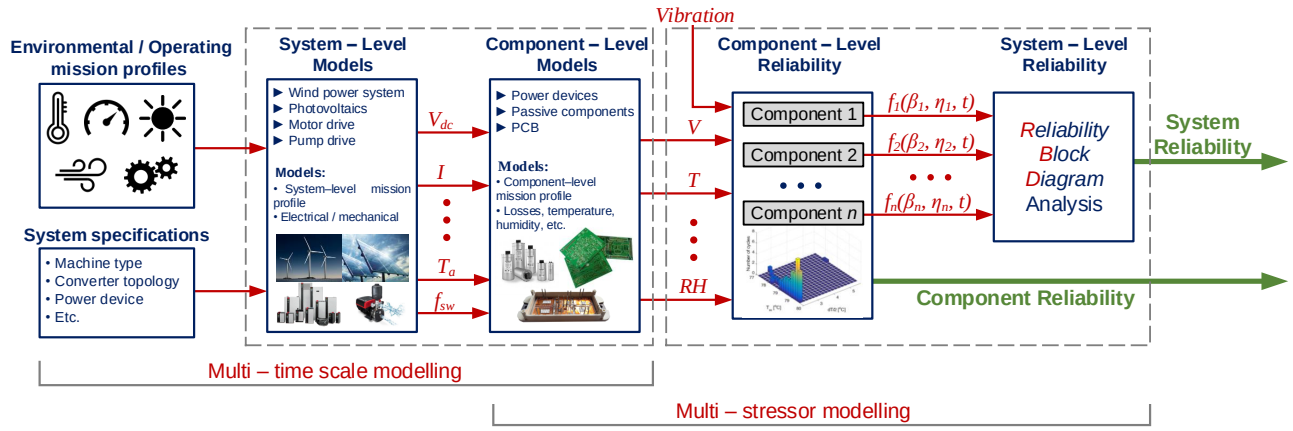


Fig. 3. Generic reliability assessment procedure for power electronic components/systems [9].

where, n represents the number of layers of the thermal network, R_i represents the thermal resistance and τ_i represents the thermal time constant. The values of the thermal resistance and thermal time constant have been extracted from the manufacturer datasheet, for each of the four layers of the Foster network.

Assuming a constant case-to-ambient temperature ($T_{\mathrm{c-a}} = 15[^oC]$), used for characterizing the enclosure thermal behavior, the junction temperature (T_j) of the power devices can be derived as follows:

$$T_j(t) = Z_{\text{(j-c)}}(t) \cdot P_{\mathrm{T/D,loss}} + T_{\mathrm{c-a}}(t) + T_a(t) \tag{2}$$

where, $P_{\mathrm{T/D,loss}}$ represents the total power losses generated by the transistor/diode, and T_a represents the ambient temperature mission profile.

2) DC-Link Capacitor: A similar electro-thermal modeling approach can be used for the aluminum electrolytic capacitor [14]. According to the calculated RMS value of the current flowing through the capacitor ($I_{\mathrm{C,RMS}}$) the total power losses can be determined based on the following equation:

$$P_{\mathrm{C,loss}} = I^2_{\mathrm{C,RMS}} \cdot ESR(\omega) \tag{3}$$

where, $ESR(\omega)$ represents the frequency dependent Equivalent Series Resistance (ESR) provided by the capacitor manufacturer in the datasheet.

Finally, the hotspot temperature (T_h) of the capacitor is given as,

$$T_h(t) = Z_{\text{(h-c)}}(t) \cdot P_{\mathrm{C,loss}} + T_{\mathrm{c-a}}(t) + T_a(t) \tag{4}$$

where, $Z_{\text{(h-c)}}$ represents the hotspot-to-case thermal impedance of the capacitor, $T_{\mathrm{c-a}}$ represents the assumed case-to-ambient temperature, and T_a represents the ambient temperature mission profile. Similar to power devices, the hotspot-to-case thermal impedance of the capacitor can be described, according to (1), by means of thermal resistance and thermal time constant.

C. Component-level reliability modeling

Based on the obtained component-level mission profiles (e.g. junction temperature, voltage, hotpot temperature), the reliability evaluation of the components of interest can be carried out by means of strength models [15].

1) Power Semiconductor Devices: Because the power device lifetime model requires constant and regulated thermal cycles in order to be applied correctly, a Rainflow counting algorithm is employed [16]. By applying the given counting method, the thermal stress of the devices can be represented as thermal cycle amplitude (ΔT_j), thermal cycle mean value (T_{jm}), and thermal cycle on-time period (t_{on}). The resulting thermal cycles can now be correctly mapped into a lifetime model [17], and thus obtain the estimated number of cycles to failures of the transistor/diode.

2) DC-Link Capacitor: On the other hand, there is no need to further process the thermal stress data of the capacitor by means of counting method, as it can be directly linked to a lifetime model. A simplified lifetime model [18] which considers only the wear-out failures due to voltage and temperature, will be employed for the reliability estimation of the capacitor. The analytical equation of the capacitor strength model is given below:

$$L = L_0 \cdot \left(\frac{V}{V_0}\right)^{-n_1} \cdot 2^{\frac{T_0 - T}{n_2}} \tag{5}$$

where, L and L_0 are the lifetimes under operating and reference conditions, respectively, V is the voltage under operating condition, V_0 is the voltage under reference condition, T represents the temperature under use condition and T_0 is the temperature under reference condition. Additionally, n_1 represents the voltage stress exponent (usually varies between 3.5 and 9.4) and n_2 represents the temperature stress exponent (varying between 10 and 13) [18].

The outputs of the power device/DC capacitor lifetime models can be used in order to determine the total accumulated

damage, which occurs on the component. The consumed lifetime (CL) can be described by Miner's rule [19]:

$$CL = \sum_{n=1}^{m} \frac{100}{N_n}(\%) \tag{6}$$

where, m represents the total number of cycles resulting from the Rainflow counting algorithm, and N_n represents the number of cycles till failure at the nth stress level.

Finally, the variations which might occur in the lifetime model coefficients and/or stressors can be taken into account by means of Monte Carlo simulation [20], and thus, the unreliability curves and lifetime distributions of the power electronic components can be obtained.

D. System-level reliability modeling

The individual reliability information of each component can be used in order to derive the system-level lifetime estimation through Reliability Block Diagram (RBD) analysis [21]. Due to the fact that the failures induced by random/catastrophic events are difficult to model and estimate, only the wear-out failures of the components will be taken into account. The reliability of the PV inverter power stage can be calculated according to the following equation:

$$F_{\text{Sub}}(t) = 1 - \prod(1 - F_{\text{Comp(i)}}(t)) \tag{7}$$

where, F_{Sub} represents the system failure function, and $F_{\text{Comp(i)}}$ represents the individual component failure function.

III. Reliability Performance of Power Electronics under Different Mission Profile Resolutions

The reliability evaluation of the power electronic components used within the stady-case PV application is carried out according the reliability assessment procedure presented in Fig. 3. Three mission profiles sampling rates have been selected (1 minute/data, 30 minutes/data, and 60 minutes/data), and are used in order to benchmark and quantify their impact on the lifetime prediction of the components of interest.

A. Power Semiconductor Devices

Based on the electro-thermal model presented in Section II, the junction temperature of the transistor and diode have been calculated according to the input mission profiles (Fig. 2) and system specifications (Table I). The junction temperature of the transistor under the selected mission profile sampling rates is shown in Fig. 4.

It is clear that the sampling rate does not have any major impact on the overall temperature swing which occurs in the transistor. This is due to the fact that the thermal dynamics of the transistor are in the range of milliseconds/seconds, and are much faster than the actual sampling rates of the mission profiles. Thus, the junction temperature of the transistor will manage to reach steady-state as long as the sampling rate is kept above its thermal time constant, and inherently allowing for an accurate thermal characterization. On the other hand, as shown in Fig. 4, some of the shorter cycles will be neglected when using a lower sampling rate.

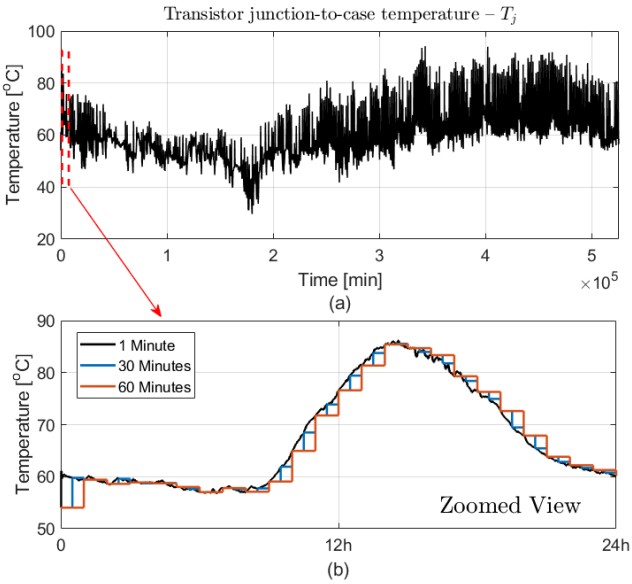


Fig. 4. Transistor junction temperature under selected mission profile sampling rates: (a) Yearly profile, and (b) Daily profile.

Similar conclusions can be drawn from the diode junction temperature, as plotted in Fig. 7.

In order to get a better insight into the resulting thermal data, and to correctly map it into the lifetime model, the previously discussed Rainflow counting algorithm is applied. As expected, from the thermal cycle representation shown in Fig. 5, it can be seen that the thermal cycles with an on-time period shorter than the mission profile sampling rate will be neglected. Thus, for lower sampling rates, less thermal cycles are expected at the output of the counting algorithm, and thus, a more optimistic lifetime estimation. A similar conclusion can be drawn for the thermal cycles representation of the diode junction temperature shown in Fig. 6.

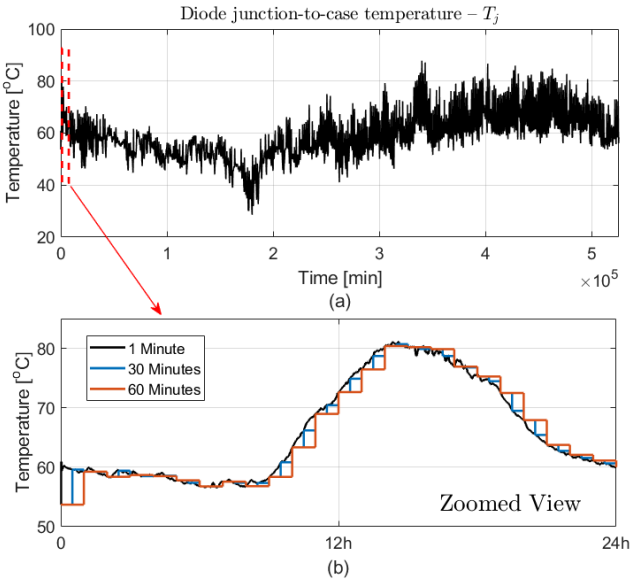
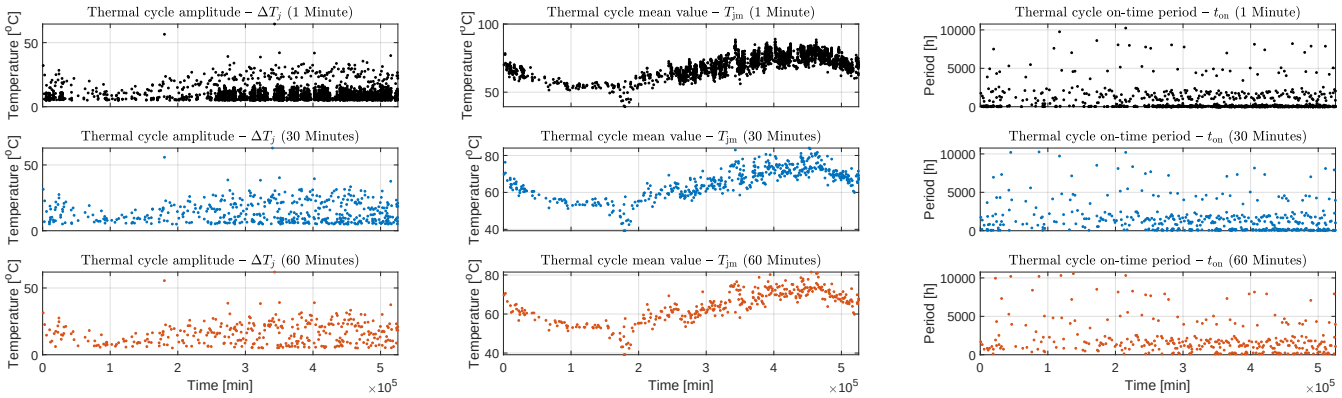
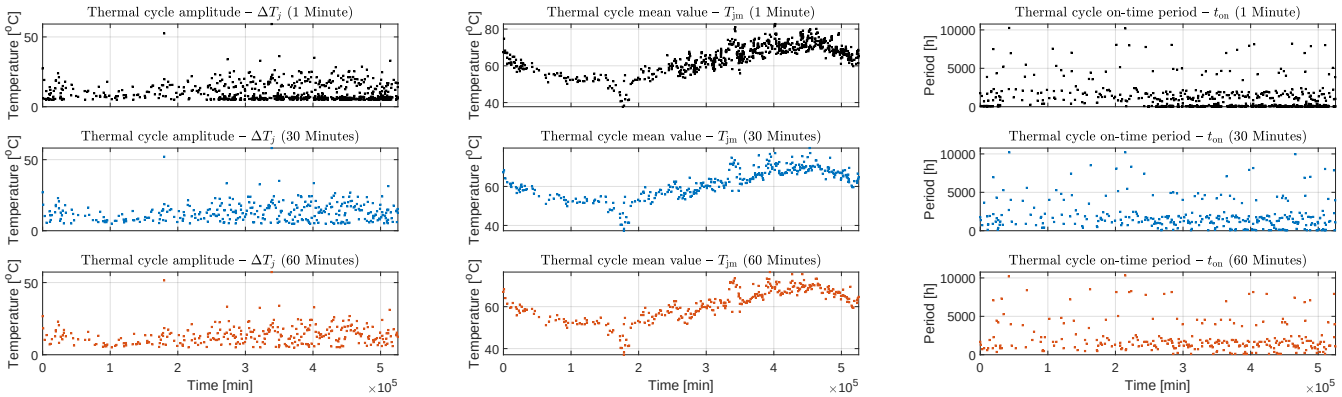


Fig. 7. Diode junction temperature under selected mission profile sampling rates: (a) Yearly profile, and (b) Daily profile.



(a) Thermal cycle amplitude. (b) Thermal cycle mean value. (c) Thermal cycle on-time period.

Fig. 5. Rainflow counting algorithm results - Transistor junction temperature representation as ΔT_j, T_{jm}, and t_{on}.



(a) Thermal cycle amplitude. (b) Thermal cycle mean value. (c) Thermal cycle on-time period.

Fig. 6. Rainflow counting algorithm results - Diode junction temperature representation as ΔT_j, T_{jm}, and t_{on}.

Considering the determined thermal stress for the transistor and diode, the component-level reliability procedure presented in the previous section is applied for a B_1 lifetime (1% probability of failure) and an assumed 5% variation in the lifetime model coefficients and stressors. The resulting unreliability curves for the transistor/diode under the selected mission profile resolutions are plotted in Fig. 8. In case of the transistor, the lower mission profiles resolutions (30 minutes/data, and 60 minutes/data) will results in a higher lifetime expectancy with approximately 20% than the original sampling rate. This is due to the fact that by neglecting the short-term thermal cycles, less damage occurs on the device.

On the other hand, since the thermal loading of the diode does not present as many short-term temperature fluctuations as the transistor, the impact of the mission profile resolution is not as significant.

B. DC-Link Capacitor

Similar to the reliability assessment procedure of the power devices, the capacitor electro-thermal models are employed in order to determine its hotspot temperature, under the given mission profiles and system operating conditions.

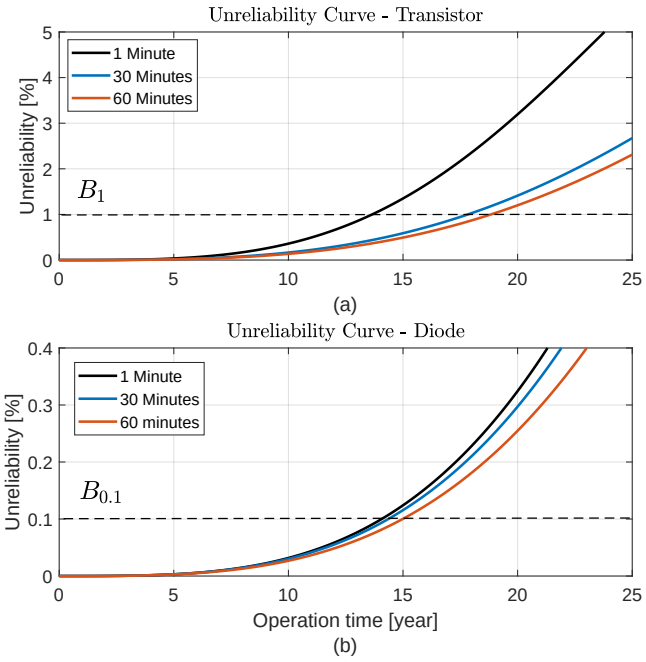


Fig. 8. Unreliability curves under selected mission profile sampling rates for: (a) transistor, and (b) diode.

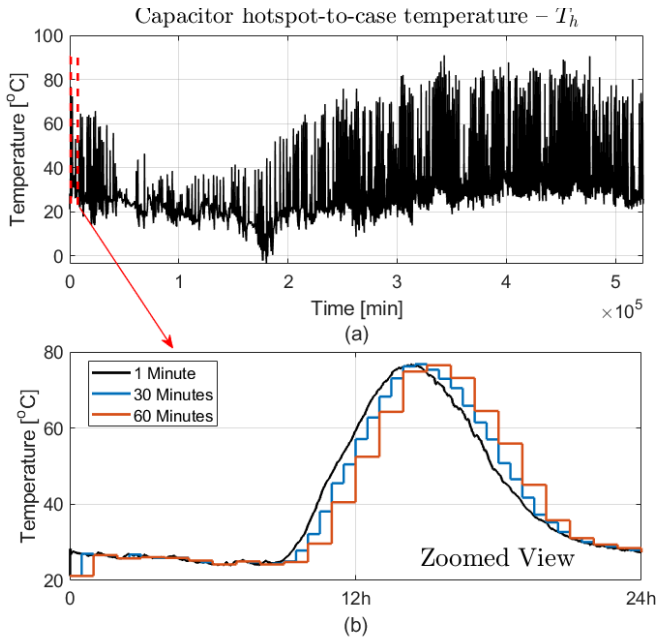


Fig. 9. Capacitor hotspot temperature under selected mission profile sampling rates: (a) Yearly profile, and (b) Daily profile.

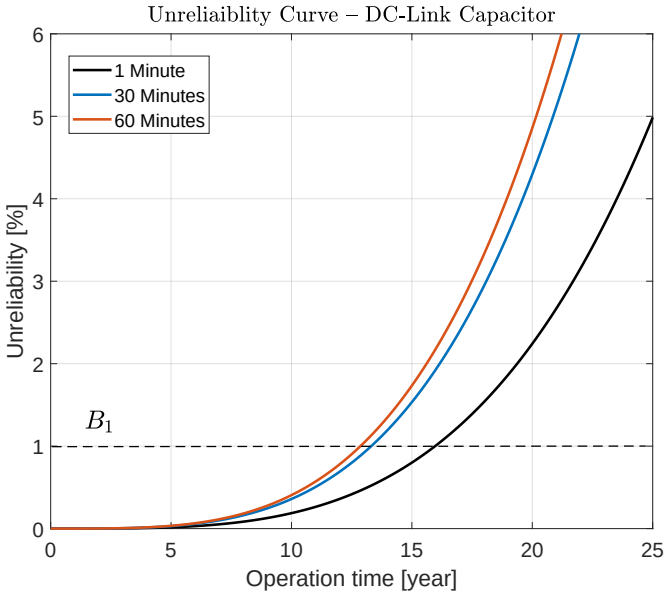


Fig. 10. Unreliability curves for DC-link capacitor under selected mission profile sampling rates.

The resulting thermal stress of the capacitor for the selected mission profile resolution is shown in Fig. 9. Although no significant impact can be seen in term of overall temperature swing, it should be noted that the thermal dynamics of the capacitor are much slower than those of the power devices. Thus, for the given capacitor, a thermal time constant of approximately 10 minutes will give a different thermal behavior.

For the high mission profile resolution (1 minute/data) the capacitor does not manage to reach its steady-state temperature, before another power pulse is applied, and thus resulting in a less accurate thermal characterization. On the other hand, for the sampling rates above the capacitors thermal time constant (30 minutes/data, and 60 minutes/data), the hotspot temperature reaches steady-state and thus more thermal stress will be applied to the capacitor.

The correlation between the mission profile sampling rate and the internal time constant of the capacitor can be more clearly seen from its unreliability curves, plotted in Fig. 10. By allowing the capacitor temperature to reach steady-state, the lower sampling rates enable a more accurate thermal characterization and inherently will lead to a lower lifetime expectancy. On the other hand, the high mission profile resolution will result in a more optimistic lifespan prediction, as the damage inflicted by the slow dynamic thermal stress will be significantly lower.

C. PV Inverter Power Stage

Finally, assuming that all six transistors of the PV inverter power stage have the same reliability performance, all six diodes have the same reliability performance as presented in Fig. 8, and both capacitors of the DC-link present the same lifetime prediction as shown in Fig. 10, the reliability estimation of the power stage can be carried out.

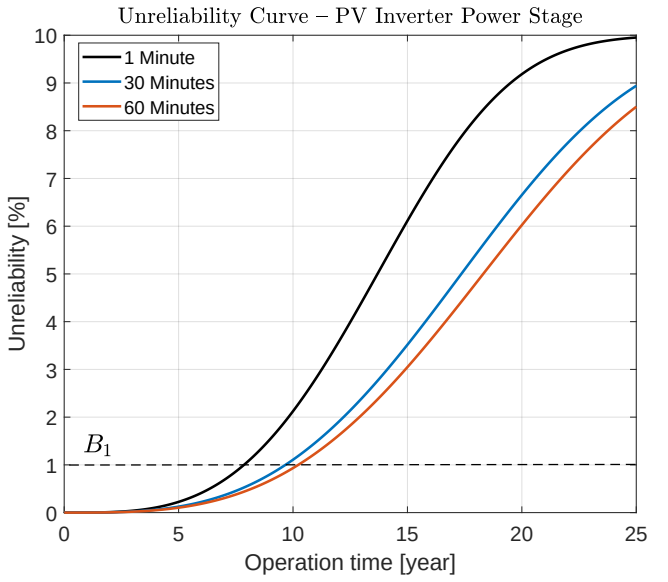
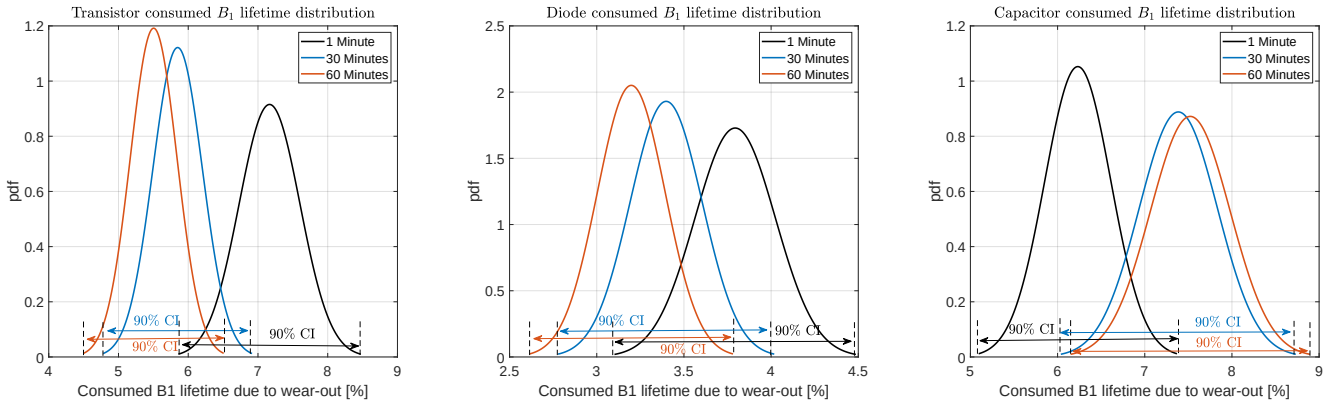


Fig. 11. Unreliability curves for PV inverter power stage under selected mission profile sampling rates.

By means of Reliability Block Diagram (RBD) analysis the individual reliability information of the components of interest are merged according to (7), and the unreliability curves of the power stage are obtained and shown in Fig. 11. Due to the stronger impact of the transistor reliability, the high sampling rate of the mission profile will lead to a decrease of approximately 30% in lifetime estimation for the power stage, compared to the lower sampling resolutions.



(a) Transistor (b) Diode (c) DC-link capacitor

Fig. 12. Consumed B_1 lifetime distribution for the components of interest, under the selected mission profile sampling rates.

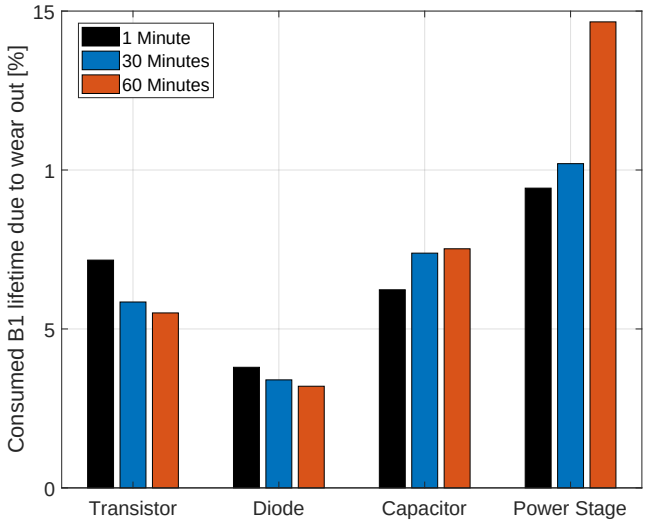


Fig. 13. Accumulated damage of the components of interest.

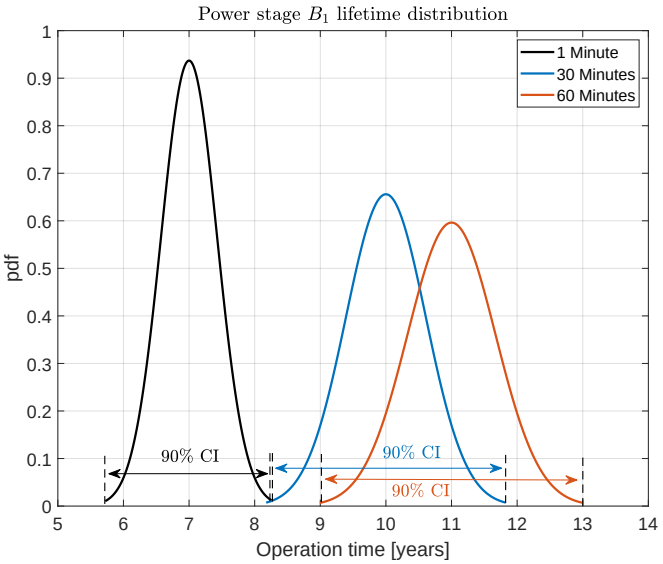


Fig. 14. B_1 lifetime distribution of the inverter power stage.

IV. Uncertainties due to Mission Profile Sampling

In order to be able to improve the confidence and accuracy of the model-based reliability assessment procedure, the underlying assumption and uncertainties introduced by the mission profile sampling rate need to be taken into account. Thus, to address this issue, an uncertainty analysis needs to be performed and the impact on the lifetime prediction outcome (shown in Fig. 13) needs to be quantitatively analyzed.

The uncertainty analysis is performed by assessing the reliability of the power electronic components under the same system operating condition and lifetime model, but with different mission profile sampling rates. In this paper the uncertainty analysis is performed under three selected resolutions.

From the probability density function (pdf) of the consumed B_1 lifetime distribution of the transistor, diode, and DC-link capacitor, shown in Fig. 12 for 90% confidence interval (CI), it is clear that the selection of mission profile resolution will have a significant impact on the lifetime prediction of power electronic components.

Similarly, by looking at the pdf of the PV inverter power stage B_1 lifetime distribution, the impact of the mission profile sampling rate becomes more clear. As shown in Fig. 14, if a 1 minute/data sampling rate is selected, the reliability assessment procedure indicates that with a 90% confidence interval 1% of the population will fail between approximately 5.8 years and 8.2 years.

On the other hand, if 60 minutes/data are used for sampling the environmental mission profiles, with a 90% confidence interval, the lifespan of 1% of the population will be between 9 and 13 years.

V. Conclusions

In this paper, the influence of long-term mission profile resolution on the reliability assessment of the power electronic components of a PV application has been investigated. Initially, a 10 kW single-stage three-phase PV application has been designed, and a model-based reliability assessment

procedure for power electronics has been introduced. The electro-thermal and reliability models used for the lifetime prediction of the active/passive components of interest have been briefly described, and successfully applied in order to assess the lifetime estimation of the power electronics under three different mission profiles sampling rates (1 minute/data, 30 minutes/data, and 60 minutes/data). From the obtained reliability metrics, it has been concluded that the impact of mission profile resolution on the power devices is different from the passive components. In case of power devices, due to their fast thermal dynamics, a higher sampling rate is recommended in order to cumulate as much information as possible in the thermal and lifetime modeling, whereas for the DC-link capacitor the optimum sampling resolution should be closely related to its thermal time constant, as to allow the capacitor hotspot temperature to reach steady-state. Finally, the impact of the mission profile sampling rates on the lifetime distribution of the transistor, diode, capacitor, and power stage have been quantified by means of uncertainty analysis, which has shown that a significant deviation in the lifetime can be seen between the selected sampling rates. The proposed study gives a better understanding of the underlying assumptions and uncertainties introduced by the mission profile resolution, during the model-based reliability analysis of power electronics in PV applications, and serves as a first step towards an optimum resolution selection for long-term mission profiles.

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