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Published in:
Proceedings of 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)

Publication date:
2018

Document Version
Accepted author manuscript, peer reviewed version

Citation for published version (APA):
Novak, M., Nyman, U. M., Dragicevic, T., & Blaabjerg, F. (2018). Statistical Performance Verification of FCS-MPC Applied to Three Level Neutral Point Clamped Converter. In *Proceedings of 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)* (pp. 1-10). Article 8515598 IEEE Press. https://www.scopus.com/record/display.uri?eid=2-s2.0-85056990476&origin=inward&txGid=61a2d2075d383c20252f0ba8217de483

Statistical Performance Verification of FCS-MPC Applied to Three Level Neutral Point Clamped Converter

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Keywords

≪Converter control≫, ≪Robustness≫, ≪Statistics≫, ≪Uninterruptible Power Supply (UPS)≫, ≪Voltage Source Converter (VSC)≫

Abstract

In this paper we demonstrate how a statistical model checking approach can be used to check the dynamic performance of the finite set model predictive control algorithm for a standalone 3-level neutral point diode clamped converter. The robustness of the control algorithm under parameter uncertainty is also analyzed. Finite control set model predictive control (FCS-MPC) algorithm has found many applications in power electronics due to the straightforward control design and the possibility to include different control objectives. The control algorithm for 3-level neutral point diode clamped (NPC) converter has to address several objectives to provide optimal reference tracking during load transients. Therefore, looking from the perspective of the implementation, the FCS-MPC algorithm suits the control requirements of NPC converter. However, the problem remains in performing an analytical performance verification of the algorithm to demonstrate its robustness, which is compulsory for any industrial application. In this paper, we present how a statistical model checking approach can be used to solve this problem and also provide valuable data about the algorithm's performance during transients and in the case of parameter uncertainty. A benchmark model is created in Matlab/Simulink to validate the correct system modeling in UPPAAL SMC toolbox.

Introduction

The basic concept of using a higher number of switching devices and sources with the aim to reach higher power levels was introduced in 1975 [1]. Today the usage of the multilevel converters is unavoidable in the medium and high voltage applications. However, with the higher number of switching devices and voltage sources, the complexity of control algorithms has also increased, since multilevel topologies introduce additional control objectives. For the Neutral Point Clamped (NPC) topology shown in Fig. 1 the additional objective might be the neutral point voltage balancing. During the switching states when the neutral point is clamped to the converter output to achieve zero voltage output, a current is flowing through the clamping diode resulting in an unbalanced capacitor charging/discharging process. Both linear and non-linear algorithms are successfully dealing with the issue using various methods presented in the literature e.g. [2–6]. Linear methods are dominating in applications as the algorithms are well known and have matured over time. However, in this paper we will address the non-linear algorithms from the family of predictive control algorithms. Simple implementation of the control objectives in the cost function is one of the main reasons why Model Predictive Control (MPC) is preferred over linear control algorithms. By adjusting the weighting factors in the cost function the control objective priorities of the algorithm can easily be changed.

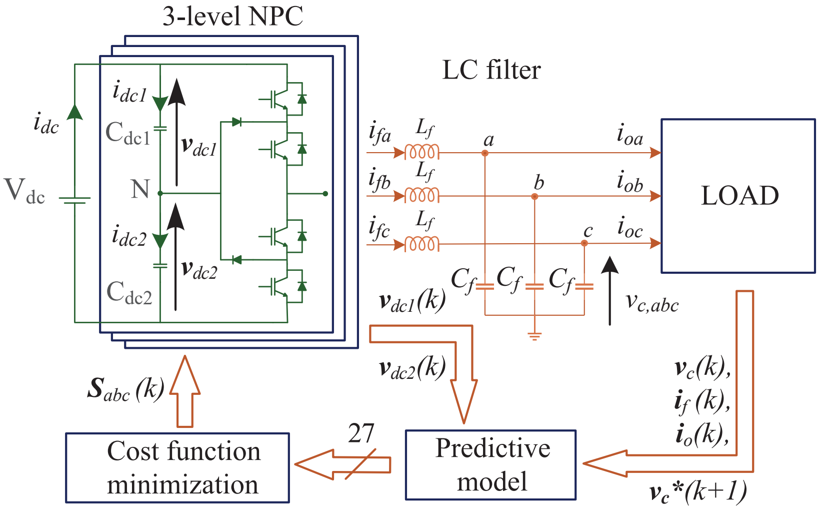


Fig. 1: Simplified system model scheme of stand-alone NPC converter using model predictive control.

One of the most intuitive algorithms in the MPC family is the Finite Control Set (FCS) MPC algorithm with a prediction horizon length $n = 1$. In [7] dynamic response and tracking reference of the FCS-MPC algorithm are compared to the responses obtained by a linear controller. The implemented FCS-MPC algorithm succeeded in maintaining the dc link voltage balance and reducing the switching frequency. Moreover, no interaction between the load current components and a lower tracking error were observed for the FCS-MPC. It is stressed that the method can easily be implemented in the available DSPs and there is no need for large look up tables or additional control blocks in order to achieve the capacitor voltage balance. FCS-MPC can also be used with a modulator to maintain a fixed switching frequency as implemented in [8] or by using commutation limitations as demonstrated in [9]. Although the FCS-MPC algorithms were successfully implemented, to the authors best knowledge, the analytically verification of the algorithm's performance and robustness are yet to be done [10, 11]. For the control algorithm to be applicable in the industry, it is required to know how it will respond to dynamics and how parameter uncertainty affects its reference tracking abilities. In other words, stability assessment of the closed loop control is needed. Steady-state and transient performance testing are usually done by running multiple simulations or experiments [12–14]. Unfortunately, these methods do not define the closed loop stability and running multiple experiments is rather time consuming and unpractical. The most relevant contribution in this area was done in [15], where the authors designed a cost function so that Lyapunov stability theory could be used to guarantee the stability of the FCS-MPC algorithm. Still the stability is guaranteed only in the neighborhood of the system reference and the cost function design lost the simple structure it had before.

To be applicable for use by industrial engineers, the approach for analytical validation should remain as simple as the control design and it should be adaptable to all topologies. Running multiple simulations does sound promising but there are certain questions that need to be answered so the procedure can be addressed as a verified method:

- How many simulation runs are required to determine the performance?
- How can we design the model to evaluate all possible transient responses and model uncertainties needed for the robustness test?
- Can we guarantee the reliability of the validation process?

Also some events have a higher occurrence rate and some events are more seldom so they should have an appropriate effect on the final results. In this paper we will present a promising approach that can answer these questions. Statistical model checking (SMC) is an approach that uses powerful tools from statistics to evaluate the models and obtains results about their behavior with defined reliability of the validation process. One of the tools that can be used to perform the SMC is Uppaal SMC [16]. Using the Verifier feature in Uppaal SMC, the performance of a deterministic or stochastic controller can be verified in a stochastic environment. By running several consecutive simulations in a time efficient manner it will estimate the probability of the specified event with confidence levels and its probability distribution. Simulation outcomes are visualized in the form of probability distributions, evolution of the number of runs with timed bounds and computation of expected values. Schedulability analysis, verification of biological systems and performance evaluation of controller strategies are some of published UPPAAL toolbox applications [16–19]. The system model under performance validation will be described in the next section. Afterwards we will illustrate the idea behind the SMC and how this approach is suitable for FCS-MPC performance validation. The results will be presented in the last section.

System model

The FSC-MPC algorithm performance verification will be presented on a 3L-NPC converter in standalone operation with an LC output filter and a resistive load as seen in Fig. 1. The execution of the algorithm can be summed up in a couple of steps that are iteratively conducted during every sampling period T_s:

- measurement of the system voltages (v_{dc1}, v_{dc2}, v_c) and currents (i_f, i_o) needed for calculation of the predicted values
- calculation of the predicted system voltages and currents for all possible converter switching states
- cost function value calculation for each prediction
- selection of the converter switching state that minimizes the cost function
- application of the selected switching state

The calculation of the predicted system voltages and currents is based on the differential equations describing the converter DC and AC side dynamics. The DC side dynamics are modeled through the DC link capacitor charging equations:

$$v_{dc1,2}(t) = C_{dc1,2}\frac{di_{dc1,2}(t)}{dt} \tag{1}$$

$$i_{dc1}(t) = i_{dc}(t) - (H_{1a}i_{fa}(t) + H_{1b}i_{fb}(t) + H_{1b}i_{fb}(t)) \tag{2}$$

$$i_{dc2}(t) = i_{dc}(t) + (H_{2a}i_{fa}(t) + H_{2b}i_{fb}(t) + H_{1b}i_{fb}(t)) \tag{3}$$

where $v_{dc1,2}(t)$ are voltages across the capacitors C_{dc1} and C_{dc2} and $i_{dc1,2}(t)$ are the respective charging currents. $i_{dc}(t)$ is the DC source current, $i_{fabc}(t)$ are the inverter phase currents, H_{1x} and H_{2x} are indicator functions. H_{1x} will return 1 if the phase leg $x \in a,b,c$ is connected to $V_{dc}/2$ while H_{2x} returns 1 if the phase leg is connected to $-V_{dc}/2$, otherwise the function values are 0. The AC side dynamics can be described by LC output filter equations in the stationary $\alpha\beta$ frame:

$$i_{f\alpha\beta}(t) = C_f\frac{dv_{c\alpha\beta}(t)}{dt} + i_{o\alpha\beta}(t) \tag{4}$$

$$v_{i\alpha\beta}(t) = L_f\frac{di_{f\alpha\beta}(t)}{dt} + v_{c\alpha\beta}(t) \tag{5}$$

where $i_{f\alpha\beta}$ and $i_{o\alpha\beta}$ are the inductor and load currents, $v_{c\alpha\beta}$ and $v_{i\alpha\beta}$ are filter capacitor and inverter output voltages, L_f and C_f are filter inductance and capacitance. These system equations are discretized using the Euler forward method and afterwards used to calculate the future states of system voltages and currents. The designed cost function for the NPC converter includes three objectives: minimization of the reference tracking error, neutral point voltage balancing and minimization of commutation number during two sampling instants. In the algorithm this is formulated as follows:

$$\begin{aligned}
g &= (v^*_{c\alpha} - v^P_{c\alpha})^2 + (v^*_{c\beta} - v^P_{c\beta})^2 + \lambda_d g_d + \lambda_{dc} g_{dc} + \lambda_{sw} g_{sw} && (6)\\
g_d &= (i^P_{f\alpha} - i_{o\alpha} + C_f \omega_{ref} \cdot v^*_{\beta})^2 + (i^P_{f\beta} - i_{o\beta} - C_f \omega_{ref} \cdot v^*_{\alpha})^2 && (7)\\
g_{dc} &= (v^P_{dc1} - v^P_{dc2})^2 && (8)\\
g_{sw} &= \sum_{x=a,b,c} |S_x(k) - S_x(k-1)|, && (9)
\end{aligned}$$

Weighting factors λ_d, λ_{dc} and λ_{sw} define the importance of each cost function part: the derivative part (g_d) is used to improve the reference tracking by taking into account the heading of the capacitor voltage trajectory as demonstrated in [20], DC link balance part (g_{dc}) to minimize the difference between the capacitor voltages caused by the flow of the neutral point current while the converter leg is clamped to the neutral point, and the switching frequency minimization part g_{sw} to minimize the number of commutations. The latter part is achieved by comparing the previous $S_x(k-1)$ and current $S_x(k)$ switching state for all converter phase legs $x \in a, b, c$.

SMC approach in power electronics

In [16] SMC is defined as a series of techniques that monitor several simulation runs of the system with respect to some properties and afterwards use the results from the statistical theory in order to get an overall estimate of the design correctness. To simplify, the system is simulated for a finite number of runs, resulting in a number of samples that are used to test the specified hypothesis. For hypothesis testing, tools from statistics like Monte Carlo simulation or sequential hypothesis testing are used. The end result of these tests is the probability of satisfaction or violation of the specified property. The SMC approach is already successfully being used in aeronautics and embedded automotive systems, sensor networks, communication systems to solve problems that are beyond the abilities of classical formal techniques [17,19,21]. The tool used to perform the SMC in this paper is Uppaal SMC. Uppaal SMC was selected as it has all the necessary features to model a hybrid system that features both continuous and discrete behavior. Moreover, in [22] the performance of Uppaal SMC was compared to other tools that implement the distributed SMC algorithms like Uppaal SMC. The tests showed that Uppaal SMC is at least two orders of magnitude faster in the hypothesis testing.

The family of Uppaal tools are all based on variants of Timed Automata [16]. So in order to apply the SMC approach on the system in Fig. 1 we have to describe the system behavior using Timed Automata. First, let's explain a simple automaton (state machine) structure in Fig. 2. It can be seen that this automaton has three locations: InitialState, HighLoad and LowLoad. To every location we've assigned a value of the variable Rload. The transitions from one location to the other is driven by the clock variable y which value is reset after each transition. A clock is a special type of variable, whose domain consists of non-negative real numbers. When an automaton is waiting in a location and time is passing then the value of its clocks are increasing. Each location has the invariant $y < 700$, which defines the maximum clock value for which the system can stay at each location. The transition edges have guards $y > 100$ and they determine the minimum clock value that has to be reached before the system is allowed to change the location. In other words, transitions will occur in each simulation run for a clock value between $100 < y < 700$. The exact transition time is not predefined, it is random and in this case all clock values between $100 < y < 700$ have an equal likelihood to trigger the transition i.e the probability distribution of the transition is uniform. Because of this ability to randomly change the location i.e. the load value, a lot of different simulation runs can be performed to see how the control algorithm of the converter will respond to transient load changes that occur at different moments.

The same modeling principle is now applied to all model components of the system. The core element of the system, the converter, is a Timed Automata with 27 locations, which describe the switching vectors of the converter. Instead of a clock variable that represented the time, system currents and voltages

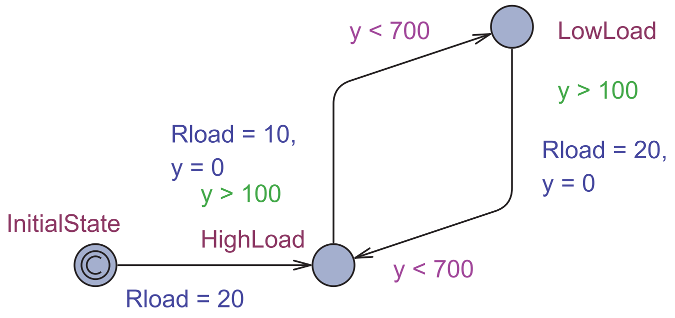


Fig. 2: Load model Timed Automata in UPPAAL Statistical Model Checker.

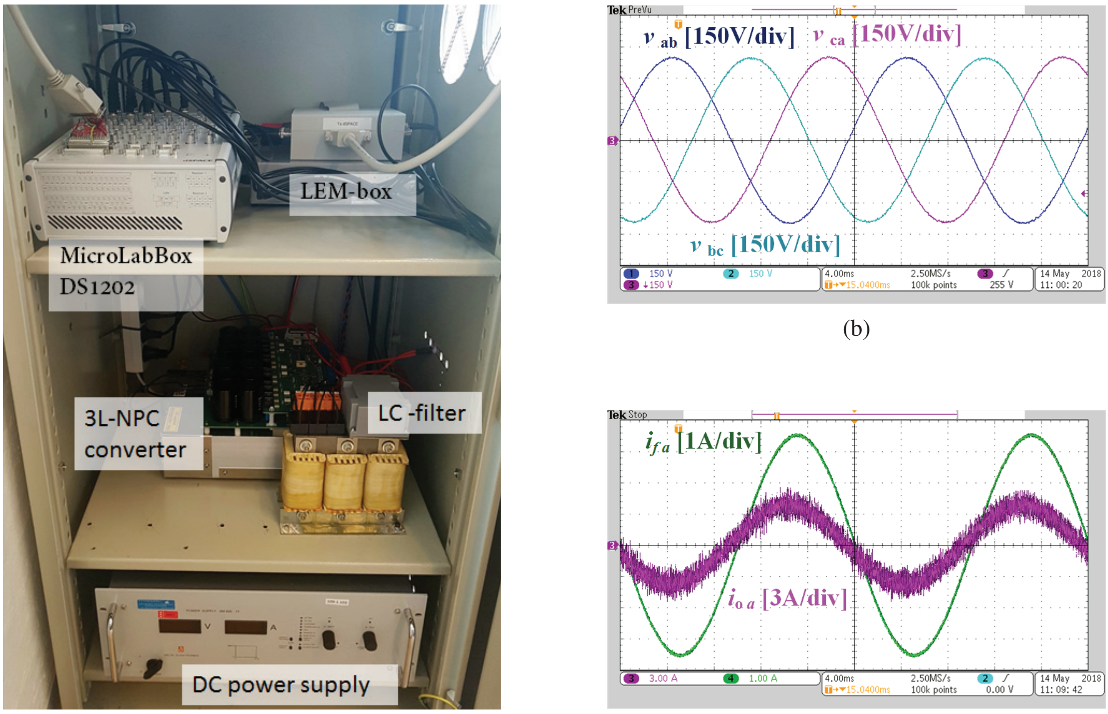
are now used as clock variables to drive the Timed Automata and they are defined by the differential equations e.g. (1). Which transition in the converter Timed Automata will occur depends on the result of the cost function of the FCS-MPC. As mentioned before there are series of statistical algorithms that will monitor the system simulations. The system verification starts by determining a system hypothesis we want to check e.g the difference between the reference and the control variable to stay below 5% during transient load changes. Next the reliability of the validation process is specified, for obtaining a very high reliability a lot of simulation samples are necessary. Afterwards using the Chernoff bound the toolbox will determine the necessary number of simulations to calculate the probability of the hypothesis being satisfied [16]. Particularly, we can compare the probabilities of the difference value staying below a specified threshold for different cost functions or under parameter uncertainties. Inherently, we will get information about the algorithm's robustness. The system model design in UPPAAL is very adaptive and modular, therefore adjusting the model to the different converter topologies is easy, it is only necessary to edit the location number according to possible converter switching states and assign the correct output voltage values. However, by increasing the number of locations the time needed for evaluation of the queries will also increase. More information about SMC and UPPAAL SMC can be found in [23].

Algorithm performance verification

The described system with the FCS-MPC algorithm was implemented in a Matlab/Simulink model and used for weighting factors selection of the cost function and also as a benchmark model for the UPPAAL model. Values of the model parameters are shown in Table I and they match the experimental set-up parameters in Fig. 3a. Weighting factors λ_d, λ_{dc} and λ_{sw} were determined performing several parameter sweep simulations where λ_{dc} was first kept fixed while λ_d and λ_{sw} were varied. In the later simulations the roles were switched and the λ_{dc} value was varied. Total harmonic distortion (THD) factor of the output voltage and average switching frequency $f_{sw_{avg}}$ were used as performance variables to select the optimum weighting factors as shown on Fig. 4a and Fig. 4b. The average switching frequency can be

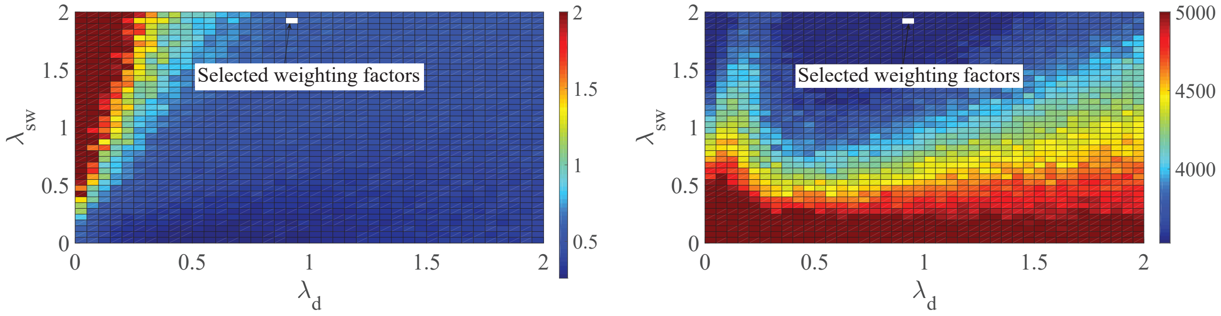
Table I: System parameters used for testing.

Parameter	Value
DC-link voltage (V_{dc})	520 V
DC-link capacitors (C_{dc1}, C_{dc2})	4 mF
Output filter inductance (L_f)	2.4 mH
Output filter capacitance (C_f)	15 μ F
Load resistance (R_{load})	60 Ω
Reference voltage and frequency (V_{ref}, f_{ref})	230 V, 50 Hz
Sampling time (T_s)	25 μ s



(a) (b) (c)

Fig. 3: 3L-NPC experimental set-up and measured results: (a) 3L-NPC experimental set-up. (b) Measured load voltage v_{oabc} (THD = 1.13%, f_{swavg} = 3.2 kHz). (c) Measured load current i_{oa} and filter current i_{fa}.



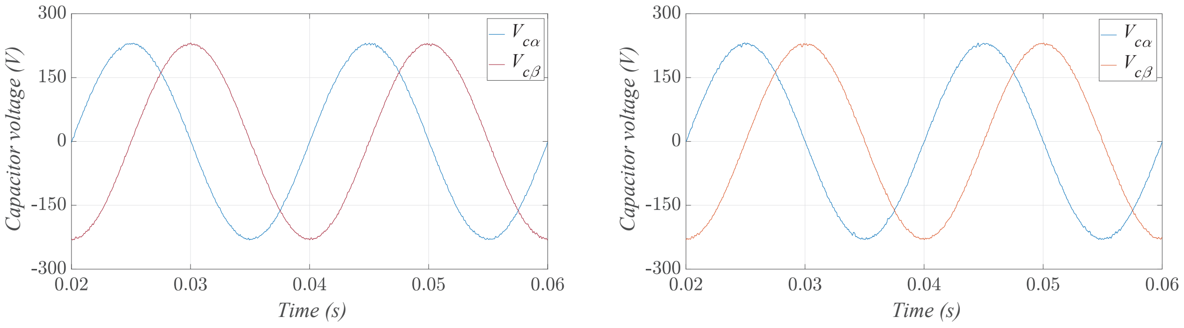
(a) (b)

Fig. 4: Influence of the weighting factor selection on : (a) Capacitor voltage THD. (b) Average switching frequency.

calculated using the following expression:

$$f_{sw_{avg}} = \sum_{i=1}^{n} \frac{f_{sw_{ai}} + f_{sw_{bi}} + f_{sw_{ci}}}{12}, \qquad i \in 1,2,3,4 \tag{10}$$

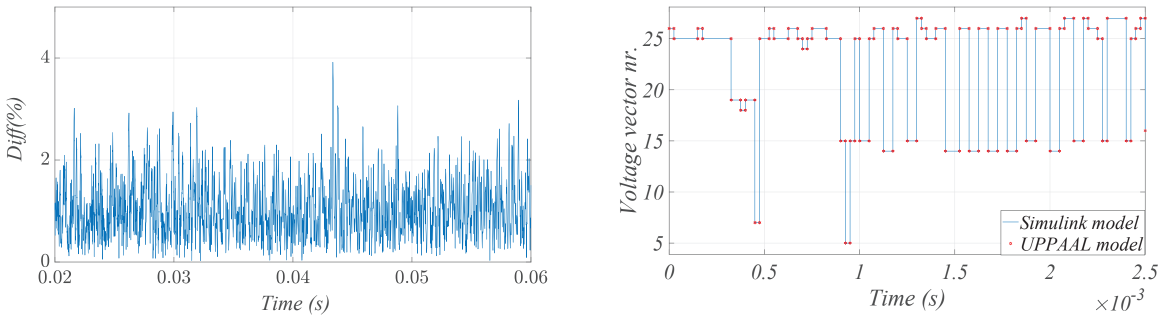
where $n = 4$ represents the number of switches in each phase leg. The values $\lambda_d = 0.9$, $\lambda_{dc} = 1$ and $\lambda_{sw} = 1.95$ were selected and used in the further analysis. The control algorithm was also verified on an experimental set-up shown in Fig. 3a, which includes a Semikron 3L SKiiP28MLI07E3V1 Evaluation Inverter, MicroLabBox DS1202 PowerPC DualCore 2 GHz processor board and DS1302 I/O board from dSpace. Good reference tracking results and low ripple in both load and filter current were obtained as it



(a)

(b)

Fig. 5: Output voltage in αβ frame in (a) Simulink model. (b) UPPAAL system model.



(a)

(b)

Fig. 6: Simulation results from UPPAAL model: (a) Output voltage error. (b) Selected voltage vectors in Simulink and UPPAAL model.

is seen in Fig. 3. Before starting the algorithm performance verification, to demonstrate the correctness of the UPPAAL model we present the resulting output voltage and its reference trajectory in the stationary αβ frame and the selected optimal voltage vectors (1-27) in the cost function minimization in Simulink model and UPPAAL model. To each output voltage vector of 3L-NPC was assigned a number from (1-27). As it can be seen in Fig. 5 and Fig. 6a the model features good reference tracking abilities in steady state and the exact vector selection proves the matching behavior of both models shown in Fig. 6b.

The performance of the algorithm is tested through queries for time interval of 40 ms:

$$diff = (v^*_\alpha - v^m_\alpha)^2 + (v^*_\beta - v^m_\beta)^2 \tag{11}$$

where v^*_α and v^*_β are the real and imaginary parts of reference voltage vector $v^*(k)$, v^m_α and v^m_β are the values of measured output voltage $v^m_c(k)$. Second query is assessing the simple moving average value (SMA) of the difference calculated on $n = 10$ sample group.

$$SMA = SMA_{prev} + \frac{diff_M}{n} - \frac{diff_M - n}{n} \tag{12}$$

During each simulation run the value of the load is changing randomly in order to check the reference tracking abilities of the control algorithm through all possible transients. The queries were also tested under parameter uncertainties to check how much false estimation of the output filter parameters will affect the algorithm performance. The results are presented in Table II with 95% reliability of the probability estimation process ($\varepsilon = 0.05$). A low number of the runs is also an indicator if some event is likely to happen or not i.e for the first query $diff < 3\%$ the probability is close to 0, meaning the chances that the difference stays below 3% is very low. On the contrary the query $diff < 6\%$ has the estimated probability

Table II: Query probability results from UPPAAL SMC toolbox verifier.

Query	Parameter uncertainty	Probability	No. of sim. runs
$diff < 3\%$	0	0 - 0.097	36
$diff < 6\%$	0	0.874 - 0.974	111
$diff < 3\%$	30%	0 - 0.097	36
$diff < 6\%$	30%	0.901 - 0.999	54
$diff < 6\%$	-30%	0 - 0.097	36
$diff < 8\%$	-30%	0.415 - 0.515	400
$diff < 10\%$	-30%	0.774 - 0.874	238
$SMA < 3\%$	0	0 - 0.097	36
$SMA < 6\%$	0	0.878 - 0.978	104
$SMA < 3\%$	30%	0.013 - 0.112	88
$SMA < 6\%$	30%	0.887 - 0.987	88
$SMA < 6\%$	-30%	0 - 0.097	36
$SMA < 8\%$	-30%	0.394 - 0.494	397
$SMA < 10\%$	-30%	0.812 - 0.912	196

close to 1, which means that we can be almost certain that query will be fulfilled.

The obtained results have confirmed a good cost function design with high probability of the difference staying below 6%. In the case of using 30% smaller parameter values of the LC filter then in the prediction model the probability of the difference staying below 6% will be very low, however with a high probability it will still stay below 10% of the reference during all possible load transients, which is still a very good performance. Furthermore, when the values of the LC filter parameters were underestimated in the prediction model the effect on the reference tracking performance was very minor and proving the robustness of the designed algorithm. This type of analytical performance evaluation can also provide useful data for weighting factor selection or comparison of different cost functions.

Conclusion

In this paper the SMC approach was proposed to perform an analytical verification of the FCS-MPC algorithm for a standalone 3L-NPC converter dynamic performance. The discrete nature of the control algorithm in a continuous system with the stochastic load model was successfully modeled in UPPAAL SMC. A benchmark test with a Simulink model validated the correct modeling approach. Good reference tracking abilities and the robustness of the FCS-MPC algorithm under parameter uncertainty, especially with underestimated parameter values in the prediction model were demonstrated. Although only a standalone application was analyzed in this paper, the presented approach can add a great contribution for grid connected converter models. Through further development of the modeling approach, the behavior of a more complex model predictive algorithms and converter topologies can also be verified.

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