Abstract—This letter experimentally demonstrates the temperature dependence of the Flatband Voltage ($V_{FB}$) in high power Insulated-Gate-Bipolar-Transistors (IGBTs). The gate voltage during the turn-on delay is shown to fluctuate up to $5\text{mV}^\circ\text{C}$ as a result of this temperature dependence. The practical implications for this temperature dependence are that the $V_{FB}$ could be a potential unreported addition to the genre of IGBT junction temperature measurement methods known as Temperature Sensitive Electrical Parameters (TSEPs). The letter will outline some possible measurement circuits and highlight areas for future research to enable the $V_{FB}$ to be used in this manner.

Index Terms—Power semiconductor devices, insulated-gate bipolar-transistor (IGBT), temperature measurement.

I. INTRODUCTION

In a MOS-gated device, the flatband voltage ($V_{FB}$) corresponds to the voltage, which, when applied to the gate terminal yields a flat energy band in the semiconductor. This voltage separates the accumulation and depletion conditions [1].

The effect of sweeping the gate voltage ($V_{GE}$) from a value below the $V_{FB}$, to a value above the $V_{FB}$ is shown in Fig. 1. Here, a capacitance-voltage (CV) profile of an Infineon FS200R12PT4 IGBT module is shown. While $V_{GE}$ is below $V_{FB}$, the accumulation condition is present and the gate capacitance consists of the oxide capacitance. When $V_{GE}$ increases beyond $V_{FB}$, a depletion region is formed, and the gate capacitance now consists of two capacitances in series: the oxide capacitance, and the depletion capacitance. Therefore, the size of the gate capacitance decreases considerably.

Despite the effect of $V_{FB}$ illustrated above, previous literature discussing the switching of IGBTs has typically omitted mentioning the influence of $V_{FB}$ [2–4]. The variance of the gate capacitance during the turn-on delay is also not accounted for in device datasheets. For example, for the Infineon FF1000R17IE4 from Fig. 2, the datasheet lists a gate capacitance of 81nF – while the actual capacitance the gate driver begins to charge in the period from 0ns to 900ns is actually close to 300nF.

The point of inflection in the $V_{GE}$ caused by the $V_{FB}$ during the turn-on delay is characterised in with respect to junction temperature, DC-link voltage, and collector current in Fig. 3.

After the point of inflection, the gate voltage exhibits a negative temperature dependence of around $-2.5\text{mV}^\circ\text{C}$, as shown in Fig. 3a. Figs. 3b and 3c display the dependence of $V_{GE}$ on collector voltage and collector current, respectively. In line with theoretical expectations, no dependence on collector current is present. Nevertheless, a large influence from the collector voltage can be seen. This data was obtained from a double pulse test on an Infineon FF1000R17IE4 where an auxiliary IGBT is used to ramp up the inductor current. In this manner, self-
heating can be eliminated from the test IGBT [2, 5]. A photo of this setup is displayed in Fig. 4. To perform the measurements with a varied junction temperature, a temperature controlled heatsink was used.

Fig. 4. Photograph of test setup used for double pulse test

### III. VFB AS A TSEP

The junction temperature of a power semiconductor device directly influences both reliability and efficiency. Therefore, it is advantageous if the junction temperature of a power semiconductor is known.

Temperature Sensitive Electrical Parameters (TSEPs) are one popular way of estimating the junction temperature inside a power semiconductor module. This genre of measurements directly use the electrical behavior of the semiconductor as the temperature sensor. In doing so, non-invasive junction temperature measurements can be performed without any modification to standard semiconductor packaging [6-8].

The past three years have seen a significant number of proposals relating to the use of TSEPs [2-5, 9-17]. There are however several practical issues that hamper the use of TSEPs. For example, several TSEPs require measurement procedures that force significant medication to the normal operation of the semiconductor [6, 7]. Another problem is that the majority of TSEPs have a dependency on load current. These TSEPs must undergo complex calibration procedures since the load current causes self-heating in the semiconductor which consequently must be compensated for [4, 6, 7].

To the authors’ knowledge, the VFB has not previously been highlighted as a TSEP in prior literature. The experiments conducted in Section II were with the intention of performing a preliminary investigation on the feasibility of VFB as a TSEP. The results showed that there is an attraction for further investigation since the VFB was shown to be independent from primary load current variation, and should be possible to observe solely by using measurements of the gate voltage during a normal hard-switching turn-on.

The following sections will describe two measurement circuits that we investigated for measuring the variation of the VFB with junction temperature, along with mentioning the drawbacks and difficulties that we encountered.

### IV. VFB MEASUREMENT CIRCUITS

For this letter we investigated two op-amp based measurement circuits in order to trigger a VGE measurement during the turn-on delay which is dependent on the temperature variation of VFB. The following circuits were investigated with a combination of experimental and simulation data. The VGE waveforms were acquired experimentally from an Infineon FF1000R171E4, while the op-amp circuits were simulated with LTSpice using the experimental data as the input.

The first option is to simply sample the VGE at a fixed point during the turn-on delay. This process can be made straightforward by using a differentiator op-amp, a comparator and a delay buffer. The concept is shown in Fig. 5, where the voltage induced by the parasitic gate inductance triggers a differentiator and comparator op-amp at the start of the turn-on process. After a fixed delay of 1.1μs, the VGE is sampled. The delay of 1.1μs is selected since this is after the VFB has been surpassed, but before the VTH is reached and the IGBT is turned on.

Fig. 5. Waveforms for the ‘Fixed Delay’ measurement principle.

The second measurement principle is a more specific attempt to measure the VFB. A schematic is included in Fig. 6 and is referred to as the ‘Second Derivative Method’. Two
differentiator op-amp stages are used to identify the $V_{GE}$ at which the fastest capacitance drop occurs (i.e. the highest point of acceleration in the charging rate). This point should correspond to the moment the $V_{FB}$ is reached.

![Fig. 6. Circuit schematic for 'Second Derivative’ measurement principle.](image)

Fig. 6. Circuit schematic for ‘Second Derivative’ measurement principle.

![Second Derivative Method Waveforms](image)

Fig. 7. Waveforms for the ‘Second Derivative’ measurement principle.

Fig. 7 displays waveforms of this measurement principle. A comparator is triggered when the output of the 2nd differentiator stage exceeds a specified reference voltage level. It can be seen from Fig. 7 that the comparator produces two positive pulses during the turn-on process. The first is due to the parasitic inductance of the gate terminal, while the second is due to the surpassing of $V_{FB}$ and the rapid acceleration in charging rate. Therefore, an additional comparator and an AND gate are used to ensure that the ADC is triggered on the correct transition.

V. $V_{FB}$ SENSITIVITY AND TSEP DRAWBACKS

The sensitivity delivered by each measurement principle is displayed in Fig. 8. The Fixed Delay method displays a negative temperature dependence of around -5.1mV/°C. The negative dependence occurs since the $V_{FB}$ increases with temperature. Therefore, the total capacitance charged by the gate driver is smaller at the point of sampling, and thus a higher gate voltage is achieved.

The Second Derivative method shows a positive temperature dependence of around +3.1mV/°C, in line with the positive sensitivity depicted in Fig. 1. However, the voltage range is between +1.2V and +1.6V – not a negative voltage expected from Fig. 1. This is due to the ratio between the external and internal gate resistors, which causes the measured gate voltage to overestimate the gate charge during fast transient conditions. This phenomenon is also experienced in $V_{TH}$ measurement during full power switching [18].

Similar to other TSEP proposals based on the switching process [10-12], the $V_{FB}$ is dependent on collector voltage (from

![Sensitivity for $V_{FB}$ Measurement Approaches](image)

Fig. 8. Waveforms for the ‘Second Derivative’ measurement principle.

![VGE vs. Sample Time](image)

Fig. 9. $V_{GE}$ samples with 2-nanosecond jitter.

VI. CONCLUSION

This letter introduces the temperature dependence of the $V_{FB}$ in high power IGBTs. The temperature dependence of the $V_{FB}$, along with its influence during the turn-on process, is experimentally demonstrated. The letter suggests $V_{FB}$ as an addition to the genre of junction temperature measurement methods known as TSEPs. Initial analysis showed the $V_{FB}$ to be attractive as a TSEP since it is one of the few TSEPs independent of load current variation. However, the method suffers from high dependence on collector voltage and is highly susceptible to noise. The letter concludes that the $V_{FB}$ is unlikely to be viable for real-world use as a TSEP, but may find some future use in controlled laboratory environments.
REFERENCES


