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Novel Screening Techniques for Wind Turbine Power Converters

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Keywords

≪IGBT≫, ≪Power cycling≫, ≪Estimation technique≫, ≪Reliability≫

Abstract

Power converters represent one of the highest failure rates in the wind turbine. Therefore converter manufacturers perform burn-in tests to prevent shipping of faulty converters. Recent developments in junction temperature estimation, based on accurate online IGBT collector-emitter voltage measurements, allow for thermal stress estimation of the IGBT modules. This is utilized to detect infant mortalities in power converters, by comparing thermal responses of IGBTs for faulty and non-faulty converters. The method proves to be a time and cost efficient candidate to replace burn-in tests of power converters for wind turbines applications.

Introduction

A key issue in modern wind turbines is the reliability. In [1], Spinato et al. investigate the reliability of wind turbine subassemblies. The highest failure rates are found in the electrical system, the rotor and the converter. Spinato et al. suggest that more thorough tests of the converter could eliminate early failures and thereby improve the overall reliability of the wind turbine. The reliability of power converters can be represented by the bathtub curve as shown in Fig. 1 [2].

To avoid infant mortalities, converter manufacturers perform burn-in tests. The purpose of the burn-in tests is to identify converters that are likely to fail early in their life period [3]. This is often done through accelerated operating conditions where the temperature in the converter is at its critical level. The high stress causes the revelation of faulty converters, which are potentially destroyed. In addition to the destruction of the faulty converters, the downside of the burn-in tests is that a vast amount of time and energy is needed to precipitate the infant mortalities. The burn-in tests therefore account for a substantial expense to the converter manufacturers.

The junction temperature is not known in conventional burn-in tests as it is impractical to measure directly. Recent developments in online measurement of temperature-sensitive electrical parameters (TSEP) has led to the possibility of accurately estimating the junction temperature during operation of an IGBT module [4], [5]. This paper aims to investigate if this method for estimating junction temperature can be utilized to detect converter failures which could potentially lead to infant mortality.

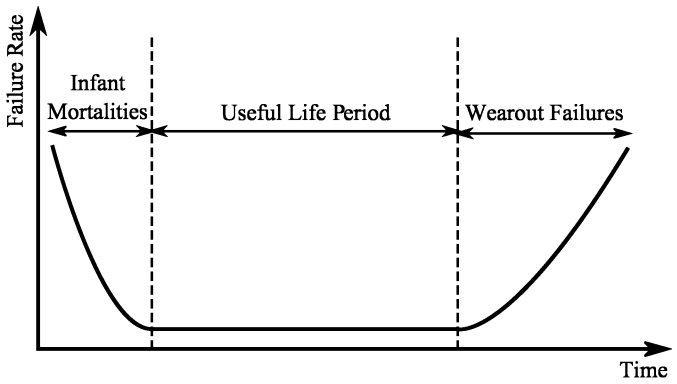

Fig. 1: Bathtub curve representing converter failure rate over time.

Faults

According to [6], possible causes of excessive increase in junction temperature and thereby potential infant mortality of the converter are: Too high losses caused by over load operation, bugs in gate driver circuit, and increased thermal impedance either internally in the power modules or in the interconnection between power module and heat sink.

To determine if a junction temperature estimation based on online measurement of TSEPs is usable for detecting increased switching loss and increased thermal impedance, four fault scenarios are examined: Partly or entirely missing thermal interface material (TIM) between module and heat sink, wrong torque applied to bolts when mounting on heat sink, wrong tightening sequence of bolts and increased switching loss by increasing the gate turn-on resistance.

The scenarios are tested on an Infineon IGBT FF1000R17IE4 power module consisting of two IGBTs and two diodes in a half bridge configuration. The module is rated to 1700 V and 1000 A nominal current.

Junction Temperature Estimation

To obtain the TSEP-T_j (junction temperature) characteristics, a calibration is done. The calibration setup is a two half bridge concept consisting of the device under test (DUT) and a control leg (CTL) connected through an inductive load, as shown in Fig. 2. The DUT is externally heated to a specified temperature, ranging from 25°C to 145°C with a 10°C increment. The heat source is a hot plate, mounted on the baseplate of the power module. For each of the temperatures, a calibration is done by ramping the load current to a desired level by having DUT_H and CTL_L conducting. Through appropriate switching, the current is conducted through the DUT_H IGBT. After a specified time (t_{meas}) the on-state voltage and the current are measured. A similar process is done for DUT_H diode, DUT_L IGBT and DUT_L diode. t_{meas} should be sufficiently high, so that the V_{ce} on-state voltage has settled. Through experiment this time period was found to be 30 μs.

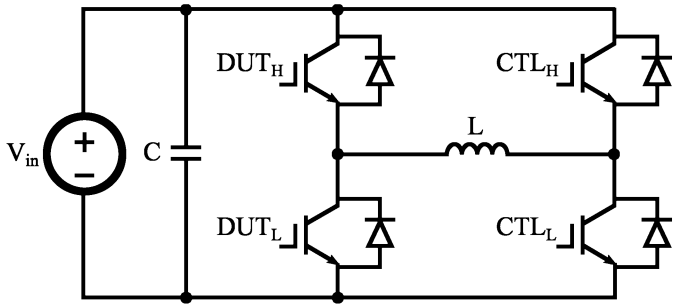

Fig. 2: Circuit scheme of calibration setup.

The calibration curves of the IGBT are shown in Fig. 3. The V_{ce}-I_c characteristics have a positive temperature coefficient (PTC) at high currents and a negative temperature coefficient (NTC) at low currents. This paper will, however, only concern the PTC region, i.e. the region related to high power operation.

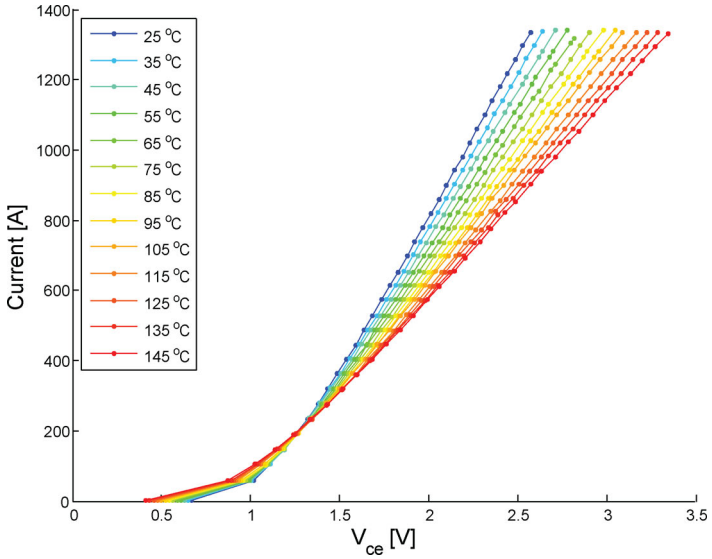

Fig. 3: IGBT I-V characteristics at different temperatures.

Temperature calculation

From the calibration curves the calibration factor (K) is obtained. The K-factor is the ratio of change in T_j to change in V_{ce} at a specific current level. Applying a linear fit to the T_j-V_{ce} relation at every measured current of Fig. 3 yields the plot shown in Fig. 4. The plot shows the PTC and NTC regions.

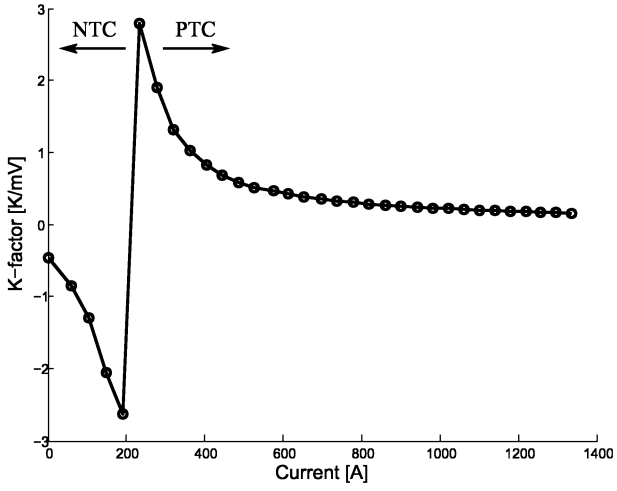

Fig. 4: K-factor plot at different current levels.

Using the K-factor and a T_j-V_{ce} reference point the junction temperature is calculated from (1).

$$T_j = T_{ref} + K(V_{ce} - V_{ref}) \tag{1}$$

V_{ce} is the measured on-state voltage and T_{ref} is the defined reference temperature, in this case 25°C. V_{ref} is the calibrated V_{ce} corresponding to the measured current and the reference temperature. Similarly K is the K-factor value relating to the measured current.

Thermal impedance

The thermal impedance from the semiconductor junction to the ambient surroundings (through the heat sink) is calculated as:

$$Z_{\text{th}}(t) = \frac{T_{\text{j}}(t) - T_{\text{a}}}{P_{\text{loss}}(t)} \tag{2}$$

Where T_{a} is the ambient temperature and P_{loss} is the power loss. If the power loss is kept constant in (2), Z_{th} will be directly proportional to the junction temperature. The power loss of the DUT_{H} is a combination of switching and conduction losses.

$$P_{\text{loss}} = P_{\text{cond}} + P_{\text{sw}} \tag{3}$$

The conduction loss is caused by the on-state voltage of the IGBT and diode when either is conducting. For the IGBT, the average conduction loss is given by

$$P_{\text{cond}} = D_{\text{D}} V_{\text{ce}} I_{\text{c}} \tag{4}$$

Where D_{D} is the duty cycle of the DUT. Switching losses occur when the semiconductor goes from conducting to blocking and vice versa, and thus occurs as pulses of power. This causes issues in regard to keeping a constant power loss in the power module.

By giving a DUT duty cycle of unity i.e. always conducting through the DUT_{H} IGBT, power losses consists only of the conduction loss. Thus the power loss can be obtained directly from the measurements of V_{ce} and I_{c}. Thereby, it is possible to calculate Z_{th} from (2) using the P_{cond} measurement and the junction temperature estimation.

Test bench

A test bench with conduction power loss control is constructed using a structure as shown in Fig. 5. Temperatures of devices in the CTL-leg are not monitored. Two CTL-legs are used in parallel to reduce the stress experienced by a single CTL leg. The two CTL power modules are cooled using Danfoss ShowerPower® whereas no active cooling is implemented on the DUT power module. By not having to apply liquid cooling to the DUT, it is easier to exchange the DUT in the setup which saves time and complexity in the test procedure. For safety reasons DC-link discharge and over/undercurrent protection circuits are designed and implemented in the setup.

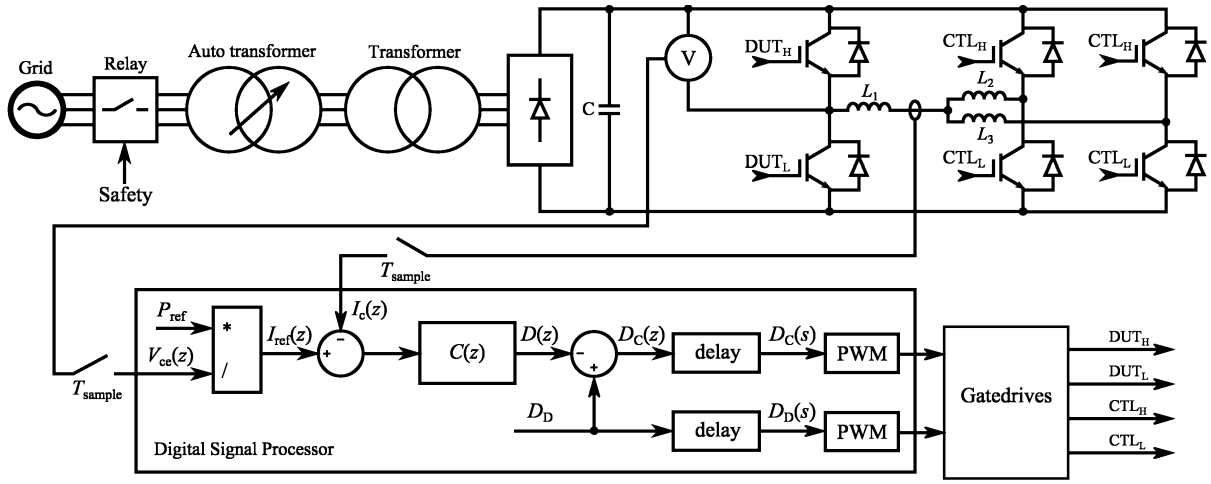

Fig. 5: Principal schematic of the test bench

Control

The control is implemented on a F28M36x digital signal processor (DSP). The duty cycle of the DUT, D_{D}, follows a given reference by feed forward, while the CTL, D_{C}, is given by the controller. D_{C} is obtained through a conduction loss controller by feedback of load current I_L and V_{ce}.

The open loop transfer function from D to I_{c} is derived to be

$$\begin{aligned} G(s) &= \frac{I_{\mathrm{c}}(s)}{D(s)} = zoh(s) \cdot delay(s) \cdot G_{\mathrm{L}}(s) \\ &= (\mathrm{e}^{-sT_{\mathrm{sample}}} - \mathrm{e}^{-2sT_{\mathrm{sample}}}) \frac{V_{\mathrm{DC}}}{s(Ls+R)} \end{aligned} \tag{5}$$

where *zoh* is the zero order hold, *delay* is the delay caused by the time period between measurement and updating the control. $G_{\mathrm{L}}(s)$ is the transfer function of the load, T_{sample} is the sampling period, L is load inductance, V_{DC} is the DC-link voltage. R is a combination of the load resistance, the IGBT on-resistance and wire resistance. When discretizing (5) becomes

$$G(z) = \frac{I_{\mathrm{c}}(z)}{D(z)} = \frac{V_{\mathrm{DC}}}{R} \frac{1 - \mathrm{e}^{-\frac{R}{L}T_{\mathrm{sample}}}}{z(z - \mathrm{e}^{-\frac{R}{L}T_{\mathrm{sample}}})} \tag{6}$$

The PI controller has the discrete transfer function as shown in (7).

$$C(z) = K_0 \frac{z - z_0}{z - 1} \tag{7}$$

K_0 is the controller gain and z_0 is the zero location. z_0 is chosen so that it cancels the $G(z)$ pole at $\mathrm{e}^{-\frac{R}{L}T_{\mathrm{sample}}}$. K_0 is chosen from a root locus analysis so that no overshoot is present. The designed discrete PI-controller settles at specified conduction power loss levels within 3.2 ms, as shown in Fig. 6

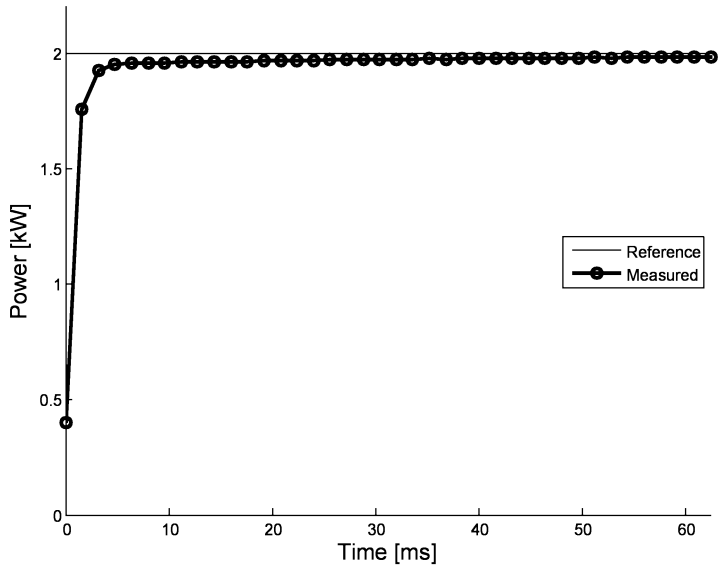

Fig. 6: Power step calculated from measured on-state voltage and current.

Faulty Assembly

Tests are performed with conduction losses at levels of 1 kW, 1.5 kW and 2 kW. In the PTC region, V_{ce} increases with rising temperature, thus the PI-controller adjusts the current accordingly to maintain constant power loss. The tests are run for 40 s, during which V_{ce} and I_{c} are measured. These measurements are used for junction temperature estimation and are finally translated into thermal impedance using (2).

The first test conducted has the purpose of being a reference for comparing with faulty assemblies. For the reference test the TIM is spread evenly and in the correct amount using a template and the mounting of the module on the heat sink is done according to the specified guidelines [7]. The TIM distribution after test is shown in Fig. 7.

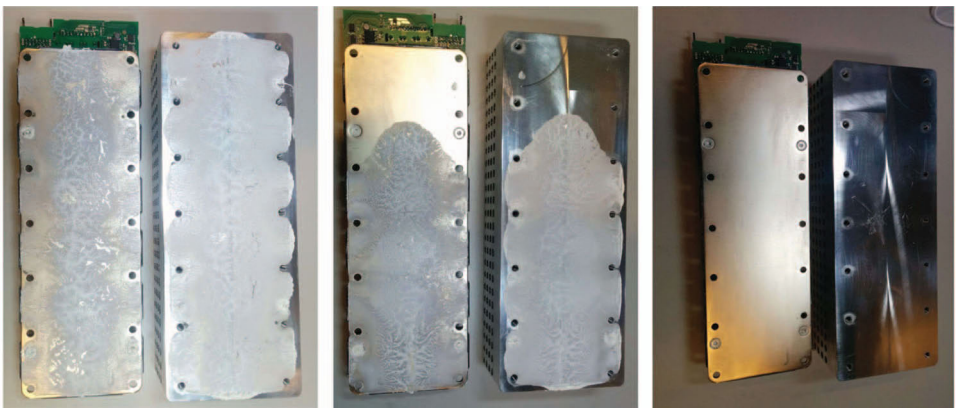

Fig. 7: IGBT and cooling block with correct TIM (left), 2/3 applied TIM (middle), and no TIM (right).

If no TIM is applied (Fig. 7 right) or only two thirds of the power module is covered with TIM (Fig. 7 middle) the heat path from semiconductor to heat sink is obstructed. This is shown in the response of the thermal impedance in Fig. 8. The three curves are equal from zero to around 400 ms. After this point the curves break apart revealing a significant difference in thermal impedance for the three different cases. This highlights that the test procedure is able to distinguish between cases of correctly or poorly distributed TIM.

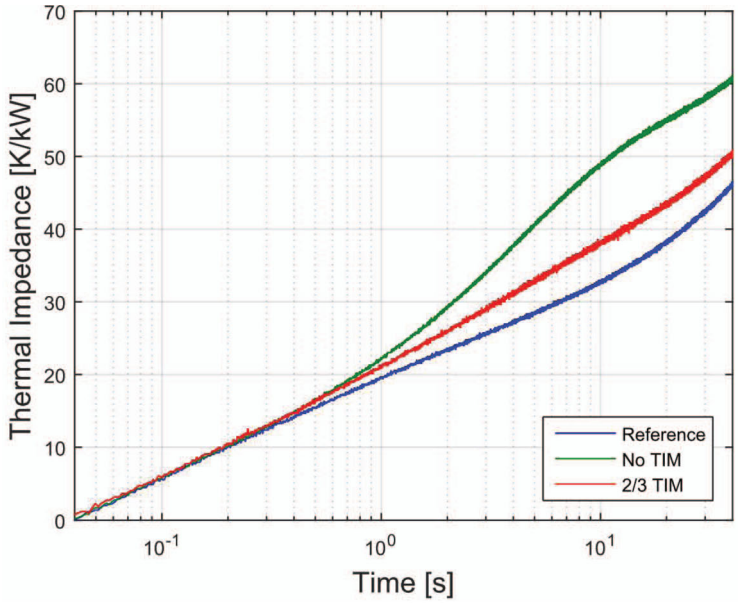

Fig. 8: Thermal impedance without TIM and with 2/3 applied TIM compared to the reference at 1.5 kW conduction loss.

Tests of wrong mounting sequence and wrong mounting torque are performed. Instead of following mounting sequence given in the guideline [7], bolts are fastened in a counter-clockwise order. In the test of mounting torque, the correct sequence is followed but the applied torque is 2 Nm instead of the recommended 6 Nm. Results of wrong mounting sequence and wrong mounting torques are omitted, as results are indistinguishable from the reference tests. The results are regarded as inconclusive and requires further investigation.

Gate-driver faults

To test if faults in gate turn-on resistance can be detected, five tests are conducted. These tests are performed with switching losses. The first test is conducted using the rated gate resistance followed by four test where the resistance is gradually increased. The tests are done with a DC-link voltage of 600 V, a DUT duty cycle of 0.5 and a reference IGBT conduction loss of 500 W.

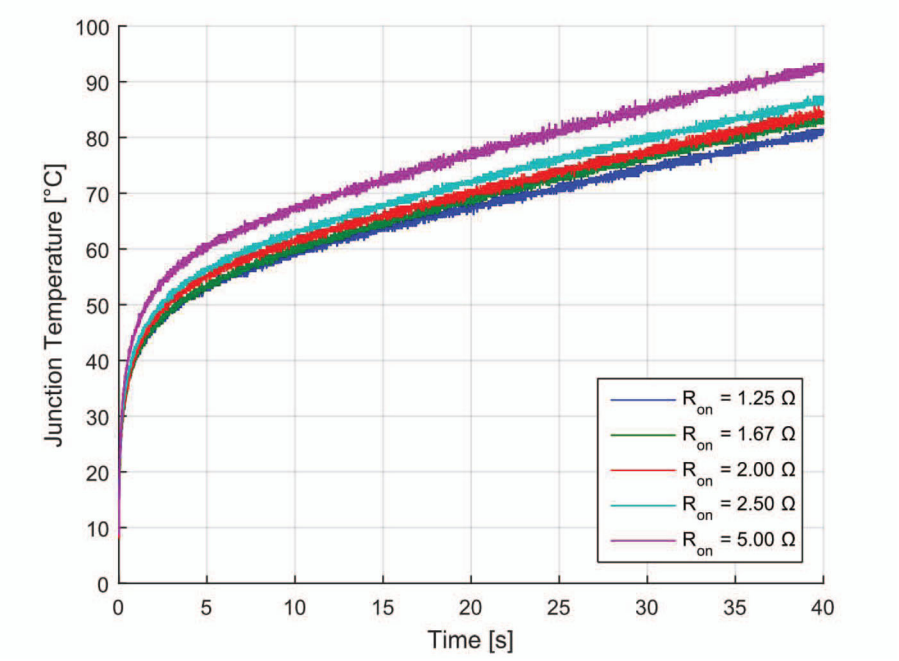

Fig. 9: Junction temperature as a function of time with various gate turn-on resistances.

The junction temperature is estimated using the calibrated data. The thermal impedance is not calculated using (2), because losses now include switching losses. The temperature curves for each of the five tests are shown in Fig. 9, calculated using (1). An increase in temperature is seen when increasing the resistance, which is caused by the increased switching loss. Thus the test enables identification of faults leading to increased switching losses.

Discussion

Z_{th}-curves of Fig. 8 break apart at the same time constant. These results indicate that the fault can be diagnosed at a distance from the junction by evaluating the time constant from which the tested power module deviates from a reference curve. This requires further investigation to be verified.

Industry might still require burn-in tests to be performed, and do not regard proposed methods as being sufficient to ensure reliable power converters. However, the proposed method enables diagnosis of faults prior to the burn-in. This allows the identification of the fault, and thus potentially save valuable hours of burn-in testing before a faulty power converter fails.

Conclusion

The thermal impedance monitoring of cases where the thermal interface material was partly or entirely missing showed clear indications of faults, whereas the results of wrong mounting momentum and sequence were inconclusive. If the turn-on gate resistance value is modified, it is detectable by examining the differences in thermal responses. The novel temperature estimation method used throughout this paper has proved to be of great potential for power converter screening applications.

References

[1] F. Spinato et al., "Reliability of wind turbine subassemblies," in IET Renewable Power Generation, vol. 3, pp. 1-15, Dec. 2009.

[2] E. E. Lewis, "Load-capacity interference and the bathtub curve," in Reliability, IEEE Transactions on, vol. 43, pp. 470-475, Sep. 1994.

[3] N. Sumikawa et al., "An Experiment of Burn-In Time Reduction Based On Parametric Test Analysis" in International Test Conference, pp. 1-10, 2012.

[4] P. Ghimire et al., "Online monitoring of high-power IGBT modules," in IEEE Industrial Electronics Magazine, vol. 8, no. 3, pp. 40-50, Sep. 2014.

[5] P. Ghimire et al., "A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application," Proc. of CIPS, Nuremberg, Germany, 2014.

[6] A. Volke and M. Hornkamp, "Quality and reliability" in *IGBT Modules: Technologies, Driver and Application*, 2nd ed., Germany, Infineon Technologies AG, ch. 14, sec. 2, pp. 490.

[7] Infineon (2009, September), *Mounting Instructions for PrimePACK™ modules Application Note (AN2009-08, V1.0)* [Online]. Available: http://www.infineon.com/cms/en/product/promo pages/primepack/